CSE 231 Lab PROJECT

The aim of the project is to assess the students' ability to tie in theoretical and experimental knowledge from CSE 231 to complete a practical project as a future Computer Science Engineer, and to work in a team. Information on groups and Team Leaders is outlined in Sec. 1.

The project consists of three phases. Each phase consists of an individual deadline that is summarized in Sec. 2. It is imperative that you meet all deadlines in order to complete the full project in due time. The mark distribution for the project is summarized in Sec. 3. The project description is given in Sec. 4. Objectives or tasks for each phase of the project are described in Sec. 5.

SEC. 1: GROUPS

Each group will consist of 3 members or less. Each group must assign a responsible Team Leader (Choose wisely!!). The responsibilities of the team leader include (but are not limited to) the following:

- Hold meeting with group and decide on the design.
- Hold regular meetings with group to ensure project is on track.
- Delegate tasks and deadlines to individual group members.
- Ensure group members complete their assigned tasks.
- Ensure project deadlines are met.
- Keep track of project budget, or assign another group member to do so.

I have created a folder in Google drive named "CSE 231L Project Folder".

Folder Link: https://drive.google.com/open?id=1GtnJf-S-E3CF435yN5GzEgxRao0-XAUu. Please use NSU mails to access the folder.

The group leaders must create a folder (within the mentioned Project Folder) and name it maintaining following format: "name1.name2.name3".

The group leaders must upload a file in that folder stating the NAMES and IDs of the group members by 20th July. On 21st July, I will check whether you have created your group's folder and uploaded the file containing Group members' information or not. You will lose some marks if you fall behind this deadline.

Upon the submission of the file, I would assign group numbers. If you wish to send me any mail apropos of the project, please use the following format for the subject: "192.NSU.CSE231L.9.GroupNumber". All future emails regarding the project should/will be sent as a reply to this email.

SEC. 2: DEADLINES

Combinational Circuit Design	**24th July**
Sequential Circuit Design	**27th July**
Combinational Circuit Implementation	**31st July**
Final Presentation (Sequential + Combinational Circuit Implementation)	**3rd August**

SEC. 3: MARKS DISTRIBUTION

Mark distribution for the project is outlined below.

Combinational Circuit Design	**25**
Sequential Circuit Design	**25**
Combinational Circuit Implementation	**25**
Final Presentation (Sequential + Combinational Circuit Implementation)	**25**

Final marks will only be confirmed upon satisfactory completion of the project. Marks will be given at the discretion of the faculty member considering the group is capable of the work submitted based on their overall performance.

SEC. 3.1: LATE SUBMISSION

Failure to meet each deadline will result in a deduction of 10% for each deadline missed. Failure to complete the project by the final deadline will result in an award of **0 marks**.

SEC. 3.2: PLAGIARISM

Plagiarism will **NOT** be tolerated. Any form of plagiarism will result in an immediate award of **0 marks** to the group for the entire project. Same applies to the hardware implementation. If multiple reports are found as copies, an immediate award of **0 marks** shall be awarded to **ALL parties** without further deliberation.

SEC. 4: PROJECT DESCRIPTION

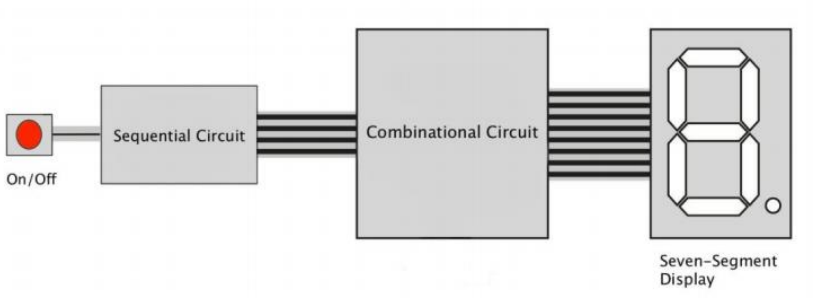


Figure 1: Circuit block diagram. Sequential circuit produces a sequence of codes. Code from sequential circuit is decoded by combinational circuit to light up corresponding segments of a seven-segment display.

Consider the digital system shown in Fig. 1. Switching on the circuit results in the string of characters "W1W2W3W4.X1X2X3X4.Y1Y2Y3Y4" being displayed on the seven-segment display one character at a time at a set time interval of 2 to 3 seconds. Here, W1W2W3W4 represents the middle 4 digits of groupMember#1's ID; X1X2X3X4 represents the middle 4 digits of groupMember#2's ID; Y1Y2Y3Y4 represents the first 4 letters of groupMember#3's name, so on and so forth. At the end of the sequence, the string is repeated.

The sequential logic circuit produces a counter sequence which in turn triggers the combinational circuit part to output the string of characters "W1W2W3W4.X1X2X3X4.Y1Y2Y3Y4". The sequential logic circuit is connected to an active high or active low seven-segment display via a combinational logic circuit. The combinational logic circuit decodes the input codes from the sequential logic circuit in order to drive the individual segments of the seven-segment display to show each character like the following: '0', '5', '9', '5', '.', '0', '6', '9', '6', '.','M', 'A', 'S', 'H', '.', 'S', 'A', 'M', 'I' as per dictated by the sequence.

NOTE: Only ONE seven-segment display is to be used and the display will show one character at a time based on the sequence.

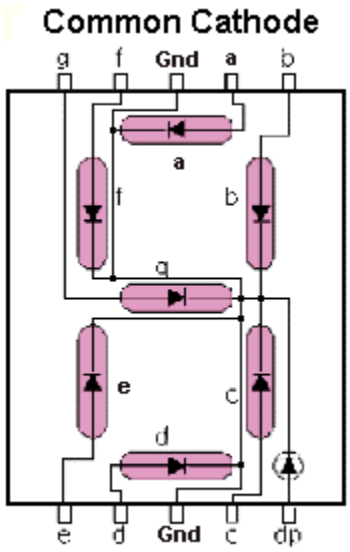


Figure 2: Segment and pin configuration of a seven-segment display. For an active high display, each segment (a – g and dot) light up when a logic high is applied to its corresponding input pin.

Fig. 2 shows the schematic of seven-segment display with its segments and corresponding input pins labeled (a – g). The COM ports are for VCC and Gnd.

SEC. 5: OBJECTIVES

1. **Combinational Circuit Design**
   Design the combinational logic part of the system described in Sec. 4, that is, the circuit to display the characters of the string "W1W2W3W4.X1X2X3X4.Y1Y2Y3Y4" on a seven segment display.

   All the groups need to design the Combinational Circuit Using:
   1. Basic Logic Gates
   2. Universal Logic Gates
   3. Multiplexer
   4. Decoder or Encoder

   Please note that you will get four different designs for the same output using these four types of IC's. And if you wish, you may design it based on programmable logic also.

   The group must complete a working schematic of the four circuit designs using Logisim and submit a soft-copy of it, on or before the deadline in the mentioned Google drive folder mentioned earlier.

2. **Combinational Circuit Implementation**
   It is at the discretion of the group to opt for their choice of implementation - minimal logic, universal logic, and decoder, multiplexer or programmable logic. However, the group must be able to provide

rationale for their design choice and it must be using relevant material covered in the course. The group must implement and demonstrate the combinational circuit to display the required characters on a seven-segment display.

3. **Sequential Circuit Design**
   Design the sequential logic part of the system described in Sec. 4, that is, the sequence generator for the string of characters "**W1W2W3W4.X1X2X3X4.Y1Y2Y3Y4**"

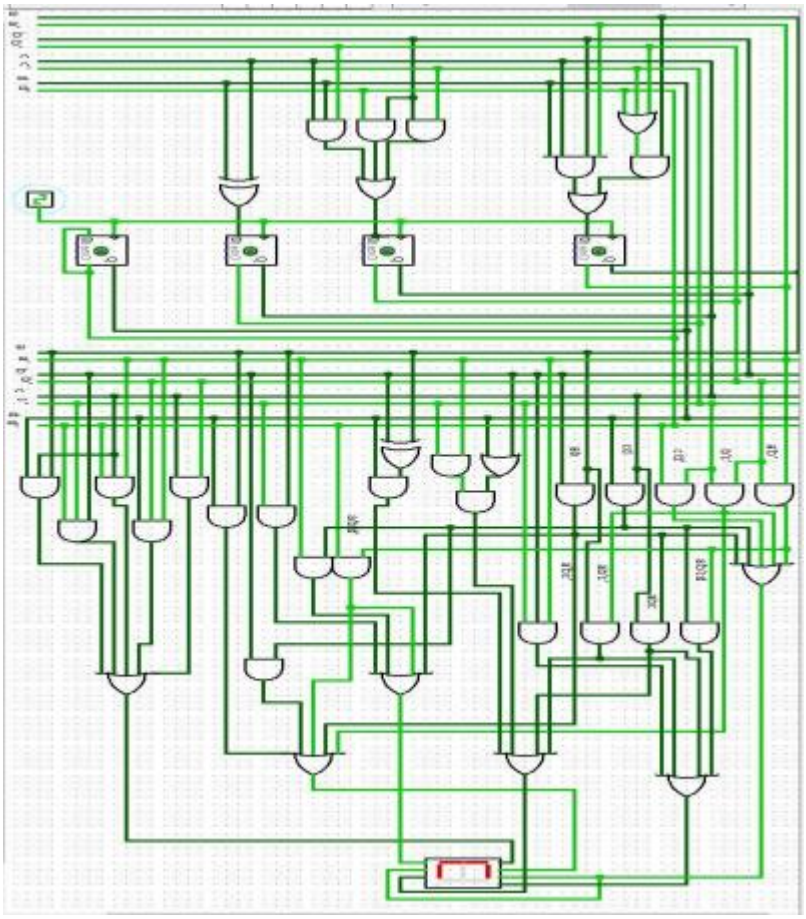
   There should be an extra input control bit. If the control bit is 0, the string should be "W1W2W3W4.X1X2X3X4.Y1Y2Y3Y4". However, if the control bit is 1, the string should show the second next digit when the next clock pulse arrives. For example, let's say that the control bit is initially 0. So, the seven segment display would show the first digit "W1W2W3W4.X1X2X3X4.Y1Y2Y3Y4". Now if we change the control bit to 1, then the string would be "W1W3. X2X4Y1Y3" and repeat "W1W3. X2X4Y1Y3" as long as the control input is kept to 1. You should provide three different designs using J-K, T and D flip flop. The group must complete a working schematic of the three circuit designs using Logisim and submit a soft-copy of it, on or before the deadline in the mentioned project folder.

4. **Viva Presentation**
   Students must provide a presentation describing their project. The presentation must contain important project details such as budget, project photos, truth tables, state diagram etc.

SEC. 6: RESOURCES

- **Logisim: Logisim software can be downloaded from:**
  http://ozark.hendrix.edu/~burch/logisim/download.html

SEC. 6: SAMPLE PROJECT THAT SHOWS “CSE231-G00-SEC08”



PLEASE NOTE THAT THIS CIRCUIT HASN’T BEEN MINIMIZED. IT’S JUST A SAMPLE THAT INCLUDES BOTH THE SEQUENTIAL AND COMBINATIONAL PART. IT ALSO INDICATES THAT ONLY A SINGLE SEVEN SEGMENT DISPLAY CAN BE USED.