A High-Efficiency Self-Oscillating Class-D Amplifier for Piezoelectric Speakers

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***Abstract*—The design tradeoffs of the class-D amplifier (CDA) for driving piezoelectric (PZ) speakers are presented, including efficiency, linearity, and electromagnetic interference. An implementation is proposed to achieve high efficiency in the CDA architecture for PZ speakers to extend battery life in mobile devices. A self-oscillating closed-loop architecture is used to obviate the need for a carrier signal generator to achieve low power consumption. The use of stacked-cascode CMOS transistors at the H-bridge output stage provides low-input capacitance to allow high-switching frequency to improve linearity with high efficiency. Moreover, the CDA monolithic implementation achieves 18 $V_{\rm PP}$ output voltage swing in a low-voltage CMOS technology without requiring expensive high-voltage semiconductor devices. The prototype experimental results achieved a minimum THD + N of 0.025%, and a maximum efficiency of 96%. Compared to available CDA for PZ speakers, the proposed CDA achieved higher linearity, lower power consumption, and higher efficiency.**

***Index Terms*—Analog integrated circuits, audio systems, closed loop systems, loudspeakers, low power electronics, portable media players.**

I. Introduction

THE consumer's demand for smartphones and tablet computers with longer battery life has required manufacturers to implement the standard multimedia tasks, such as audio reproduction, using high-efficiency circuits. Switching dc-dc converters have been used in power management modules to achieve high-efficiency power conversion in battery-powered devices [1]–[4]. The class-D amplifier (CDA) uses a similar switching output stage as dc–dc converters to provide outstanding audio performance with high efficiency; but, to truly extend battery life, low power consumption is also required when the system is active. Conventional loudspeakers used in mobile devices require large amounts of power to operate, thereby limiting the battery life despite the amplifier's high efficiency.

The preferred loudspeaker for portable applications is the electromagnetic (EM) speaker, which consist of a magnet, a voice coil, and an acoustic cavity that require large-form factors to deliver high-sound pressure level (SPL) [5]. However, the electrical impedance of EM speakers across the audio frequency bandwidth behaves as a low-value resistor between 4 and 32 Ω, needing large electrical power to generate high SPL. On the other hand, the piezoelectric (PZ) speaker is an electromechanical transducer that consumes little electrical power, while providing high SPL in small-form factors [6]; these properties make the PZ speaker an attractive alternative to extend battery life in portable devices, especially when a high-efficiency switching amplifier such as the CDA is used [7], [8].

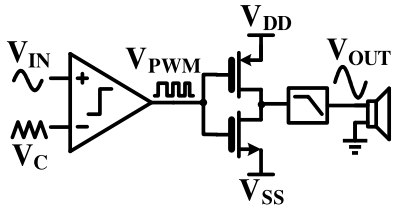

Fig. 1. Class-D output stage single-ended open-loop architecture.

Fig. 1 shows a single-ended open loop CDA, where a high-frequency carrier signal V_C is used to achieve pulse-width modulation (PWM) of a low-frequency input signal $V_{\rm IN}$. The modulated signal $V_{\rm PWM}$ is used to switch the output power transistors between the voltage rails with high efficiency. An output low-pass filter is typically used to recover the low-frequency signal and apply it to the speaker.

Open loop CDA architectures are cost effective and simple to implement. However, the absence of error correction limits their audio performance. To achieve outstanding audio performance in a CDA, closed-loop architectures are typically used, where the negative feedback mechanism helps to correct errors in the amplification process. The closed-loop CDA has been analyzed for intermodulation distortion (IMD) in time domain [9] and in frequency domain [10]. Moreover, the carrier distortion and its effect on the system has been analyzed in [11], and the effect of power-supply noise was analyzed in [12]. The conclusion is that large loop gain and a high-frequency carrier in the system help to attenuate the distortion components and supply noise of the closed-loop system, improving the audio performance.

Closed-loop CDA architectures have been proposed to achieve high efficiency and good audio performance using different modulation techniques, such as PWM [13]–[15], pulse-frequency modulation (PFM) [16], [17], or sliding-mode control [18], [19]. However, these architectures have an output stage that is typically optimized to drive low-impedance loads, such as the EM speaker and might not be suited to provide the high-voltage output swing needed for the PZ speaker. Typical voltage levels across the PZ speaker terminals should be in the range of 10–20 V_{pp} to achieve the maximum SPL, and could be generated from the battery using high-efficiency step-up voltage circuits [4], [20], [21].

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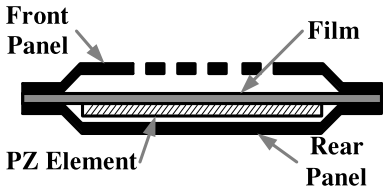

Fig. 2. PZ speaker physical structure.

High-voltage semiconductor devices, such as DMOS, LDMOS, or drain-extended MOS transistors are typically used to withstand the large-voltage potential needed at the output stage. Unfortunately, these devices are typically optimized to minimize conduction losses, and their parasitic capacitors can be large, increasing the power consumption due to their large switching losses, especially when a high-frequency carrier signal is used [22]–[26]. Furthermore, using these devices in monolithic implementations would require additional fabrication steps and/or a larger silicon area; thus, increasing the cost of the amplifier. Commercial CDA architectures for PZ speakers provide high-voltage outputs using these devices, but the distortion and power consumption are still large [27]–[30].

Other switching output stages have been proposed to drive high-voltage capacitive actuators for different applications [31], [32]. Nonetheless, the primary objective of these applications is to deliver the maximum amount of energy at the actuator's resonant point, making them not suitable for audio applications.

This paper discusses the design tradeoffs of the CDA architecture for driving PZ speakers, especially when low power consumption and high efficiency are desired. An example implementation is proposed to achieve high efficiency and high linearity in the CDA architecture for PZ speakers to extend battery life in mobile devices. The self-oscillating closed-loop architecture is used to obviate the need of a carrier signal generator to achieve high linearity with low power consumption. Moreover, the CDA monolithic implementation is able to provide an 18-$V_{\rm pp}$ output voltage swing in an 1.8-V core-voltage twin-well 11-16 Ω-cm p-type substrate CMOS technology without requiring expensive special high-voltage semiconductor devices. The use of stacked-cascode CMOS transistors at the H-bridge output stage provides low-input capacitance to allow high switching frequency to improve linearity without sacrificing the high efficiency.

This paper is organized as follows: Section II reviews the PZ speaker details and design considerations for the CDA. Section III discusses the CDA architecture for PZ speakers and its tradeoffs. Section IV presents the measurement results of the monolithic implementation prototype, and Section V concludes the paper.

II. Piezoelectric Speakers

A. Structure and Operation

The physical structure of a typical PZ speaker is shown in Fig. 2, where a PZ element is attached to a film encased between a front panel and rear panel. The PZ element deflects with voltage applied across its terminals, causing the film to warp and bend up and down according to the voltage applied across the PZ element. The deflecting/bending action creates pressure waves pushing air through one or more openings that are arranged on the front panel that resonate and amplify the response of the speaker.

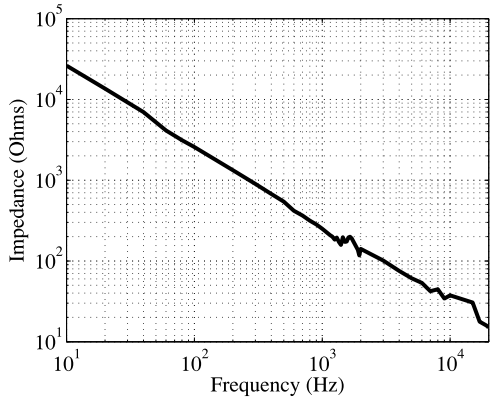

Fig. 3. PZ speaker electrical impedance versus frequency.

The PZ element in the speaker is typically a multilayer ceramic component that behaves electrically as a capacitor across the audio frequency bandwidth [6]. Fig. 3 shows the measured impedance versus frequency of a typical PZ speaker. The capacitive behavior of the PZ speaker presents a high impedance load to the driving amplifier, using low power to operate. The transducer has some dielectric losses in the ceramic material that will dissipate some power as heat with dissipation factors ranging from 0.4% up to 1% for most typical PZ speakers available.

B. Class-D Amplifier Considerations for PZ Speakers

1) Efficiency: The CDA power efficiency is typically estimated as the output power divided by the input (supply) power, using the average power over a sinewave signal period ($T = 2\pi/\omega$) defined as

$$P_{\rm AVERAGE} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\cdot dt = V_{\rm RMS}\cdot I_{\rm RMS}\cdot\cos(\varphi) \tag{1}$$

where the phase angle between the current relative to the voltage is represented by φ. For a conventional EM speaker the load is almost resistive, and the term $\cos(\varphi)$ in the output power is close to one, meaning that the power is being dissipated by the load. However, the PZ speaker is a highly reactive component, where the term $\cos(\varphi)$ is close to zero, appearing as if very little power is being dissipated by the load since the energy supplied by the battery is stored in the load and returned to the battery each cycle. Thus, if the average output power is used for the efficiency definition of the CDA driving a PZ speaker, the efficiency will appear very low [7].

Another alternative is to define the efficiency in terms of energy transfer between the supply and load [32], [33]. However, the energy analysis requires an estimation of the energy for each switching cycle, making it a complex procedure. A more

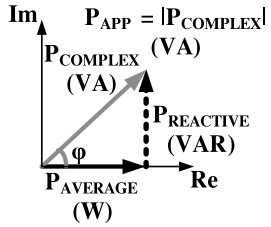

Fig. 4. Complex power definition.

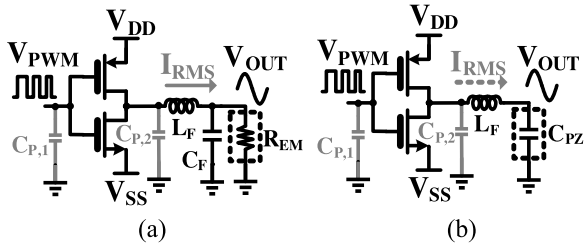

Fig. 5. Class-D output stage driving (a) EM speaker, or (b) PZ speaker.

suitable definition of the amplifier's power efficiency for capacitive transducers have been proposed in [34]–[36], where the apparent power is used for the efficiency calculation.

The apparent power, measured as $P_{\rm APP} = V_{\rm RMS} \cdot I_{\rm RMS}$, is the magnitude of the complex power vector, which contains the information of the reactive power and the average or real power, as observed in Fig. 4. Thus, the amplifier's power efficiency for capacitive loads could be defined as [34]–[36]

$$\eta \cong \frac{P_{\rm OUT,APP}}{P_{\rm OUT,APP} + P_{\rm LOSS}} \tag{2}$$

$$P_{\rm OUT,APP} = V_{\rm OUT,RMS} \cdot I_{\rm OUT,RMS} \cong \frac{V_{\rm OUT,RMS}^2}{|Z_L|} \tag{3}$$

$$P_{\rm LOSS} = P_Q + P_{\rm CL} + P_{\rm SW} + P_{\rm BD} + P_{\rm FILT} \tag{4}$$

where the power dissipation in the CDA $P_{\rm LOSS}$ is mainly dominated by the amplifier quiescent power P_Q, the conduction losses $P_{\rm CL}$, switching losses $P_{\rm SW}$, and body-diode losses $P_{\rm BD}$ of the output stage, and the losses due to the current ripple in the output filter together with the dielectric losses of the PZ speaker $P_{\rm FILT}$. To achieve high efficiency, the CDA has to process the power of the highly reactive load with minimum power dissipation dominated by the power losses in the amplifier and output filter.

A comprehensive analysis for the power losses in switching power stages can be found extensively in the literature [22]–[26]; for the purpose of this paper, a brief review will be discussed in detail the tradeoffs of the CDA driving a PZ speaker. Conduction losses occur due to the ohmic losses of the output switches' drain to source ON resistance $R_{ds\rm ON}$ and are more prominent when the current demanded by the load is large. Switching losses occur due to the power dissipated by the charging and discharging of parasitic capacitors, especially in the output stage. Body-diode losses occur due to the body-diode conduction and its reverse recovery charge that could be considerable for large output currents. These power losses can be expressed as

$$P_{\rm CL} \cong I_{\rm OUT,RMS}^2 \cdot R_{ds\rm ON} \tag{5}$$

$$P_{\rm SW} \cong \sum_i F_{\rm SW} \cdot V_{\rm CP}^2 \cdot C_{P,i} \tag{6}$$

$$P_{\rm BD} \cong V_{\rm SD} \cdot F_{\rm SW} \cdot (I_{pk} \cdot t_{\rm deadtime} + I_{rrm} \cdot t_{rr}) \tag{7}$$

where $I_{\rm OUT,RMS}$ is the output RMS current, $F_{\rm SW}$ is the CDA switching frequency, $C_{P,i}$ are the parasitic capacitors in the output stage, $V_{\rm CP}$ is the voltage across each $C_{P,i}$, $V_{\rm SD}$ is the body-diode voltage drop, I_{pk} is the peak output current, $t_{\rm deadtime}$ is the deadtime used to avoid shoot-through current, I_{rrm} is the body-diode maximum reverse recovery current, and t_{rr} is the body-diode reverse recovery time. The real power losses in the output filter can be expressed as

$$P_{\rm FILT} = I_{\rm OUT,RMS}^2 \cdot |Z_F| \cos(\varphi) + C_{\rm PZ} \cdot V_{\rm OUT,RMS}^2 \cdot 2\pi \cdot F_{\rm audio} \cdot {\rm DF} \tag{8}$$

where $|Z_F| \cos(\varphi)$ is the resistive part of the output filter impedance at $F_{\rm SW}$, $C_{\rm PZ}$ is the equivalent capacitance of the PZ speaker, $F_{\rm audio}$ is the output audio frequency applied to the PZ speaker, and DF is the dissipation factor of the PZ speaker. It can be noticed that the output filter component selection affects the real power dissipation, and the DF of the PZ speaker could dominate the $P_{\rm FILT}$ for large operating frequencies and amplitudes.

Fig. 5 illustrate the output stage of the CDA when driving the electrical models of an EM speaker or a PZ speaker, respectively. The main contributors of $P_{\rm SW}$ are the input and output capacitance of the output stage that can be large if the switches are sized to obtain small $R_{ds\rm ON}$. The advantage of using a PZ speaker is that its high impedance requires small current to operate, minimizing the impact of $P_{\rm CL}$ in the efficiency. This would allow smaller output switches to obtain the same $P_{\rm CL}$, but will decrease the $P_{\rm SW}$, enhancing the overall efficiency. Moreover, the small output current together with a short $t_{\rm deadtime}$ will reduce the $P_{\rm BD}$ contribution to the total power losses. To reduce the impact of the supply voltage drop due to the body-diode di/dt, a low-inductance package can be used with several bonding wires in parallel for the supply, ground, and outputs.

2) Linearity: The output stage in the closed-loop CDA can be modeled as a 1-bit quantizer, where oversampling by the high-frequency carrier signal shapes the quantization noise using the loop filter, enhancing the output signal linearity [17]. Increasing the carrier's frequency helps to dramatically decrease the distortion components [9]; but, the switching losses would drastically increase the power consumption, limiting the efficiency of the system.

The high-voltage special semiconductor devices needed at the output stage to safely operate with the high-voltage swing required by the PZ speakers possess large input and output capacitances, which would restrict the carrier signal frequency due to their large switching losses. The advantage of using cascode devices at the output stage switches is that the input and output capacitances are reduced considerably since smaller thick oxide transistors could be used as switches to withstand the

high-voltage output signal. Thus, the carrier signal frequency can be increased to enhance linearity with low power consumption.

3) EMI: Another important consideration for the CDA is the electromagnetic interference (EMI) radiated by the inductance of the cables and/or PCB traces connecting the CDA with the speaker. Several techniques to improve the EMI have been proposed to spread the energy of the high-frequency carrier signal used in PWM modulation [14], [15]. However, this comes at the expense of additional power consumption and design complexity.

A similar energy spreading of the carrier signal can be achieved in self-oscillating architectures without increasing the complexity of the design [11], [19]. Nonetheless, the energy spreading is limited, and filtering would be required at the CDA output to decrease even more the energy of the high-frequency carrier. The advantage of using the PZ speaker is its inherent filtering, as observed in Fig. 5(b), that can be leveraged to minimize the high-frequency energy at the output.

III. High-Efficiency Class-D Architecture for PZ Speakers

A. Architecture Description

The proposed CDA architecture for driving PZ speakers with low power consumption and high linearity is shown in Fig. 6. A self-oscillating first-order loop was employed to avoid the extra power consumption of the modulation carrier generator. Unlike PWM or PFM modulations, the self-oscillating modulation provides inherent frequency spreading of the carrier signal without any extra power consumption.

A fully differential architecture was implemented to provide more dynamic range, low distortion, and higher PSRR in the CDA. The amplifier A_1 implements a first-order integrator as loop filter to obtain the error signal from the difference between the input and feedback signals. The integrator's output signals are modulated by a pseudodifferential arrangement of hysteretic comparators to generate low-voltage switching signals (V_{H+}, V_{H-}). These signals pass through nonoverlapping, level shift, and predriver circuits generating the gate signals for the stacked-cascode output stage. For this implementation, to achieve the desired 18-$V_{\rm PP}$ output signal from the H-bridge, the high-voltage supply $V_{\rm CC} = 9V$ was chosen.

The stacked-cascode H-bridge output stage applies the high-voltage output switching signals ($V_{\rm SW+}$, $V_{\rm SW-}$) to the PZ speaker through an impedance Z_F. The impedance Z_F is used in series with the PZ speaker to limit the current consumption at high frequencies and implement a low-pass filter to reduce the energy of the carrier's frequency components at the output.

Finally, the output high-voltage switching signals are fed back to the integrator using a resistive divider with factor $K_F = 1/5$ to adjust the high-voltage signal back to the nominal voltage of the technology. This selection would fix the differential closed-loop gain of the CDA to 10 V/V or 20 dB. Resistors $R_3 = 10\ \text{k}\Omega$ and $R_4 = 40\ \text{k}\Omega$ were chosen taking into account the tradeoff between their effect on the integrator's time constant and the power consumption [16].

B. Loop Filter Considerations

A fully differential first-order integrator was employed to provide high loop gain to correct errors in the feedback loop. A higher order loop filter could be used to achieve better performance, but at the cost of more power consumption and design complexity to maintain stability for all modulation indexes [13], [16].

The integrator's ideal time constant is $\tau_{\rm int} = R_1 \cdot C_1$, and its value selection depends on several tradeoffs between the passive component values, amplifier A_1 power consumption, linearity, and in-band noise. Considering the finite loop gain of amplifier A_1, the transfer function for the implemented integrator yields

$$\begin{aligned} G_{\rm int,actual}(s) &= -\frac{G_{\rm int,ideal}(s)}{1+\frac{1}{A_1(s)\cdot\beta_{\rm int}(s)}} \\ &\cong -\frac{\left(\frac{1}{s\cdot R_1\cdot C_1}\right)}{1+\frac{s}{\rm GBW}\cdot\left(\frac{s\cdot R_{1,2}\cdot C_1+1}{s\cdot R_{1,2}\cdot C_1}\right)} \end{aligned} \tag{9}$$

where $R_{1,2} = R_1 // R_2$, the amplifier's transfer function is characterized as $A_1(s) \cong \text{GBW/s}$, and $\beta_{\rm int}(s)$ is the integrator's amplifier feedback transfer function. To avoid significant deviations in the integrator's performance, the amplifier's gain-bandwidth product (GBW) has to be higher than $f_{\rm int} = 1/(2\pi\tau_{\rm int})$. A large value for $f_{\rm int}$ would provide a higher bandwidth for the CDA loop that will result in high linearity, high PSRR at higher frequencies, and smaller values for the integrator passive components. However, the amplifier's power would need to be increased to avoid deviations in $f_{\rm int}$ due to limited GBW. The $f_{\rm int} = 50\ \text{kHz}$ was chosen as a compromise between these tradeoffs to provide high loop gain across the audio frequency bandwidth with low power consumption.

The input resistor values have to be chosen considering the tradeoff between the resistor's thermal noise contribution and its matching requirements for loop performance [12]. For this implementation, the integrator's component values are $C_1 = 8\ \text{pF}$ and $R_1 = R_2 = 400\ \text{k}\Omega$. The amplifier A_1 provides a dc gain of 45 dB with a GBW of 70 MHz. This design selection yields a magnitude error and phase error in the integrator function of 0.5% and 0.07% [37], respectively.

C. Self-Oscillating Modulator Considerations

The hysteresis window of the comparators in the modulator, the integrator's time constant, and the propagation delay in the loop will determine the modulation frequency of the self-oscillating system [11]. The $F_{\rm SW}$ as a function of the duty cycle ($D = V_{\rm IN}/V_{\rm supply}$) could be expressed as

$$F_{\rm SW}(D) = \frac{D\cdot(1-D)}{\frac{V_{\rm hyst}\cdot\tau_{\rm int}}{V_{\rm supply}}+\tau_d} \tag{10}$$

where $V_{\rm supply}$ is the supply voltage of the comparator, $V_{\rm hyst}$ is the voltage hysteresis window of the comparator, $\tau_{\rm int}$ is the integrator's time constant, and τ_d is the propagation delay from the comparator to the input of the integrator, including the comparator delay.

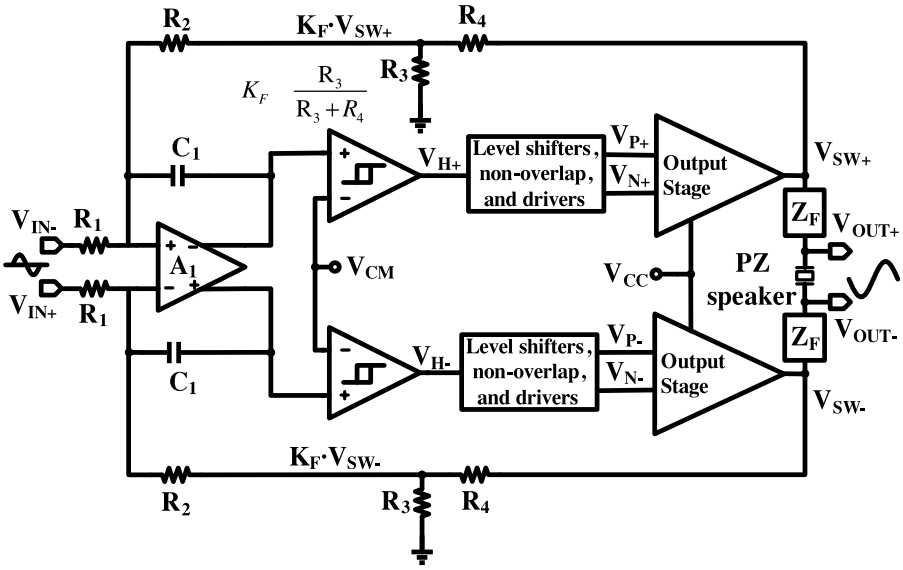

Fig. 6. Proposed CDA architecture for PZ speakers.

The average value of $F_{\rm SW}$ could be chosen taking into account the tradeoffs between power consumption, distortion, output filter components, and the excitation of undesired mechanical resonant modes in the PZ speaker [6]. A higher value of $F_{\rm SW}$ would result in less distortion and smaller output filter components, but at the expense of extra power consumption due to higher switching losses [16], and wider GBW of A_1. On the other hand, a low value of $F_{\rm SW}$ would reduce the power consumption, but at the expense of more distortion and bigger output filter component values [11].

Leveraging the low-input capacitance of the stacked-cascode output stage in the proposed CDA, a high-frequency carrier is used to achieve high linearity with high efficiency. The average value of $F_{\rm SW} = 800$ kHz was chosen as a compromise between these tradeoffs for this implementation. Therefore, from (10), $V_{\rm hyst}$ can be found for a $D = 0.5$ as

$$V_{\rm hyst} = \frac{V_{\rm supply}}{\tau_{\rm int}} \cdot \left(\frac{1}{4 \cdot F_{\rm SW}} - \tau_d \right). \tag{11}$$

For a $V_{\rm supply} = 1.8$ V, $F_{\rm SW} = 800$ kHz, $\tau_{\rm int} = 3.2\ \mu$s, and $\tau_d = 100$ ns, a $V_{\rm hyst} \cong 120$ mV was obtained. Fig. 7 shows the variation of the calculated switching frequency $F_{\rm SW}$ versus the duty cycle D for several τ_d cases as expressed in (10). It can be seen that $F_{\rm SW}$ is a parabolic function of D, and the delay τ_d would impose a limit in the maximum achievable $F_{\rm SW}$. For the assumed $\tau_d = 100$ ns, the average switching frequency decreases from 800 to 300 kHz as the peak input amplitude increases.

One of the drawbacks of the variable-frequency modulation is that the output current ripple will be increasing for large audio signals due to the decreasing $F_{\rm SW}$. Thus, the output RMS current will increase, and the real power dissipation in the nonideal components of the output filter will increase as expressed in (8).

The $F_{\rm SW}$ variation could be reduced if needed by controlling the main parameters in (10), such as the propagation delay [1], the hysteresis window [38], [39], or the integration time constant [40]. For this implementation, the variable $F_{\rm SW}$ will be exploited to help spread the energy of the high-voltage high-frequency switching signal at the output of the audio amplifier to decrease the radiated EMI components.

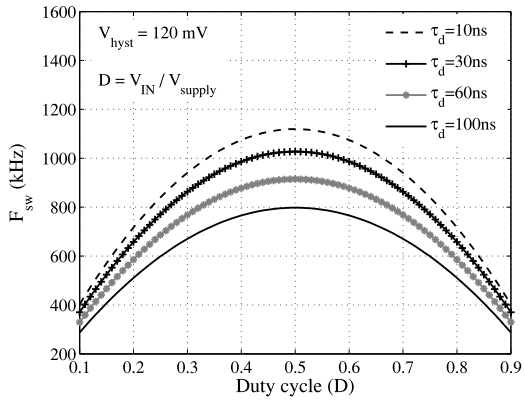

Fig. 7. Calculated switching frequency ($F_{\rm SW}$) versus duty cycle (D) for several propagation delay (τ_d) cases with a fix hysteresis window.

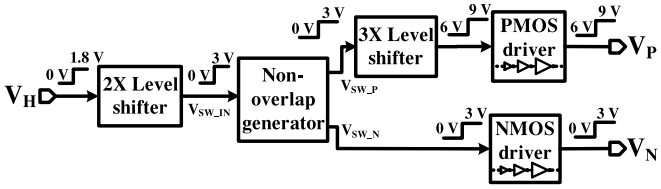

Fig. 8. Block diagram of gate drivers for the stacked-cascode output stage.

D. Gate Driver Design

Fig. 8 shows the block diagram for the proposed gate driver of the stacked-cascode output transistors for half-bridge of the output stage. The switching output of the comparators V_H is

level shifted from 1.8 to 3 V using a cross-coupled-level shifter circuit. Then, the 3-V switching signals pass through a nonoverlap signal generator to avoid excessive short-circuit current at the output stage. A nonoverlap time of 2 ns or dead time of 0.16% of the period is chosen as a tradeoff between the propagation delay τ_d in the loop, efficiency, and distortion [41]. The nonoverlapped signals are applied to the predriver circuits that will drive the gates of the stacked-cascode output transistors.

The gate signal V_P of the output PMOS switch connected to $V_{\rm CC}$ needs to switch between 6 and 9 V to avoid excessive high-voltage potential across its terminals. This is achieved by level-shifting the switching signal from 0–3 to 6–9 V using a high-speed 3X level-shifter [42] with triple-well NMOS transistors in the inverters to shift the ground level to 6 V. The PMOS predrivers also use floating inverters to keep the signal switching between 6 and 9 V.

The PMOS signal path has an extra level-shift block that introduces some delay and makes the nonoverlap delay at the output signals (V_P/V_N) asymmetrical. To correct this, the nonoverlap delay for the NMOS path was adjusted to the PMOS path by introducing extra delay elements.

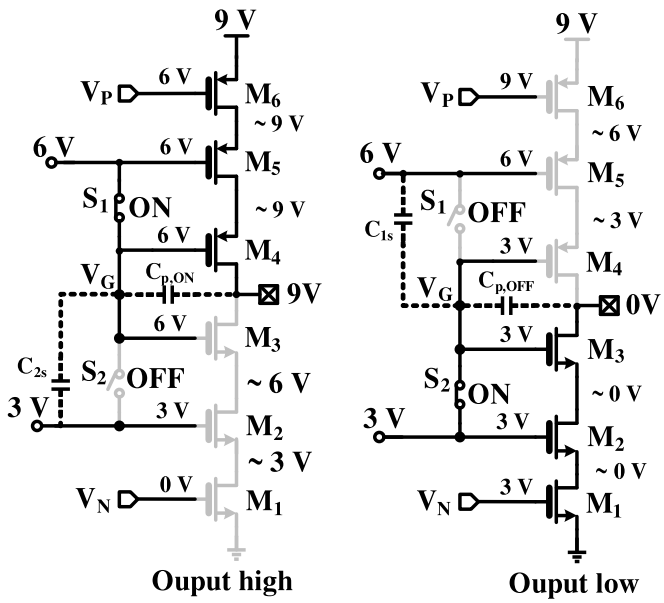

Fig. 10. Proposed stacked-cascode output stage simplified operation.

E. Stacked-Cascode H-bridge Output Stage Considerations

The main motivation to use cascodes as switches in the H-bridge output stage is to minimize its input and output capacitors to reduce the switching losses. Moreover, it allows to handle high voltages in monolithic implementations, while ensuring sufficient lifetime in a CMOS technology with a significantly lower supply voltage.

The use of cascodes in the output stage of the CDA presents two main challenges. First, the switching output signal $V_{\rm SW}$ is changing between $V_{\rm CC}$ and GND. Therefore, two different gate voltages for the cascode transistor connected to the output terminal are required [43]. This is to avoid exceeding the maximum allowed voltage potential across any of its terminals during the output high or low state. Therefore, a simple adaptive biasing structure is proposed for this implementation to safely operate the stacked-cascode H-bridge. Second, the $R_{ds\rm ON}$ and $V_{\rm SD}$ increase by adding cascodes. The impact of the conduction losses will depend on the average output current flowing through the stacked-cascode switches. Each additional stacked-cascode switch will increase the total $V_{\rm SD}$ that will increase the $P_{\rm BD}$. However, since the PZ speakers appear as a high impedance to the amplifier, the RMS current flowing through the H-bridge is small, lessening the impact of large $R_{ds\rm ON}$ and $V_{\rm SD}$ on the efficiency.

The proposed stacked-cascode output stage for driving PZ speakers is illustrated in Fig. 9. Thick-oxide 3.3-V transistors were used in the output stage; however, to achieve safe operation the top PMOS transistor has to ensure that its N-well to substrate potential does not exceed the reverse bias breakdown voltage of 10.8 V for this technology, limiting the $V_{\rm CC}$ to 9 V. Also, the thick-oxide devices can tolerate sustained operation within 10% of their voltage rating, but they can suffer from irreversible damage if the voltage across its terminals exceed the technology gate oxide breakdown voltage of 5.2 V. All the transistors have their sources tied to their bulk to avoid larger $R_{ds\rm ON}$ due to the body effect, where the NMOS cascode devices use triple-well transistors with N-well voltage ($V_{\rm NW}$) of 7.5 V to reverse bias the P-well to N-well diode.

The transistors M_1, M_6, M_7, and M_{12} are the input switches of the H-bridge. Two cascode transistors are stacked vertically on top of each input switch to avoid exceeding the maximum allowed voltage potential across any of their terminals. The gate voltage of M_2 and M_{11} is fixed to 3 V, while the gate voltage of M_5 and M_8 is fixed to 6 V. Transistors $M_{13} - M_{16}$ are switches used to alternate the gate voltage V_G of the cascode transistors M_3, M_4, M_9, and M_{10}, between 3 and 6 V, depending on the switching state. These gate voltages allow safe operation during the switching transient for the transistors. Capacitors $C_{1s} = C_{3s} = 9\,\text{pF}$ and $C_{2s} = C_{4s} = 2\,\text{pF}$ are used to stabilize the node V_G by absorbing the charge injected at this node during the switching transients.

The steady-state operation of the proposed stacked-cascode output stage of the two switching states for half of the H-bridge is depicted in Fig. 10 for the switching output high state and low state; for simplicity, transistors M_{14} and M_{13} were replaced for switches S_1 and S_2, respectively. For the switching high state, transistors $M_4 - M_6$ and switch S_1 are ON, and transistors $M_1 - M_3$ and switch S_2 are OFF. On this operating condition, the voltage at V_G is 6 V, allowing a maximum voltage drop of 3 V across any of the terminals of transistors $M_2 - M_5$. The capacitor C_{2s} was chosen to provide a low impedance path for the current injected during the low to high transition by the parasitic capacitance $C_{p,\rm ON}$, that is, mainly composed of $C_{gd,M4}$, $C_{gs,M4}$, and $C_{gs,M14}$. Similarly, for the switching low state, transistors $M_4 - M_6$ and switch S_1 are OFF, and transistors $M_1 - M_3$ and switch S_2 are ON. For this operating condition, the voltage at V_G is 3 V, allowing a maximum voltage drop of 3 V across any of the terminals of transistors $M_2 - M_5$. The capacitor C_{1s} absorbs the current injected during the high

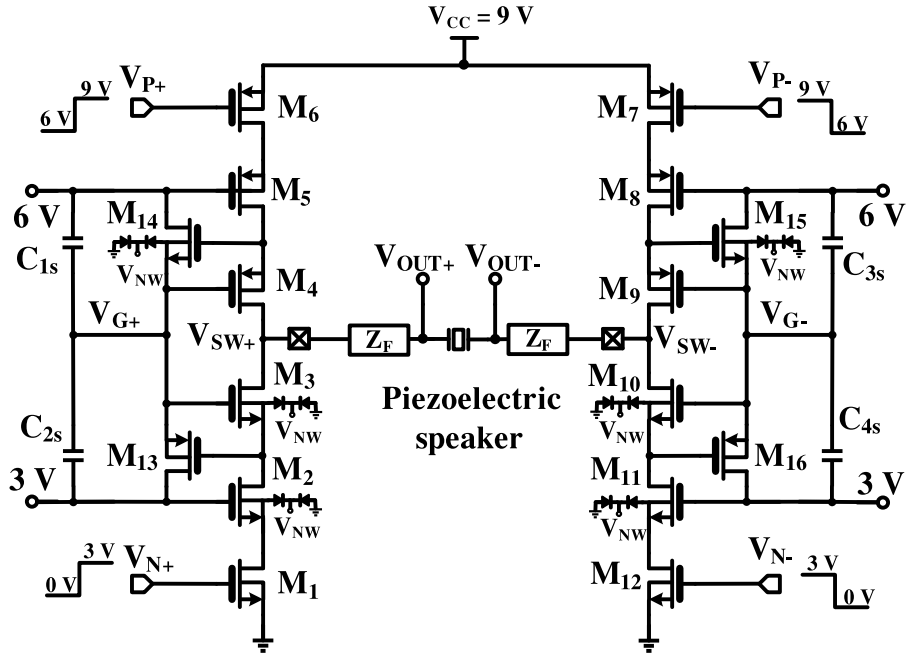

Fig. 9. Proposed stacked-cascode output stage schematic.

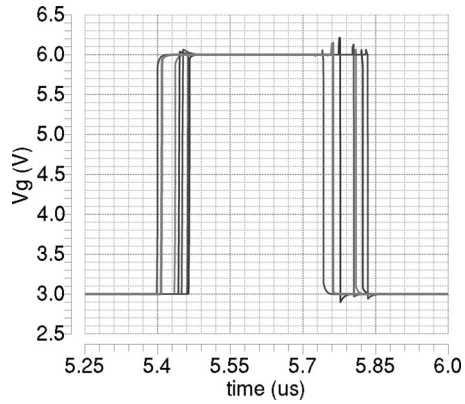

Fig. 11. Transient simulation of node V_G across process and temperature variations.

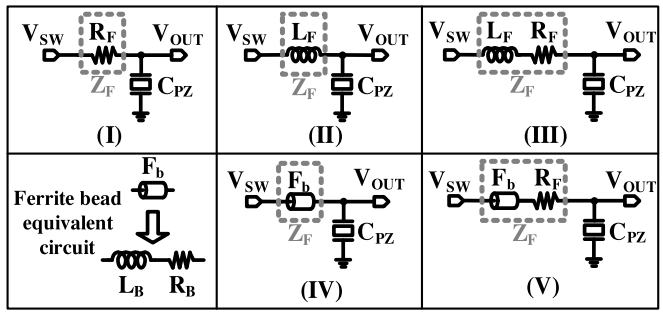

Fig. 12. Different output filter configurations for impedance Z_F together with PZ speaker equivalent impedance C_{PZ}.

to low transition by the parasitic capacitance $C_{p,\mathrm{OFF}}$ mainly comprised of $C_{gd,M3}$, $C_{gs,M3}$, and $C_{gs,M13}$.

The automatic adjustment of V_G allows a safe operation for the cascode transistors connected to the output terminal. To verify this, the circuit was simulated across process and temperature variations as shown in Fig. 11. It can be observed that V_G never exceeds the 6.5 or 2.5 V limits, avoiding stress in the transistors that could deteriorate their performance. The timing variations observed are expected since the blocks used in the implementation of the CDA will vary the loop delay τ_d by small amounts, changing the F_{SW} as shown in Fig. 7.

F. Output Filter Considerations

Another consideration about the capacitive behavior of the PZ speaker is that it presents a low impedance value at high frequencies, especially close to F_{SW}, that will increase the current consumption of the speaker if it is driven directly by the switching output signal. To minimize this effect, an impedance Z_F can be placed in series with the PZ speaker to limit the current delivered to it at high frequencies that makes it possible to use smaller transistors in the stacked-cascode output stage. An additional benefit of using Z_F in series with the PZ speaker is the inherent filtering function since the PZ speaker behaves as a capacitor. This inherent output filter will mitigate the high-frequency components of the high-voltage switching output that could negatively impact the EMI.

Several options for implementing Z_F can be selected as shown in Fig. 12; single-ended configurations are shown for simplicity. A current limit resistor R_F can be used as in (I) since its impedance is constant and independent of frequency. However, using a resistor could impact the efficiency of the overall audio system since it would dissipate power. Its value selection needs to take into account the cutoff frequency of the

low-pass filter, current limit, and power dissipation. The transfer function of the resulting first-order *RC* low-pass filter with cutoff frequency $\omega_{\rm RC}$, given by R_F and the PZ speaker impedance $C_{\rm PZ}$, is expressed as

$$\frac{V_{\rm OUT}(s)}{V_{\rm SW}(s)}_{I} = \frac{1}{1+s/\omega_{\rm RC}} = \frac{1}{1+s\cdot C_{\rm PZ}\cdot R_F}. \quad (12)$$

A more power-efficient alternative is to use a reactive element to implement Z_F. An inductor can be used as in (II). The inductor high impedance at high frequencies compensates for the low impedance of the PZ speaker to have a more constant output impedance, thereby limiting the current. Moreover, the resulting low-pass filter is second order, minimizing the EMI and the carrier signal energy at the PZ speaker. R_F is used as in (III) to introduce damping in the second-order filter to avoid unwanted peaking that can increase the output signal distortion. However, the R_F value needs to be chosen taking into account its power dissipation since the inductor ripple would dissipate real power across the resistor. The transfer function of the second-order low-pass filter, with cutoff frequency $\omega_{\rm LC}$ given by the L_F and $C_{\rm PZ}$, is expressed as

$$\frac{V_{\rm OUT}(s)}{V_{\rm SW}(s)}_{III,V} = \frac{\omega_{\rm LC}^2}{s^2+s\cdot 2\cdot\zeta\cdot\omega_{\rm LC}+\omega_{\rm LC}^2} = \frac{1/(L_F\cdot C_{\rm PZ})}{s^2+s\cdot(R_F/L_F)+1/(L_F\cdot C_{\rm PZ})}. \quad (13)$$

The main drawbacks of choosing Z_F as an inductor are the component cost and PCB area occupied. On the other hand, if an application does not require a low cutoff frequency in the low-pass filter, but requires low EMI, a ferrite bead (Fb) can be used as the reactive element to filter out the high-frequency components as in circuit (IV) and (V). The ferrite bead behaves as an inductance L_B at high frequencies and as a low-value resistor R_B at low frequencies as shown in Fig. 12. Ferrite beads cost less than an inductor and use less PCB area. However, the ferrite bead selection needs to take into consideration the peak current capability of the core material to avoid current saturation and variations in the equivalent inductance that could increase signal distortion. Also, the equivalent series resistor R_B value needs to be considered to avoid extra power dissipation.

IV. Experimental Results

The proposed CDA for PZ speakers was fabricated in 0.18-μm CMOS standard technology and tested with a System One Dual-Domain Audio Precision instrument as shown in Fig. 13. Fig. 14 shows the die micrograph of the fabricated CDA, where blocks I–IV correspond to the integrator, hysteretic comparators, predriver circuits, and stacked-cascode output stage, respectively. The total active area occupied by the proposed CDA for PZ speakers is 0.4165 mm^2, where the stacked-cascode H-bridge uses 0.2571 mm^2 (61.72%) of the active silicon area.

Fig. 15 shows the measured CDA supply current versus the output RMS voltage for a 1-kHz signal. The RMS value (i) represents the capacity of the CDA to process the demanded current by the PZ speaker; the RMS current is dominated by the switching frequency ripple at lower output voltages and by the PZ speaker at higher voltages. The average current value (ii) represents the power dissipation of the system and is expected to be very low since the load is highly reactive; it was obtained by averaging the supply current waveform for several audio signal periods. The measured quiescent supply current of the proposed CDA driving the PZ speaker at idle condition (e.g., when no audio signal is present) is 0.7 mA. The power efficiency of

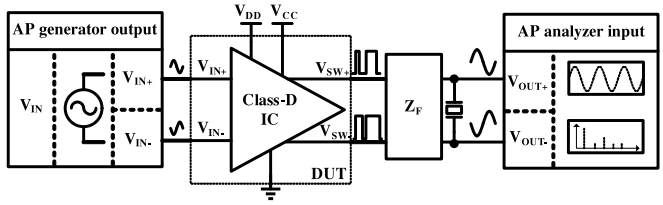

Fig. 13. Measurement test configuration of CDA for PZ speakers.

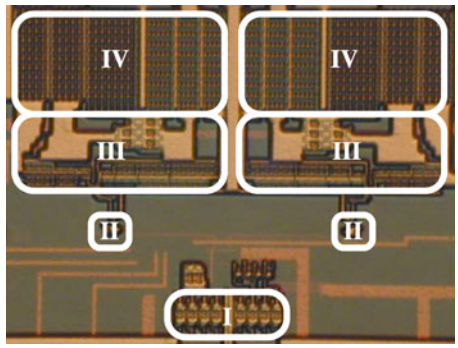

Fig. 14. Class-D audio amplifier die micrograph, I integrator (0.0715 mm^2), II comparator (0.0026 mm^2), III Predrivers (0.0852 mm^2), and IV stacked-cascode output stage (0.2571 mm^2).

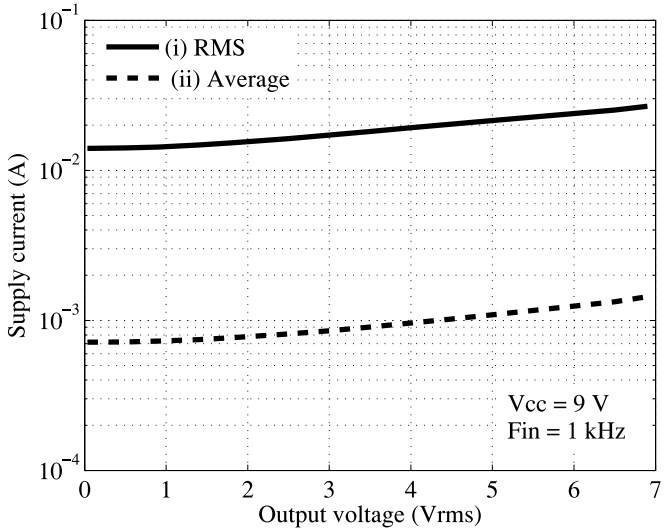

Fig. 15. Measured supply current for the CDA driving a PZ speaker with a $C_{\rm PZ} = 470$ nF at 1 kHz.

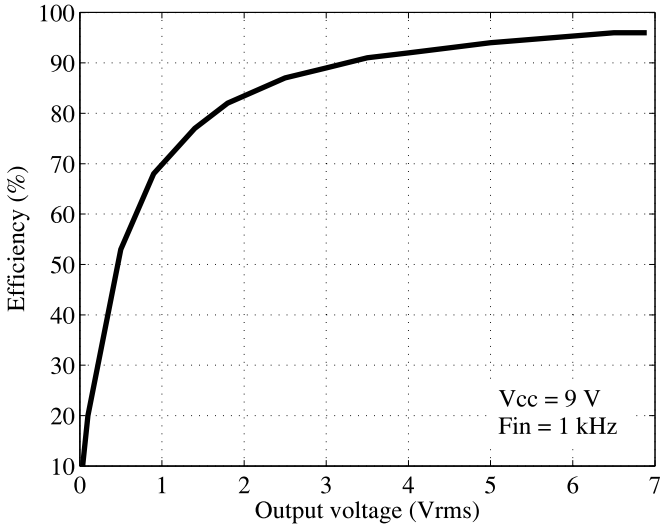

Fig. 16. Measured power efficiency for the CDA driving a PZ speaker with a $C_{\rm PZ} = 470$ nF at 1 kHz.

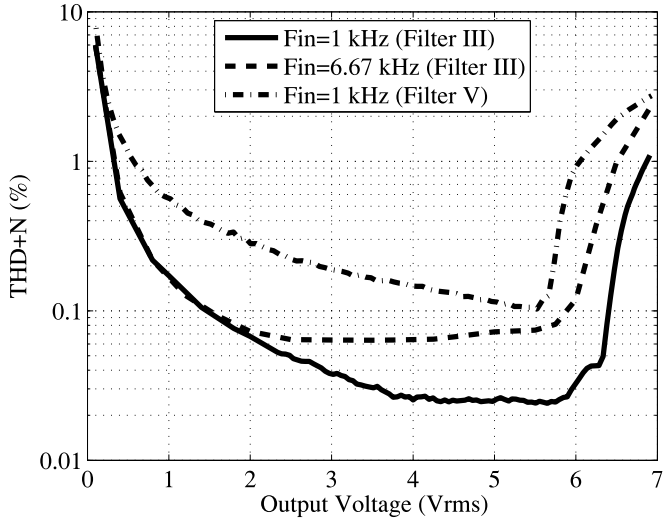

Fig. 18. Comparison of the measured THD + N versus output voltage.

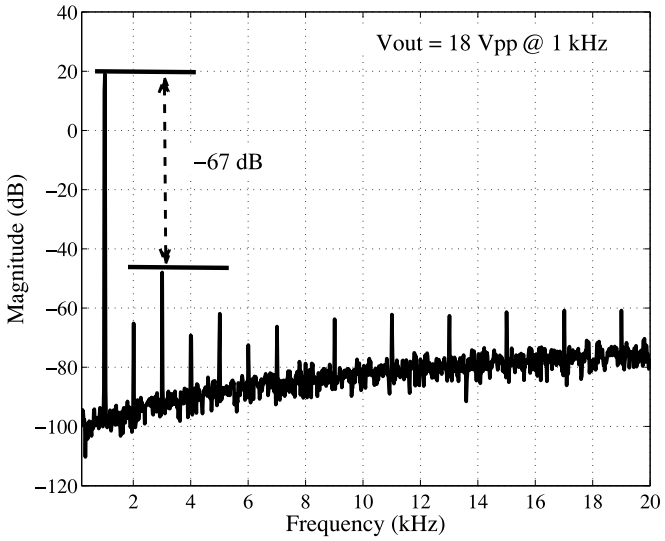

Fig. 17. Measured frequency spectrum for 18 $V_{\rm PP}$ output signal at 1 kHz.

the CDA with the PZ speaker was measured using the apparent power as described in Section II-B1. Fig. 16 shows the measured efficiency versus the output RMS voltage for a 1-kHz signal, achieving a maximum efficiency of 96%.

The measured frequency spectrum of the system for an output $V_{\rm OUT} = 18\ V_{\rm PP}$ at 1 kHz is illustrated in Fig. 17, where the difference between the fundamental tone and the highest harmonic is -67 dB. The integrated output noise voltage from 20 Hz–20 kHz (unweighted) for the idle condition was 167 μV.

To evaluate the impact of different reactive elements at the output filter, two Z_F implementations, (III) and (V) with $C_{\rm PZ} = 470$ nF, $R_F = 5.6\ \Omega$, $L_F = 47\,\mu$H, $R_B = 100\ {\rm m}\Omega$, and $L_B = 1\ \mu$H as shown in Fig. 12, were used for the THD + N measurement. The measured THD + N of the proposed CDA for both Z_F configurations with a 1-kHz signal is shown in Fig. 18; the system with the output filter (III) achieves better THD + N performance than the system with the output filter (V). The minimum measured THD + N is 0.025% and 0.1% for the CDA with Z_F configurations (III) and (V), respectively. The degradation in THD + N in filter (V) appears to be caused by the ferrite bead material due to its magnetic history curve (B-H curve) nonlinear behavior, and a nonconstant permeability μ_m that changes with the magnitude of the magnetic field and operating frequency [44]. The THD + N for the output filter (III) with a signal at 6.67 kHz is also included in Fig. 18, where a degradation in the THD + N can be observed due to the third harmonic distortion being dominant.

Power-supply intermodulation distortion (PS-IMD) provides a metric to evaluate the effect of the amplifier's power-supply noise when the audio signal is also present [9], [10], [12]. A 1-kHz sine wave with 0.5 $V_{\rm PP}$ was used as the input of the audio amplifier together with 0.2 $V_{\rm PP}$ at 217-Hz signal at the amplifier's high-voltage supply $V_{\rm CC}$. The measured frequency spectrum of the output signal is shown in Fig. 19. As can be seen, both intermodulation tones are at least 96 dB below the fundamental tone, showing that the high-frequency carrier helps to attenuate the IMD components as expected [9].

To quantify the maximum SPL of a typical PZ speaker driven by the proposed amplifier, an 18-$V_{\rm PP}$ output signal at 2 kHz was used to measure the SPL. The obtained SPL was 96 dB at 10 cm and 60 dB at 1 m, producing a comparable SPL to EM speakers but with less power consumption.

To the author's best knowledge, other CDAs for PZ speakers could not be found in the technical literature. Therefore, commercial products were used to compare the performance of the proposed CDA architecture. Table I summarizes the performance of the proposed CDA and compares it with commercial amplifiers for PZ speakers. It is evident that the proposed architecture is able to drive PZ speakers with 18 $V_{\rm PP}$ with higher linearity, high efficiency, and low power consumption.

The PZ speakers offer a compact and low power alternative to deliver outstanding audio performance in mobile devices. Future

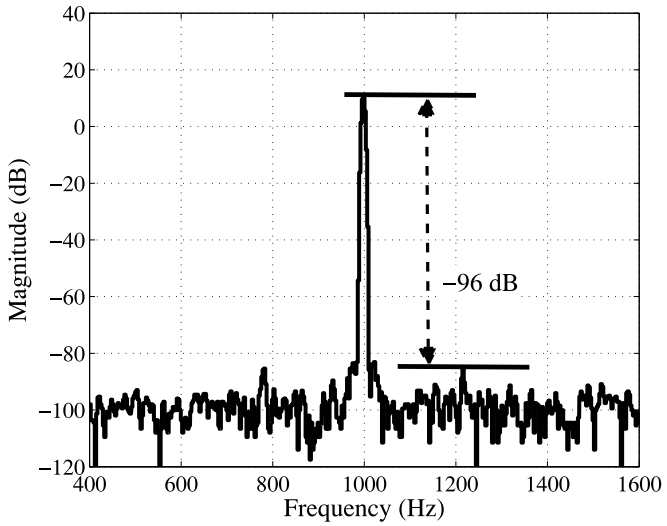

Fig. 19. Measured power-supply intermodulation frequency spectrum with 1-kHz signal and supply-ripple at 217 Hz.

TABLE I
PERFORMANCE COMPARISON WITH AUDIO AMPLIFIERS FOR PZ SPEAKERS

Parameter	This work[a]	[27]	[28]	[29]	[30]
Vout (Vpp)	18	19	14	20	14
THD + N (%)	**0.025**	0.070	0.100	0.100	0.080
I_Q (mA)	**0.7**	4	17	13	8
P_Q (mW)	**6.3**	22	61	48	29
Efficiency (%)[b]	**96**	92	72	90	84
PSRR (dB)	90	100	65	-	77
SNR (dB)	95	94	80	80	108
F_s (kHz)	750	300	250	250	-
Amplifier class	D	D	D	D	G

[a] High-Voltage supply generation not included.
[b] Estimated for 1 KHz signal using apparent power.

work for the CDA driving PZ speakers could include the speaker current sensing and smart signal processing to extract the real impedance of the device to maximize its SPL or protect the speaker from overloading. Also, a three-level modulation at the output stage could be implemented to enhance the THD + N and reduce further the EMI of the CDA by doubling the effective $F_{\rm SW}$; this would help to reduce the size of the output filter components.

V. CONCLUSION

The design tradeoffs of the CDA for driving PZ speakers were introduced, including efficiency, linearity, and EMI. A simple implementation was proposed to demonstrate the advantage of using a CDA to drive PZ speakers. The monolithic implementation used stacked-cascode thick-oxide CMOS transistors at the H-bridge output stage, avoiding expensive special high-voltage semiconductor devices and making it possible to handle high voltages in a low-voltage standard CMOS technology. The output stage's low input capacitance allowed high switching frequency to improve linearity with high efficiency. A self-oscillating modulation was used to obviate the need for a carrier signal generator and provide good audio performance using low quiescent power.

The CDA prototype driving the PZ speaker consumed 0.7 mA of quiescent current and was capable of delivering 18-$V_{\rm PP}$ output amplitude with a maximum efficiency of 96%. The minimum measured THD + N was 0.025% at 5 $V_{\rm RMS}$. The prototype occupies an active silicon area of 0.4165 mm^2 in standard CMOS 0.18-μm technology. Compared to other CDAs for PZ speakers, the proposed CDA achieved higher linearity, lower power consumption, and higher efficiency.

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