Block diagram – GP8B_V4 – Revision 1

Main connector

Peripheral communication
5Bits peripheral selection

Peripheral communication
5Depend of motherboard

External clock
50Mhz max theoretical

D-latch output registers

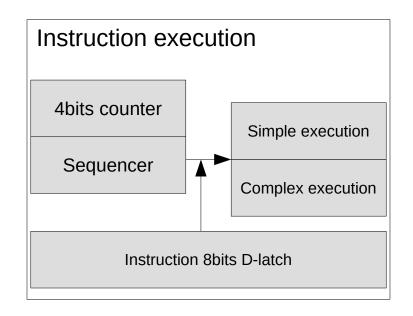
SPI

Number source selector

External Internal

External RAM

64kByte max



CPLD – 8bits ALU

XC95288XL Xilinx CPLD

JTAG access

Unused pins access