

1

2

3

4

A

A

B

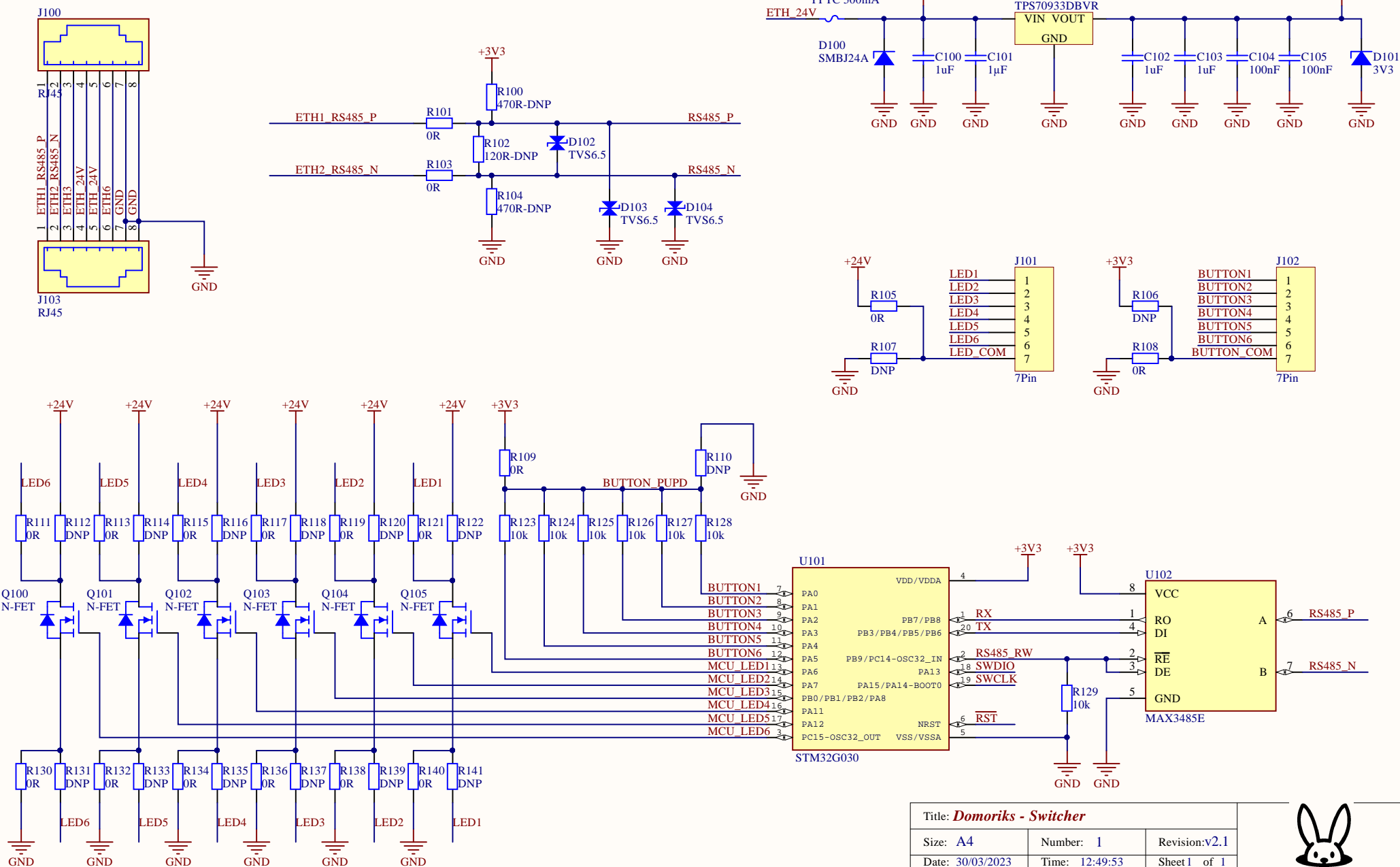
B

C

C

D

D

Title: **Domoriks - Switcher**Size: **A4**Number: **1**Revision: **v2.1**Date: **30/03/2023**Time: **12:49:53**Sheet **1** of **1**File: **MainSheet.SchDoc**

# Domoriks Switcher v2.1

power

PS435

open source  
hardware

MCU

CON1

CON2

L1

L2

L3

L4

L5

L6

COM

B1

B2

B3

B4

B5

B6

COM

## Design Rules Verification Report

Filename : C:\Users\Jorik Wittevrongel\LocalProjects\960-Domoriks\Domoriks\PCB-Design\Domoriks\_Switch\CircuitStudio\PCB.CSPcbDoc

Warnings 0  
Rule Violations 0

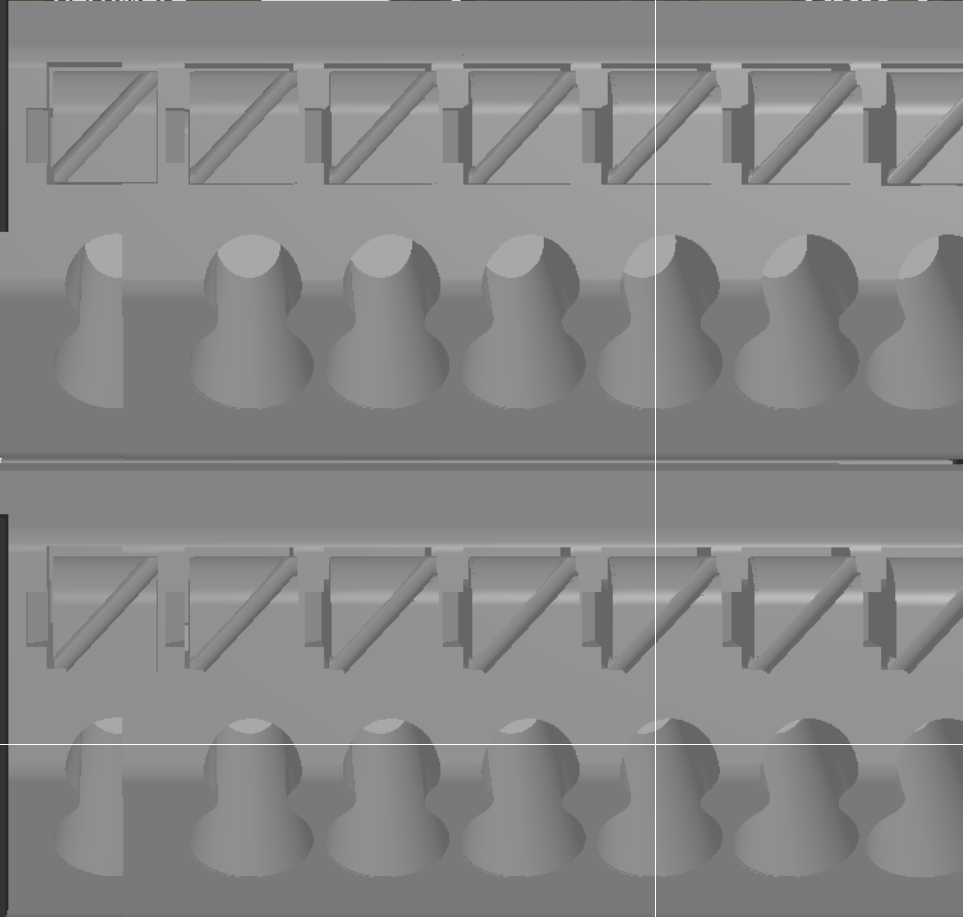
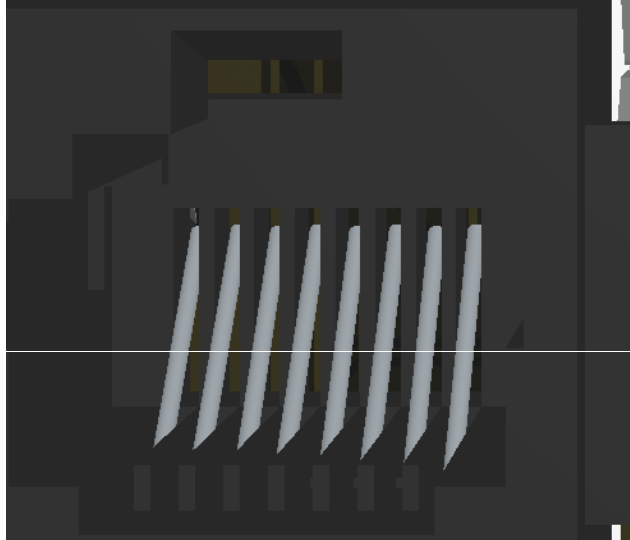
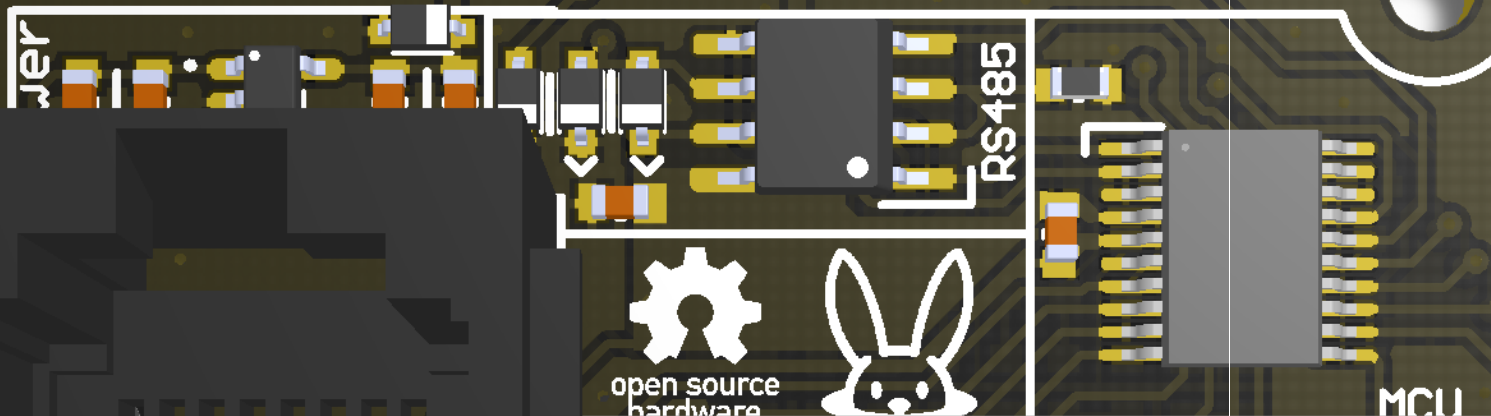
Warnings	
Total	0

Rule Violations	
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Clearance Constraint (Gap=0.25mm) (All),(All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Width Constraint (Min=0.15mm) (Max =1mm) (Preferred=0.25mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=4mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.05mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.005mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Silk primitive without silk layer	0
Unpoured Polygon (Allow unpoured: False)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for Domoriks_Switch.PrjPcb

# Domoriks Switcher v2.1



1	L1	L2	L3	L4	L5	L6	COM
2	B1	B2	B3	B4	B5	B6	COM