Kunlin Han

kunlinha@usc.edu | Phone: 123-456-7890 | Linkedin (kunlinhan) | Github (Karl-Han) | Detailed Resume

EDUCATION

- **University of Southern California (USC)** — Los Angeles, CA
  Master of Electrical Engineering (MS Honors Fellow); GPA: 4.0/4.0 — Dec 2021 - Dec 2023
- **South China Normal University (SCNU)** — Guangzhou, China
  Bachelor of Network Engineering; GPA: 3.78/4.0; Rank: 1/72 — Sep 2017 - Jun 2021

SKILLS

Programming Languages: Python, C/C++, Verilog, VHDL, SystemVerilog, Tcl, Perl, Java, Rust, SQL
Libraries: Scrapy, BeautifulSoup, Requests, Pyrogram, Django
EDA Tools: Virtuoso, Spectre, QuestaSim, Calibre, Intel Quartus, Xilinx Vivado, Innovus, StarRC, PrimeTime
Protocols: AXI, PCIe, MOESI **Tools:** UNIX, Linux, VIM, Git, Docker, Makefile

PROJECTS

- **Branch Predictor and Prefetcher Implementation and Simulation** — Aug 2023 - Oct 2023
  - Implemented and simulated bimodal predictor and correlated-branch predictor with Pin Tool to compare performance on benchmarks.
  - Designed and explored design space by trading off cache hierarchy, execution unit and issue width on OoO CPU on gem5, and achieve 25% higher throughput with 5% extra transistor count comparing with the baseline design.
  - Studied and simulated prefetchers, including Markov predictor, content-directed prefetcher and access map pattern matching prefetcher.
- **Tomasulo Out-of-Order CPU Design** — Jun 2023 - Aug 2023
  - Implemented Issue Unit, 2-stage Dispatch Unit, Re-Order Buffer and FPGA-friendly Copy-Free Check Pointing for FRAT and RRAT.
  - Integrated, synthesized and programmed the overall system on Xilinx Artix-7 FPGA board.
  - Validated the correctness of design with both simulation and on-chip logic analyzer (Chipscope).
- **512-bit 6T SRAM Array Design** — Jan 2023 - May 2023
  - Designed and drew layout of 1-bit SRAM cell, row/column decoder, sense amplifier, write driver, precharge circuit, latch and flip-flop with Cadence Virtuoso and GPDK 45nm.
  - Achieved the Read SNM of 210 mV and Write SNM of 395 mV by proper sizing with VDD=1V.
  - Integrated components into 4 8x16-bit SRAM banks to construct a 512-bit SRAM Array with the area of 2208 nm^2 in 2.6 Ghz (cycle time=0.4 ns).
  - Measured the power consumption with Spectre, in which the average consumption for reading is 21.2 fJ, the average consumption for writing is 342 fJ and leakage is 20 fJ.
  - Validated the correctness of all aforementioned components with vector file in Spectre and passed DRC and LVS.
- **Extendable Asynchronous SNN Accerlator Design** — Jan 2023 - May 2023
  - Designed extendable asynchronous SNN accelerator in SystemVerilog with SystemVerilogCSP library on a 5x5 filter and 25x25 ifmap with stride=1.
  - Implemented configurable fork-join computation module for partial computation.
  - Integrated computation modules with two memory modules on a deterministic mesh network.
  - Verified correctness of computation module and the accelerator separately with timestep=2 in QuestaSim.

EXPERIENCE

- **CS Department, USC** — Los Angeles, CA
  Graduate Teaching Assistant — May 2022 - Aug 2022

LEADERSHIP AND INVOLVEMENT

- **Hope Center, Reality L.A.** — Los Angeles, CA
  Volunteer — Mar 2022 - Aug 2022
- **Network Club, SCNU** — Guangzhou, China
  Vice President of Technical Department — Sep 2017 - Jun 2019