# Kunlin Han

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## EDUCATION

- **University of Southern California (USC)** — Los Angeles, CA
  **Master of Electrical Engineering; GPA: 4.0/4.0** — 12/2021-12/2023
- **South China Normal University (SCNU)** — Guangzhou, China
  **Bachelor of Network Engineering; GPA: 3.78/4.0; Rank: 1/72** — 09/2017-06/2021

## SKILLS

**Programming Languages**: Python, C/C++, Verilog, VHDL, SystemVerilog, Java, Rust, SQL, x86 ASM
**Libraries**: Scrapy, BeautifulSoup, Requests, Pyrogram, Django
**EDA Tools**: Virtuoso, Spectre, QuestaSim, Calibre, Intel Quartus, Xilinx Vivado
**Protocols**: AXI, PCIe, MOESI **Tools:** UNIX, Linux, VIM, Git, Docker, Makefile

## EXPERIENCE

- **CS Department, USC** — Los Angeles, CA
  **Graduate Teaching Assistant** — 05/2022-08/2022

## PROJECTS

- **Tomasulo Out-of-order CPU** — 06/2023-08/2023
  - Implemented Issue Unit, 2-stage Dispatch Unit, Re-Order Buffer and FPGA-friendly Copy-Free Check Pointing, which restores FRAT with RRAT.
  - Integrated, synthesized and programmed the overall system on Xilinx Artix-7 FPGA board.
  - Validated the correctness of design with both simulation and on-ship logic analyzer (Chipscope).
- **512-bit 6T SRAM Array Design** — 01/2023-05/2023
  - Designed and drew layout of 1-bit SRAM cell, row/column decoders, sense amplifier, write driver, precharge circuit, latch and flip-flop with Cadence Virtuoso and GPDK 45nm.
  - Achieved the Read SNM of 210 mV and Write SNM of 395 mV by proper sizing with VDD=1V while minimizing the size of 1-bit SRAM cell.
  - Integrated components into 4 8x16-bit SRAM banks to construct a 512-bit SRAM Array with the area of 2208 $nm^2$ in 2.6 Ghz (cycle time=0.4 ns).
  - Measured the power consumption with Spectre, in which the average consumption for reading is 21.2 fJ, the average consumption for writing is 342 fJ and leakage is around 20 fJ.
  - Validate the functionality of all aforementioned components with vector in Spectre and clear DRC and LVS errors.
- **Extensible Asynchronous SNN Accerlator** — 01/2023-05/2023
  - Designed extensible asynchronous SSN accelerator in SystemVerilog with SystemVerilogCSP library on a 5x5 filter and 25x25 ifmap with stride=1.
  - Implemented fork-join computation module that can calculate part of the overall computation with pre-configured parameter for extensibility.
  - Integrated computation modules with two memory modules, which contain filter map and ifmap respectively, on a mesh network.
  - Verified correctness of computation module and the accelerator separately with timestep=2 in QuestaSim.
- **Full-Custom Design Layout of Arbiter System with Multiplier and Divider** — 11/2022-12/2022
  - Designed, implemented and drew layout of a ALU supporting 5-bit multiplication and 10-bit division and a 2-1 Round-Robin-based Arbiter with multiply and divide request with the Cadence Virtuoso and GPDK 45nm.
  - Planned, routed and simulated all aforementioned components with Cadence Virtuoso and Spectre and clear DRC and LVS errors with Mentor Graphics Calibre.

## LEADERSHIP AND INVOLVEMENT

- **Hope Center, Reality L.A.** — Los Angeles, CA
  **Volunteer** — 03/2022-08/2022
- **Network Club, SCNU** — Guangzhou, China
  **Vice President of Technical Department** — 09/2017-06/2019