Kunlin Han

kunlinha@usc.edu | Phone: 123-456-7890 | Linkedin (kunlinhan) | Github (Karl-Han) | Detailed Resume

SUMMARY

Proactive learner who changed Master degree from Computer Science to Electrical Engineering at USC (GPA 4.0).
Participated proactively in courses and organized study groups. Passionate about building bonds with local community.
Eager to join $< company >$ as $< title >$ to contribute to $< company's benefit >$.

EDUCATION

- **University of Southern California (USC)** Los Angeles, CA
  Master of Electrical Engineering (MS Honors Fellow); GPA: 4.0/4.0 Dec 2021 - Dec 2023
- **South China Normal University (SCNU)** Guangzhou, China
  Bachelor of Network Engineering; GPA: 3.78/4.0; Rank: 1/72 Sep 2017 - Jun 2021

EXPERIENCE

- **CS Department, USC** Los Angeles, CA
  Graduate Teaching Assistant May 2022 - Aug 2022
  - Coordinated with Prof. Saty Raghavachary as teaching assistant (course producer) in CSCI-455X Introduction to Programming Systems Design.
  - Presented labs to help students to understand the usage and importance of debugging (GDB) and get an overview of Computer Systems.
  - Held weekly office hours to help students with problems in assignments and labs.
- **Lab 131, School of Computer Science, SCNU** Los Angeles, CA
  Instructor Sep 2018 - Jun 2021

PROJECTS

- **Branch Predictor and Prefetcher Implementation and Simulation** Aug 2023 - Oct 2023
  - Implemented and simulated bimodal predictor and correlated-branch predictor with Pin Tool to compare performance on benchmarks.
  - Designed and explored design space by trading off cache hierarchy, execution unit and issue width on OoO CPU on gem5, and achieve 25% higher throughput with 5% extra transistor count comparing with the baseline design.
  - Studied and simulated prefetchers, including Markov predictor, content-directed prefetcher and access map pattern matching prefetcher.
- **Arm Cortex-A7 MPCore Block-Level Implementation** Aug 2023 - Oct 2023
  - Developed floorplans for Cortex-A7 Core with 32KB L1 DCache and 32KB L1 ICache on 700x840um budget in Innovus using TSMC N28HPC_1P10M_5x2y2z.
  - Completed Clock Tree Synthesis and optimization with clock tree length around 410ps and clock skew around 40ps.
  - Extracted RC with StarRC, passed timing signoff in PrimeTime and applied ECO from PrimeTime to optimize slack of setup and hold.
  - Cleared DRC and LVS problems in the merged GDSII with Calibre.
- **Performance Analysis of Predictors with Pin Tool** Aug 2023 - Oct 2023
  - Implemented always-taken Branch Predictor, 2-bit Global Branch Predictor, 32-entry 2-bit Bimodal Branch Predictor, 32-entry Correlated Branch Predictor with 4-bit history.
  - Profiled the performance of the above branch predictors.
- **Tomasulo Out-of-Order CPU Design** Jun 2023 - Aug 2023
  - Implemented Issue Unit, 2-stage Dispatch Unit, Re-Order Buffer and FPGA-friendly Copy-Free Check Pointing for FRAT and RRAT.
  - Integrated, synthesized and programmed the overall system on Xilinx Artix-7 FPGA board.
  - Validated the correctness of design with both simulation and on-chip logic analyzer (Chipscope).
- **PCIe Physical Layer Design** Jun 2023 - Aug 2023

- Designed Elastic Buffer with Primed Method

- **General Purpose Graphical Processing Unit (GPGPU)** Jun 2023 - Aug 2023
  - Case study on dual-issue GPGPU with Scoreboard, SIMT stack, operand collector, banked register file, memory address coalescing.
  - Wrote multiple assembly programs to draw different geometrical shapes for GPGPU supporting SIMT stack.
- **512-bit 6T SRAM Array Design** Jan 2023 - May 2023
  - Designed and drew layout of 1-bit SRAM cell, row/column decoder, sense amplifier, write driver, precharge circuit, latch and flip-flop with Cadence Virtuoso and GPDK 45nm.
  - Achieved the Read SNM of 210 mV and Write SNM of 395 mV by proper sizing with VDD=1V.
  - Integrated components into 4 8x16-bit SRAM banks to construct a 512-bit SRAM Array with the area of 2208 nm^2 in 2.6 Ghz (cycle time=0.4 ns).
  - Measured the power consumption with Spectre, in which the average consumption for reading is 21.2 fJ, the average consumption for writing is 342 fJ and leakage is 20 fJ.
  - Validated the correctness of all aforementioned components with vector file in Spectre and passed DRC and LVS.
- **Extendable Asynchronous SNN Accerlator Design** Jan 2023 - May 2023
  - Designed extendable asynchronous SNN accelerator in SystemVerilog with SystemVerilogCSP library on a 5x5 filter and 25x25 ifmap with stride=1.
  - Implemented configurable fork-join computation module for partial computation.
  - Integrated computation modules with two memory modules on a deterministic mesh network.
  - Verified correctness of computation module and the accelerator separately with timestep=2 in QuestaSim.
- **5-stage Pipeline MIPS Processor Design** Sep 2022 - Oct 2022
  - Described Data Path Unit and Control Unit for single-cycle CPU with basic MIPS instructions.
  - Resolved problems related to Data Dependency and Early Branching.
  - Implemented 5-stage pipeline with encoded control signal, Internal Forwarding Register File and Early Branching in Verilog.
- **Full-Custom Design Layout of Arbiter System with Multiplier and Divider** Nov 2022 - Dec 2022
  - Designed, implemented and drew layout of an ALU supporting 5-bit multiplication and 10-bit division and a 2-1 Round-Robin-based Arbiter with the Cadence Virtuoso and GPDK 45nm.
  - Planned, routed and simulated all aforementioned components with Cadence Virtuoso and Spectre.
  - Cleared DRC and LVS errors with Mentor Graphics Calibre.
- **RSA, AES and SHA-3 Implementation in Rust** Sep 2019 - Dec 2019
  - Theoretically studied and programmatically implemented an array of cryptographic algorithms
  - Implemented RSA public-key algorithm, Advanced Encryption Standard (AES) symmetric encryption algorithm, and SHA-3 in Rust.

LEADERSHIP AND INVOLVEMENT

- **Hope Center, Reality L.A.** Los Angeles, CA
  Volunteer Mar 2022 - Aug 2022
  - Sorted, organized and shelved food donations for storage to preserve food and accelerate cooking.
  - Managed and distributed cooked food with other volunteers.
  - Coordinated and collaborated in cleaning utensils after food distribution.
- **Network Club, SCNU** Guangzhou, China
  Vice President of Technical Department Sep 2017 - Jun 2019
  - Managed existing members and held interviews to recruit members for Technical department.
  - Provided technical supports to on-campus IT activities, including development and maintenance of school forum, holding CTF competition.
  - Organized members to write articles about popular computer-related topics, such as resolution of DNS, anti-phishing, and published them in social media to enrich students' knowledge.

SKILLS

Programming Languages: Python, C/C++, Verilog, VHDL, SystemVerilog, Tcl, Perl, Java, Rust, SQL
Libraries: Scrapy, BeautifulSoup, Requests, Pyrogram, Django
EDA Tools: Virtuoso, Spectre, QuestaSim, Calibre, Intel Quartus, Xilinx Vivado, Innovus, StarRC, PrimeTime
Protocols: AXI, PCIe, MOESI **Tools:** UNIX, Linux, VIM, Git, Docker, Makefile