RTD2545L Series

Flat Panel Display Controller

Fully Technology
Version 1.01
Last updated: 2007/9/28

1. Overview

Realtek RTD2545L series products are all-in-one LCD monitor controllers supporting UXGA/WSXGA+/WXGA+/SXGA(optional), and integrate Realtek high performance ADC, TMDS Rx with HDCP(optional), scaling engine, OSD engine, LVDS Tx, and so on. Moreover, all products are pin compatible in QFN 48-pin package to save cost and make the design easier .The RTD2545L series derivative pin compatible products are listed below by application:

Part Number	ADC	DVI	HDCP	Resolution	Output	Package
RTD2545L	210MHz	Yes	No	UXGA/WSXGA+	LVDS	48 QFN
RTD2045L	210MHz	No	No	UXGA/WSXGA+	LVDS	48 QFN
RTD2545LH	210MHz	Yes	Yes	UXGA/WSXGA+	LVDS	48 QFN
RTD2525LH	165MHz	Yes	Yes	SXGA/WXGA+	LVDS	48 QFN

Note:
The following datasheet will take RTD2545LH as an example and if it exists any optional feature not supported in all RTD2545L series products, we will mark "optional" after it.

2. Features

General
- Programmable Scaling up and down
- No external memory required.
- Require only one crystal to generate all timing.
- Programmable 3.3V detection for multi-power domain in a system
- 2 channels 8 bits PWM output, and wide range selectable PWM frequency.
- Support input format up to 1920/1440 width(optional)
- DDC/CI(MCCS) supported

Analog RGB Input Interface
- Integrated 8-bit triple-channel 210/165 MHz ADC/PLL (optional)
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync On Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- Auto Black Level Adjustment

Digital Video Input Interface (Optional)
- Support 8-bit video (ITU 656) format input
- Built-in YUV to RGB color space converter & de-interlace

DVI Compliant Digital Input Interface (Optional)
- Single link on-chip TMDS receiver
- Up to 165Mhz
- Adaptive algorithm for TMDS capability
- Data enable only mode support
- HDCP 1.1 supported (optional)

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

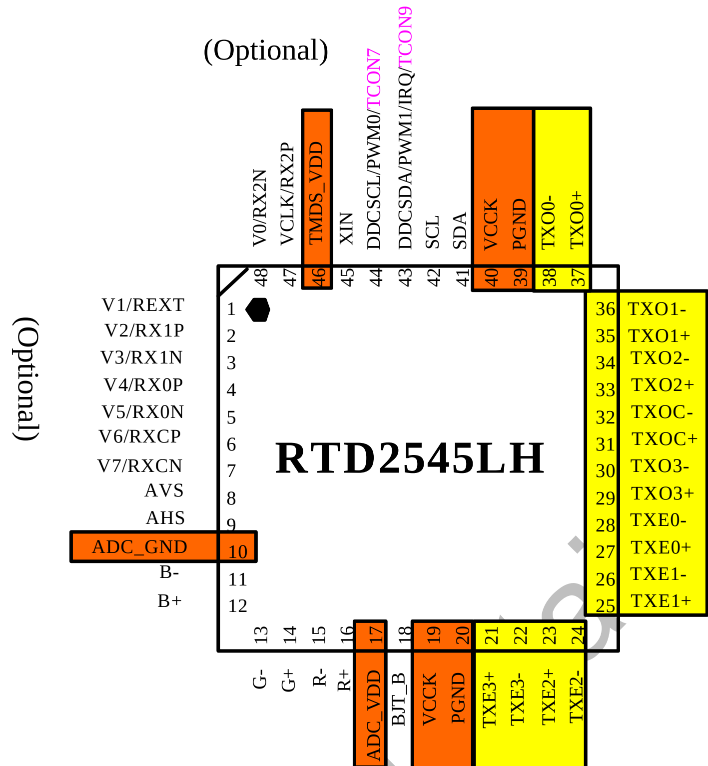
Vivid Color™
- True 10 bits color processing engine
- Dynamic Contrast Control engine(DCC) (Patent Pending)
- Independent Color Management (ICM)
- sRGB compliance
- Advanced Dithering logic for 18-bit panel color depth enhancement
- Peaking and Coring function supported
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support

Output Interface
- Fully programmable display timing generator
- 1 and 2 pixel/clock panel support and up to 170MHz, 1920/1440-pixel width (optional)
- Support LVDS output interface
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Host Interface
- Support MCU serial bus interface.
- Support MCU dual edge data latch.

Embedded OSD
- Embedded 16.5K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 16 color palette with 24bit true color selection
- Maximum 8 window with alpha-blending/ gradient/dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 hardware proportional font
- Decompress OSD font

Power & Technology
- 3.3V power supplier
- 0.18um CMOS process,48 pin QFN package
- Embedded 3.3V to 1.8V voltage regulator



Pin Out Diagram of RTD2545LH

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

INPUT PORT

Name	I/O	No	Description	Note
B0+	AI	12	Positive BLUE analog input	
B0-	AI	11	Negative BLUE analog input	
G0+	AI	14	Positive GREEN analog input	
G0-	AI	13	Negative GREEN analog input	
R0+	AI	16	Positive RED analog input	
R0-	AI	15	Negative RED analog input	
AVS	I	8	ADC vertical sync input	no power 5V tolerance
AHS	I	9	ADC horizontal sync input Adjustable Schmidt trigger	no power 5V tolerance

PLL

Name	I/O	Pin No	Description	Note
XI	AI	45	Reference clock input from external crystal or from single-ended CMOS/TTL OSC	3.3V tolerance

Host interface

Name	I/O	Pin No	Description	Note
SDA	I/O	41	Serial control I/F data (Open drain w/ ST)	5V tolerance
SCL	O	42	Serial control I/F clock (Open drain w/ ST)	5V tolerance

TMDS (When Video 8 off) (Optional)

Name	I/O	Pin No	Description	Note
REXT	AI	1	Impedance Match Reference.	
RX2P	AI	47	Differential Data Input	
RX2N	AI	48	Differential Data Input	
RX1P	AI	2	Differential Data Input	
RX1N	AI	3	Differential Data Input	
RX0P	AI	4	Differential Data Input	
RX0N	AI	5	Differential Data Input	
RXCP	AI	6	Differential Data Input	
RXCN	AI	7	Differential Data Input	

Video 8 (When TMDS off) (Optional)

Name	I/O	Pin No	Description
V8_0 ~ V8_7	I	48~7	Video 8 data input (3.3V tolerance)
VCLK	I	47	Video8 clock input (3.3V tolerance)

Power and Ground

Name	I/O	Pin No	Description
ADC_GND	G	10	ADC 1.8V Ground
ADC_VDD	P	17	ADC 1.8V Power
TMDS_VDD	P	46	TMDS 3.3V Power
VCCK	P	19/40	Digital 1.8V Power
PGND	G	20/39	Digital 1.8V Ground

LVDS Display Interface

Name	I/O	No	Description
TXE3+	O	21	

TXE3-	O	22	
TXE2+	O	23	
TXE2-	O	24	
TXE1+	O	25	
TXE1-	O	26	
TXE0+	O	27	
TXE0-	O	28	
TXO3+	O	29	
TXO3-	O	30	
TXOC+	O	31	
TXOC-	O	32	
TXO2+	O	33	
TXO2-	O	34	
TXO1+	O	35	
TXO1-	O	36	
TXO0+	O	37	
TXO0-	O	38	

- **DDC/CI Channel**

Name	I/O	No	Description
DDCSDA	I/O	43	Open drain, no power 5V tolerance with **Schmitt trigger pad**
DDCSCL	I	44	Open drain, no power 5V tolerance with **Schmitt trigger pad**

- **PWM**

Name	I/O	No	Description
PWM0	O	44	Open drain, with 5V tolerance
PWM1	O	43	Open drain, with 5V tolerance

- **MISC**

Name	I/O	No	Description
BJT_B	O	18	Embedded regulator P type BJT control pin out

- **Timing Controller**

Name	I/O	No	Description
TCON7	O	44	Timing controller output
TCON9	O	43	Timing controller output

3. Chip Data Path Block Diagram

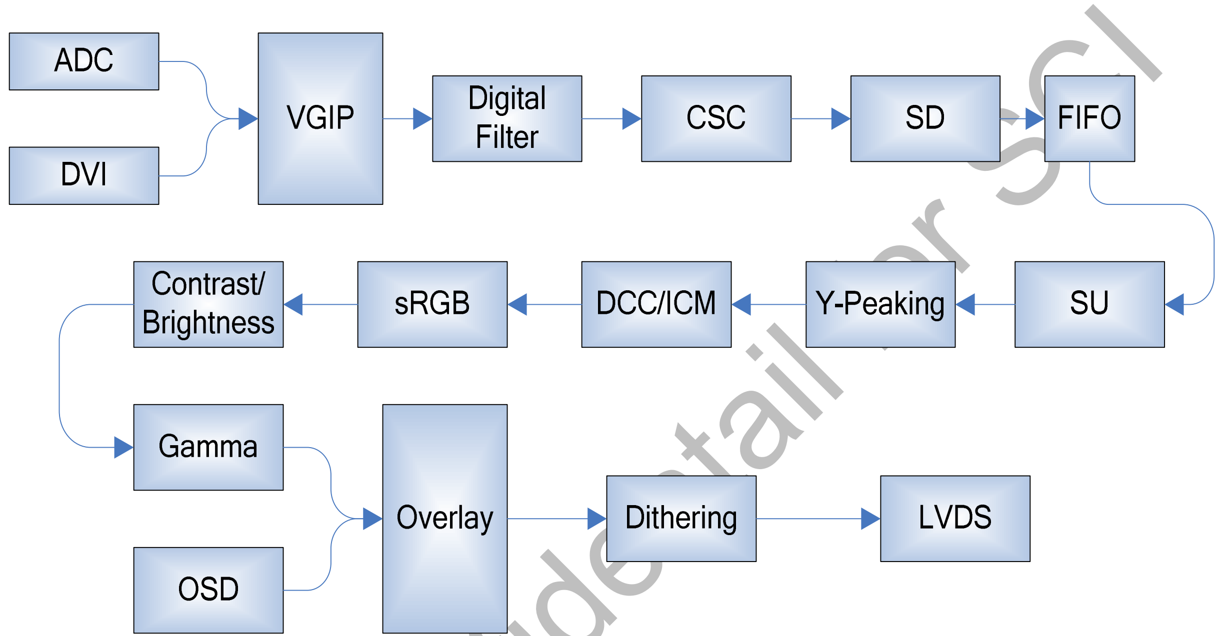


Figure 1

4. Architecture

5. Functional Description

5.1 Input

Digital Input (ITU 656)

RTD is designed to connect the interface of digital signal from video decoder. Input data is latched within a capture window defined in registers. The timing scheme designed for input devices are showed in the following diagram.

There are not H sync、V sync signals provided by the video decoder with ITU BT.656, these synchronal signals have to be generated by decoding the EAV & SAV timing reference signals.

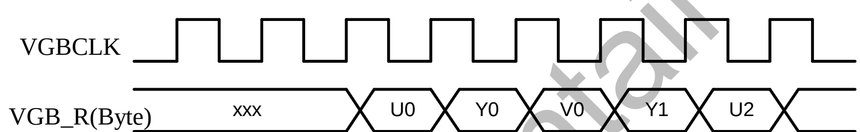


Figure 3 Input YUV 4:2:2(8-bits) Timing

Only 254 of possible 256 8-bit words may be used to express a signal value, 0 and 255 are reserved for data identification purposes. Video 8 data stream is as below:

Blanking period			Timing reference code				720 pixels YUV 422 DATA									Timing reference code				Blanking period		
…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	Cb2	Y2	…	Cr718	Y719	FF	00	00	EAV	80	10	…

Cbn: U(B-Y) colour difference component

Yn : luminance component

Crn: V(R-Y) colour difference component

SAV/EAV format

Bit 7	Bit 6(F)	Bit 5(V)	Bit 4(H)	Bit 3(P3)	Bit 2(P2)	Bit 1(P1)	Bit 0(P0)
1	Field bit 1st field F=0 2nd field F=1	Vertical blanking bit V=1 Active video V=0	H=0 in SAV H=1 in EAV	Protection bits			

Hardware can recognize the occurrence of EAV & SAV by detecting the 0xff , 0x00 , 0x00 data sequence, and then generate the Hsync、Vsync、Field signals internally by decoding the fourth word of the timing reference signal(EAV 、 SAV). F & V change state synchronously with the EAV(End of active video) reference code at the beginning of the digital line.

Bits P0, P1, P2, P3, have states dependent on the states of the bits F, V and H as shown below. At the receiver this permits one-bit errors to be corrected and two-bits errors to be detected.

Protection bits

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

Error correction

A = P1 xor F xor V
B = P2 xor F xor H
C = P3 xor V xor H
D = F xor V xor H xor P3 xor P2 xor P1 xor P0

F’ = F xor (D · A · B · C#)
V’ = V xor (D · A · B# · C)
H’ = H xor (D · A# · B · C)

SAV/EAV one-bit error occurs when D · (A + B + C)
SAV/EAV two-bit error occurs when D# · (A + B + C)

Analog Input

RTD integrates three ADC’s (analog-to-digital converters), one for each color (red, green, and blue). The sync-processor can deal with Separate-Sync, Composite-Sync, and Sync-On-Green. And the PLL can generate very low jitter clock from HS to sample the analog signal to digital data. Input data is latched within a capture window defined in registers relative to VS and HS leading edge.

TMDS Input

RTD integrates high-speed single link receiver function. It can operate up to 165 M at 25 meters cable. RTD integrates an equalizer to enhance the cable loss weakness in long cable application and the advanced tracking algorithm to have better performance in DVI RX.

Input Capture Window

Inside RTD, there are four registers IPH_ACT_STA, IPH_ACT_WID, IPV_ACT_STA & IPV_ACT_LEN to define input capture window for the selected input video on either A or B input port while programmed analog input mode. The horizontal sync (IHS) & vertical sync (IVS) signals are used from the selected port to determine the capture window region.

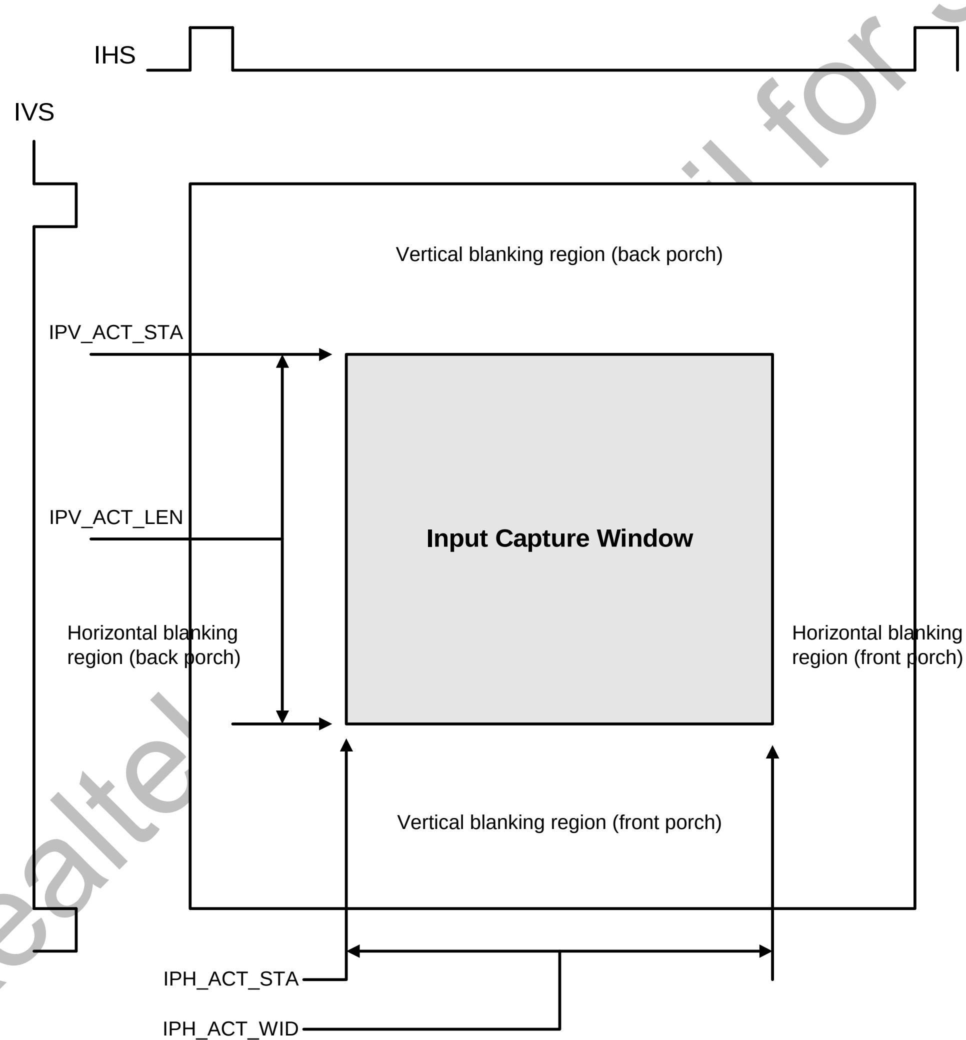


Figure 4 Input Capture Window

5.2 Output Timing

Display Output Timing

The display output port sends single/double pixel data transfer and synchronized display timing to LVDS transmitter. RTD supports 18/24 unbalanced mode LVDS signaling shown as below.

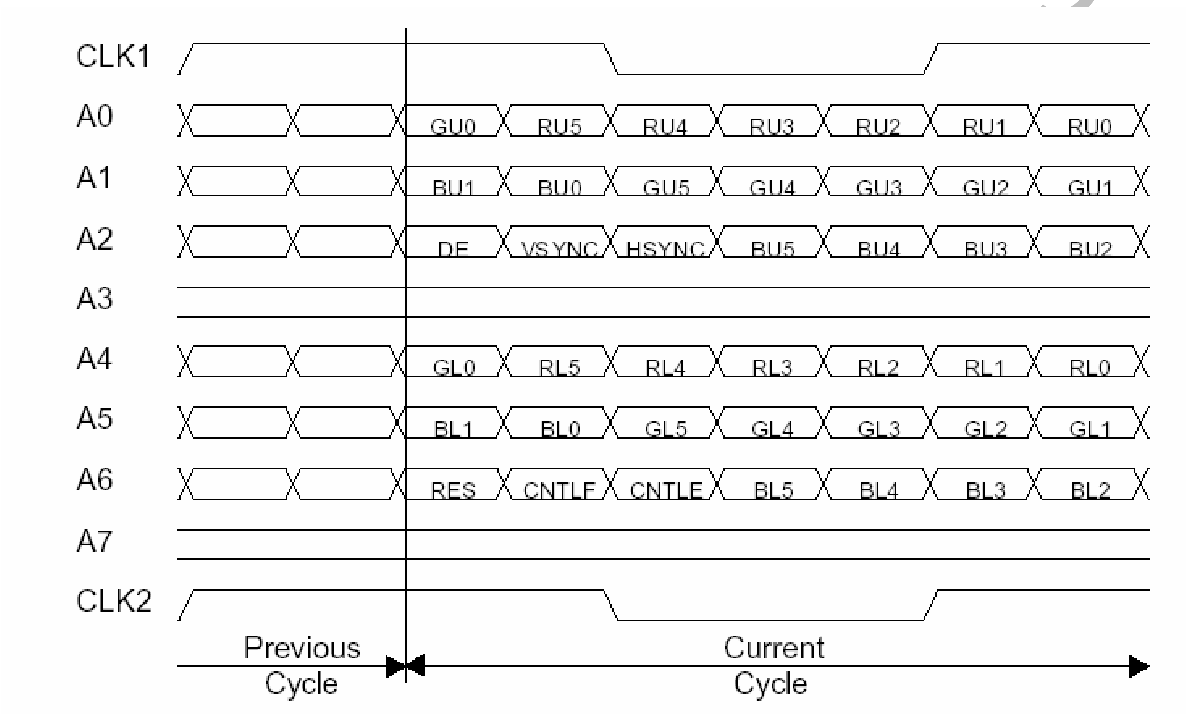


Figure 5 LVDS 18bit Display Timing

Figure 6 LVDS 24 bit Display Timing

Display Active Window

These registers define the **display active window** shown below in application of frame sync mode. Refer to the register description for detail.

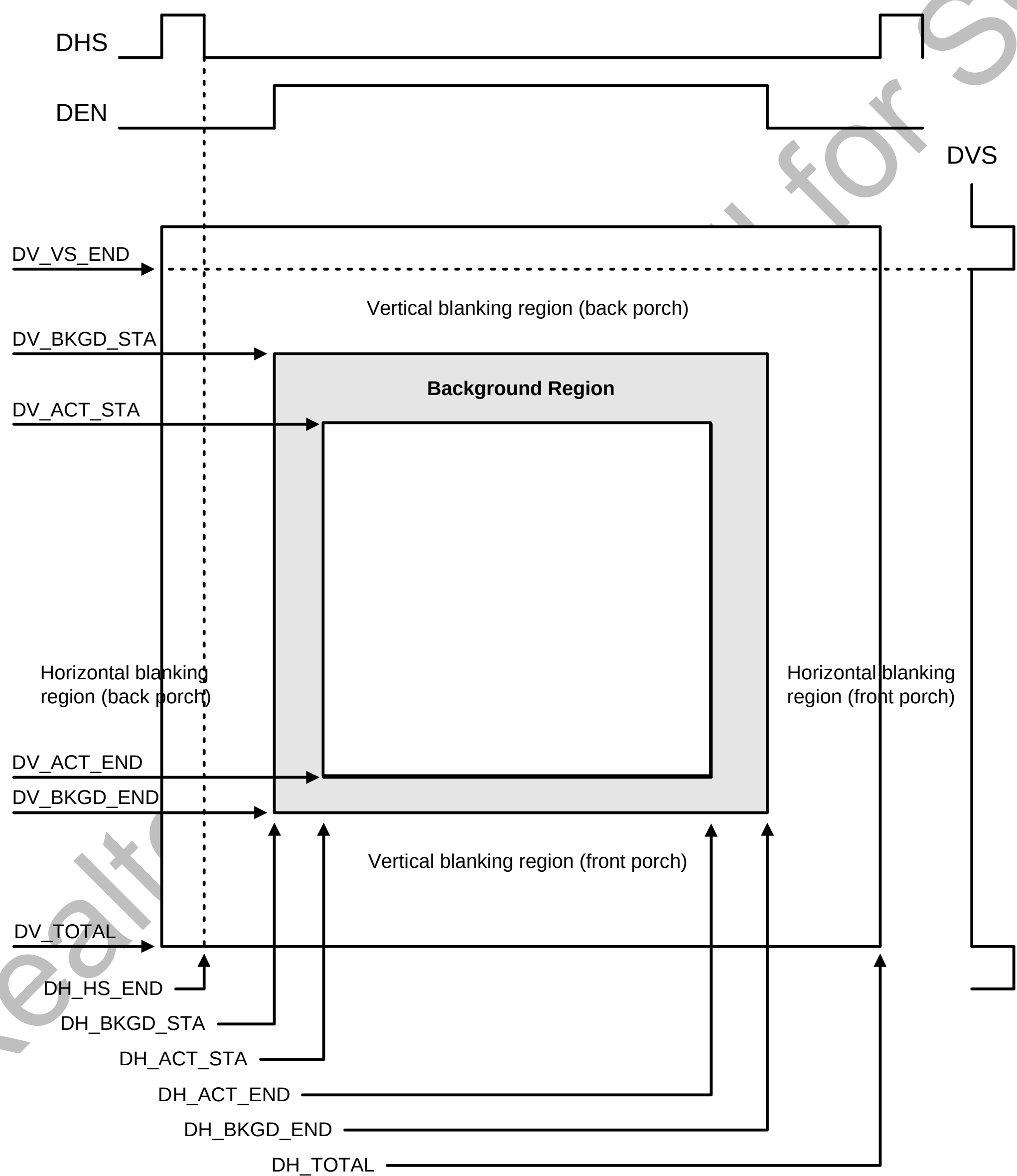


Figure 7 Display Active Window Diagram

5.3 Color Processing

Digital color R & G & B independent channel sRGB, contrast, brightness, gamma, dithering controls are built in RTD. sRGB compliance function is provided with 9 multipliers. The contrast control is performed a multiply value from 0 to 2 for each R/G/B channel. The brightness control is used to set an offset value from –512 to +511 also for each R/G/B channel. Also RTD provided 10 bit gamma and a high performance dithering function.

5.4 OSD & Color LUT

Build-In OSD

The detailed function-description of build-in OSD, please refer to the application note for RTD embedded OSD.

Color LUT & Overlay Port

The following diagram presents the data flow among the gamma correction, dithering, overlay MUX, OSD LUT and output format conversion blocks.

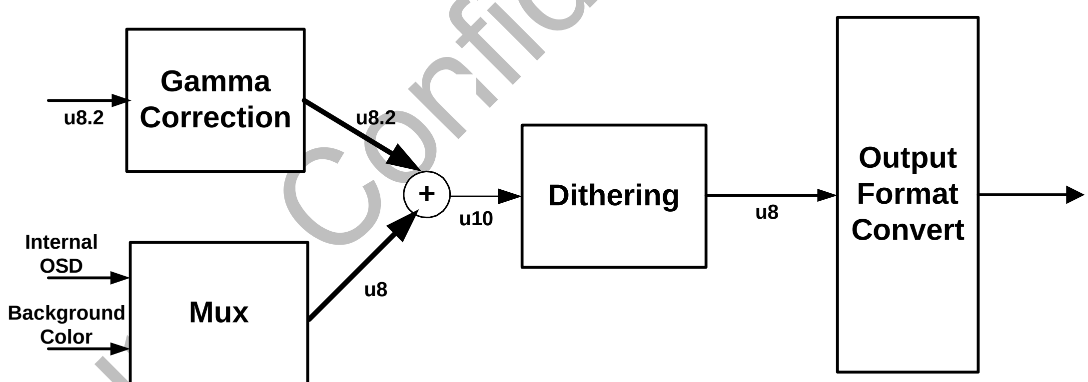


Figure 8 OSD color look-up table data path diagram

5.5 Auto-Adjustment

There are two main independent auto-adjustment functions supported by RTD, including auto-position & auto-tracking. The operation procedure is as following;

Auto-Position

1. Define the RGB color noise margin: When the value of color channel R or G or B is greater than these noise margins, a valid pixel is found.
2. Define the threshold-pixel for vertical boundary search
3. Define the boundary window of searching for horizontal boundary search.
4. Start auto-function.
5. The result can be read from register.

Auto-Tracking

1. Setting the control-registers for the function (auto-phase, auto-balance) according to the Control-Table.
2. Define the Threshold
3. Define the boundary window of searching for tracking window.
4. Start auto-function.
5. The result can be read from register

5.6 PLL System

Inside the RTD, there are four PLL systems for display clock and ADC sample clock (PLL1, PLL2, M2PLL, DPLL).

DCLK PLL

DPLL frequency = F_IN * DPM / DPN * Divider.

F_IN is input crystal frequency. DPM and DPN is in ***DPLL_M*** and ***DPLL_N***. Divider is in ***DPLL_N***, and it divide PLL frequency by 1, 2, 4 or 8.

According to parameter DPN, you must set LPF Mode in ***DPLL_WD***. If LPF Mode is 1, the charge pump current, Ich, must be DPM/17.6, while Ich must be DPM/1.67 if LPF Mode is 0. The charge pump current Ich is in ***DPLL_CRNT***.

Spread-Spectrum function is also build in DCLK to reduce EMI.

MPLL (Multiply PLL)

MPLL is a phase locked loop system providing system clock synthesis and FIFO clock.

ADC Pixel Sampling PLL

The input pixel sampling PLL of RTD compose of PLL1 and PLL2 and DDS, the hybrid PLL system inherently has a process-independent advantages comparing with pure analog PLL, DDS synthesizer is in charge of the phase-frequency control, PLL1 provided a high frequency to get a larger bandwidth letting the system fast locking, PLL2 finally synthesize the desired pixel sampling clock. The block diagram shown below describes our high-performance tracking system.

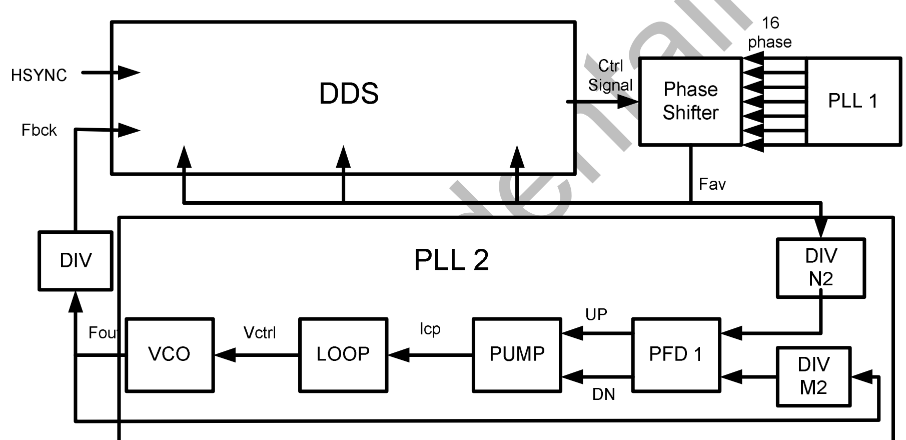


Figure 9 APLL System Block Diagram

5.7 LVD and Multi-power anti-crash system

In RTD2545LH, we introduce a Multi-power anti-crash system, RTD can detect the 3.3V power itself, and then introduce a flag. This helps us to understand the power condition of RTD (scalar side). We call the mechanism "LVD"(low voltage detection). In RTD2525LH, we introduce SCSB pin as the traditional reset in pin. When SCSB asserts low, RTD will reset itself. When ESD test is performed, the power condition will vary each side (RTD or MCU), MCU has its own LVR circuit, so it can keep awake when abnormal power condition occur. And if RTD side encounters abnormal power condition, it can reset the bit to default value, then we can monitor the bit to re-start the system including firmware and IC hardware.

For the LVD, the specification are shown below:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Detection Voltage	$-V_{det}$	1.8		2.4	V
Release Voltage	$+V_{det}$	-	2.6	-	V
Delay Time	td	50	-	-	ms

5.8 The Programmable Schmitt Trigger of HSYNC

To get better waveform of the input HSYNC, we have a programmable Schmitt Trigger circuit. For different HSYNC amplitude and polarity, we can select different setting of the threshold voltage. The $\mathbf{V_t}^+$ and the $\mathbf{V_t}^-$ can be selected by register CR97

We can select the old mode or the new mode. When using the new mode we can directly determine the positive threshold voltage (1.4V, 1.6V… 2.6V), and we can choose the hysterias from the $\mathbf{V_t}^+$ to determine the $\mathbf{V_t}^-$ (0.6V, 0.8V, 1.0V, 1.2V). We also can finely tune the voltage by minus 0.1V. For application, we can select different threshold voltage by the polarity of the HSYNC. The control register is CR97

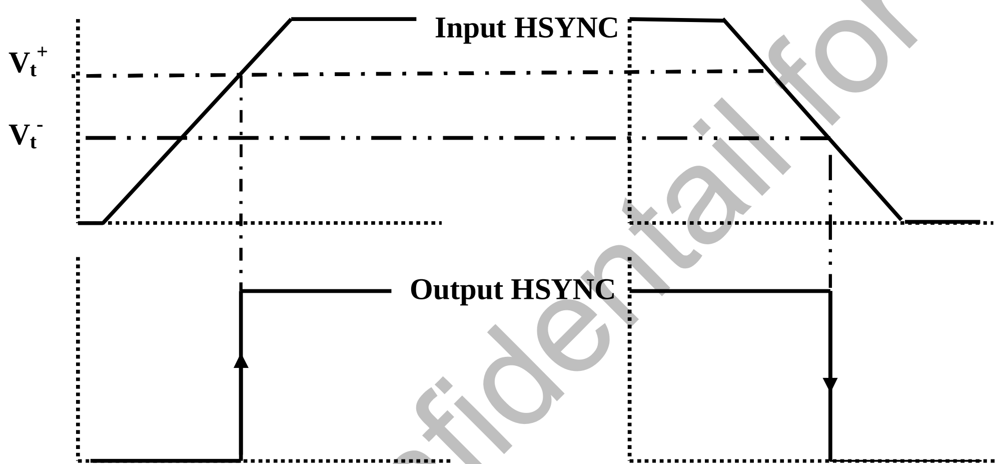


Figure 10 the Schmitt Trigger Behavior Diagram

6. Register description

Global event flag

Reading unimplemented registers will return 0.

Address: 00 **ID_REG** **Default: 41h**

Bit	Mode	Function
7:0	R	**MSB 4 bits:** 0100 product code **LSB 4 bits:** 0001 rev. code

Address: 01 **HOSTCTRL** **Default: 02h**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**Reset Check** Once scalar is reset, this value will be cleared to 0. You can write 1 to this bit for checking if LVR is ever triggered.
5:3	R/W	**Reserved to 0**
2	R/W	**Power Down Mode Enable** 0: Normal (Default) 1: Enable power down mode Turn off ADC R/G/B/Banggap/DPLL/LVDS/PLL1/PLL2/SOG/SYNC PROC/TMDS
1	R/W	**Power Saving Mode Enable** 0: Normal 1: Enable power **saving** mode (Default) Turn off ADC R/G/B/DPLL/LVDS/PLL1/PLL2 **But don't turn off** bias current of V0H0
0	R/W	**Software Reset Whole Chip (Low pulse at least 8ms)** 0: Normal (Default) 1: Reset (All registers are reset to default except CR01 HOST_CTRL & M2PLL)

Address: 02 **STATUS0 (Status0 Register)** **Default: 00h**

Bit	Mode	Function
7	R	**ADC_PLL Non-Lock:** If the ADC_PLL non-lock occurs, this bit is set to "1".
6	R	**Input VSYNC Error** If the input vertical sync occurs within the programmed active period, this bit is set to "1".
5	R	**Input HSYNC Error** If the input horizontal sync occurs within the programmed active period, this bit is set to "1".

4	R	**Input ODD Toggle Occur (For internal field odd toggle, refer to CR0F[5])** If the ODD signal (From SAV/EAV) toggle occurs, this bit is set to “1”.
3	R	**Video8 Input Vertical/Horizontal Sync Occurs** If the YUV input V or H sync edge occurs, this bit is set to “1”.
2	R	**ADC Input Vertical/Horizontal Sync Occurs** Input V or H sync edge occurs; this bit is set to “1”.
1	R	**Input Overflow Status** (Frame Sync Mode) If an overflow in the input data capture buffer occurs, this bit is set to “1”.[1]
0	R	**Line Buffer Underflow status** (Frame Sync Mode) If an underflow in the line-buffer occurs, this bit is set to “1”.

Write to clear status.

Address: 03 **STATUS1 (Status1 Register)** **Default: 00h**

Bit	Mode	Function
7	R	**Line Buffer Overflow Status**[2] 1: Line Buffer overflow has occurred since the last status cleared
6	R	**Line Buffer Underflow Status** 1: Line Buffer underflow has occurred since the last status cleared
5	R	**DENA Stop Event Status** 1: If the DENA stop event occurred since the last status cleared
4	R	**DENA Start Event Status** 1: If the DENA start event occurred since the last status cleared
3	R	**DVS Start Event Status** 1: If the DVS start event occurred since the last status cleared
2	R	**IENA Stop Event Status** 1: If the IENA stop event occurred since the last status cleared
1	R	**IENA Start Event Status** 1: If the IENA start event occurred since the last status cleared
0	R	**IVS Start Event Status** 1: If the IVS start event occurred since the last status cleared

Write to clear status.

Address: 04 **IRQ_CTRL0 (IRQ Control Register 0)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Internal IRQ Enable: (Global)** 0: Disable these interrupt.

[1] Only the first event of input overflow/underflow will be recorded at the same time.

[2] Both input overflow/underflow status will be recorded whenever it happens.

		1: Enable these interrupt. The IRQ event of CRF9 & CR04 will be logically "OR" together.
6	R/W	**IRQ (ADC_PLL Non-Lock)** 0: Disable the ADC_PLL non-lock error event as an interrupt source 1: Enable the ADC_PLL non-lock error event as an interrupt source
5	R/W	**IRQ (Input VSYNC/HSYNC Error) (DEN across Vsync or Hsync)** 0: Disable the Input VSYNC/HSYNC error event as an interrupt source 1: Enable the Input VSYNC/HSYNC error event as an interrupt source
4	R/W	**IRQ (Input ODD Toggle Occur) (EAV/SAV from Video8)** 0: Disable the Input ODD toggle event as an interrupt source 1: Enable the Input ODD toggle event as an interrupt source
3	R/W	**IRQ (Video8 Input Hsync/Vertical Sync Occurs)** 0: Disable the Video8/16 Input Hsync or Vsync event as an interrupt source 1: Enable the Video8/16 Input Hsync or Vsync event as an interrupt source
2	R/W	**IRQ (ADC Input Hsync/Vertical Sync Occurs)** 0: Disable the ADC Input Hsync or Vsync event as an interrupt source 1: Enable the ADC Input Hsync or Vsync event as an interrupt source
1	R/W	**IRQ (Line Buffer Underflow/Overflow Status)** 0: Disable the Line Buffer underflow/overflow event as an interrupt source 1: Enable the Line Buffer underflow/overflow event as an interrupt source
0	R/W	**IRQ(Input ENA Start Event Occurred Status)** 0: Disable this event as an interrupt source 1: Enable this event as an interrupt source

Input Video Capture

Address: 05 **VGIP_CTRL (Video Graphic Input Control Register)** **Default: 00h**

<table>
<tr><th>Bit</th><th>Mode</th><th>Function</th></tr>
<tr><td>7</td><td>R/W</td><td>8 bit Random Generator
0: Disable(Default)
1: Enable</td></tr>
<tr><td>6</td><td>R/W</td><td>Input Test Mode:
0: Disable (Default)
1: Video8 input will go through RGB channel, AVS=>IVS, AHS=>IHS, VCLK=>ICLK</td></tr>
<tr><td>5</td><td>R/W</td><td>VGIP Double Buffer Ready
0: Not Ready to Apply
1: Ready to Apply
When the list table of CR05 [4] is set, then enable CR05 [5], finally, hardware will auto load these value into RTD as the trigger event happens and clear CR05 [5] to 0.</td></tr>
<tr><td>4</td><td>R/W</td><td>VGIP Double Buffer Mode Enable(Each register describe below has its own double buffer)
0: Disable (Original- Write instantly by MCU write cycles)
1: Enable (Double Buffer Function Write Mode)
<table>
<tr><th>Register</th><th>Trigger Event</th></tr>
<tr><td>IPH_ACT_STA(CR09,CR0A)</td><td>IDEN STOP
(Falling edge of IDEN)</td></tr>
<tr><td>IPV_ACT_STA (CR09,CR0A)
IV_DV_LINES (CR40)</td><td>IDEN STOP
(Falling edge of IDEN)</td></tr>
<tr><td>IHS Delay(for capture)
(CR12, CR13[0])</td><td>IDEN STOP
(Falling edge of IDEN)</td></tr>
<tr><td>PLLPHASE(CRAB,CRAC)
Add 1-clk Delay to IHS Delay
(CR07[4])
HSYNC Synchronize Edge
(CR07[3])</td><td>IDEN STOP
(Falling edge of IDEN)</td></tr>
<tr><td>IVS_DELAY(for capture)
(CR[11],CR13[1])</td><td>IDEN STOP
(Falling edge of IDEN)</td></tr>
</table></td></tr>
<tr><td>3:2</td><td>R/W</td><td>Input Pixel Format
00: Embedded ADC (ADC_HS)(Default)
01: Embedded TMDS
10: Video 8
11: Reserved</td></tr>
</table>

1	R/W	**Input graphic/video mode** 0: From analog input (input captured by 'Input Capture Window') (Default) 1: From digital input (captured start by 'enable signal', but sill stored in 'capture window size')
0	R/W	**Input Sampling Run Enable** 0: No data is transferred (Default) 1: Sampling input pixels

Address: 06 VGIP_SIGINV (Input Control Signal Inverted Register) Default: 00h

Bit	Mode	Function
7	R/W	**Safe Mode** 0: Normal (Default) 1: Safe Mode Enable, mask 1 frame IVS of every 2 frame IVS, slow down input frame rate.
6	R/W	**IVS Sync with IHS Control (avoid VS bouncing)** 0: Enable (Default) 1: Disable
5	R/W	**HS Signal Inverted for Field Detection** 0: Negative Edge (Default) 1: Positive Edge
4	R/W	**Interlace source ODD signal invert enable** 0: Not inverted (ODD = positive polarity) (Default) 1: Inverted (ODD = negative polarity)
3	R/W	**Input VS Signal Polarity Inverted** 0: Not inverted (VS = positive polarity) (Default) 1: Inverted (VS = negative polarity)
2	R/W	**Input HS Signal Polarity Inverted** 0: Not inverted (HS = positive polarity) (Default) 1: Inverted (HS = negative polarity)
1	R/W	**Input ENA Signal Polarity Inverted** 0: Not inverted (input high active) (Default) 1: Inverted (while input low active)
0	R/W	**Input Clock Polarity** 0: Rising edge latched (Default) 1: Falling edge latched

Address: 07 VGIP_DELAY_CTRL Default: 00h

Bit	Mode	Function
7	R	**6-Iclk-delay HS level latched by VS rising edge**
6	R	**HS level latched by VS rising edge**

5	R	**HS level latched by 6-Iclk-delay VS rising edge**
4	R/W	**Add one clock delay to IHS delay** 0: Disable (Default) 1: Enable
3	R/W	**HSYNC Synchronize Edge** 0: HSYNC is synchronized by the positive edge of the input clock 1: HSYNC is synchronized by the negative edge of the input clock (HSYNC source is selected by **CR48[0]** and then synchronized)
2	R/W	**VSYNC Synchronize Edge** 0: latch VS by the negative edge of input HSYNC(Default) 1: latch VS by the positive edge of input HSYNC
1:0	R/W	**Input Clock Delay Control:** 00: Normal (Default) 01: 1ns delay 10: 2ns delay 11: 3ns delay

Address: 08 **VGIP_ODD_CTRL (Video Graphic Input ODD Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**ODD invert for ODD-Controlled-IVS_delay.** 0: Not Invert (Default) 1: Invert
6	R/W	**ODD-Controlled-IVS delay one line Enable** 0: Disable (Default) 1: Enable **For both Auto and Capture**
5	R/W	**Safe Mode ODD inversion** 0: Not inverted (Default) 1: Inverted
4	R/W	**Force ODD toggle enable (Without ODD/EVEN toggle select in Safe Mode)** 0: Disable (Default) 1: Enable
3	R/W	**Video 4:2:2->4:4:4 enable before Scale Down (Duplicate)** 0: Disable (Default) 1: Enable i.e. This bit should be always enable when in Video8 mode.
2	R/W	**Decode Video8 when ADC or TMDS active**

		0: Disable (Default) 1: Enable
1	R/W	**EAV Error Correction Enable in Video8** 0: Disable 1: Enable
0	R/W	**Internal ODD signal selection** 0: ODD signal from EAV ~~or YPbPr~~ (Default) 1: Internal Field Detection ODD signal (Also support under VGA, DVI input)

Input Frame Window

(All capture windows setting unit is 1)

Address: 09 **IPH_ACT_STA_H (Input Horizontal Active Start)** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**Input Source Horizontal Active Start** -- High Byte [10:8]

Address: 0A **IPH_ACT_STA_L (Input Horizontal Active Start Low)** **Default: 00h**

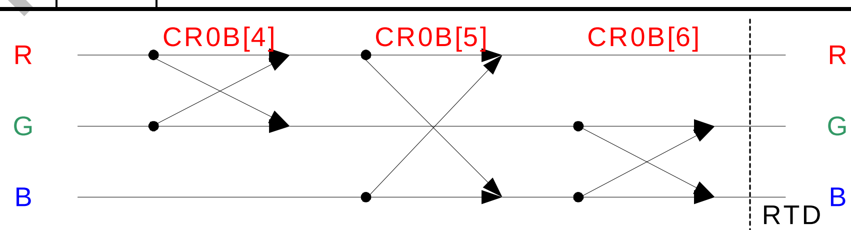
Bit	Mode	Function
7:0	R/W	**Input Source Horizontal Active Start** -- Low Byte [7:0]

- In analog mode, the number of pixel clocks from the leading edge of HS to the first pixel of the active line.

  Target = IPH_ACT_STA(>=2) +2,
- In digital mode, the **IPH_ACT_STA** is actually the same as it set.

Address: 0B **IPH_ACT_WID_H (Input Horizontal Active Width High)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Video8 Port Input Latch Bus MSB to LSB Swap Control:** 0: Normal (Default) 1: Switched Video8 port MSB to LSB sequence into LSB to MSB
6	R/W	**ADC input G/B Swap** 0: No Swap 1: Swap
5	R/W	**ADC input R/B Swap** 0: No Swap 1: Swap
4	R/W	**ADC input R/G Swap** 0: No Swap 1: Swap
3	R/W	**Double Clock Input** 0: Single Clock 1: Double Clock this bit should be set double clock when using video 8 input
2:0	R/W	**Input Source Horizontal Active Width** – High Byte [10:8]



Address: 0C **IPH_ACT_WID_L (Input Horizontal Active Width Low)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input Source Horizontal Active Width** -- Low Byte [7:0]

This register defines the number of active pixel clocks to be captured.

Address: 0D **IPV_ACT_STA_H (Input Vertical Active Start High)** **Default: 00h**

Bit	Mode	Function
2:0	R/W	**Input Source Vertical Active Start** – High Byte [10:8]

Address: 0E **IPV_ACT_STA_L (Input Vertical Active Start Low)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input Source Vertical Active Start** – Low Byte [7:0]

The numbers of lines from the leading edge of selected input source VSYNC to the first line of the active window.

The value above should be larger than 1.

Address: 0F **IPV_ACT_LEN_H (Input Vertical Active Lines)** **Default: 00h**

Bit	Mode	Function
7	R	**SAV/EAV two-bit error (write to clear)**
6	R	**SAV/EAV one-bit error (write to clear)**
5	R	**Internal Field Detection ODD toggle happen** **The function should be worked under no input clock**
4:3	R	**The number of input HS between 2 input VS. LSB bit [1:0]**
2:0	R/W	**Input Source Vertical Active Lines** – High Byte [10:8]

Address: 10 **IPV_ACT_LEN_L (Input Vertical Active Lines)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input Source Vertical Active Lines** – Low Byte [7:0]

This register defines the number of active lines to be captured.

Address: 11 **IVS_DELAY (Internal Input-VS Delay Control Register)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input VS delay count by Input HSYNC [7:0]** It's IVS delay for capture and digital filter, not for auto function

Address: 12 **IHS_DELAY (Internal Input-HS Delay Control Register)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Input HS delay count by Input clock [7:0]** It's IHS delay for capture and digital filter, not for auto function

Address: 13 **VGIP_HV_DELAY** **Default: 00h**

Bit	Mode	Function
7:6	R/W	**Input HS delay count by input clock for Auto function**

		00: No delay 01: 32 pixels 10: 64 pixels 11: 96 pixels
5:4	R/W	**Input VS delay count by input HSYNC for Auto function** 00: No delay 01: 3 line 10: 7 line 11: 15 line
3:2	--	**Reserved to 0**
1	R/W	**Input VS delay count by Input HSYNC[8]**
0	R/W	**Input HS delay count by Input clock[8]**

FIFO Window

Address: 14 **DRL_H_BSU (Display Read High Byte Before Scaling-Up)** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved**
6:4	R/W	**Display window read width before scaling up:** High Byte [10:8]
3	--	**Reserved**
2:0	R/W	**Display window read length before scaling up:** High Byte [10:8]

Address: 15 **DRW_L_BSU (Display Read Width Low Byte Before Scaling-Up)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Display window read width before scaling up:** Low Byte [7:0]

Address: 16 **DRL_L_BSU (Display Read Length Low Byte Before Scaling-Up)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Display window read length before scaling up:** Low Byte [7:0]

- The setting above should be use 2 as unit

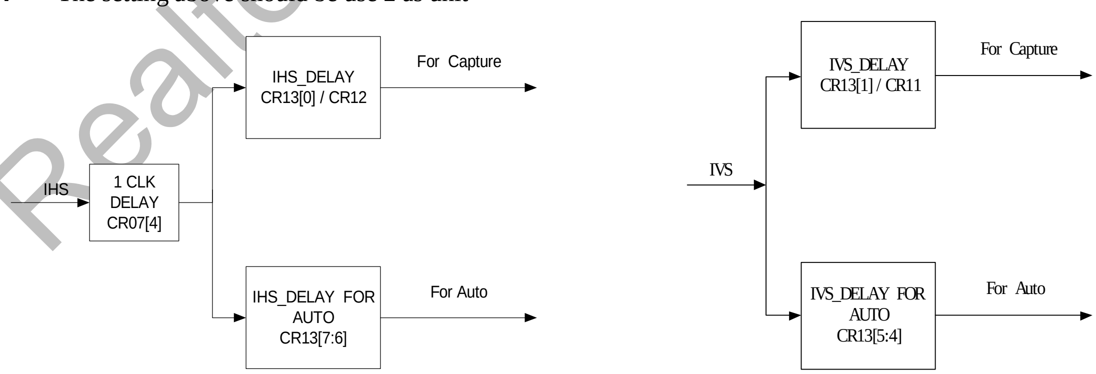


Figure 2 IHS_DELAY Path Diagram

Digital Filter

Address: 17 **DIGITAL_FILTER_CTRL** **Default: 00h**

Bit	Mode	Function
7:4	R/W	**Access Port Write Enable** 0000: disable 0001: phase access port 0010: negative smear access port 0011: positive smear access port 0100: negative ringing access port 0101: positive ringing access port 0110: mismatch access port 0111: Y(B)/Pb(G)/Pr(R) channel digital filter enable 1xxx: noise reduction access port
3:2	R/W	Two condition occur continuous (ringing to smear) 00: disable(hardware is off , depend on firmware) 01: only reduce ringing condition 10: only reduce smear condition 11: no adjust (hardware is on, but do nothing)
1	R/W	**When noise reduction and mismatch occur, select** 0: mismatch 1: noise reduction
0	--	**Reserved to 0**

Address: 18 **DIGITAL_FILTER_PORT** DIGITAL_FILTER_CTRL [7:4] = 0111 **Default: 00h**

Bit	Mode	Function
7	R/W	**Y EN (G)**: function enable 0: function disable 1: function enable
6	R/W	**Pb EN (B)** : function enable 0: function disable 1: function enable
5	R/W	**Pr EN (R)** : function enable 0: function disable 1: function enable
4	R/W	**Initial value**: 0: raw data 1: extension

3:0	--	**Reserved to 0**

Bit7~5 only support both Y_EN(100) and RGB enable (111).

DIGITAL_FILTER_PORT DIGITAL_FILTER_CTRL[7:5] = 000 ~ 110 **Default: 00h**

Bit	Mode	Function
7	R/W	**EN**: function enable 0: function disable 1: function enable
6:4	R/W	**THD_OFFSET** Threshold value of phase and mismatch and noise reduction or offset value of smear and ringing
3:2	R/W	**DIV: divider value of phase and mismatch or offset value of smear and ringing** 00: 0 01: 1 10: 2 11: 3
1:0	--	**Reserved to 0**

THD_OFFSET define:

The THD value definition of phase enhance function

Bit6~4	000	001	010	011	100	101	110	111
Value	112	128	144	160	176	192	208	224

The offset value definition of smear and ringing reduce function

Bit6~4	000	001	010	011	100	101	110	111
Value	no use	16	32	48	64	80	96	112

The THD value definition of mismatch enhance function

Bit6~4	000	XX1
Value	1	2

The THD value definition of noise reduction function

Bit6~4	000	001	010	011	100	101	110	111
Value	0	1	2	3	4	5	6	7

Scaling Up Function

Address: 19 **SCALE_CTRL (Scale Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Video mode compensation:** 0: Disable (Default) 1: Enable
6	R/W	**Internal ODD-signal inverse for video-compensation** 0: No invert (Default)

		1: invert
5	R	**Display Line Buffer Ready** 0: Busy 1: Ready
4	R/W	**Enable Full Line buffer:** 0: Disable (Default) 1: Enable
3	R/W	**Vertical Line Duplication** 0: Disable 1: Enable
2	R/W	**Horizontal pixel Duplication** 0: Disable 1: Enable
1	R/W	**Enable the Vertical Filter Function:** 0: By pass the vertical filter function block (Default) 1: Enable the vertical filter function block
0	R/W	**Enable the Horizontal Filter Function:** 0: By pass the horizontal filter function block (Default) 1: Enable the horizontal filter function block

- When using H/V duplication mode, FIFO window width set original width, but FIFO width height should be 2X the original height.

Address: 1A **SF_ACCESS_Port** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable scaling-factor access port**
6:5	--	**Reserved to 0**
4:0	R/W	**Scaling factor port address**

- When disable scaling factor access port, the access port pointer will reset to 0

Address: 1B-00 **HOR_SCA_H (Horizontal Scale Factor High)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Bit [19:16] of horizontal scale factor**

Address: 1B-01 **HOR_SCA_M (Horizontal Scale Factor Medium)**

Bit	Mode	Function
7:0	R/W	**Bit [15:8] of horizontal scale factor**

Address: 1B-02 **HOR_SCA_L (Horizontal Scale Factor Low)**

Bit	Mode	Function

7:0	R/W	**Bit [7:0] of horizontal scale factor**

Address: 1B-03 **VER_SCA_H (Vertical Scale Factor High)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Bit [19:16] of vertical scale factor**

Address: 1B-04 **VER_SCA_M (Vertical Scale Factor Medium)**

Bit	Mode	Function
7:0	R/W	**Bit [15:8] of vertical scale factor**

Address: 1B-05 **VER_SCA_L (Vertical Scale Factor Low)**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of vertical scale factor**

This scale-up factor includes a 20-bit fraction part to present a vertical scaled up size over the stream input. For example, for 600-line original picture scaled up to 768-line, the factor should be as follows:

(600/768) x 2^20 = 0.78125 x 2^20 = 819200 = C8000h = 0Ch, 80h, 00h.

Address: 1B-06 **Horizontal Scale Factor Segment 1 Pixel** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**Bit [10:8] of Scaling Factor Segment 1 pixel**

Address: 1B-07 **Horizontal Scale Factor Segment 1 Pixel** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of Scaling Factor Segment 1 pixel**

Address: 1B-08 **Horizontal Scale Factor Segment 2 Pixel** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**Bit [10:8] of Scaling Factor Segment 2 pixel**

Address: 1B-09 **Horizontal Scale Factor Segment 2 Pixel** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of Scaling Factor Segment 2 pixel**

Address: 1B-0A **Horizontal Scale Factor Segment 3 Pixel** **Default: 00h**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**Bit [10:8] of Scaling Factor Segment 3 pixel**

Address: 1B-0B **Horizontal Scale Factor Segment 3 Pixel** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of Scaling Factor Segment 3 pixel**

Address: 1B-0C **Horizontal Scale Factor Delta 1** **Default: 00h**

Bit	Mode	Function
7:5	--	**Reserved**
4:0	R/W	**Bit [12:8] of Horizontal Scale Factor delta 1**

Address: 1B-0D **Horizontal Scale Factor Delta 1** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of Horizontal Scale Factor delta 1**

Address: 1B-0E **Horizontal Scale Factor Delta 2** **Default: 00h**

Bit	Mode	Function
7:5	--	**Reserved**
4:0	R/W	**Bit [12:8] of Horizontal Scale Factor delta 2**

Address: 1B-0F **Horizontal Scale Factor Delta 2** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Bit [7:0] of Horizontal Scale Factor delta 2**

Address: 1B-10 **Horizontal Filter Coefficient Initial Value** **Default: C4h**

Bit	Mode	Function
7:0	R/W	**Accumulate Horizontal filter coefficient initial value**

Address: 1B-11 **Vertical Filter Coefficient Initial Value** **Default: C4h**

Bit	Mode	Function
7:0	R/W	**Accumulate Vertical filter coefficient initial value**

Address: 1C **FILTER_CTRL (Filter Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Filter Coefficient Access** 0: Disable (Default) 1: Enable
6	R/W	**Select H/V User Defined Filter Coefficient Table for Access Channel** 0: 1st coefficient table (Default) 1: 2nd coefficient table
5	R/W	**Select Horizontal user defined filter coefficient table** 0: 1st Horizontal Coefficient Table (Default) 1: 2nd Horizontal Coefficient Table
4	R/W	**Select Vertical user defined filter coefficient table** 0: 1st Vertical Coefficient Table (Default) 1: 2nd Vertical Coefficient Table
3:0	--	**Reserved to 0**

- The User Defined Filter Coefficient Table can be modified on-line. Only the non-active coefficient-table can be modified, and then switch it to active.

Address: 1D **FILTER_PORT (User Defined Filter Access Port)** **Default: 00h**

Bit	Mode	Function
7:0	W	**Access port for user defined filter coefficient table**

- When enable filter coefficient accessing, the first write byte is stored into the LSB(bit[7:0]) of coefficient #1 and the second byte is into MSB (bit[8:11]). Therefore, the valid write sequence for this table is c0-LSB, c0-MSB, c1-LSB, c1-MSB, c2-LSB, c2-MSB … c63-LSB & c63-MSB, totally 64 * 2 cycles. Since the 128 taps is symmetric, we need to fill the 64-coefficient sequence into table only.

Address: 1E **OSD_REFERENCE__DEN** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Position Of Reference DEN for OSD[7:0]**

Address: 1F **NEW_DV_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**New Timing Enable** 0: Disable 1: Enable
6	R/W	**Line Compensation Enable** 0: Disable 1: Enable
5	R/W	**Pixel Compensation Enable** 0: Disable 1: Enable
4	R/W	**Reserved to 0**
3:0	R/W	**DCLK_Delay[11:8]**

Address: 20 **NEW_DV_DLY** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**DCLK_Delay[7:0]**

When CR 1F[7]=1, CR1F[3:0] & CR20 can’t be 0

Address: 21 Reserved

FIFO Frequency

Address: 22 **FIFO Frequency** **Default: 00h**

Bit	Mode	Function
7	R/W	**Test Mode**

		0: disable 1: input data of VGIP replaced by Background Color in CR6D
6:5	R/W	**Reserved to 0**
4	R/W	**Bounding Select** 0: Single Chip 1: MCM
3	R/W	**M2PLL_DIV** 0: x 1/10 1: x 1/11
2	R/W	**Internal Xtal Frequency** 0: Fxtal 1: Fxtal * M2PLL_M / M2PLL_N * M2PLL_DIV
1:0	R/W	**FIFO frequency** 00: MPLL 01: ICLK 10: DCLK 11: Reserved

Scaling Down Control

Address: 23 **SCALE_DOWN_CTRL (Scale Down Control Register)** **Default: 00h**

Bit	Mode	Function
7	R	**Bist result for FIFO** 0: Fail 1: Ok
6	R	**Bist result for Line Buffer one & two** 0: Fail 1: Ok
5	R/W	**FIFO Bist Function Start (Auto clear to 0 when finish)** 0: Finish 1: Start
4	R/W	**Line Buffer Bist Function Start (Auto clear to 0 when finish)** 0: Finish 1: Start
3	R/W	**Horizontal non-linear scale down** 0: linear 1: non-linear
2	R/W	**Vertical Scale-Down Compensation**

		0: Disable (Default) 1: Enable
1	R/W	**Horizontal scale down function enable:** 0: Disable scale down function (Default) 1: Enable scale down function
0	R/W	**Vertical scale down function enable:** 0: Disable scale down function (Default) 1: Enable scale down function

Address: 24 **Scale_Down_Access_Port Control** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable scale-down access port**
6:5	--	**Reserved to 0**
4:0	R/W	**Scale-down port address**

Address: 25-00 **V_SCALE_INIT**

Bit	Mode	Function
7:6	--	**Reserved**
5:0	R/W	**Vertical Scale Down Initial Select [5:0]**

- Scale Down Initial Point Select: for example, if the value is 43, we select the initial point is 43/64

Address: 25-01 **V_SCALE_DH (Vertical scale down factor register)**

Bit	Mode	Function
7:3	R/W	**Reserved**
2:0	R/W	**Vertical Scale Down Factor** [18:16]

Address: 25-02 **V_SCALE_DM (Vertical scale down factor register)**

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor** [15:8]

Address: 25-03 **V_SCALE_DL (Vertical scale down factor register)**

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor** [7:0]

- Registers {V_SCALE_DH, V_SCALE_DM, V_SCALE_DL} = (Yi/Ym)*(2^17).
- The largest scale down ratio is 1/4 (integer part 2 bits)
- Meanwhile, Yi = vertical input length; Ym=vertical memory write length

Address: 25-04 **H_SCALE_INIT**

Bit	Mode	Function
7:6	--	**Reserved**
5:0	R/W	**Horizontal Scale Down Initial Select [5:0]**

- Scale Down Initial Point Select: for example, if the value is 43, we select the initial point is 43/64

Address: 25-05 **H_SCALE_DH**

Bit	Mode	Function

7:0	R/W	**Horizontal Scale Down Factor** [23:16]

Address: 25-06 **H_SCALE_DM**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor** [15:8]

Address: 25-07 **H_SCALE_DL**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor** [7:0]

- First left side point is always latched, then the remaining points interpolates by the shrinking ratio.
- Horizontal scaling down factor should be (Xi / Xm))* (2^{20}) truncate.
- The largest scale down ratio is 1/16 (integer part 4 bits)
- Meanwhile, Xi = horizontal input width; Xm = horizontal memory write width

Address: 25-08 **H_SCALE_DCCH**

Bit	Mode	Function
7	--	**Reserved**
6:0	R/W	**Horizontal Scale Down Accumulated Factor** [14:8]

Address: 25-09 **H_SCALE_DCCL**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Accumulated Factor** [7:0]

Address: 25-0A **SD_DCC_WIDTHH**

Bit	Mode	Function
7:2	--	**Reserved**
1:0	R/W	**Horizontal Scale Down Accumulated Width** [9:8]

Address: 25-0B **SD_DCC_WIDTHL**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Accumulated Width** [7:0]

Address: 25-0C **SD_FLAT_WIDTHH**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**Horizontal Scale Down Flat Width** [10:8]

Address: 25-0D **SD_DCC_WIDTHL**

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Flat Factor** [7:0]

Y-Peaking filter and coring control (For Display Domain)

Address: 26 **peaking/coring access port control** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable peaking / coring access port**
6	R/W	**Peaking/coring Enable** 0: Disable

		1: Enable
5	R/W	**Y peaking Coefficient Resolution** 0: n/32 1: n/64
4:3	--	**Reserved**
2:0	R/W	**Peaking/coring port address**

Address: 27-00 **Peaking_Coef0**

Bit	Mode	Function
7:0	R/W	**Coefficient C0 of Peaking filter:** Valid Range: -128/32(-128) ~ 127/32 (127) (2's complement)

Address: 27-01 **Peaking_Coef1**

Bit	Mode	Function
7:0	R/W	**Coefficient C1 of Peaking filter:** Valid Range: -128/32(-128) ~ 127/32 (127) (2's complement)

Address: 27-02 **Peaking_Coef2**

Bit	Mode	Function
7:0	R/W	**Coefficient C2 of Peaking filter:** Valid Range: -128/32(-128) ~ 127/32 (127) (2's complement)

Address: 27-03 **Coring_Min**

Bit	Mode	Function
7:5	R/W	**Reserved**
4:0	R/W	**Coring Minimum value**

Address: 27-04 **Coring_Max_Pos**

Bit	Mode	Function
7:0	R/W	**Coring Maximum Positive value**

Address: 27-05 **Coring_Max_Neg**

Bit	Mode	Function
7:0	R/W	**Coring Maximum Negitive value** (2's complement)

Y'[n] = C0*Y[n] + C1*(Y[n-1]+Y[n+1]) + C2*(Y[n-2]+Y[n+2]) , -256<=Y'<=255

Ypeak = Y'[n] – Coring_Min, if Y'[n] >= 0,

= Y'[n] + Coring_Min, if Y'[n] < 0

if (|Y'[n]| <= Coring_Min)

Y"[n] = 0,

else if Ypeak >= Coring_Max_Pos

Y"[n] = Coring_Max_Pos

else if Ypeak <= Coring_Max_Neg

Y"[n] = Coring_Max_Neg

else

Y"[n] = Ypeak

Yo[n] = Y[n] + Y''[n], 0 <= Yo[n] <= 255

Display Format

Address: 28 **VDIS_CTRL (Video Display Control Register)** **Default: 20h**

Bit	Mode	Function
7	R/W	**Force Display Timing Generator Enable: (Should be set when in Free-Run mode)** 0: wait for input IVS trigger 1: force enable
6	R/W	**Display Data Output Inverse Enable** 0: Disable (Default) 1: Enable (only when data bus clamp to 0)
5	R/W	**Display Output Force to Background Color** 0: Display output operates normally 1: Display output is forced to the color as selected by background color (CR6D) (Default)
4	R/W	**Display 18 bit RGB Mode Enable** 0: All individual output pixels are full 24-bit RGB (Default) 1: All individual output pixels are truncated to 18-bit RGB (LSB 2 bits = 0)
3	R/W	**Frame Sync Mode Enable** 0: Free running mode (Default) 1: Frame sync mode
2	R/W	**Display Output Double Port Enable** 0: Single port output (Default) 1: Double port output
1	R/W	**Display Output Run Enable** 0: DHS, DVS, DEN & DATA bus are clamped to "0" (Default) 1: Display output normal operation.
0	R/W	**Display Timing Run Enable** 0: Display Timing Generator is halted, Zoom Filter halted (Default) 1: Display Timing Generator and Zoom Filter enabled to run normally

Steps to disable output: First set CR28[1]=0, set CR28[6], then set CR28[0]=0 to disable output.

Address: 29 **VDISP_SIGINV (Display Control Signal Inverted)** **Default: 00h**

Bit	Mode	Function
7	R/W	**DHS Output Format Select (only available in Frame Sync)** 0: The first DHS after DVS is active (Default) 1: The first DHS after DVS is inactive
6	R/W	**Display Data Port Even/Odd Data Swap:** 0: Disable (Default)

		1: Enable
5	R/W	**Display Data Port Red/Blue Data Swap** 0: Disable (Default) 1: Enable
4	R/W	**Display Data Port MSB/LSB Data Swap** 0: Disable (Default) 1: Enable
3	R/W	**Skew Display Data Output** 0: Non-skew data output (Default) 1: Skew data output
2	R/W	**Display Vertical Sync (DVS) Output Invert Enable:** 0: Display Vertical Sync output normal active high logic (Default) 1: Display Vertical Sync output inverted logic
1	R/W	**Display Horizontal Sync (DHS) Output Invert Enable:** 0: Display Horizontal Sync output normal active high logic (Default) 1: Display Horizontal Sync output inverted logic
0	R/W	**Display Data Enable (DEN) Output Invert Enable:** 0: Display Data Enable output normal active high logic (Default) 1: Display Data Enable output inverted logic

Address: 2A **DH_TOTAL_H (Display Horizontal Total Pixels)**

Bit	Mode	Function
7:4	--	**Reserved to 0**
3:0	R/W	**Display Horizontal Total Pixel Clocks**: High Byte[11:8]

Address: 2B **DH_TOTAL_L (Display Horizontal Total Pixels)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Total Pixel Clocks:** Low Byte[7:0]

Real DH_Total (Target value)= DH_Total (Register value)+ 4

Address: 2C **DH_HS_END (Display Horizontal Sync End)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Sync End[7:0]:** Determines the width of DHS pulse in DCLK cycles

Address: 2D **DH_BKGD_STA_H (Display Horizontal Background Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Background Start**: High Byte [11:8]

Address: 2E **DH_BKGD_STA_L (Display Horizontal Background Start)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background Start**: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Background region.

Real DH_BKGD_STA (Target value)= DH_BKGD_STA (Register value)+ 10

Address: 2F **DH_ACT_STA_H (Display Horizontal Active Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Active Region Start**: High Byte [11:8]

Address: 30 **DH_ACT_STA_L (Display Horizontal Active Start)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active Region Start**: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Active region.

Real DH_ACT_STA (Target value)= DH_ACT_STA (Register value)+ 10

Address: 31 **DH_ACT_END_H (Display Horizontal Active End)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Active End**: High Byte [11:8]

Address: 32 **DH_ACT_END_L (Display Horizontal Active End)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active End**: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to the pixel of background region.

Real DH_ACT_END (Target value)= DH_ACT_END (Register value)+ 10

Address: 33 **DH_BKGD_END_H (Display Horizontal Background End)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Horizontal Background end**: High Byte [11:8]

Address: 34 **DH_BKGD_END_L (Display Horizontal Background End)**

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background end**: Low Byte [7:0]

Real DH_BKGD_END (Target value) = DH_BKGD_END (Register value)+ 10

Address: 35 **DV_TOTAL_H (Display Vertical Total Lines)**

Bit	Mode	Function
7:4	--	**Reserved to 0**
3:0	R/W	**Display Vertical Total**: High Byte [11:8]

Address: 36 **DV_TOTAL_L (Display Vertical Total Lines)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Total:** Low Byte [7:0]

CR35, CR36 use as watch dog reference value in ***frame sync*** mode, the event should be the line number of display HS is equal to DV Total.

Address: 37 **DVS_END (Display Vertical Sync End)**

Bit	Mode	Function
7:5	--	**Reserved**
4:0	R/W	**Display Vertical Sync End[4:0]:** Determines the duration of DVS pulse in lines

Address: 38 **DV_BKGD_STA_H (Display Vertical Background Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Vertical Background Start:** High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of background region.

Address: 39 **DV_BKGD_STA_L (Display Vertical Background Start)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Background Start:** Low Byte [7:0]

Address: 3A **DV_ACT_STA_H (Display Vertical Active Start)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Vertical Active Region Start:** High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of active region.

Address: 3B **DV_ACT_STA_L (Display Vertical Active Start)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region Start:** Low Byte [7:0]

Address: 3C **DV_ACT_END_H (Display Vertical Active End)**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**Display Vertical Active Region End:** High Byte [11:8]

Address: 3D **DV_ACT_END_L (Display Vertical Active End)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region End**: Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of following background region.

Address: 3E **DV_BKGD_END_H (Display Vertical Background End)**

Bit	Mode	Function

7:4	--	**Reserved to 0**
3:0	R/W	**Display Vertical Background end:** High Byte [11:8]

Address: 3F **DV_BKGD_END_L (Display Vertical Background End)**

Bit	Mode	Function
7:0	R/W	**Display Vertical Background End:** Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of start of vertical blanking.

Frame Sync Fine Tune

Address: 40 **IVS2DVS_DEALY_LINES (IVS to DVS Lines)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**IVS to DVS Lines:** (Only for FrameSync Mode) The number of input HS from IVS to DVS. Should be double buffer by CR05[5:4]

Address: 41 **IV_DV_DELAY_CLK_ODD (Frame Sync Delay Fine Tuning)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Frame Sync Mode Delay Fine Tune [7:0] "00" to disable** **Applied to all fields when Interlaced_FS_Delay_Fine_Tuning is disabled (CR43[1] = 0)** **Only for odd-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1)**

In Frame Sync Mode , CR40[7:0] represents output VS delay fine-tuning. For example, it delays the number of (CR41 [7:0] *16 + 16) input clocks. Fill 00h, means 0, fill 01h, and means 32

Address: 42 **IV_DV_DELAY_CLK_EVEN (Frame Sync Delay Fine Tuning)** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Frame Sync Mode Delay Fine Tune [7:0] "00" to disable** **Only for even-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1)**

Address: 43 **FS_DELAY_FINE_TUNING** **Default: 00h**

Bit	Mode	Function
7:2	R/W	**Reserved to 0**
1	R/W	**Interlaced_FS_Delay_Fine_Tuning** 0: Disable (Default) 1: Enable
0	R/W	**Internal ODD-signal inverse for Interlaced_FS_Delay_Fine_Tuning** 0: No invert (Default) 1: Invert

Address: 44 **LAST_LINE_H** **Default: 00h**

Bit	Mode	Function
7	R/W	**Last-line-width / DV-Total Selector :** 0: CR44 [3:0] and CR45 indicate last-line width counted by display clock (Default) 1: CR44 [3:0] and CR45 indicate DHS total number between 2 DVS.
6	R/W	**DV sync with 4X clock** 0: Disable 1: Enable
5	R/W	**BIST Test Enable** 0: Disable

		1: Enable (Auto clear when finish)
4	R/W	**BIST Test Result** 0: Fail 1: Ok
3:0	R	**DV Total or Last Line Width[11:8] Before Sync in Frame Sync Mode**

Address: 45 **LAST_LINE_L**

Bit	Mode	Function
7:0	R	**DV Total or Last Line Width[7:0] Before Sync in Frame Sync Mode**

Display Fine Tune

Address: 46 **DIS_TIMING (Display Clock Fine Tuning Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Reserved to 0**
6:4	R/W	**Display Output Clock Fine Tuning Control:** 000: DCLK rising edge correspondents with output display data 001: 1ns delay 010: 2ns delay 011: 3ns delay 100: 4ns delay 101: 5ns delay 110: 6ns delay 111: 7ns delay
3:0	--	**Reserved**

Sync Processor

Address: 47 SYNC_SELECT Default: 00h

Bit	Mode	Function
7	R/W	**Sync Processor Power Down (Stop Crystal Clock In)** 0: Normal Run (Default) 1: Power Down
6	R/W	**Hysnc Type Detection Auto Run** 0: manual (Default) 1: automatic
5	R/W	**De-composite circuit enable** 0: Disable (Default) 1: Enable
4	R/W	**Input HS selection** 0 : HS_RAW(SS/CS) (Default) 1: SOG/SOY
3:2	--	**Reserved to 0**
1	R/W	**Measured by Crystal clock (Result showed in CR59) (in Digital Mode)** 0: Input Active Region (Vertical IDEN start to IDEN stop) (measure at IDEN STOP) (Default) 1: Display Active Region(Vertical DEN start to DEN stop) (measure at DEN STOP) The function should work correctly when IVS or DVS occurs and enable by CR50[4].
0	R/W	**HSYNC & VSYNC Measured Mode** 0: HS period counted by crystal clock & VS period counted by HS (Analog mode) (Default) 1: H resolution counted by input clock & V resolution counted by ENA (Digital mode) (Get the correct resolution which is triggered by enable signal, ENA)

Address: 48 SYNC_INVERT Default: 00h

Bit	Mode	Function
7	R/W	**COAST Signal Invert Enable:** 0: Not inverted (Default) 1: Inverted
6	R/W	**COAST Signal Output Enable:** 0: Disable (Default) 1: Enable
5	R/W	**HS_OUT Signal Invert Enable:** 0: Not inverted (Default) 1: Inverted

4	R/W	**HS_OUT Signal Output Enable:** 0: Disable (Default) 1: Enable
3	R/W	**CS_RAW Inverted Enable** 0: Normal (Default) 1: Invert
2	R/W	**CLAMP Signal Output Enable** 0: Disable (Default) 1: Enable
1	R/W	**HS Recovery in Coast** 0: Disable (Default) (SS/SOY) 1: Enable (CS or SOG)
0	R/W	**HSYNC Synchronize source** 0: AHS (Default) 1: Feedback HS

Address: 49 **SYNC_CTRL (SYNC Control Register)** **Default: 06h**

Bit	Mode	Function
7	R/W	**CLK Inversion to latch Feedback HS for Coast Recovery** **(Coast Recovery means HS feedback to replace input HS)** 0: Non Inversion (Default) 1: Inversion
6	R/W	**Select HS_OUT Source Signal** 0: Bypass (SeHs)(Use in Separate Mode) 1: Select De-Composite HS out(DeHs) (In Composite mode)
5	R/W	**Select ADC_VS Source Signal(Auto switch in Auto Run Mode)** 0: VS_RAW 1: DeVS
4	R/W	**CLK Inversion to latch ADC HS for Clamp** 0: Non Inversion (Default) 1: Inversion
3	R/W	**Inversion of HS to measure Vsync** 0: Non Inversion (Default) 1: Inversion
2	R/W	**HSYNC Measure Source(ADC_HS1)** 0: Select ADC_HS1 (Default) 1: Select SeHS or DeHS by CR49[6]

Bit	Mode	Function
1:0	R/W	**Measure HSYNC/VSYNC Source Select:** 00: TMDS 01: VIDEO8 10: ADC_HS1/ADC_VS (Default) 11: CS_RAW/ ADC_VS

Address: 4A **STABLE_HIGH_PERIOD_H** **Default: 00h**

Bit	Mode	Function
7	R	**Even/Odd Field of YPbPr**(By Line-Count Mode) 0: Even 1: Odd
6	R	**The toggling of polarity of YPbPr Field happens**(By Line-Count Mode) 0: No toggle 1: Toggle
5	R	**Even/Odd Field of YPbPr** (By VS-Position Mode) 0: Even 1: Odd
4	R	**The Toggling of Polarity of YPbPr Field Happened** (By VS-Position Mode) 0: No toggle 1: Toggle
3	R/W	**Odd Detection Mode** 0: Line-Count Mode (Default) 1: VS-Position Mode
2:0	R	**Stable High Period[10:8]** Compare each line's high pulse period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 4B **STABLE_HIGH_PERIOD_L**

Bit	Mode	Function
7:0	R	**Stable High Period[7:0]** Compare each line's high pulse period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 4C **VSYNC_COUNTER_LEVEL_MSB** **Default: 0Bh**

Bit	Mode	Function
7	R	**Hysnc Type Detection Auto Run Result ready**
6:4	R	**Hysnc Type Detection Auto Run Result** 000: No Signal 001: Not Support 010: YPbPr

		011: Serration Composite SYNC 100: XOR/OR-Type Composite SYNC with Equalizer 101: XOR/OR-Type Composite SYNC without Equalizer 110: HSYNC with VS_RAW (Separate HSYNC) 111: HSYNC without VS_RAW (HSYNC only) Reference when Hsync type detection auto run result ready (CR4C[7])
3	R/W	**TMDS/Video8 switch** 0: Video8 1: TMDS (Default)
2:0	R/W	**Vsync counter level count [10:8] MSB** Vsync detection counter start value.

Address: 4D **VSYNC_COUNTER_LEVEL_LSB** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Vsync counter level count [7:0] LSB**

Address: 4E **HSYNC_TYPE_DETECTION_FLAG**

Bit	Mode	Function
7	R	**HS Overflow(16-bits)**
6	R	**Stable Period Change (write clear when CR4E[6]=1 or CR4F[0]=1)**
5	R	**Stable Polarity Change (write clear when CR4E[5]=1 or CR4F[0]=1)**
4	R	**VS_RAW Edge Occurs (write clear when CR4E[4]=1 or CR4F[0]=1)** If VS_RAW edge occurs, this bit is set to “1”.
3	R	**Detect Capture Window Unlock repeated 32 times (write clear when CR4E[3]=1 or CR4F[0]=1)**
2	R	**HSYNC has Equalization (write clear when CR4E[2]=1 or CR4F[0]=1)**
1	R	**HSYNC Polarity Change (write clear when CR4E[1]=1 or CR4F[0]=1)**
0	R	**Detect Capture Window Unlock (write clear when CR4E[0]=1 or CR4F[0]=1)**

Address: 4F **STABLE_MEASURE** **Default: 00h**

Bit	Mode	Function
7	R	**Stable Flag** 0: Period or polarity can’t get continuous stable status. 1: Both polarity and period are stable.
6	R	**Stable Polarity** 0: Negative 1: Positive Compare each line’s polarity; if we get continuous ~~N~~ 64 lines with the same one, the polarity is

		updated as the stable polarity.
5:4	R/W	**Feedback Hsync High Period Select by ADC Clock:** 00: 32 (Default) 01: 64 10: 96 11: 128
3	R/W	**Stable Period Tolerance** 0: ±2 crystal clks (Default) 1: ±4 crystal clks
2	R/W	**Vsync measure invert Enable** 0: Disable (Default) 1: Enable
1	R/W	**Pop Up Stable Value** 0: No Pop Up (Default) 1: Pop Up Result, (CR4A[2:0], CR4B[7:0], CR4E[3], CR50[2:0], CR51[7:0])
0	R/W	**Stable Measure Start** 0 : Stop (Default) 1 : Start

Address: 50 **Stable_Period_H** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R	**CS_RAW Inverted by Auto Run Mode** 0: Not inverted 1: Inverted
5	R/W	**HS_OUT Bypass PLL into VGIP** 0: Disable (Default) 1: Enable
4	R/W	**Active Region Measure Enable** 0: Disable (Default) 1: Enable
3	R/W	**ADC_VS Source Select in Test Mode** 0: Select ADC_VS Source in Normal Mode or Auto Mode by CR47[6] (Default) 1: Select ADC_VS Source in Test Mode (Select VS_RAW or DeVS by CR49[5])
2:0	R	**Stable Period[10:8]** Compare each line's period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 51 **Stable_Period_L**

Bit	Mode	Function
7:0	R	**Stable Period[7:0]** Compare each line's period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 52 **MEAS_HS_PER_H (HSYNC Period Measured Result)** **Default: 8'b000xxxxx**

Bit	Mode	Function
7	R/W	**On Line Auto Measure Enable** 0: Disable (Default) 1: Enable
6	R/W	**Pop Up Period Measurement Result** 0: No Pop Up (Default) 1: Pop Up Result
5	R/W	**Start a HS & VS period / H & V resolution & polarity measurement (on line monitor)** 0: Finished/Disable (Default) 1: Enable to start a measurement, auto cleared after finished
4	R	**Over-flow bit of Input HSYNC Period Measurement** 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	**Input HSYNC Period Measurement Result:** High Byte[11:8]

Address: 53 **MEAS_HS_PER_L (HSYNC Period Measured Result)**

Bit	Mode	Function
7:0	R	**Input HSYNC Period Measurement Result:** Low Byte[7:0]

- The result is expressed as the **average number** of crystal clocks (CR47[0]=0), or input clocks (CR47[0]=1) between 2 HSYNC.
- The result is the total number of crystal/input clocks inside 16-HSYNC periods divided by 16.
- Fractional part of measure result is stored in CR56[3:0].

Address: 54 **MEAS_VS_PER_H (VSYNC Period Measured Result)**

Bit	Mode	Function
7	R	**Input VSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
6	R	**Input HSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
5	R	**Time-Out bit of Input VSYNC Period Measurement (No VSYNC occurred)** 0: No Time Out

		1: Time Out occurred
4	R	**Over-flow bit of Input VSYNC Period Measurement** 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	**Input VSYNC Period Measurement Result:** High Byte[11:8]

Address: 55 **MEAS_VS_PER_L (VSYNC Period Measured Result)**

Bit	Mode	Function
7:0	R	**Input VSYNC Period Measurement Result:** Low Byte[7:0]

- This result is expressed in terms of input HS pulses.
- When measured digitally, the result is expressed as the number of input ENA signal within a frame.

Address: 56 **MEAS_HS&VS_HI_H (HSYNC&VSYNC High Period Measured Result)**

Bit	Mode	Function
7:4	R	**Input HSYNC High Period Measurement Result: High Byte[11:8]** (CR58[0] = 0) **Input VSYNC High Period Measurement Result: High Byte[11:8]** (CR58[0] = 1)
3:0	R	**Input HSYNC Period Measurement Fractional Result** (See CR52,53)

Address: 57 **MEAS_HS_HI_L (HSYNC High Period Measured Result)**

Bit	Mode	Function
7:0	R	**Input HSYNC High Period Measurement Result: Low Byte[7:0]** (CR58[0] = 0) **Input VSYNC High Period Measurement Result: Low Byte[7:0]** (CR58[0] = 1)

- This result of HSYNC high-period is expressed in terms of crystal clocks. When measured digitally, the result of HSYNC high-period is expressed as the number of input clocks inside the input enable signal.
- This result of VSYNC high-period is expressed in terms of input HS pulses

Address: 58 **MEAS_VS_HI_L (VSYNC High Period Measured Result)**

Bit	Mode	Function
7:1	R/W	**Reserved to 0**
0	R/W	**HSYNC/VSYNC High Period Measurement Result Select** 0: HSYNC 1: VSYNC (See CR56~CR57)

Address: 59 **MEAS_ACTIVE_REGION_H (Active Region Measured by CRSTL_CLK Result)**

Bit	Mode	Function
7:0	R/W	**Active Region Measured By Crystal Clock** **1st read: Measurement Result:** High Byte[23:16] **2nd read: Measurement Result:** High Byte[15:8] **3rd read: Measurement Result:** High Byte[8:0] Read pointer is auto increase, if write, the pointer is also reset to 1st result.

Address: 5A **SYNC_TEST_MISC** **Default: 00h**

Bit	Mode	Function
7	R/W	**Test-Mode for Clamp, HS_RAW is directly from PAD** 0: Clamp source from normal HS 1: Clamp source from HS_RAW
6	R/W	**Sync Processor Test Mode** 0: Normal (Default) 1: Enable Test Mode; (switch 70ns-ck to the time-out & polarity counters)
5:3	R/W	**Reserved**
2:0	R	**The Number of Input HS between 2 Input VSYNC**. LSB bit [2:0] for YpbPr

Address: 5B Reserved

Address: 5C **SYNC_PROC_PORT_ADDR** **Default: 00h**

Bit	Mode	Function
7:5	R/W	**Reserved**
4:0	R/W	**Sync Processor Access Port Address**

Address: 5D **SYNC_PROC_PORT_DATA** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Sync Processor Access Port Data**

Port address will increase automatically after read/write.

Address: 5D-00 **CLAMP_START (Clamp Signal Output Start)** **Default: 04h**

Bit	Mode	Function
7:0	R/W	**Start of Output Clamp Signal Pulse for Y/G Channel [7:0]:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 5D-01 **CLAMP_END (Clamp Signal Output End)** **Default: 10h**

Bit	Mode	Function
7:0	R/W	**End of Output Clamp Signal Pulse for Y/G Channel [7:0]:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal.

Address: 5D-02 **BR_CLAMP_START (Clamp Signal Output Start)** **Default: 04h**

Bit	Mode	Function
7:0	R/W	**Start of Output Clamp Signal Pulse for B/Pb and R/Pr Channel [7:0]:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 5D-03 **BR_CLAMP_END (Clamp Signal Output End)** **Default: 10h**

Bit	Mode	Function
7:0	R/W	**End of Output Clamp Signal Pulse for B/Pb and R/Pr Channel [7:0]:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal.

Address: 5D-04 **CLAMP _CTRL0** **Default:00h**

Bit	Mode	Function
7	R/W	**Clamp Trigger Edge Inverse for Y/G Channel** 0: Trailing edge (Default) 1: Leading edge
6	R/W	**Clamp Trigger Edge Inverse for B/Pb and R/Pr Channel** 0: Trailing edge (Default) 1: Leading edge
5:0	R/W	**Mask Line Number before DeVS [5:0]**

Address: 5D-05 **CLAMP _CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Clamp Mask Enable** 0: Disable (Default) 1: Enable
6	R/W	**Select Clamp Mask as De VS** 0: Disable 1: Enable
5:0	R/W	**Mask Line Number after DeVS [5:0]**

CR5D-02[5:0] and CR5D-03[5:0] will set number of Mask Line before/after DeVS for Clamp Mask.

Address: 5D-06 **CAPTURE_WINDOW_SETTING** **Default: 02h**

Bit	Mode	Function
7:5	R/W	**Hsync Debounce Length Selection** 000: disable xxx: 1~ 7clks
4	R/W	**Capture Miss Limit during Hsync Extraction** 0: 32 (Default) 1: 16
3	R/W	**Capture Window add step as Miss Lock** 0: ±1 crystal clks (Default) 1: ±2 crystal clks
2:0	R/W	**Capture Window Tolerance** 000: ±1 crystal clks for capture window

		001: ±2 crystal clks for capture window 010: ±4 crystal clks for capture window (Default) 011: ±8 crystal clks for capture window 100: ±16 crystal clks for capture window 101: ±32 crystal clks for capture window 110 ~ 111: Reserved

Address: 5D-07 **COAST_CTRL** **Default: 21h**

Bit	Mode	Function
7:4	R/W	**Start of COAST before DeVS Leading Edge [3:0]**
3:0	R/W	**End of COAST after DeVS Trailing Edge [3:0]**

Address:5D-08~0F Reserved

Macro Vision

Address: 5D-10 **MacroVision Control** **Default: 06h**

Bit	Mode	Function
7:4	R/W	**Skip Line[3:0]** Skip Lines after Vsync detected
3:2	--	**Reserved to 0**
1	R	**MacroVision Detected** (On-line monitor) When detected Macrovision occurred, this bit set to 1, else clear to 0.
0	R/W	**MacroVision Enable** 0: Disable (Default) 1: Enable

Address: 5D-11 **MacroVision Start Line 0**

Bit	Mode	Function
7	**R**	**Indicate the validity of Macro Vision Line in Even Field** 0: not valid 1: valid
6:0	R	**MacroVision Start Line in Even Field [6:0]**

Address: 5D-12 **MacroVision End Line 0**

Bit	Mode	Function
7:0	R	**MacroVision End Line 0 [7:0]**

Address: 5D-13 **MacroVision Start Line 1**

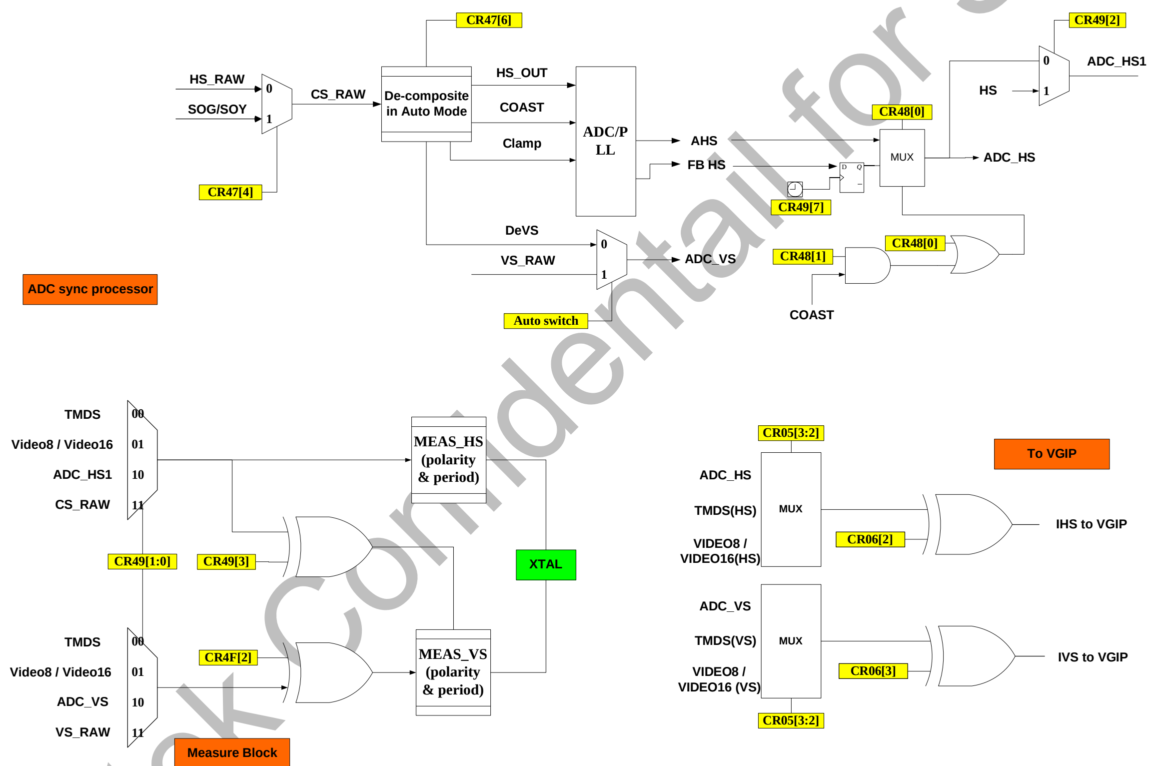
Bit	Mode	Function

7	R	**Indicate the validity of Macro Vision Line in Odd Field** 0: not valid 1: valid
6:0	R	**MacroVision Start Line in Odd Field [6:0]**

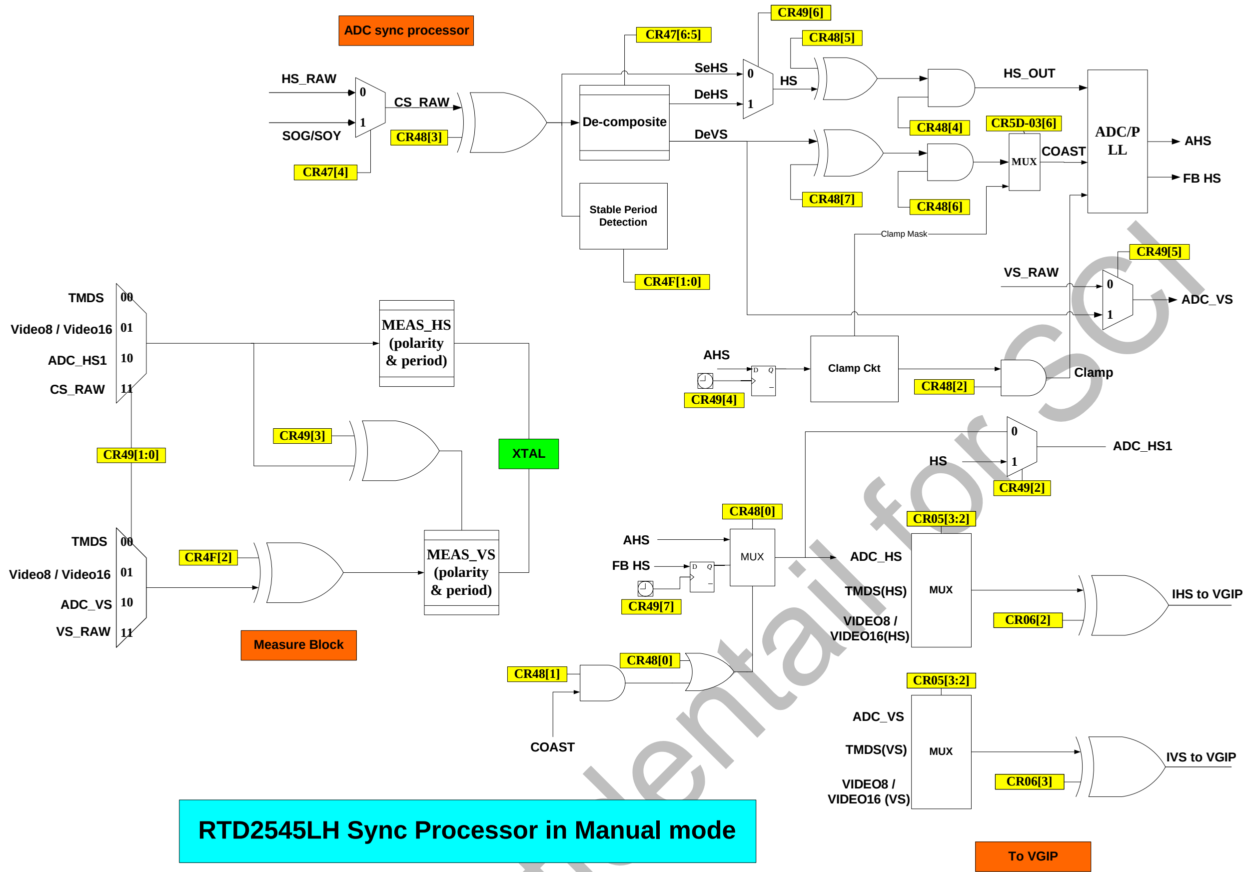
Address: 5D-14 **MacroVision End Line 1**

Bit	Mode	Function
7:0	R	**MacroVision End Line 1 [7:0]**

Address: 5D-15~1F Reserved



RTD2545LH Sync Processor in Automatic mode



RTD2545LH Sync Processor in Manual mode

Address: 5F Reserved

Highlight window

Address: 60 **highlight window access port control** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable highlight window access port** **0: Disable** **1: Enable**
6	R/W	**Enable highlight window** **0: Disable** **1: Enable**
5:4	--	**Reserved**
3:0	R/W	**Highlight-window access port address**

Address: 61-00 **highlight window horizontal start**

Bit	Mode	Function
7:0	--	**Reserved**
2:0	R/W	**highlight window horizontal start[10:8]**

Address: 61-01 **highlight window horizontal start**

Bit	Mode	Function
7:0	R/W	**highlight window horizontal start[7:0]**

Address: 61-02 **highlight window horizontal end**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**highlight window horizontal end[10:8]**

Address: 61-03 **highlight window horizontal end**

Bit	Mode	Function
7:0	R/W	**highlight window horizontal end[7:0]**

Address: 61-04 **highlight window vertical start**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**highlight window vertical start[10:8]**

Address: 61-05 **highlight window vertical start**

Bit	Mode	Function
7:0	R/W	**highlight window vertical start[7:0]**

Address: 61-06 **highlight window vertical end**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	R/W	**highlight window vertical end[10:8]**

Address: 61-07 **highlight window vertical end**

Bit	Mode	Function
7:0	R/W	**highlight window vertical end[7:0]**

Highlight window horizontal/vertical reference point is DEN (display background start).

Address: 61-08 **highlight window border**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	R/W	**highlight window border width**

Address: 61-09 **highlight window border color**

Bit	Mode	Function
7:6	--	**Reserved**

5:0	R/W	**highlight window border red color MSB 6bit (red color 2-bit LSB = 00)**

Address: 61-0A **highlight window border color**

Bit	Mode	Function
7:6	--	**Reserved**
5:0	R/W	**highlight window border green color MSB 6bit (green color 2-bit LSB = 00)**

Address: 61-0B **highlight window border color**

Bit	Mode	Function
7:6	--	**Reserved**
5:0	R/W	**highlight window border blue color MSB 6bit (blue color 2-bit LSB = 00)**

Address: 61-0C **Brightness/Contrast highlight window control** **default : 00h**

Bit	Mode	Function
7:6	R/W	**Contrast / brightness application control** 00: Set A used on full region 01: Set B used inside highlight window 10: Set A used outside highlight window 11: Set A used outside highlight window, and Set B used inside highlight window

Contrast (CR62[1])	Application control	Inside window	Outside window
0	X	bypass	bypass
1	CR61-0C[7:6]=00 || CR60[6]=0	Set A	Set A
1	CR61-0C[7:6]=01 && CR60[6]=1	Set B	bypass
1	CR61-0C[7:6]=10 && CR60[6]=1	bypass	Set A
1	CR61-0C[7:6]=11 && CR60[6]=1	Set B	Set A

Brightness (CR62[0])	Application control	Inside window	Outside window
0	X	bypass	bypass
1	CR61-0C[7:6]=00 || CR60[6]=0	Set A	Set A
1	CR61-0C[7:6]=01 && CR60(6)=1	Set B	bypass
1	CR61-0C[7:6]=10 && CR60[6]=1	bypass	Set A
1	CR61-0C[7:6]=11 && CR60[6]=1	Set B	Set A

Bit	Mode	Function
5:4	R/W	**Gamma application control** 00 : gamma used on full region 01: gamma used inside window 10: gamma used outside window 11: reserved

Gamma (CR67[6])	Application control	Inside window	Outside window
0	X	bypass	bypass
1	CR61-0C[5:4]=00 || CR60[6]=0	Gamma	Gamma
1	CR61-0C[5:4]=01 && CR60[6]=1	Gamma	bypass
1	CR61-0C[5:4]=10 && CR60[6]=1	bypass	Gamma

Bit	Mode	Function
3:2	R/W	**ICM/DCC application control** 00 : DCC used on full region 01: ICM/DCC used inside window 10: ICM/DCC used outside window 11: Reserved

ICM (CRE0[7])	Application control	Inside window	Outside window
0	X	bypass	bypass
1	CR61-0C[3:2]=00 || CR60[6]=0	ICM	ICM
1	CR61-0C[3:2]=01 && CR60[6]=1	ICM	bypass
1	CR61-0C[3:2]=10 && CR60[6]=1	bypass	ICM

DCC (CRE4[7])	Application control	Inside window	Outside window
0	X	bypass	bypass
1	CR61-0C[3:2]=00 || CR60[6]=0	DCC	DCC
1	CR61-0C[3:2]=01 && CR60[6]=1	DCC	bypass
1	CR61-0C[3:2]=10 && CR60[6]=1	bypass	DCC

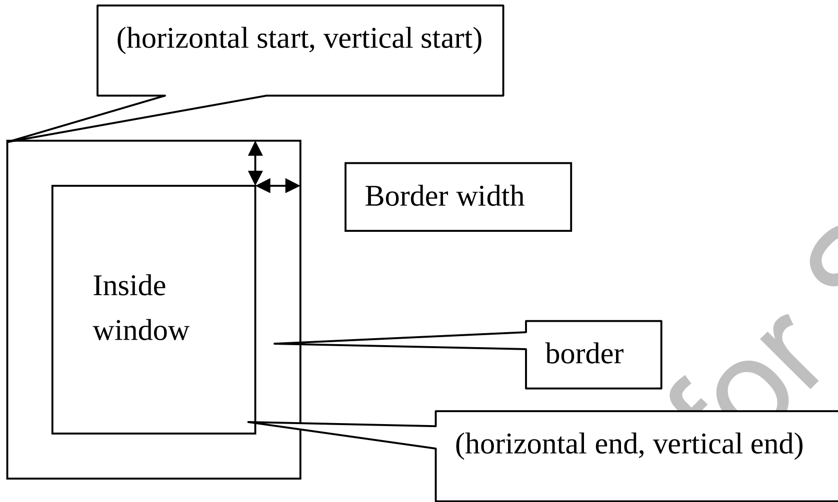
Bit	Mode	Function
1:0	R/W	**Peaking application control** 00: Peaking used on full region 01: Peaking used inside window 10: Peaking used outside window 11: reserved

Peaking (CR26 &CR27)	Application control	Inside window	Outside window
0	X	bypass	bypass
1	CR61-0C[1:0]=00 || CR60[6]=0	Peaking	Peaking
1	CR61-0C[1:0]=01 && CR60[6]=1	Peaking	bypass

		1	CR61-0C[1:0]=10 && CR60[6]=1	bypass	Peaking	

Address: 61-0D **sRGB highlight window control** **default : 00h**

<table>
<tr><th>Bit</th><th>Mode</th><th>Function</th></tr>
<tr><td>7:6</td><td>R/W</td><td>sRGB application control
00: sRGB used on full region
01: sRGB used inside window
10: sRGB used outside window
11: reserved
<table>
<tr><th>sRGB
(CR62[1])</th><th>Application control</th><th>Inside window</th><th>Outside window</th></tr>
<tr><td>0</td><td>X</td><td>bypass</td><td>bypass</td></tr>
<tr><td>1</td><td>CR61-0D[7:6]=00 || CR60[6]=0</td><td>sRGB</td><td>sRGB</td></tr>
<tr><td>1</td><td>CR61-0D[7:6]=01 && CR60[6]=1</td><td>sRGB</td><td>bypass</td></tr>
<tr><td>1</td><td>CR61-0D[7:6]=10 && CR60[6]=1</td><td>bypass</td><td>sRGB</td></tr>
</table></td></tr>
<tr><td>5:0</td><td>--</td><td>Reserved to 0</td></tr>
</table>



Inside window left-top point = (horizontal start + border width, vertical start + border width)
Inside window right-bottom point = (horizontal end, vertical end)
Border window left-top point = (horizontal start, vertical start)
Border window right-bottom point = (horizontal end+ border width, vertical end + border width)
Border = border window – inside window
Outside window = screen – border window

Color Processor Control

Address: 62 **COLOR_CTRL (Color Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	**sRGB coefficient write ready** 0: Not ready or cleared after finished 1: Ready to apply (Wait for DVS to apply) When users finished to program CR62[5:3], then turn this bit on, after finishing load into registers, the bit will be 0
6	R/W	**sRGB precision** 0: Normal (Default) 1: Multiplier Coefficient Bit Left Shift 2 bit shift left (MSB 2^1)
5:3	R/W	**sRGB Coefficient Write Enable (should be double buffered at DVS)** 000: Disable 001: Write R Channel (RRH,RRL,RGH,RGL,RBH,RBL) (address reset to 0 when written)

		010: Write G Channel (GRH,GBL,GGH,GGL,GBH,GBL) (address reset to 0 when written) 011: Write B Channel (BRH,BRL,BGH,BGL,BBH,BBL) (address reset to 0 when written) 100: R Offset 101: G Offset 110: B Offset
2	R/W	**Enable sRGB Function** 0: Disable (Default) 1: Enable
1	R/W	**Enable Contrast Function:** 0: disable the coefficient (Default) 1: enable the coefficient
0	R/W	**Enable Brightness Function:** 0: disable the coefficient (Default) 1: enable the coefficient

Address: 63 **SRGB_ACCESS_PORT**

Bit	Mode	Function
7:0	W	sRGB_COEF[7:0]

- For Multiplier coefficient: 9 bit: 1 bit sign, 8 bit fractional part (should fill using 2's compliment)
- For filling multiplier coefficient, the sequence should be SIGN bit (High Byte), 8 bit fractional (Low Byte) (should fill using 2's compliment)
- For Offset Coefficient: 1 sign, 5 integer, 2 bit fractional part (should fill using 2's compliment)
- sRGB output saturation to 1023 and Clamp to 0
- sRGB Output is 10 bit

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} 1+RR & RG & RB \\ GR & 1+GG & GB \\ BR & BG & 1+BB \end{bmatrix} \begin{bmatrix} R+Roffset \\ G+Goffset \\ B+Boffset \end{bmatrix}$$

Contrast/Brightness Coefficient:

Address: 64 **Contrast /Brightness Access Port Control** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Contrast /Brightness access port**
6	R/W	**sRGB multiplier coefficient precision** 0: 1-bit Shift-left (Default) 1: 2-bit Shift-left
5:4	--	**Reserved**
3:0	R/W	**Contrast /Brightness port address**

Access data port continuously will get address auto increase.

Address: 65-00 **BRI_RED_COE (Set A)**

Bit	Mode	Function
7:0	R/W	**Brightness Red Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-01 **BRI_GRN_COE (Set A)**

Bit	Mode	Function
7:0	R/W	**Brightness Green Coefficient: Valid range:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-02 **BRI_BLU_COE (Set A)**

Bit	Mode	Function
7:0	R/W	**Brightness Blue Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-03 **CTS_RED_COE (Set A)**

Bit	Mode	Function
7:0	R/W	**Contrast Red Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-04 **CTS_GRN_COE (Set A)**

Bit	Mode	Function
7:0	R/W	**Contrast Green Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-05 **CTS_BLU_COE (Set A)**

Bit	Mode	Function
7:0	R/W	**Contrast Blue Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-06 **BRI_RED_COE (Set B)**

Bit	Mode	Function
7:0	R/W	**Brightness Red Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-07 **BRI_GRN_COE (Set B)**

Bit	Mode	Function
7:0	R/W	**Brightness Green Coefficient: Valid range:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-08 **BRI_BLU_COE (Set B)**

Bit	Mode	Function

7:0	R/W	**Brightness Blue Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-09 **CTS_RED_COE (Set B)**

Bit	Mode	Function
7:0	R/W	**Contrast Red Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0A **CTS_GRN_COE (Set B)**

Bit	Mode	Function
7:0	R/W	**Contrast Green Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0B **CTS_BLU_COE (Set B)**

Bit	Mode	Function
7:0	R/W	**Contrast Blue Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

When highlight window is disabled, coefficient set A is used.

Gamma Control

Address: 66 **GAMMA_PORT**

Bit	Mode	Function
7:0	W	**Access port for gamma correction table**

- The input data sequence is {g0[9:2]}, {g0[1:0], 1'b0, d0[4:0]}, {3'b0, d1[4:0]}; {g2[9:2]}, {g2[1:0], 1'b0, d2[4:0]}, {3'b0, d3[4:0]}; … ; {g254[9:2]}, {g254[1:0] , 1'b0, d254[4:0]}, {3'b0, d255[4:0]} for full gamma table.
- The input data sequence is {g0[9:2]}, {g0[1:0], 1'b0, d0[4:0]}, {g2[9:2]}, {g2[1:0] , 1'b0, d2[4:0]} … , {g254[9:2]}, {g254[1:0] ,1'b0, d254[4:0] } for compact gamma table.
- For compact gamma table, d1[4:0]=d0[4:0], d3[4:0]=d2[4:0], … , d(2n+1)[4:0]=d(2n)[4:0].
- g(n) is 10bit gamma coefficient, and d(n) is g(n+1) – g(n) with 5bit.
- If n is even, Gamma-port output is g(n) + d(n)*(2bit LSB brightness output)/4.
- If n is odd, Gamma-port output is g(n-1) + d(n-1) + d(n)*(2bit LSB brightness output)/4.
- Gamma can be only accessed when DCLK exists.
- The latest stage of d[n] can't let gamma curve exceed 255.

Address: 67 **GAMMA_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Access Channels for Gamma Correction Coefficient:** 0: disable these channels (Default) 1: enable these channels
6	R/W	**Gamma table enable** 0: by pass (Default)

		1: enable
5:4	R/W	**Color Channel of Gamma Table** 00: Red Channel (Default) 01: Green Channel 10: Blue Channel 11: Red/Green/Blue Channel (R/G/B Gamma are the same)
3:1	--	**Reserved to 0**
0	R/W	**Gamma Access Type** 0: access compact gamma table (Default) 1: access full gamma table

- Access Gamma_Access register will reset GAMMA_PORT index.

Address: 68 **GAMMA_BIST (Color Control Register)** **Default: 00h**

Bit	Mode	Function

7	R/W	**Test_mode**
		0: Disable, dither_out = dither_result[9:2]; // truncate to integer number (Default)
		1: Enable, dither_out = dither_result[7:0]; // propagate decimal part for test

6:4	--	**Reserved to 0**
3:2	R/W	**Gamma BIST select** 00: BIST Disable (Default) 01: Red LUT 10: Green LUT 11: Blue LUT
1	R/W	**Gamma BIST_Progress** 0: BIST is done (Default) 1: BIST is running
0	R	**Gamma BIST Test Result** 0: SRAM Fail 1: SRAM OK

Dithering Control

Address: 69 **DITHERING_DATA_TABLE**

Bit	Mode	Function
7:0	W	**Dithering Data Port (Refer to the following instruction)**

A. When CR6B[7:6] is 2'b01, dithering sequence table access is enabled:

- There are three set of dithering sequence table, each table contains 32 elements, s0, s1, … , s31. Each element has 2 bit to index one of 4 dithering table.
- Input data sequence is {sr3,sr2,sr1,sr0}, {sr7,sr6,sr5,sr4}, … , {sr31,sr30,sr29,sr28}, {sg3,sg2,sg1,sg0}, … , {sg31,sg30,sg29,sg28}, {sb3,sb2,sb1,sb0}, … , {sb31,sb30,sb29,sb28} for red, green and blue channel.
- R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.

B. When CR6B[7:6] is 2'b10, dithering table access is enabled:

- For dithering table access, the red, green, blue each channel has 4 dithering table, each table is 2x2 elements, and one element has 4 bit for 10B/8B, the elements should fill 0 to 3, for 10B/6B, the elements should fill 0 to 15.
- Input data sequence is [Dr00 Dr01],[Dr02,Dr03], … , [Dr30,Dr31],[Dr32,Dr33], [Dg00,Dg01],[Dg02,Dg03], … , [Dg30,Dg31],[Dg32,Dg33], [Db00,Db01],[Db02,Db03], … , [Db30,Db31],[Db32,Db33].

D00	D01
D02	D03

D10	D11
D12	D13

D20	D21
D22	D23

D30	D31
D32	D33

C. When CR6B[7:6] is 2'b11, temporal offset access is enabled:

- There are 16 element for temporal offset table, t0, t1, … , t15.
  Each element has 2 bit to index one of 4 temporal offset.
- Input data sequence is {t3,t2,t1,t0}, {t7,t6,t5,t4}, {t11,t10,t9,t8}, {t15,t14,t13,t12}.

Address: 6A **DITHERING_CTRL** **Default: 00h**

Bit	Mode	Function
7:6	R/W	**Enable Access Control** 00: disable (Default) 01: enable access dithering sequence table 10: enable access dithering table 11: enable access temporal offset
5	R/W	**Enable Dithering Function** 0: disable (Default) 1: enable
4	R/W	**Temporal Dithering** 0: Disable (Default) 1: Enable
3	R/W	**Dithering Table Value Sign** 0: unsigned 1: signed (2's complement)
2	R/W	**Dithering Mode** 0: New (Default) 1: Old
1	R/W	**Vertical Frame Modulation** 0: Disable (Default) 1: Enable
0	R/W	**Horizontal Frame Modulation** 0: Disable (Default) 1: Enable

- {Dithering sequence + Frame Number (if temporal dithering)} mod 4 determine which dithering table to use

Address: 6B **Reserved**

Overlay/Color Palette/Background Color Control

Address: 6C **OVERLAY_CTRL (Overlay Display Control Register)** **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**Background color access enable** 0: Disable(Reset CR6D Write Pointer to R) 1: Enable
4:2	R/W	**Alpha blending level (Also enable OSD frame control register 0x003 byte 1[3:2]** 000: Disable (Default) 001 ~111: 1/8~ 7/8
1	R/W	**Overlay Sampling Mode Select:** 0: single pixel per clock (Default) 1: dual pixels per clock (The OSD will be zoomed 2X in horizontal scan line)
0	R/W	**Overlay Port Enable:** 0: Disable (Default) 1: Enable **Turn off overlay enable and switch to background simultaneously when auto switch to background.**

Address: 6D **BGND_COLOR_CTRL** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Background color RGB 8-bit value[7:0]**

- There are 3 bytes color select of background R, G, B, once we enable Background color access channel(CR6C[5] and the continuous writing sequence is R/G/B

Address: 6E **OVERLAY_LUT_ADDR (Overlay LUT Address)** **Default: 00h**

Bit	Mode	Function
7	R/W	**Enable Overlay Color Plate Access:** 0: Disable (Default) 1: Enable
6	R/W	**Reserved to 0**
5:0	R/W	**Overlay 16x24 Look-Up-Table Write Address [5:0]**

- Auto-increment while every accessing "Overlay LUT Access Port".

Address: 6F **COLOR_LUT_PORT (LUT Access Port)**

Bit	Mode	Function
7:0	W	**Color Palette 16x24 Look-Up-Table access port [7:0]**

- Using this port to access overlay color plate which addressing by the above registers.
- The writing sequence into LUT is [R0, G0, B0, R1, G1, B1, … R15, G15, and B15] and the address counter will

be automatic increment and circular from 0 to 47.

Image Auto Function

Address: 70 **H_BOUNDARY_H**

Bit	Mode	Function
7	--	**Reserved**
6:4	R/W	**Horizontal Boundary Start:** High Byte [10:8]
3:0	R/W	**Horizontal Boundary End:** High Byte [11:8]

Address: 71 **H_BOUNDARY_STA_L**

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary Start:** Low Byte [7:0]

Address: 72 **H_BOUNDARY_END_L**

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary End:** Low Byte [7:0]

Address: 73 **V_BOUNDARY_H**

Bit	Mode	Function
7	--	**Reserved**
6:4	R/W	**Vertical Boundary Start:** High Byte [10:8]
3:0	R/W	**Vertical Boundary End:** High Byte [11:8]

Vertical boundary search should be limited by Vertical boundary start.

Address: 74 **V_BOUNDARY_STA_L**

Bit	Mode	Function
7:0	R/W	**Vertical Boundary Start:** Low Byte [7:0]

Address: 75 **V_BOUNDARY_END_L**

Bit	Mode	Function
7:0	R/W	**Vertical Boundary End:** Low Byte [7:0]

Address: 76 **RED_NOISE_MARGIN (Red Noise Margin Register)**

Bit	Mode	Function
7:2	R/W	**Red pixel noise margin setting register**
1:0	--	**Reserved to 0**

Address: 77 **GRN_NOISE_MARGIN (Green Noise Margin Register)**

Bit	Mode	Function
7:2	R/W	**Green pixel noise margin setting register**
1:0	--	**Reserved to 0**

Address: 78 **BLU_NOISE_MARGIN (Blue Noise Margin Register)**

Bit	Mode	Function
7:2	R/W	**Blue pixel noise margin setting register**
1:0	--	**Reserved to 0**

Address: 79 **DIFF_THRESHOLD**

Bit	Mode	Function
7:0	R/W	**Difference Threshold** (Threshold for DIFF no matter CR7D[2] = 0 or 1)

Address: 7A **AUTO_ADJ_CTRL0** **Default: 00h**

Bit	Mode	Function
7	R/W	**Field_Select_Enable:** Auto-Function only active when Even or Odd field. 0: Disable (Default) 1: Enable
6	R/W	**Field_Select:** Select Even or Odd field. Active when **Field_Select_Enable**. 0: Active when ODD signal is "0" (Default) 1: Active when ODD signal is "1"
5	**R/W**	**Low Pass Filter (121-LPF)** 0: Disable (Default) 1: Enable
4	R/W	**Auto Function Acceleration** 0: Disable (Default) 1: Enable For auto-balance(CR7D[1] = 0), this function must be disabled.
3:2	R/W	**Vertical boundary search:** 00: 1 pixel over threshold (Default) 01: 2 pixel over threshold 10: 4 pixel over threshold 11: 8 pixel over threshold
1:0	R/W	**Color Source Select for Detection:** 00: B color (Default) 01: G color 10: R color 11: ALL When CR7A[1:0]=11`b, SOD of all color will be available after 3 frames, and the result in CR[84]~[87] will be : {(SOD_R + SOD_G + SOD_B) / 2}, if CR7D[2] = 0. {(SOD_R + SOD_G + SOD_B) / 8}, if CR7D[2] = 1.

Address: 7B **HW_AUTO_PHASE_CTRL0** **Default: 00h**

Bit	Mode	Function
7:3	R/W	**Number of Auto-Phase Step** (Valut+1) **(How many times (steps reference CR7B[2:0]) jumps when using Hardware Auto)**
2:0	R/W	**Hardware Auto Phase Step** 000: Step =1 (Default) 001 :Step =2 010: Step =4 011: Step =8 1xx: Step =16

Address: 7C **HW_AUTO_PHASE_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Hardware Auto Phase Select Trigger** 0: IVS 1: Vertical Boundary End
6:0	R/W	**Initial phase of Auto-Phase** (0~63) For High Freq: the phase sequence is 0,1,2…………..,63 (Default) For Low Freq: the phase sequence is 0,2,4,6,8……….,126

Address: 7D **AUTO_ADJ_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**Measure Digital Enable Info when boundary search active** 0: Normal Boundary Search (Default) 1: Digital Enable Info Boundary Search.(Digital mode)
6	R/W	**Hardware / Software Auto Phase Switch** 0: Software (Default) 1: Hardware
5	R/W	**Color Max or Min Measured Select:** 0: MIN color measured (Only when Balance-Mode, result must be complemented) (Default) 1: MAX color measured
4	R/W	**Accumulation or Compare Mode** 0: Compare Mode (Default) 1:Accumulation Mode
3	R/W	**Mode Selection For SOD** 0: SOD Edge Mode (Original TYPE II MODE I) (Default) 1: SOD Edge + Pulse Mode
2	R/W	**Type Selection For DIFF**

		0: DIFF 1: (DIFF/4) * (DIFF/4) Total result for each color is divided by 8 if this bit is 1.
1	R/W	**Function (Phase/Balance) Selection** 0: Auto-Balance (Default) 1: Auto-Phase
0	R/W	**Start Auto-Function Tracking Function:** 0: stop or finished (Default) 1: start

Control Table/ Function	Sub-Function	CR7D.6	CR7D.5	CR7D.4	CR7D.3	CR7D.1	CR7C
Auto-Balance	**Max pixel**	X	1	0	0	0	X
	Min pixel	X	0	0	0	0	X
Auto-Phase Type	**Mode1**	1	1	1	0	1	Th
	Mode2	1	1	1	1	1	Th
Accumulation	**All pixel**	1	1	1	0	0	0

Table 1 Auto-Tracking Control Table

Address: 7E **VER_START_END_H (Active region vertical start Register)**

Bit	Mode	Function
7:4	R	**Active region vertical START measurement result:** bit[11:8]
3:0	R	**Active region vertical END measurement result:** bit[11:8]

Address: 7F **VER_START_L (Active region vertical start Register)**

Bit	Mode	Function
7:0	R	**Active region vertical start measurement result:** bit[7:0]

Address: 80 **VER_END_L (Active region vertical end Register)**

Bit	Mode	Function
7:0	R	**Active region vertical end measurement result:** bit[7:0]

Address: 81 **H_START_END_H (Active region horizontal start Register)**

Bit	Mode	Function
7:4	**R**	**Active region horizontal START measurement result:** bit [11:8]
3:0	R	**Active region horizontal END measurement result:** bit[11:8]

Address: 82 **H_START_L (Active region horizontal start Register)**

Bit	Mode	Function
7:0	R	**Active region horizontal start measurement result:** bit[7:0]

Address: 83 **H_END_L (Active region horizontal end Register)**

Bit	Mode	Function
7:0	R	**Active region horizontal end measurement result:** bit[7:0]

Address: 84 **AUTO_PHASE_3 (Auto phase result byte3 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[31:24]

Address: 85 **AUTO_PHASE_2 (Auto phase result byte2 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[23:16]

Address: 86 **AUTO_PHASE_1 (Auto phase result byte1 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[15:8]

Address: 87 **AUTO_PHASE_0 (Auto phase result byte0 register)**

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[7:0] The measured value of R or G or B color max or min. (Auto-Balance)

Address: 88 Reserved to 0

Video (Color Space Conversion)

Address: 89 **YUV2RGB_CTRL (YUV to RGB Control Register)** **Default: 00h**

Bit	Mode	Function
7:5	R/W	**YUV Coefficient Write Enable:** 000: h12 high byte 001: h12 low byte 010: h22 high byte 011: h22 low byte 100: h23 high byte 101: h23 low byte 110: h33 high byte 111: h33 low byte
4	--	**Reserved to 0**
3	R/W	**Enable YUV/RGB coefficient Access:** 0: Disable 1: Enable If this bit is set, the address of the data port will reset to original, and continuously writes 6 bytes
2	R/W	**Cb Cr Clamp** 0: Bypass

		1: Cb-128, Cr-128
1	R/W	**Y Gain/Offset:** 0 : Bypass 1: (Y-16)*1.164
0	R/W	**Enable YUV to RGB Conversion:** 0: Disable YUV-to-RGB conversion (Default) 1: Enable YUV-to-RGB conversion

Address: 8A **YUV_RGB_COEF_DATA**

Bit	Mode	Function
7:0	**W**	**COEF_DATA[7:0]**

YUV/RGB matrix $$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1.164(or1) & h12 & 0 \\ 1.164(or1) & -h22 & -h23 \\ 1.164(or1) & 0 & h33 \end{bmatrix} \begin{bmatrix} Y-16(orY) \\ Cr-128 \\ Cb-128 \end{bmatrix}$$

- h12: 11 bits, 1 bit integer and 10-bit fractional bits (Default: 5_80h)
- h22: 10 bits, all fractional bits (Default: 1_40h)
- h23: 9 bits, the MSB mean 0.25 (Default: 0_A0h)
- h33: 12 bits, 2 bit integer and 10-bit fractional bits (Default: 7_00h)
- To fill ‘h’ coefficients expressed by 2’s complement without signed bit.
- h22 and h23 can’t be 000h

Embedded Timing Controller

Address: 8B **TCON_ADDR _PORT** **Default: 00h**

Bit	Mode	Function
7:0	**R/W**	**Address port for embedded TCON access**

Address: 8C **TCON_DATA _PORT** **Default: 00h**

Bit	Mode	Function
7:0	**R/W**	**Data port for embedded TCON access**

Address: 8C-00 TC_CTRL1 (Timing Controller control register1) **Default: 01h**

Bit	Mode	Function
7	R/W	**Enable Timing Controller Function (Global)** 0: Disable (Default) 1: Enable **Reset all TCON pins after Enable TCON function is set and ties low.**
6	R/W	**TCON [n] Toggle Function Reset** 0: Not reset (Default) 1: reset by DVS
5	--	Reserved
4	R/W	TCON_HS compensation 0: Real TCON_HS = TCON_HS-4, Real TCON_HS = TCON_HS-4 1: Real TCON_HS = TCON_HS-27, Real TCON_HS = TCON_HS-27 If setting TCON_HS > DH_Total, then setting TCON_HS must subtract DH_Total.
3	R/W	**Reserved to 0**
2	--	Reserved
1:0	R/W	**Display Port Configuration:** 00: Reserved 01: HZ (pin 21~38) 10: LVDS 11: Reserved

Address: 8C-01 LVDS Location Pin Driving Control **Default: 08h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**Clock pair driving current doubled strength** 0: 1X 1: 2X
4	R/W	**Pin 41/42/43/44 drive current setting (digital pad)**

		0: 4mA 1: 6mA
3:2	R/W	**Display Port Driving Current Control** (Refer to 8C-01[5]) Pin 21~38 00: 2.5mA 01: 3mA 10: 3.5mA 11: 4mA
1:0	--	**Reserved**

8C-02~8c-07 Reserved

TCON Horizontal/Vertical Timing Setting

Address: 8C-08 TCON [0]_VS_LSB (TCON [0] Vertical Start LSB Register)

Bit	Mode	Function
7:0	W	**Line number [7:0] at which TCON control generation begins**

Address: 8C-09 TCON [0]_VS_MSB (TCON [0] Vertical Start/End MSB Register)

Bit	Mode	Function
7:4	W	**Line number [11:8] at which TCON control generation ends**
3:0	W	**Line number [11:8] at which TCON control generation begins**

Address: 8C-0A TCON [0]_VE_LSB (TCON [0] Vertical End LSB Register)

Bit	Mode	Function
7:0	W	**Line number [7:0] at which TCON control generation ends**

Address: 8C-0B TCON [0]_HS_LSB (TCON [0] Horizontal Start LSB Register)

Bit	Mode	Function
7:0	W	**Pixel count [7:0] at which TCON goes active**

Address: 8C-0C TCON [0]_HS_MSB (TCON [0] Horizontal Start/End MSB Register)

Bit	Mode	Function
7:4	W	**Pixel count [11:8] at which TCON goes inactive**
3:0	W	**Pixel count [11:8] at which TCON goes active**

To be triggered on rising edge of the DCLK

Address: 8C-0D TCON [0]_HE_LSB (TCON [0] Horizontal End LSB Register)

Bit	Mode	Function
7:0	W	**Pixel count [7:0] at which TCON goes inactive**

If the register number is large than display format, the horizontal component is always on.

Real TCON_HS = TCON_HS-4, Real TCON_HS = TCON_HS-4

Address: 8C-0E TCON [0]_CTRL (TCON [0] Control Register) **Default: 00h**

Bit	Mode	Function
7	R/W	**TCON [n] Enable** (Local) 0: Disable (TCON [n] output clamp to '0') (Default) 1: Enable
6	R/W	**Polarity Control** 0: Normal output (Default) 1: Inverted output
5:4	--	**Reserved to 0**
3	R/W	**Toggle Circuit Enable/Disable** 0: Normal TCON output (Default) 1: Toggle Circuit enable When using toggle circuit enable mode, the TCON[n] will be 1 clock earlier than TCON[n-1] and then toggling together, finally output will be 1 clock delay comparing to toggling result.
2:0	R/W	**TCON [5] (TCON Combination Select)** 000: Normal TCON output (Default) 001~111: Reserved **TCON [6] & TCON [7] (TCON Combination Select)** 000: Normal TCON output (Default) 001: Select TCON [n] "AND" with TCON [n-1] 010: Select TCON [n] "OR" with TCON [n-1] 011: Select TCON [n] "XOR" with TCON [n-1] 100: Select TCON [n-1] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [n-1] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [n-1] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select TCON [n] and TCON [n-1] on alternating frames. **TCON [9] (TCON Combination Select)** 000: Normal TCON output (Default) 001: Select TCON [9] "AND" with TCON [7] 010: Select TCON [9] "OR" with TCON [7] 011: Select TCON [9] "XOR" with TCON [7] 100: Select TCON [7] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [7] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [7] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select TCON [9] and TCON [7] on alternating frames.

TCON [5] /TCON [6]/TCON[7]/TCON[9] Control Registers Address Map

Address	Data(# bits)	Default

32,31,30	TCON [5]_VS_REG (11)	
35,34,33	TCON [5]_HS_REG (11)	
36	TCON [5]_CTRL_REG	00
37	Reserved	
3A,39,38	TCON [6]_VS_REG (11)	
3D,3C,3B	TCON [6]_HS_REG (11)	
3E	TCON [6]_CTRL_REG	00
3F	Reserved	
42,41,40	TCON [7]_VS_REG (11)	
45,44,43	TCON [7]_HS_REG (11)	
46	TCON [7]_CTRL_REG	00
47	Reserved	
52,51,50	TCON [9]_VS_REG (11)	
55,54,53	TCON [9]_HS_REG (11)	
56	TCON [9]_CTRL_REG	00
57	Reserved	

Control For LVDS

Address: 8C-78 LVDS_CTRL0 **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**Power up LVDS even-port** 0: Power down (Default) 1: Normal
4	R/W	**Power up LVDS odd-port** 0: Power down (Default) 1: Normal
3:2	R/W	**Watch Dog Model** 00: Enable Watch Dog(Default) 01: Keep PLL VCO = 1V 1x: Disable Watch Dog
1	--	**Reserved to 0**
0	R	**Watch Dog Control Flag**

		0: Watch dog not active (Default) 1: Watch dog active, Reset PLL and set VCO = 1V

Address: 8C-79 LVDS_CTRL1 **Default: 28h**

Bit	Mode	Function
7	R/W	**Reserved to 0**
6:4	R/W	**STSTL [2:0]: select test attribute** 000: WD 001: VCOM 010: IB40u (default) 011: IBVOCM 100: PLLTST-fbak 101: PLLTST-fin 110: LVTST-CKDIN 111: LVTST-LVDSIN[6] Note: a. Should bond to the test pad b. Signal must output at pin 28 c. Because of the pad is open drain, an external 200Ω pull high resistance is needed d. Even port must power down (CR8C-78[5])
3:0	R/W	**RSDS / LVDS Output Common Mode** (Default: 1000) 0000 : 0.67v 0001 : 0.72v 0010 : 0.77v 0011 : 0.82v 0100 : 0.88v 0101 : 0.93v 0110 : 0.98v 0111 : 1.03v 1000 : 1.08v (default) 1001 : 1.13v 1010 : 1.18v 1011 : 1.23v 1100 : 1.28v 1101 : 1.33v 1110 : 1.38v 1111 : 1.42v

Address: 8C-7A LVDS_CTRL2 **Default: 03h**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**ENIB40UX2 (Double the LVDS/RSDS output swing)** 0: 1X (default) 1: 2X
5	R/W	**ENSLOW (Inverse the Data Select)** 0: Disable (default) 1: Enable (Leading half period)
4	R/W	**CKPOLAR (Inverse the CK7X)** 0: No Inverse (default) 1: Inverse (Leading half period)
3	R/W	**PLL lock edge** 0: positive 1: negative
2:0	R/W	**Bias Generator Adjust** (011)

Address: 8C-7B LVDS_CTRL3 **Default: 1Ch**

Bit	Mode	Function
7:6	R/W	**Reserved to 0**
5:3	R/W	**SIL [2:0]**: PLL charge pump current (I=5uA+5uA*code) (Default: 011)
2:1	R/W	**SRL [1:0]**: PLL resistor (R=6K+2K*code) (Default: 10)
0	R/W	**BMTS**: Bit-Mapping Table Select 0: Table 1 (Default) 1: Table 2

TCLK+ 

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER1	ER0	EG0	ER5	ER4	ER3	ER2	ER1	ER0	EG0	ER5
TXE1	EG2	EG1	EB1	EB0	EG5	EG4	EG3	EG2	EG1	EB1	EB0
TXE2	EB3	EB2	DEN	VS	HS	EB5	EB4	EB3	EB2	DEN*6	VS*5
TXE3	ER7	ER6	RSV	EB7	EB6	EG7	EG6	ER7	ER6	RSV*7	EB7
TXO0	OR1	OR0	OG0	OR5	OR4	OR3	OR2	OR1	OR0	OG0	OR5
TXO1	OG2	OG1	OB1	OB0	OG5	OG4	OG3	OG2	OG1	OB1	OB0
TXO2	OB3	OB2	DEN	VS	HS	OB5	OB4	OB3	OB2	DEN*2	VS*1
TXO3	OR7	OR6	RSV	OB7	OB6	OG7	OG6	OR7	OR6	RSV*3	OB7

TABLE 1 Bit-Mapping 6bit(5~0)+2bit(7~6)

TCLK+ 

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5

TXE0	ER3	ER2	EG2	ER7	ER6	ER5	ER4	ER3	ER2	EG2	ER7
TXE1	EG4	EG3	EB3	EB2	EG7	EG6	EG5	EG4	EG3	EB3	EB2
TXE2	EB5	EB4	DEN	VS	HS	EB7	EB6	EB5	EB4	DEN*6	VS*5
TXE3	ER1	ER0	RSV	EB1	EB0	EG1	EG0	ER1	ER0	RSV*7	EB1
TXO0	OR3	OR2	OG2	OR7	OR6	OR5	OR4	OR3	OR2	OG2	OR7
TXO1	OG4	OG3	OB3	OB2	OG7	OG6	OG5	OG4	OG3	OB3	OB2
TXO2	OB5	OB4	DEN	VS	HS	OB7	OB6	OB5	OB4	DEN*2	VS*1
TXO3	OR1	OR0	RSV	OB1	OB0	OG1	OG0	OR1	OR0	RSV*3	OB1

TABLE 2 Bit-Mapping 6bit(7~2)+2bit(1~0)

Address: 8C-7C LVDS_CTRL4 Default: 80h

Bit	Mode	Function
7:6	R/W	**E_RSV**: even port reserve signal select 11: Always ‘1’ 10: Always ‘0’ 01: TCON[5] 00: PWM_0
5:4	R/W	**E_DEN**: even port data enable signal select 11: Always ‘1’ 10: Always ‘0’ 01: TCON[6] 00: DENA
3:2	R/W	**E_VS**: even port VS signal select 11: Always ‘1’ 10: DENA 01: TCON [7] 00: DVS
1:0	R/W	**E_HS**: even port HS signal select 11: Always ‘1’ 10: DENA 01: TCON[9] 00: DHS

Address: 8C-7D LVDS_CTRL5 Default: 80h

Bit	Mode	Function
7:6	R/W	**O_RSV**: odd port reserve signal select 11: Always ‘1’ 10: Always ‘0’ 01: TCON[5] 00: PWM_1
5:4	R/W	**O_DEN**: odd port data enable signal select 11: Always ‘1’

		10: Always ‘0’ 01: TCON[6] 00: DENA
3:2	R/W	**O_VS**: odd port VS signal select 11: Always ‘1’ 10: DENA 01: TCON [7] 00: DVS
1:0	R/W	**O_HS**: odd port HS signal select 11: Always ‘1’ 10: DENA 01: TCON[9] 00: DHS

Pin share

Address: 8D   **Pin Share ADDR Port**   **Default: 00h**

Bit	Mode	Function
7:0	R/W	Address port for pin share control access

Address: 8E   **Pin Share DATA Port**   **Default: 00h**

Bit	Mode	Function
7:0	R/W	Data port for pin share control access

Address: 8E-00   PIN_SHARE_CTRL0   Default: 00h

Bit	Mode	Function
7:6	R/W	**Pin 43** 00: DDCSDA/DDCSCL (43/44) 01: Ref to 8E-03 10: IRQ 11: DCLK_test(Input)
5	R/W	**Pin 44** 0: TCON7 1: PWM0
4	R/W	**Test Mode Enable** 0: Disable (Default) 1: Enable
3:2	R/W	**Test Mode LVDS_1(Even Port) Control(Pin 21~28)** 00: TTLO 01: TTLI 10: Reserved 11: DIFFTST
1:0	R/W	**Test Mode LVDS_2 (Odd Port) Control: (Pin 29-38)** 00: TTLO 01: TTLI 10: Reserved 11: DIFFTST

Address: 8E-01   PIN_SHARE_CTRL1   Default: 00h

Bit	Mode	Function
7	R/W	**Test Mode TLLO Output Port Select (Even Data or Odd Data Output)** 0: EVEN (default) 1: ODD
6:3	R/W	**CR8D[3:2] = 00 (TTL0) : (Pin29~38)** 0000: ADC_CLK, IVS_DLY, INPUT_RED[7:0]

		0001: ADC_CLK, IHS_DLY, INPUT_GREEN[7:0] 0010: ADC_CLK, EN_FLAG, INPUT_BLUE[7:0] 0011: ADC_CLK, RAW_ODD, FIFO_CLK,VGIP_CLK, internal_crystal , IHS_DLY, RAW_HS, RAW_VS, ABL_AVG, ABL_WAIT 0100: DCLK, DVS, DHS, DEN, ODDX, HS0_SCHMITT, TCON[3:0] 0101: DRED[7:0], DITHER_R[1:0] 0110: DBLU[7:0], DITHER_B[1:0] 0111: DGRN[7:0],DITHER_G[1:0] 1000: ADC_CLK, HS_OUT, COAST, CLAMP_G, RAW_VS, SYNC_CAP_WINDOW, RAW_ODD, IFD_ODD, SOG_IN, HS_FB 1001: MCUWR, MCU_ADR_INC, MIN[7:0] 1010: MCU_ADR_INC, MADR[7:0], MCURD 1011 : TMDS_DBG_OUT[17:8]
3	R/W	**Reserved**
2:0	R/W	**CR8D[1:0] = 00 (TTLO) : (Pin21-28)** 000: DRED[7:0] 001: SD_GREEN[7:0] 010: SD_BLUE[7:0] 011: VGIP_CLK, IVS_DLY, IHS_DLY, IFD_ODD, IENA, AUTO_HS, AUTO_VS AUTO_FIELD 100: DVS, DHS, DEN, ODDX, DITHER_R[1:0], DECMP_HS, Clamp_RB 101: IVS_DLY, IHS_DLY, RAW_ODD, RAW_DEN, MEAS_IHS, PHASE_ERROR, FAV4, MSB_2 110: DCLK, DVS, DHS, DCLK_16, SDMOUT_TST[3:0] 111: TMDS_DBG_OUT[7:0] **CR8D[1:0] = 01 (TTLI): (Pin21-28)** Pin21 (TEST_CLK for ADC)

Address: 8E-02 **PIN_SHARE_CTRL2** **Default: 00h**

Bit	Mode	Function
7	R/W	**Pin21 & Pin22(ADC clock from PLL2)** 0:Disable (Default) 1:Enable
6	R/W	**Pin23 & Pin24 (PLL1 Clock)** 0:Disable (Default) 1:Enable
5	R/W	**Pin25& Pin26 (DPLL Status)**

		0:Disable (Default) 1: Enable
4	R/W	**Pin27 & Pin28 (PLL2 Phase0 Clock)** 0:Disable (Default) 1: Enable
3	R/W	**Pin29 & Pin30 (DPLL clock)** 0:Disable (Default) 1: Enable
2	R/W	**Pin31 & Pin32 (PLL1 Status)** 0:Disable (Default) 1: Enable
1	R/W	**Pin33 & Pin34 (FAV clock from PLL1)** 0:Disable (Default) 1: Enable
0	R/W	**Pin35 & Pin36 (PLL2 Status)** 0:Disable (Default) 1: Enable

Address: 8E-03 **PIN_SHARE_CTRL3** **Default: 00h**

Bit	Mode	Function
7	R/W	**Pin37 & Pin38 (MPLL Clock)** 0:Disable (Default) 1:Enable
6	R/W	**Pin 43 sub option** 0: PWM1 1: TCON9
5:0	--	**Reserved**

Embedded OSD

Address: 90 **OSD_ADDR_MSB (OSD Address MSB 8-bit)**

Bit	Mode	Function
7:0	R/W	**OSD MSB 8-bit address**

Address: 91 **OSD _ADDR_LSB (OSD Address LSB 8-bit)**

Bit	Mode	Function
7:0	R/W	**OSD LSB 8-bit address**

Address: 92 **OSD_DATA_PORT (OSD Data Port)**

Bit	Mode	Function
7:0	W	**Data port for embedded OSD access**

Refer to the embedded OSD application note for the detailed.

Address: 93 **OSD_SCRAMBLE** **Default: 05h**

Bit	Mode	Function
7	R/W	**BIST Start** 0: stop (Default) 1: start (auto clear)
6	R	**BIST Result** 0: fail (Default) 1: success
5	R	**MCU writes data when OSD ON status (Queue 1 byte data)** 0: MCU writes data to OSD but not to real position (There is one level buffer here) 1: MCU doesn't write data, or data has been written to real position
4	R	**Double_Buffer_Write_Status** 0: double buffer write out is finish, or data write to double buffer is not ready, or no double buffer function. 1: after data write to dbuf and before dbuf write out, such that double buffer is busy.
3	R/W	**OSDADRHSB** **0: If initial address lower than or equal to 12K** **1: If initial address higher than 12K** The bit will be designed to control 16.5K bytes SRAM. However it will have no effect for WINDOW setting. Also please remember to set {OSDADRHSB, OSDADRMSB(CR90), OSDADRLSB(CR91) } again while you like to R/W a new address.
2:0	R/W	**Double buffer depth (Default=6)** **000~101=>1~6**

Address: 94 **OSD_TEST**

Bit	Mode	Function
7:0	R/W	**Testing Pattern**

Low Voltage Detection

Address: 95 **POWER_ON_RESET_REGULATOR** **Default: 14h**

Bit	Mode	Function
7:6	R/W	**Negative Threshold Value For Power on Reset** 00:1.8V(Default) 01:2.0V 10:2.2V 11:2.4V
5:0	--	**Reserved**

Address: 96 **EBD_REGLATOR_VOL** **Default: 88h**

Bit	Mode	Function
7:5	R/W	**Embedded Regulator Voltage Value[2:0]** 000 to 111 => 2.2V to 1.5V (Default 100=>1.8V)
4:3	R/W	**Band-gap Voltage of Regulator Adjust** 00: 1.147V 01: 1.219V 10: 1.291V 11: 1.136V Default: 01
2:0	--	**Reserved to 0**

Schmitt Trigger Control

Address: 97 **HS_SCHMITT_TRIGGE_CTRL** **Default: 41h**

Bit	Mode	Function
7	R/W	**HSYNC Schmitt Power Down (Only for Schmitt trigger new mode)** 0: Power down (Default) 1: Normal
6	R/W	**Polarity Select** 0: Negative HSYNC (high level) 1: Positive HSYNC (low level) (Default)
5	R/W	**Schmitt Trigger Mode** 0: Old mode (Default) 1: New mode
4	R/W	**Threshold Voltage Fine Tune (only for Schmitt trigger new mode)** 0: 0V (Default)

		1: -0.1V
3:2	R/W	**Positive Threshold Voltage**
1:0	R/W	**Negative Threshold Voltage**

- There are 3 mode of the HSYNC Schmitt trigger.
  1. Old mode 1: original HSYNC Schmitt trigger.
     bit[6:5]=00 è V_t^+ = 1.5V, V_t^- = 1.0V
  2. Old mode 2: The easy HSYNC Schmitt trigger.
     bit[6:5]=10 è

Bit[1:0]	V_t^+	V_t^-
01	2.0V	1.5V
11	1.5V	1.0V

  3. New mode: Fully programmable Schmitt trigger.
     The following table will determine the Schmitt Trigger positive and negative voltage:

bit[6]=1 (Positive HSYNC)				**bit[6] = 0** (Negative HSYNC)			
bit[3:2]	V_t^+	**bit[1:0]**	V_t^-	**bit[3:2]**	V_t^+	**bit[1:0]**	V_t^-
00	1.4V	00	V_t^+ - 1.2V	00	1.8V	00	V_t^+ - 1.2V
01	1.6V	01	V_t^+ - 1.0V	01	2.0V	01	V_t^+ - 1.0V
10	1.8V	10	V_t^+ - 0.8V	10	2.2V	10	V_t^+ - 0.8V
11	2.0V	11	V_t^+ - 0.6V	11	2.4V	11	V_t^+ - 0.6V

- After we get the threshold voltage by the table, we still can fine tune it:
  Final Positive Threshold Voltage = V_t^+ - 0.1* bit[4]
  Final Negative Threshold Voltage = V_t^-- 0.1* bit[4]

Phase-Lock-Loop (PLL)

DDS Setting for ADC

Address: 98 **PLL_DIV_CTRL** **Default: 04h**

Bit	Mode	Function
7	R/W	**PFD Selection** 0: New PFD fine (Default) 1: New PFD coarse (the resolution will be 1/2 of the PFD fine mode)
6	R/W	**DDS Tracking Edge** 0: HS positive edge (Default) 1: HS negative edge
5	R/W	**DDS Reset Enable** 0: Normal function (Default) 1: DDS circuit's reset will be asserted, for test only
4	R/W	**Test Mode**: (for production test) 0: Normal (Default) 1: Test Mode
3	R/W	**HS output synchronized by** 0: phase 32 1: phase 0 (Default)
2:1	R/W	**Delay Compensation Mode** 00: Mode 0 01: Mode 1 10: Mode 2 (Default) 11: Mode 3
0	R/W	**Clock select for DIV** 0: phase 0 (phase-0 of PLL2) (Default) 1: internal CLK (Fav)

Address: 99 **I_CODE_L** **Default: 47h**

Bit	Mode	Function
7:3	R/W	**Old/New mode:** I_Code [9:5] (Default: 01000)
2	R/W	**Old mode:** I_Code [4] (Default=1) **New mode:** I-code control mechanism 0: new linear mode, PE*(2+NEW_I[13]) 1: old mode, P-code = I[17:0] – 1 (Default)
1:0	R/W	**Old mode:** I_Code [3:2] (Default: 11) **New mode**: P-code protection mode 00 => No protection 01 => 1 bit protection 10 => 2 bits protection 11 => 3 bits protection (Default)

Address: 9A **I_CODE_M** **Default: 00h**

Bit	Mode	Function
7:6	R/W	**Old mode :**I_Code [15:14] (Default: 00)
5	R/W	**Old mode :**I_code [13] (Default:0)

		New mode : I_code calibrated setting
4	R/W	**Old mode :** I_Code [12] (Default:0) **New mode :** P_code calibrated setting
3	R/W	**Old mode :** I_Code [11]
2	R/W	**I_Code [10] or PFD type selection** 0: Old PFD (Default) 1: New PFD
1	R/W	**Old mode :** I_Code [1] (Default: 0) **New mode :** P-code mapping curve 0: choose the new P-code mapping curve (PE*2+NEW_I[12])* 2^{NEW_P+2} 1: choose the old P-code mapping curve
0	R/W	**Old mode:** I_Code [0] (Default: 0) **New mode:** I-code multiplication factor 0: choose the new I-code multiplication factor = $2^{(NEW\_I[9:5]+2)}$ 1: choose the old I-code multiplication factor

I CONTROL =(I-CODE control mechanism)*(I-code multiplication factor)

Address: 9B **P_CODE** **Default: 18h**

Bit	Mode	Function
7	R/W	**Phase Swallow Down Enable** 0: Swallow Up (Default) 1: Swallow Down
6:5	R/W	**I_Code[17:16]** Default: 00b
4:0	R/W	**P_Code[4:0]** Default: 18h

Address: 9C **PFD_CALIBRATED_RESULTS** **Default: 8'b 00xxxxxx**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**PFD Calibration Enable** Overwrite 0 to 1 return a new PFD calibrated value.
5:0	R	**PFD Calibrated Results[5:0]**

Address: 9D **PE_MEARSURE** **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved to 0**
5	R/W	**PE Measure Enable** 0: Disable (Default) 1: Start PE Measurement, clear after finish.
4:0	R	**PE Value Result [4:0]**

Address: 9E **PE_MAX_MEASURE** **Default: 00h**

Bit	Mode	Function
7	---	**Reserved to 0**
6	R/W	**PE Max. Measure Enable** 0: Disable (Default) 1: Start PE Max. Measurement
5	R/W	**PE Max. Measure Clear** 0: clear after finish (Default) 1: write '1' to clear PE Max. Value
4:0	R	**PE Max Value[4:0]**

Address: 9F **FAST_PLL_CTRL** **Default: 00h**

Bit	Mode	Function
7	--	**Reserved to 0**
6	R/W	**Enable APLL Setting** 0: Disable (Default) 1: Enable (Auto clear when finished) When CR9F[5] enabled, enable this bit will write PLL2M/N, PLLDIV and DDS SUM_I at the end of input vertical data enable
5	R/W	**Enable Fast PLL Mechanism** 0: Disable (Default) 1: Enable
4	--	**Reserved to 0**
3	R/W	**DDS I_SUM Setting Updated Enable** 0: Disable (Default) 1: Enable (Auto clear when finished)
2	R/W	**Measure I_SUM** 0: Disable 1: Enable (Auto clear after finish)
1	R/W	**Enable Port A0** 0: Disable Port A0 Access 1: Enable Port A0 Access When this bit is 0, port address will be reset to 00, and will auto increase when read or write
0	R/W	**Select I_SUM for Read** 0: Select SUM_I_PRE [32:1] for read 1: Select SUM_I_NOW [32:1] for read

Address: A0 **FAST_PLL_ISUM**

Bit	Mode	Function

7:0	R/W	**I_SUM (Auto Increase)** **1st I_SUM[31:24]** **2nd I_SUM[23:16]** **3rd I_SUM[15:8]** **4th I_SUM[7:0]**

ADC PLL1

Address: A1 **PLL1_M (M Parameter Register)** **Default: 0Fh**

Bit	Mode	Function
7:0	R/W	**PLL1M[7:0] (PLL1 DPM value – 2)**

Address: A2 **PLL1_N (N Parameter Register)** **Default: 80h**

Bit	Mode	Function
7	R/W	**PLL1PWDN (PLL1 Power Down)** 0: Normal Run 1: Power Down (Default)
6:4	---	**Reserved to 0**
3:0	R/W	**PLL1N[3:0] (PLL1 DPN value – 2)**

- PLL1_N modify to only 4-bit.
- Assume PLL1_M=0x0B, P1M=0x0B+2=13; PLL1_N=0x03, P1N=0x03+2=5; F_IN = 24.576MHz. F_PLL1 = F_IN x P1M / P1N = 24.576 x 13 / 5 = 63.8976MHz
- If the target frequency is F_ADC, the constraint of F_PLL1 is (15/16)*F_ADC < F_PLL1 < F_ADC

Address: A3 **PLL1_CRNT (PLL1 Current/Resistor Register)** **Default: 33h**

Bit	Mode	Function
7	R/W	**Reserved to 0**
6:4	R/W	**PLL1VR[2:0] (PLL1 Loop Filter Resister Control)** 000: 20K 001: 21K 010: 22K 011: 23K (Default) 100: 24K 101: 25K 110: 26K 111: 27K
3:0	R/W	**PLL1SI[3:0] (PLL1 Charger Pump Current IchDpll) (Default: 0011b)** Icp = 2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]+20uA*bit[3]

- **Keep Icp/DPM constant**

Address: A4 **PLL1_WD (PLL1 Watch Dog Register)** **Default: 0Eh**

Bit	Mode	Function
7	R	**PLL1STATUS (PLL1 WD Status)**

		0: Normal (Default) 1: Abnormal
6	R/W	**PLL1WDRST (PLL1 WD Reset)** 0: Normal (Default) 1: Reset
5	R/W	**PLL1WDSET (PLL1 WD Set)** 0: Normal (Default) 1: Set
4:3	R/W	**PLL1WDVSET[1:0] (PLL1 WD Voltage Set)** 00: 2.46V 01: 1.92V(Default) 10: 1.36V 11: 1.00V
2	R/W	**PLL1UPDN (PLL1 Frequency Tuning Up/Down)** 0: Freq Down 1: Freq Up (Default)
1	R/W	**PLL1MSBSTOP (PLL1 Frequency Tuning Enable)** 0: Disable 1: Enable (Default)
0	---	**Reserved to 0**

ADC PLL2

Address: A5 **PLL2_M (M Parameter Register)** **Default: 3Eh**

Bit	Mode	Function
7:0	R/W	**PLL2_M[7:0] (PLL2 DPM value – 2) (Default 3E)**

Address: A6 **PLL2_N (N Parameter Register)** **Default: 3Dh**

Bit	Mode	Function
7:0	R/W	**PLL2_N[7:0] (PLL2 DPN value – 2) (Default 3D)**

- Assume PLL2_M=0x0A, P2M=0x0A+2=12; PLL2_N=0x04, P2N=0x04+2=6; F_IN =65 MHz .
- F_PLL2 = F_IN x P2M x 2 / P2N /2 = 65 x 12 x 2 / 6 / 2 = 130 MHz
- the constraint of F_PLL2 is that *P2N =(int)(F_IN / 10)*

Address: A7 **PLL2_CRNT (PLL2 Current/Resistor Control)** **Default: 6Fh**

Bit	Mode	Function
7:5	**R/W**	**PLL2VR[2:0] (PLL2 Loop Filter Resister Control)** 000: 15K 001: 16K 010: 17K 011: 18K 100: 19K

		101: 20K 110: 21K 111: 22K
4:0	**R/W**	**PLL2SI[4:0] (PLL2 Charger Pump Current IchDpll)** Icp = 2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]+20uA*bit[3]+30uA*bit[4]

- **Keep Icp/DPM constant**

Address: A8 **PLL2_WD (PLL2 Watch Dog Register)** **Default: 08h**

Bit	Mode	Function
7	R	**PLL2STATUS (PLL2 WD Status)** 0: Normal (Default) 1: Abnormal
6	R/W	**PLL2WDRST (PLL2 WD Reset)** 0: Normal (Default) 1: Reset
5	R/W	**PLL2WDSET (PLL2 WD Set)** 0: Normal (Default) 1: Set
4:3	R/W	**PLL2WDVSET[1:0] (PLL2 WD Voltage Set)** 00: 2.46V 01: 1.92V(Default) 10: 1.36V 11: 1.00V
2:1	R/W	**ADCKMODE[1:0] (ADC Input Clock Select Mode)** 00 : Single Clock Mode (Default) 01 : Single Inverse-Clock Mode 10 : External Clock Mode 11 : Dual Clock Mode (1x and 2x Clock)
0	R/W	**PLL2PWDN (PLL2 Power Down)** 0: Normal Run(Default) 1: Power Down

Address: A9 **PLLDIV_H** **Default: 05h**

Bit	Mode	Function
7	---	**Reserved to 0**
6	**R/W**	**Phase_Select_Method** 0: Manual (Default) 1: Look-Up-Table
5	**R/W**	**PLL2PH0PATH**

		0: Short Path (Default) 1: Long Path (Compensate PLL_ADC path delay)
4	**R/W**	**PLL2D2** 0:ADC CLK=1/2 VCO CLK (Default) 1:ADC CLK=1/4 VCO CLK
3:0	**R/W**	**PLL Divider Ratio Control. High-Byte [11:8]. (Default: 5h)**

When the ADC CLK is about 25MHz or 13.5MHz , we suggest that PLL2D2 should be **"1"**

Address: AA **PLLDIV_L** **Default: 3Fh**

Bit	Mode	Function
7:0	R/W	**PLL Divider Ratio Control**. **Low-Byte [7:0]**. PLLDIV should be double buffered when PLLDIV_LO changes and IDEN_STOP occurs.

- This register determines the number of output pixel per horizontal line. PLL derives the sampling clock and data output clock (DCLK) from input HSYNC. *The real operation Divider Ratio = PLLDIV+1*
- The power up default value of PLLDIV is 053Fh(=1343, VESA timing standard, 1024x768 60Hz, Horizontal time).
- The setting of PLLDIV must include sync, back-porch, left border, active, right border, and front-porch times.
- Control-Register A9 & AA will filled in when Control-Register AA is written.

Address: AB **PLLPHASE_CTRL0 (Select Phase to A/D)** **Default: 30h**

Bit	Mode	Function
7	R/W	**PLL2D2X control** (Default=0)
6	R/W	**PLL2D2Y control** (Default=0)
5	R/W	**PLL2X (PLL2 X Phase control)** (Default=1)
4	R/W	**PLL2Y (PLL2 X Phase control)** (Default=1)
3:0	R/W	**PLL2SCK[4:1] (PLL2 32 Phase Pre-Select Control)** (Default=0h)

Address: AC **PLLPHASE_CTRL1 (Select Phase to A/D)** **Default: 00h**

Bit	Mode	Function
7	R/W	**PLL2SCK[0] (PLL2 32 Phase Pre-Select Control)** (Default=0)
6	R/W	**MSB of 128 phase** (Only for ADC CLK=1/4 VCO CLK) (Default=0)
5:0	R/W	**Phase Select the index of Look-Up-Table[5:0]** (Default=0)

- **When Phase_Select_Method=1, Phase is selected by CR[AC]-Bit[6:0].**
- **When Phase_Select_Method=0, PLL2D2X, PLL2D2Y, PLL2X, PLL2Y, PLL2SCLK[4:0] Should be double buffered when PLL2SCK[0] is updated**

Address: AD **PLL2_PHASE_INTERPOLATION** **Default: 50h**

Bit	Mode	Function
7:6	R/W	**PLL2 Phase Interpolation Control Load (Default: 01)**
5:3	R/W	**PLL2 Phase Interpolation Control Source (Default: 010)**
2:1	R/W	**PLL2 Add Phase Delay** 00: Original phase selected by X,Y and 16-phase pre-select 01-11: Add 1-3 delay to Original phase selected by X,Y and 32-phase pre-select

0	R/W	**Reserved to 0**

When the ADC CLK is 13.5 MHz, PLL2D2 is set to “1” or “PLL2 Phase Interpolation Control Load” should be “00”

When the ADC CLK is NOT 13.5 MHz, “PLL2 Phase Interpolation Control Load” could be the default value

Phase	[XY^^^^^]	Phase	[XY ^^^^^]	Phase	[XY ^^^^^]	Phase	[XY ^^^^^]
0	[11 00000]	**16**	[01 10000]	**32**	[10 00000]	**48**	[00 10000]
1	[11 00001]	**17**	[01 10001]	**33**	[10 00001]	**49**	[00 10001]
2	[11 00010]	**18**	[01 10010]	**34**	[10 00010]	**50**	[00 10010]
3	[11 00011]	**19**	[01 10011]	**35**	[10 00011]	**51**	[00 10011]
4	[11 00100]	**20**	[01 10100]	**36**	[10 00100]	**52**	[00 10100]
5	[11 00101]	**21**	[00 10101]	**37**	[10 00101]	**53**	[00 10101]
6	[11 00110]	**22**	[00 10110]	**38**	[10 00110]	**54**	[00 10110]
7	[11 00111]	**23**	[01 10111]	**39**	[10 00111]	**55**	[00 10111]
8	[11 01000]	**24**	[01 11000]	**40**	[10 01000]	**56**	[00 11000]
9	[11 01001]	**25**	[01 11001]	**41**	[10 01001]	**57**	[00 11001]
10	[01 01010]	**26**	[10 11010]	**42**	[10 01010]	**58**	[11 11010]
11	[01 01011]	**27**	[10 11011]	**43**	[10 01011]	**59**	[11 11011]
12	[01 01100]	**28**	[10 11100]	**44**	[00 01100]	**60**	[11 11100]
13	[01 01101]	**29**	[10 11101]	**45**	[00 01101]	**61**	[11 11101]
14	[01 01110]	**30**	[10 11110]	**46**	[00 01110]	**62**	[11 11110]
15	[01 01111]	**31**	[10 11111]	**47**	[00 01111]	**63**	[11 11111]

DISPLAY PLL

Address: AE **DPLL_M (DPLL M Divider Register)** **Default: 2Ch**

Bit	Mode	Function
7:0	R/W	**DPLLM[7:0] (DPLL DPM value – 2)**

Address: AF **DPLL_N (DPLL N Divider Register)** **Default: 83h**

Bit	Mode	Function
7	R/W	**DPLLPWDN (DPLL Power Down)** 0: Normal Run 1: Power Down (Default)
6	R/W	**DPLLFREEZE (DPLL Output Freeze)** 0: Normal (Default) 1: Freeze
5:4	R/W	**DPLLO[1:0] (DPLL Output Divider)** 00: Div1 (Default) 01: Div2 10: Div4

		11: Div8
3:0	R/W	**DPLLN[3:0] (DPLL DPN value – 2) (Default: 3h)**

- Assume DPLL_M=0x7D, DPM=0x7D+2=127; DPLL_N=0x0A, DPN=0x0A+2=12; Divider=1/4, F_IN = 24.576MHz. F_DPLL = F_IN x DPM / DPN x Divider = 24.576 x 127 / 12 / 4 = 65.024MHz.
- If LPF_Mode = 1, suppose DPM=110, DPN = 12, Ich = Idch[0010] = 3.2uA, DPLL=225MHz, then DPM / Ich =36.67 Please keep the ratio as constant.
- If LPF_Mode = 0, suppose DPM=46, DPN = 5, Ich = Idch [1000] =9.15uA, DPLL=226MHz, then DPM / Ich = 5.11 Please keep the ratio as constant.

Address: B0 **DPLL_CRNT (DPLL Current/Resistor Register)** **Default: 88h**

Bit	Mode	Function
7:6	R/W	**DPLLVR[1:0] (DPLL Loop Filter Resister Control)** 00: 16K (LPF Mode = 0), 46K (LPF Mode = 1) 01: 18K (LPF Mode = 0), 53K (LPF Mode = 1) 10: 20K (LPF Mode = 0), 60K (LPF Mode = 1) (Default) 11: 22K (LPF Mode = 0), 67K (LPF Mode = 1)
5:4		**Reserved**
3:0	R/W	**DPLLSI[3:0] (DPLL Charger Pump Current IchDpll) (Default: 1000)** Icp=(1uA+1uA*bit[0]+2uA*bit[1]+4uA*bit[2]+8uA*bit[3])

- Keep Icp/DPM constant

Address: B1 **DPLL_WD (Watch Dog Register)** **Default: 16h**

Bit	Mode	Function
7	R	**DPLLSTATUS (DPLL WD Status)** 0: Normal 1: Abnormal
6	R/W	**DPLLWDRST (DPLL WD Reset)** 0: Normal (Default) 1: Reset
5	R/W	**DPLLWDSET (DPLL WD Set)** 0: Normal (Default) 1: Set
4:3	R/W	**DPLLWDVSET[1:0] (DPLL WD Voltage Set)** 00: 0.58V 01: 0.74V 10: 0.88V (Default) 11: 1.17V
2	R/W	**DPLLUPDN (DPLL Frequency Tuning Up/Down)** 0: Freq Up 1: Freq Down (Default)
1	R/W	**DPLLSTOP (DPLL Frequency Tuning Enable)**

		0: Disable 1: Enable (Default) Turn on before CRBB[0].
0	R/W	**DPLLLPFMODE (DPLL LPF Mode)** 0: DPN<=5 è LPFMode=0 Ich=9.15uA DPM=46 DPN=5 (Default) 1: 16>=DPN>=5 è LPFMode=1 Ich=3.2uA DPM=110 DPN=12

Address: B2 **DPLL Other** **default: 06h**

Bit	Mode	Function
7:5	--	**Reserved**
4	**R/W**	**DPLL Clock to SSCG** 0: DPLLVCO/4 (Defalult) 1: (DPLLVCO+Phase_Swallow)/4
3	**R/W**	**DPLL Reference Frequency Select** 0: Original Crystal Clock (Default) 1: Clock After M2PLL
2	**R/W**	**DPLL VCO RON (increase VCO_OP Phase Margin)** 0: Disable 1: Enable (Default)
1	**R/W**	**DPLL VCO START (startup VCO)** 0: Disable 1: Enable (Default)
0	**R/W**	**DPLL BPN (DPLL dividend enable)** 0: DPLL_N dividend enable 1: N dividend disable

MULTIPLY PLL FOR INPUT CYRSTAL

Address: B3 **M2PLL_ADDR_PORT**

Bit	Mode	Function
7:3	--	**Reserved**
2:0	**R/W**	**Address for M2PLL access**

Address: B4 **M2PLL_DATA _PORT**

Bit	Mode	Function
7:0	**R/W**	**Data Port for M2PLL**

Address: B4-00 **MULTI_PLL_CTRL0** **Default: 92h**

Bit	Mode	Function
7:3	R/W	**M2PLL M Code[4:0]-2 (DPM) (shall not be 0)** **Default = 20 => 10010**

2	R/W	**M2PLL Power Down** 0: Normal Run (Default) 1: Power Down
1	R/W	**M2PLL N Code** 0: N=1 1: N=2 (Default)
0	R/W	Reserved to 0

VCO range = 120MHz ~ 250MHz
FIF0_ clock = Fxtal_ * M2PLL_M / M2PLL_N
POR clock = Fxtal * M2PLL_M / M2PLL_N / 8

Address: B4-01 **MULTI_PLL_CTRL1** **Default: 94h**

Bit	Mode	Function
7:6	R/W	**M2PLL Loop Filter Resistor Control** 00: 15K 01: 18K 10: 21K(Default) 11: 24K
5:4	R/W	**M2PLL Loop Filter Charge Current Control(Default:01)** Icp=5uA+5uA*bit[4]+10uA*bit[5] i.e.: Keep Icp/DPM constant
3:2	R/W	**M2PLL WD Voltage** 00: 0.80V 01: 1.0V (Default) 10: 1.2V 11: 1.4V
1	R/W	**M2PLL_WDRST** 0: Normal (Default) 1: Reset (M2PLL Function as a Normal PLL, regardless WD)
0	R/W	**M2PLL_WDSET** 0: Normal (Default) 1: Set (Free Run by WD asserts VCO Voltage)

Address: B4-02 **MULTI_PLL_CTRL2** **Default: 40h**

Bit	Mode	Function
7	R	**M2PLL WD Status** 0: Normal 1: Abnormal
6	R/W	**M2PLL Output Freeze (FIFO clock)** 0: Normal

		1: Freeze (Default) i.e.: when output is frozen, the internal PLL is still operating
5:0	--	**reserved**

CRB4-00~02 are not controlled by software reset.

DCLK Spread Spectrum

Address: B5 **DCLK_FINE_TUNE_OFFSET_MSB** **Default: 00h**

Bit	Mode	Function
7:6	--	**Reserved**
5	R/W	**Only Even / Odd Field Mode Enable** 0: Disable (Default) 1: Enable
4	R/W	**Even / Odd Field Select** 0: Even (Default) 1: Odd
3:0	R/W	**DCLK Offset** [11:8] in Fixed Last Line DVTOTAL & DHTOTAL

Address: B6 **DCLK_FINE_TUNE_OFFSET_LSB** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**DCLK Offset** [7:0] in Fixed Last Line DVTOTAL & DHTOTAL

Address: B7 **SPREAD_SPECTRUM** **Default: 00h**

Bit	Mode	Function
7:4	R/W	**DCLK Spreading range** (0.0~7.5%) The bigger setting, the spreading range will bigger, but not uniform
3	R/W	**Spread Spectrum FMDIV** (SSP_FMDIV)//(0) 0: 33K 1: 66K
2	R/W	**Spread Spectrum Setting Ready for Writing** (Auto Clear) 0: Not ready 1: Ready to write
1:0	R/W	**Frequency Synthesis Select** (F & F-N*dF) 00~11: N=1~4

- The "Spread Spectrum Setting Ready for Writing" means 4 kinds of registers will be set after this bit is set:
  1. DCLK spreading range
  2. Spread spectrum FMDIV
  3. DCLK offset setting
  4. Frequency synthesis select

Address: B8 **FIXED_LAST_LINE_MSB**

Bit	Mode	Function

6:4	R/W	**Fixed Last Line Length** [11:8]
3:0	R/W	**Fixed DVTOTAL** [11:8]

Address: B9 **FIXED_LAST_LINE_DVTOTAL _LSB**

Bit	Mode	Function
7:0	R/W	**Fixed DVTOTAL** [7:0]

Address: BA **FIXED_LAST_LINE_ LENGTH_LSB**

Bit	Mode	Function
7:0	R/W	**Fixed Last Line Length** [7:0]

- Fixed last line value can't be zero, and can't smaller than DH_Sync width.

Address: BB **FIXED_LAST_LINE_CTRL** **Default: 00h**

7:4	--	**Reserved to 0**
3	R/W	**Enable New Design Function in Fixed Last Line Mode** 0: Disable (Default) 1: Enable
2	R/W	**DDS Spread Spectrum Test Enable** 0: Disable (Default) 1: Enable
1	R/W	**Enable the Fixed DVTOTAL & Last Line DHTOTAL Function** 0: Disable (Default) 1: Enable
0	R/W	**Enable DDS Spread Spectrum Output Function** 0: Disable (Default) 1: Enable

Procedure:

- First, we have set M/N code and then we need to tune DCLK OFFSET to achieve frame-sync, every step of offset frequency is DCLK/ 2^{15}.
- When we finished the frame-sync, we turn on CR BB[1] to let the system running in to free-run mode, at this time, the CRB8,CRB9,CRBA are the reference DV and DH total and Fixed last Line Length.
- But the free-run mode DVS' should be close to frame-sync mode DVS to achieve pseudo-frame-sync(actually, it is free run mode now)
- Then we use CRB7 [1:0] (F-N*dF) to keep DVS' and DVS very closely to achieve pseudo-frame-sync.

Notice:

- In RTD2525LH, when all the setting above is ready, then we open spread spectrum function, the DCLK OFFSET will shift, please keep the DCLK OFFSET keeps steady when we open spread spectrum function.
- In Real free-run mode, the DV_TOTAL refers to CR32/CR33, and in Fixed-Last-Line mode, the free-run timing DV_TOTAL refers to CRB8/CRB9, at this time CR35/36 serve for Vsync-timeout watch dog reference.

Embedded TMDS

Address: BC **TMDS_MEASURE_SELECT** **Default: 00h**

Bit	Mode	Function
7	R/W	**Transition measurement method** 0: measure the number of transition for N-clock duration (CRBC[3:0]) 1: measure the number of transition smaller than 16 or 64 clock period (CRBD[0]) for 1-frame duration
6:4	R/W	**Measure times(exponential of 2)** 000: 1 001: 2 010: 4 011: 8 100: 16 101: Not available 110: Not available 111: Not available
3:0	R/W	**Numbers of Clock Period, measurement duration (where clock frequency is 12Khz)** 0000: 16 0001: 1 0010: 2 0011: 3 ……. 1111: 15

This function will do bit [6:4] times, each time lasts for bit [3:0]/12 ms.

Address: BD **TMDS_MEAS_RESULT0** **Default: 0000_0110b**

Bit	Mode	Function
7	R/W	**Transition measurement** 0:Stop measure, Cleared after finish (Default) 1:Start measure
6:5	R/W	**Measure Result Select** 00: AVE Value (Default) 01: Max Value 10: Min Value
4:3	R/W	**Measure Select** 00: Measure Hsync transition times before error correction.

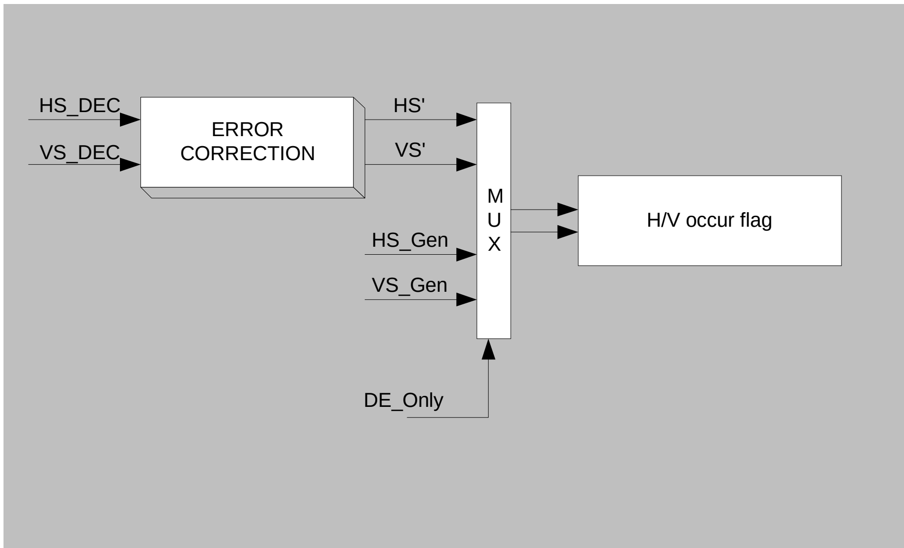
		01: Measure Hsync transition times after error correction. 10: Measure Data Enable transition times before error correction. 11: Measure Data Enable transition times after error correction.
2	**R/W**	**Clock DC Offset** 0: Disable 1: Enable DC Offset Compensation
1	**R/W**	**R/G/B DC Offset** 0: Disable 1: Enable DC Offset Compensation
0	**R/W**	**Criterion of Transition Count, duration smaller than** 0: 16 clock 1: 64 clock

Address: BE **TMDS_MEAS_RESULT1**

Bit	Mode	Function
7	**---**	**Reserved**
6:0	**R**	**Value of measure result**[6:0] (Item refer to CRBD[6:5])

Address: BF **TMDS_CTRL**

Bit	Mode	Function
7	R	**B channel detect (DE low 128 clock)(write clear)** 0: no 1: yes
6	R	**G channel detect (DE low 128 clock)(write clear)** 0: no 1: yes
5	R	**R channel detect (DE low 128 clock)(write clear)** 0: no 1: yes
4	R	**Hsync occur (write clear)** 0: no 1: yes
3	R	**Vsync occur (write clear)** 0: no 1: yes
2:0	--	**Reserved**



Address: C0 **CRC_OUTPUT_BYTE_2**

Bit	Mode	Function
7:0	R/W	**1st read=> Output CRC-24 bit 23~16** **2nd read=> Output CRC-24 bit 15~8** **3rd read=> Out put CRC-24 bit 7~0**

- The read pointer should be reset when 1. CRC Output Byte is written 2. CRC Check starts.
- The read back CRC value address should be auto-increase, the sequence is shown above

Address: C1 **TMDS_OUTPUT_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**Auto Output Enable** 0: Disable (Default) 1: Enable
6	R/W	**TMDS R Channel Output Enable** 0: Disable (Default) 1: Enable
5:	R/W	**TMDS G Channel Output Enable** 0: Disable (Default) 1: Enable
4	R/W	**TMDS B Channel Output Enable** 0: Disable (Default) 1: Enable
3	R/W	**OCLK Enable** 0: Disable (Default) 1: Enable

Bit	Mode	Function
2	R/W	**OCLK Invert enable** 0: Normal (Default) 1: Enable
1	--	**Reserved**
0	R/W	**CLK25XINV** 0: No Invert (Default) 1: Invert

Address: C2 **POWER_ON_OFF_CTRL** **Default: 20h**

Bit	Mode	Function
7	R/W	**DE-only: Generate VS/HS from DE signal** 0: Disable (Default) 1: Enable
6	R/W	**B/R channel swap** 0: No swap (Default) 1: Swap
5	R/W	**Input Channel control by auto function** 0: Manual 1: Auto (Default)
4	R/W	**Enable Clock channel: turn on clock channel PLL (For manual use)** 0: Disable (Default) 1: Enable
3	R/W	**Enable Red input port (For manual use, cut off 50ohm internal resistor)** 0: Disable (Default) 1: Enable
2	R/W	**Enable Green input port (For manual use, cut off 50ohm internal resistor)** 0: Disable (Default) 1: Enable
1	R/W	**Enable Blue input port (For manual use, cut off 50ohm internal resistor)** 0: Disable (Default) 1: Enable
0	R/W	**CRC check** 0: Stop 1: Start CRC check during the next full frame and clear after finish (CRC value in reg. 0xC0)

Address: C3 **ANALOG_COMMON_CTRL0** **Default: 03h**

Bit	Mode	Function

7:4	R	**RESL<3:0> Z0 value** 0000: max. 1111: min. Read back Z0 value when calibration is finished.
3:0	--	**Reserved**

Address: C4 **ANALOG_COMMON_CTRL1** **Default: 00h**

Bit	Mode	Function
7:6	R/W	ENVBNL[1:0] 00: normal(default) 01: +0.06V 10: +0.1V 11: +0.14V
5	R/W	**ENTSTL**: enable internal test signal list below 0: off 1: on
4:0	--	**Reserved**

Address: C5 **ANALOG_BIAS_CTRL** **Default: 31h**

Bit	Mode	Function
7	R/W	**Auto equalizer setting by HW** 0: disable 1: enable (It will effect CRC6 [6:4] automatically)
6:3	R/W	**SBIASL<3:0>** (Default: 0110)
2:0	R/W	**SBIASGENL<2:0>**: bias generator (Default: 001)

Address: C6 **ANALOG_COMMON_CTRL2** **Default: 2xh**

Bit	Mode	Function
7	R/W	**SIBINL**: select bias source 0: auto generate (Default) 1: bias source is set to IB2IN.
6:5	R/W	**PAGINL<1:0>**: preamp gain selection of R/G/B port (Default=01) (CRC5 [7] indicates this register will be effected by HW or FW) 00: max. 11: min.
4	R/W	**Analog Equalizer Enable(ENEQL)** 0: Disable (Default) 1: Enable
3	R	**TMDS internal CTL3 signal status**
2	R	**TMDS internal CTL2 signal status**

1	R	**TMDS internal CTL1 signal status**
0	R	**TMDS internal CTL0 signal status**

Address: C7 **Z0_CALIBRATION_CTRL2** **Default: A3h**

Bit	Mode	Function
7	R/W	**STUNEL**: select calibration 0: Z0 is set by ADJRL<3:0> (Manual) 1: Z0 is auto calibrated (Default)
6	R/W	**Z0POWL**: (control of clock channel internal 50ohm resistor) 50 ohm impedance match calibration starts after power is stable, then status changes from 0→1 0: off 1: on
5:2	R/W	**ADJRL<3:0>**: select Z0 impedance value (default 1000)
1:0	R/W	**SREXTL<1:0>**: select REXT value (select corresponding REXT value on the PCB to SREXTL) 00:4k 01:2k 10:4k/3 11:1k

Address: C8 **CLOCK_PLL_SETTING** **Default: 32h**

Bit	Mode	Function
7	---	**Reserved to 0**
6:5	R/W	**SCKLVCSETL<1:0>**: when reset CLK PLL, the reset value of VC node 00: 2.17V 01: 1.98V (Default) 10: 1.79V 11: 1.60V
4:2	R/W	**SCKIL<2:0>**: PLL charge-pump current (Default= 3'b100) 10u + <4>*20u + <3>*10u + <2>*10u
1:0	R/W	**SCKRL<1:0>**: PLL LPF resistor 8k + <1>*4k + <0>*2k

Address: C9 **RGB_PLL_SETTING** **Default: 28h**

Bit	Mode	Function
7	---	**Reserved to 0**
6:5	R/W	**SSAVCSETL<1:0>**: when reset R/G/B PLL, the reset value of VC node 00: 2.17 01: 1.98 (Default) 10: 1.79 11: 1.60

4:2	R/W	**SSAIL<2:0>**: PLL charge-pump current (Default:3'b010) 5u+[4]*20u+[3]*10u+[2]*5u,
1:0	R/W	**SSARL<1:0>**: PLL LPF resistor (Default: 2'b00) 8k+<1>*4k+<0>*2k

Address: CA **WATCH_DOG_CTRL** **Default: 40h**

Bit	Mode	Function
7	---	**Reserved to 0**
6	R/W	**FIFO R/W Auto Calibration** 0: Manual 1: Auto (Default)
5	R/W	**R Channel Manual Mode** 0: Not Invert (Default) 1: Invert
4	R/W	**G Channel Manual Mode** 0: Not Invert (Default) 1: Invert
3:2	R/W	**CKWDCONL<1:0>**: PLL watch dog mode, when CKL<0.7Mhz, reset PLL (Clock) 00: Enable (Default) 01: Keep PLL VCO=SCKVCSETL<1:0> (break PLL loop) 1x: Disable watch dog
1:0	R/W	**SAWDCONL<1:0>**: PLL watch dog mode, when CKL<0.7Mhz, reset PLL (Sampling Data) 00: Enable (Default) 01: Keep PLL VCO=SSAVCSETL<1:0> (break PLL loop) 1x: Disable watch dog

Address: CB **CDR_CTRL0** **Default: 00x0_0010b**

Bit	Mode	Function
7:6	**R/W**	**UDCNT_SEL<1:0>** Indicate which channel to be R/W in CRCC[5], CRCF (Only when manual mode (CRCF[7]=0)) 1x:Red 01:Green 00:Blue
5	**R**	**OV_FLAG: When UDCNT fall in undefined phase number (#80~127)**
4	**R/W**	**OV_FLAG_CLN: To clean OV_FLAG**
3:2	**R/W**	**ADJ_GAIN<1:0> Phase adjust gain.** One UP/DOWN could mean to change the phase by 1~4 minimum step sizes.

1:0	**R/W**	**LPF<1:0>** LPF selection 00: ACCUMULATION type x1: CONSECUTIVE type, 10: CASCADE type. (Consecutive →Accumulation) (Default)

Address: CC **CDR_CTRL1** **Default: 0Ah**

Bit	Mode	Function
7:0		**THR_DCC<7:0>:** Threshold to assert UP/DOWN in accumulation LPF

Address: CD **CDR_CTRL2** **Default: 0Ah**

Bit	Mode	Function
7:0	R/W	**THR_CONSEC<7:0>:** Threshold to assert UP/DOWN in consecutive LPF

CRCC and CRCD values can't be zero.

Address: CE **UP_DOWN_ADJUSTING0** **Default: 80h**

Bit	Mode	Function
7	R/W	**UD_AUTO**: 1: Auto; 0:Manual
6:0	R/W	**UDCNT_FW<6:0>** Specify which phase number (#0~79) sent to analog.

Address: CF **UP_DOWN_ADJUSTING1** **Default: 14h**

Bit	Mode	Function
7:0	R/W	**WAIT_TIME<7:0>:** The minimum period between two phases adjusts. (phase change responding time)

Address: D0 **Adaptive Equalizer** **Default: 00h**

Bit	Mode	Function
7	R/W	**Adaptive Equalizer Enable** 0: disable 1: enable
6	R/W	**Reserved to 0**
5:4	R	**Adaptive Equalizer up/down by HW (cleared by writing CRC6)** 00: the same 01: down 1x: up
3	R/W	**Adaptive Equalizer auto stop enable** 0: disable 1: enable
2	R	**Adaptive Equalizer auto stop** 0: not stop 1: stop
1:0	R/W	**HDCP MP Test**

Address: D1 **UP_DOWN_CTRL0** **Default: 92h**

Bit	Mode	Function
7	R/W	**ADJ_AUTO_R**: Phase adjusting automatically by digital or not, for RED channel. 1: automatic (Default) 0: manual by firmware
6:5	R/W	**UPDOWN_R<1:0>:** Manually adjust of up/down for PLL, in RED channel. This is only useful when ADJ_AUTO_R is set to 0. 10: UP 01: DOWN 00: hold (Default)
4	R/W	**ADJ_AUTO_G** : Phase adjusting automatically by digital or not, for GREEN channel. 1: automatic (Default) 0: manual by firmware
3:2	R/W	**UPDOWN_G<1:0>:** Manually adjust of up/down for PLL, in GREEN channel. This is only useful when ADJ_AUTO_G is set to 0. 10: UP 01: DOWN 00: hold (Default)
1	R/W	**ADJ_AUTO_B** :Phase adjusting automatically by digital or not, for BLUE channel. 1: automatic (Default) 0: manual by firmware
0	R/W	**UP side DOWN** 0: Disable 1: Enable

Address: D2 **UP_DOWN_CTRL1** **Default: 0001_xxxxb**

Bit	Mode	Function
7:6	R/W	**UPDOWN_B<1:0>:** Manually adjust of up/down for PLL, in BLUE channel. This is only useful when ADJ_AUTO_B is set to 0. 10: UP 01: DOWN 00: hold
5	R/W	**Reserved to 0**
4	R/W	**NL_AUTO** : Frequency range selection by digital part automatically. 1: automatic by digital (Default) 0: manual selected by firmware

3:0	R	**NL<3:0>:** Frequency selected by digital part. 0000: 0Hz 0001: >165MHz or <25MHz 1110: 25-50 MHz 1000: 50-80 MHz 0110: 80-112 MHz 0100: 112-140 MHz 0011: 140-165 MHz otherwise: invalid

Address: D3 **UP_DOWN_CTRL2** **Default: 30h**

Bit	Mode	Function
7	R/W	**CPTEST** 0: normal mode, in which clock and data from analog are used. 1: select TSTCKIN/TSTDIN as input 2X5 clock and data respectively, for TESTING.
6:4	R/W	**STABLE_CNT<2:0>:** Numbers of consecutive frequency change command after which N_FREQ can be adjusted.
3:0	R/W	**NL_FW<3:0>:** Frequency selected by firmware. The valid values are the same as those listed in previous row. (Read back value in CRD3)

Address: D4 **UP_DOWN_CRTL3** **Default: 00h**

Bit	Mode	Function
7:6	R/W	**ERRC_SEL<1:0>** 00: original signal 01: debouncing 1 cycle 10: debouncing 1+8 cycle 11: 1+8 cycle debouncing + DE masking transition of vs/hs+vs+(hs88) to masking DE
5:0	R/W	**DEBUG_SEL**

Address: D5 **Device Key Access Port**

Bit	Mode	Function
7:0	R/W	When enable device key accessing 40x56 table, the 56-bit key table will be transferred to 64-bit pseudo data with 7^{th}, 15^{th}, 23rd, 31st, 39^{th}, 47^{th}, 55^{th} bits inserted. The inserted data are '0'.And the write sequence is: {D0-Byte0, D0-Byte1, D0-Byte2, D0-Byte3,D0-Byte4, D0-Byte5, D0-Byte6, D0-Byte7}, {D1-Byte0, D1-Byte1, 1-Byte2,D1-Byte3, D1-Byte4, D1-Byte5, D1-Byte6, D1-Byte7}, …………………………………………… *Accessing this port must be coded/decoded by REALTEK protection code.*

Address: D6 **HDCP CTRL** **default : 0000_0000b**

Bit	Mode	Function
7	R/W	**HDCP Key Access SRAM BIST Action** 0: stop & clear after finish. 1: start
6	R	**HDCP Key Access SRAM BIST Status** 0: Fail 1: OK, when test start, clear this bit
5	R	**Indicate VSYNC Polarity** 0: Positive, which means VS pulse is high. 1: Negative
4	R/W	**Invert VSYNC for HDCP** 0: Not Inverted 1: Inverted
3	R/W	**Indicate VSYNC Polarity Mode:** 0: auto, indicate by 0x70[5] 1: manual, decided by 0x70[4]
2	R/W	**MCU Access DDC data first** 0: enable DDC channel and MCU access only when DDC is not busy 1: disable DDC channel and MCU access only
1	R/W	**Device Key Access Port download enable** 0: disable, this would reset the address of Device Key Access Port to 0. 1: enable
0	R/W	**HDCP Enable** 0: Disable HDCP, except for output. 1: Auto Enable HDCP function, when Tx I2C write Aksv

Address: D7 **HDCP_ADDR_PORT** **default: 00h**

Bit	Mode	Function
7:0	R/W	Address port for embedded HDCP access, auto increase after DATA_PORT being accessed. (For Host Side controlled by D7)

Address: D8 **HDCP_DATA_PORT**

Bit	Mode	Function
7:0	R/W	Data port for embedded HDCP access

Address: D8-C0 **HDCP frame counter** **default: 0**

Bit	Mode	Function
7	R	**Read as 0**

6:0	R	**HDCP_frame counter**[6:0]

Address: D8-C1 ***Reserved***

Bit	Mode	Function
7:0	R	Reserved

Address: D8-C2 **HDCP system. Info** **default: 00000000b**

Bit	Mode	Function
7	---	**Reserved**
6	R	**Authst (Means bksv of RTD pass Tx authorization, Tx is ready to do HDCP transaction)**
5	R	**Authkm (Means RTD finish computing KM, ri) //Hidden**
4	R	**Authdone (means TX admitted ri value, start to do HDCP transmission)**
3:2	--	**Reserved**
1	R	**NO CTRL3, HDCP 1.0 fail flag**
0	R	**Internal buffer for Ainfo[1].** Since Ainfo[1] in DDC port is 0 at most of time, we need to know what Tx wrote.

Address: D8-C3 **HDCP flow control** **default: 0000_0000b**

Bit	Mode	Function
7:4	R/W	Reserved to 0
3	R/W	ENC_EN / ENC_DIS Error Correction for EESS mode 0: ENC_EN: CTL3~CTL0=1001; ENC_DIS: CTL3~CTL0=0001 1: ENC_DIS = ~ ENC_EN
2	R	ENC_EN status
1	R	ENC_DIS status
0	R	ENC_EN | ENC_DIS

Address: D9 Reserved

Watch Dog

Address: DA **WATCH_DOG_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	**Auto Switch When Input HSYNC/VSYNC Error** 0: Disable (Default) 1: Enable (See CR02[6] and CR02[5])
6	R/W	**Auto Switch When Input HSYNC/VSYNC Timeout or Overflow** 0: Disable (Default) 1: Enable (See CR52[4] and CR54[5:4])
5	R/W	**Auto switch when Display Vsync timeout**

		0: Disable (Default) 1: Enable
4	R/W	**Auto switch when ADC-PLL non-lock** 0: Disable (Default) 1: Enable
3	R/W	**Auto switch when overflow or underflow** 0: Disable (Default) 1: Enable
2	R/W	**Auto switch event happen action (for timing)** 0: Disable (Default) 1: Free Run
1	R/W	**Auto switch event happen action (for data)** 0: Disable (Default) 1: Background **Turn off overlay enable and switch to background simultaneously.**
0	R	**Display Vsync timeout flag (status with CRDA [5])** 0: Vsync is present 1: Vsync Timeout The line number of Display HS is equal to Display Vertical Total; this bit is set to “1”. Write to clear status.

Embedded ADC

Address: DC **ADC access port** **Default: 00h**

Bit	Mode	Function
7	R/W	Enable ADC access port
6:5	R/W	Reserved to 0
4:0	R/W	ADC port address

Address: DD **ADC Data Port**

Bit	Mode	Function
7:0	R/W	ADC data port

Address: DD-00 **ADC_ RGB_CTRL** **Default: 5Eh**

Bit	Mode	Function
7:6	R/W	PGA (00: Ash=0.9 01: Ash=1.0 10: Ash=1.1 11: Ash=1.2) (Default: 01)
5:4	R/W	PGA (00: Aref=0.9 01: Aref=1.0 10: Aref=1.1 11: Aref=1.2)(Default: 01)
3	R/W	**ADC source select (Need to select corresponding ADC_OUT_SOG 0 or 1)** 0 : Input0 1 : Input1(Default)
2	R/W	**ADC input mode selection** 0 : Single Ended 1 : Differential (Default)
1:0	R/W	**Bandwidth Adjustment** 00 : 75M 01 : 150M 10 : 300M (Default) 11 : 500M

Address: DD-01 **ADC_ RED_CTRL** **Default: 40h**

Bit	Mode	Function
7	R/W	**RED channel clamp mode selection** 0: Low clamp (Default) 1: Middle clamp
6:4	R/W	**RED channel Clamp Voltage** 0~700mV, Step=100mV (Default: 100)
3	R/W	**RED channel Offset Depends on Gain** 0: RGB Dependent, YPbPr Independent (Default) 1: RGB Independent, YPbPr Independent
2:0	R/W	**Red Channel ADC Fine Tune Delay** (Step=90ps) (Default: 000)

Address: DD-02 **ADC_GRN_CTRL** **Default: 20h**

Bit	Mode	Function
7	R/W	**GREEN channel clamp mode selection** 0: Low clamp (Default) 1: Middle clamp
6:4	R/W	**GREEN channel Clamp Voltage** 0~700mV, Step=100mV(Default:010)
3	R/W	**GREEN channel Offset Depends on Gain** 0: RGB Dependent, YPbPr Independent(Default) 1: RGB Independent, YPbPr Independent
2:0	R/W	**Green Channel ADC Fine Tune Delay** (Step=90ps) (Default:000)

Address: DD-03 **ADC_BLU_CTRL** **Default: 40h**

Bit	Mode	Function
7	R/W	**BLUE channel clamp mode selection** 0: Low clamp(Default) 1: Middle clamp
6:4	R/W	**BLUE channel Clamp Voltage** 0~700mV, Step=100mV (Default:100)

3	R/W	**BLUE channel Offset Depends on Gain** 0: RGB Dependent, YPbPr Independent(Default) 1: RGB Independent, YPbPr Independent
2:0	R/W	**Blue Channel ADC Fine Tune Delay** (Step=90ps) (Default: 000)

Address: DD-04 **RED_GAIN** **Default: 80h**

Bit	Mode	Function
7:0	R/W	**Red Channel Gain Adjust**

Address: DD-05 **GRN_GAIN** **Default: 80h**

Bit	Mode	Function
7:0	R/W	**Green Channel Gain Adjust**

Address: DD-06 **BLU_GAIN** **Default: 80h**

Bit	Mode	Function
7:0	R/W	**BLUE Channel Gain Adjust**

Address: DD-07 **RED_OFFSET** **Default: 80h**

Bit	Mode	Function
7:0	R/W	**Red Channel Offset Adjust**

Address: DD-08 **GRN_OFFSET** **Default: 80h**

Bit	Mode	Function
7:0	R/W	**Green Channel Offset Adjust**

Address: DD-09 **BLU_OFFSET** **Default: 80h**

Bit	Mode	Function
7:0	R/W	**BLUE Channel Offset Adjust**

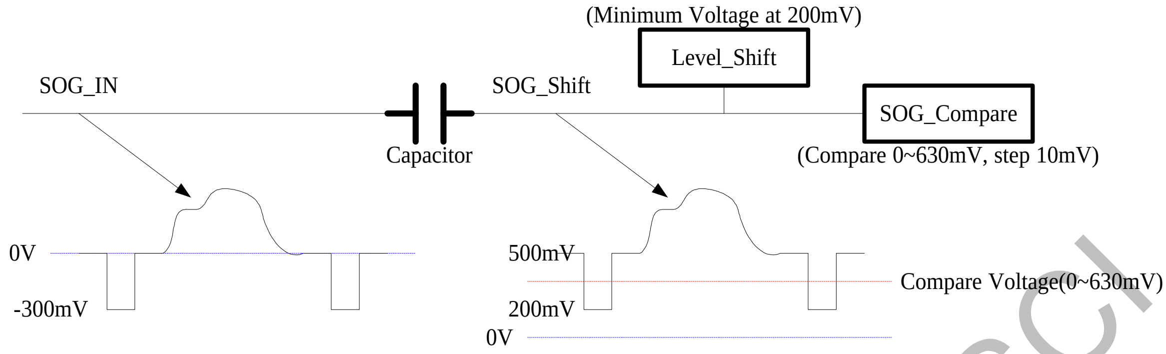
Address: DD-0A **SOG_CTRL0** **Default: 20h**

Bit	Mode	Function
7	R/W	**R Channel Clamp to Top** 0: Normal 1: Top
6	R/W	**G Channel Clamp to Top** 0: Normal 1: Top
5:0	R/W	**SOG0 Reference Control** 0~630mV, Step=10mV (Default: 100000)

Address: DD-0B **SOG_CTRL1** **Default: 20h**

Bit	Mode	Function
7	R/W	**B Channel Clamp to Top** 0: Normal 1: Top
6	R/W	**R, B Clamp Value from G** 0: No 1: Yes
5:0	R/W	**SOG1 Reference Control** 0~630mV, Step=10mV (Default: 100000)

- The lowest voltage of SOG_IN is clamped to about 200mV.
- SOG reference control set the threshold voltage to extract the sync signal from G. The threshold voltage maps the value 0~63 to 0~630 mV.



Address: DD-0C ADC_POWER_CTRL **Default: 08h**

Bit	Mode	Function
7	R/W	**SOG Mode** 0: NMOS/R 1: Clamping
6	R/W	**SOG Channel Clamp to –300mV** 0: 500mV 1: 200mV
5	R/W	**SOG0 Power On** 0 : Power Down(Default) 1 : Power On
4	R/W	**SOG1 Power On** 0 : Power Down(Default) 1 : Power On
3	R/W	**Band-gap Power On** 0 : Power Down 1 : Power On (Default)
2	R/W	**Red Channel ADC Power On** 0 : Power Down (Default) 1 : Power On
1	R/W	**Green Channel ADC Power On** 0 : Power Down (Default) 1 : Power On
0	R/W	**Blue Channel ADC Power On** 0 : Power Down (Default) 1 : Power On

- Note that Band-gap power can only turn off just in the power down mode, or the chip may run abnormally.
- When in power saving mode, only R/G/B channel will be power down, it doesn't include the SOG & band-gap.

Address: DD-0D ADC_CLOCK **Default: 01h**

Bit	Mode	Function
7	R/W	**Input Clock Polarity** 0: Negative (Default) 1: Positive
6	R/W	**Output Clock Polarity** 0: Normal (Default) 1: Inverted
5:4	R/W	**ADC_Out Pixel Extra Delay** 00: 1.05ns (Default) 01: 1.39ns 10: 1.69ns 11: 1.97ns

3	R/W	**1x or 2x from APLL (For better clock duty cycle)** 0: 1X (Default) 1: 2X
2	R/W	**Single Ended or Differential clock from APLL** 0: Differential (Default) 1: Single Ended
1:0	R/W	**Duty Stabilizer** (Default: 01)

Address: DD-0E **ADC_TEST** **Default: 04h**

Bit	Mode	Function
7	R/W	**Clock input** 0: from APLL/3.3V (Default) 1: from TTL/1.8V
6:4	R/W	**Test Output Selection (PAD : G+)** 000: X(Hi-Z) Normal SOG Mode (Default) 001: GND 010: VREFN 011: VCMO 100: VREFP 101: GND 110: GND 111:VDD
3:2	R/W	**SOG Resistor** 00: open 01: Poly R=500K, external C=10nf (Default) 10: MOS R=1M, external C=4.7nF 11: MOS R=5M, external C=1nF
1:0	R/W	**Clock Output Divider** 00 : 1/1 (Default) 01 : 1/2 10 : 1/3 11 : 1/4

Address: DD-0F **ADC_IBIAS2** **Default: 53h**

Bit	Mode	Function
7:6	R/W	**HSYNC_CURRENT[1:0] (default=2b'01)** Bias Current of HSYNC_IB60U 00:48u 01:60u 10:72u 11:84u
5:4	R/W	**ADC_SF[1:0]** Bias Current of ADC_SF 00:15u 01:20u (Default) 10:25u 11:30u
3	R/W	**ADC_REF**

		Bias Current of ADC_REF 0:60u (Default) 1:80u
2:0	R/W	**ADC_OP[2:0]** Bias Current of ADC_OP 000:5u 001:10u 010:15u 011:20u 100:25u 101:30u 110:35u 111:40u

Address: DD-10 **ADC_VBIAS0** **Default: 21h**

Bit	Mode	Function
7	R/W	**Resistor Reference** (REFIO) 0:Ref. To Internal R (Default) 1:Ref. To External R=2K
6:4	R/W	**ADC_VBIAS0[6:4]** Band gap Voltage 000:0.890 001:0.841 010:0.792 (Default) 011:0.742 100:0.693 101:0.644 110:0.594 111:0.545
3:2	R	**Temperature sensor 0~120 (70+38*1.2)** 00: 30 degree 01: 30-60 degree 10: 60-90 degree 11: 120 degree
1:0	R/W	**ADC_VBIAS0[1:0]** Band gap Voltage 00:0.775 01:0.792 (Default) 10:0.810 11:0.829

Address: DD-11 **ADC_VBIAS1** **Default: 0Dh**

Bit	Mode	Function
7	R/W	**ADC Gain Calibration** 0: Normal 1: Calibration
6	R/W	**R Channel Clamp to -300mV** 0: 0mV (Default) 1: -300mV
5	R/W	**G Channel Clamp to -300mV** 0: 0mV (Default) 1: -300mV
4	R/W	**B Channel Clamp to -300mV** 0: 0mV (Default) 1: -300mV
3	R/W	**RGB Input Range Adjust** 0: 0.3V-1.2V 1: 0.5V-1.0V
2	R/W	**Vcmo from VBG or from VDD //(1)**

		0:from VBG (constant) 1:from VDD (Default)
1:0	R/W	**Vcmo Voltage[1:0] //(01)** 00:0.90 01:1.00 (Default) 11:1.05 11:1.10

Address: DD-12 **PTNPOS_H** **Default: 00h**

Bit	Mode	Function
7	**R/W**	**Enable Test** 0: Finish (and result sequence is R-G-B) (Default) 1: Start
6:4	**R/W**	**Test Pattern V Position Register [10:8]** Assign the test pattern digitized position in line after V_Start.
3	--	**Reserved to 0**
2:0	**R/W**	**Test Pattern H Position Register [10:8]** Assign the test pattern digitized position in pixel after H_Start.

Address: DD-13 **PTNPOS_V_L**

Bit	Mode	Function
7:0	R/W	**Test Pattern V Position Register [7:0]** Assign the test pattern digitized position in line after V_Start..

Address: DD-14 **PTNPOS_H_L**

Bit	Mode	Function
7:0	R/W	**Test Pattern H Position Register [7:0]** Assign the test pattern digitized position in line after H_Start..

Use PTNPOS to assign the pixel position after HSYNC leading edge that input signal digitized. Each time the PTNPOS is written, the digitized results will be loaded into PTNRD, PTNGD and PTNBD. For test issue, make the input signal a fixed pattern before PTNPOS is written. Then the same digitized output will be got.

Address: DD-15 **PTNRD**

Bit	Mode	Function
7:0	R	**Test Pattern Red-Channel Digitized Result.**

Address: DD-16 **PTNRD**

Bit	Mode	Function
7:0	R	**Test Pattern Green-Channel Digitized Result.**

Address: DD-17 **PTNRD**

Bit	Mode	Function
7:0	R	**Test Pattern Blue-Channel Digitized Result.**

- The test pattern digitized result after HSYNC leading edge about PTNPOS pixel.

Auto Black Level (ABL)

Address: DD-18 **AUTO_BLACK_LEVEL_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**ABL Mode** 0: RBG (Default) 1: YPbPr
6	R/W	**On-line/Off-line ABL Mode** 0: Off-line (Default) 1: On-line
5:4	R/W	**Width of ABL region in each line** 00: 16 pixels (Default) 01: 32 pixels 10: 64 pixels 11: 4 pixels
3	R	**R/Pr Channel ABL Result (write clear)** 0: not equal 1: equal (Black Level = Target Value) On-line mode: |Black Level - Target Value| <=LOCK_MGN Off-line mode: |Black Level - Target Value| <= EQ_MGN
2	R	**G/Y Channel ABL Result (write clear)** 0: not equal 1: equal (Black Level = Target Value) On-line mode: |Black Level - Target Value| <= LOCK _MGN Off-line mode: |Black Level - Target Value| <= EQ_MGN
1	R	**B/Pb Channel ABL Result (write clear)** 0: not equal 1: equal (Black Level = Target Value) On-line mode: |Black Level - Target Value| <= LOCK _MGN Off-line mode: |Black Level - Target Value| <= EQ_MGN
0	R/W	**Auto Black Level Enable (write 0 force stop)** 0: Finished/Disable (Default) 1: Enable to start ABL, auto cleared after finished Cleared to 0 when off-line mode completes.

- Parameters can only be changed when EN_ABL is 0
- The on-line mode never stops unless EN_ABL is 0.
- Off-line mode completes when MAX_FRAME is measured or the result is equal.
- ABL Enable must be disable before switching On-line/Off-line mode and enable again.

Address: DD-19 **AUTO_BLACK_LEVEL_CTRL2** **Default: 84h**

Bit	Mode	Function
7:6	R/W	**Line averaged for each ABL adjustment** 00: 8 01: 16 10: 32 (Default) 11: 64
5	--	**Reserved**
4:0	R/W	**Start Vertical Position of ABL in each line** Determine the start line of auto-black-level after the leading edge of Vsync

Address: DD-1A **AUTO_BLACK_LEVEL_CTRL3** **Default: 10h**

Bit	Mode	Function
7:4	R/W	**Y/R/G/B Target value** 0000: 1 0001: 2 (Default) 0010: 3 0011: 4 …. 1111:16 (Pb/Pr Target level is fixed 128)
3:2	R/W	**Lock Margin** 00: 1 (Default) 01: 2 10: 4 11: 6
1:0	R/W	**End Vertical Position of ABL measurement region [9:8]** Determine the last line of auto-black-level measurement for every frame/field which is counted by double-line..

- Off-line mode rule:

  Measures once for each field/ frame and the offset is the delta.

- On-line mode rule:

  If (delta <= EQ_MGN) offset = 0

  Else if (delta < L_MGN) offset = +/-1

  Else offset = +/-L_MGN

- ADC offset is updated immediately.

Address: DD-1B **AUTO_BLACK_LEVEL_CTRL4** **Default: 82h**

Bit	Mode	Function
7:0	R/W	**End Vertical Position of ABL measurement region [7:0]** Determine the last line of auto-black-level measurement for every frame/ field, which is counted by double-line.

- Note: ABL will be failed if End Vertical Position < Start Vertical Position + Average Line(CRDD19[7:6]).

Address: DD-1C **AUTO_BLACK_LEVEL_CTRL5** **Default: 04h**

Bit	Mode	Function
7:0	R/W	**Start Position of ABL in each line** Determine the start position of auto-black-level after the trailing edge of reference signal. (When ABL mode in YPbPr, the reference signal is input Hsync. In RGB mode, the reference signal is clamp signal.)

- In each region, hardware compare the average value in the target region (fixed 16 input pixels after start position of ABL) with target value and add +1/-1 or +L_MGN /- L_MGN to ADC offset. (+ for greater than target value, - for smaller than target value).

Address: DD-1D **AUTO_BLACK_LEVEL_CTRL6** **Default: C0h**

Bit	Mode	Function
7:6	R/W	**Large Error Margin (L_MGN) (For on-line Mode)** 00: 2 01: 4 10: 6 11: 8(Default)
5:4	R/W	**Max. Frame/Field Count (For off-line mode)** 00: 4 (Default) 01: 5 10: 6 11: 7
3	--	**Reserved**
2:0	R/W	**Lines delayed between each measurement region (For on-line Mode)** 000: 16 (Default) 001: 32 010: 64 011: 128

		100: 192 101: 256 110: 384 111: 640

Address:DD-1E **AUTO_BLACK_LEVEL_CTRL7** **Default: 60h**

Bit	Mode	Function
7	--	**Reserved**
6	R/W	**Equal Condition (Off-line mode)** 0: To trigger status until measurement achieve Max Frame/Field Count. 1: To trigger status once if |Black Level - Target Value| <= EQ_MGN. (Default) (If set 0, the ABL Result will not go low even noise comes for the next frames.)
5	R/W	**Measure Pixels Method** 0: Average value 1: Minimum value (Default)
4	R/W	**Measure Error Flag Reset** 0: Normal 1: Reset
3	R	**Measure Error Flag** 0: Normal 1: Error (This flag is occurred when Hsync trailing edge is met during measurement.)
2	R/W	**Hsync Start Reference Select** 0: HS leading edge (Default) 1: HS trailing edge
1:0	R/W	**Equal margin (EQ_MGN)** 00: 0 (Default) 01: 1 10: 2 11: 3

Address: DD-1F **AUTO_BLACK_LEVEL__RED_VALUE**

Bit	Mode	Function
7:0	R	**Minimum/Average value of R Channel in Test Mode**

Address:DD-20 AUTO_BLACK_LEVEL_NOISE_VALUE_OF_RED_CHANNEL

Bit	Mode	Function
7:0	R	**Noise Value of Red Channel in Test Mode after Equal status is triggered.**

Address: DD-21 AUTO_BLACK_LEVEL__Green_VALUE

Bit	Mode	Function
7:0	R	**Minimum/Average value of G Channel in Test Mode**

Address:DD-22 AUTO_BLACK_LEVEL_NOISE_VALUE_OF_GREEN_CHANNEL

Bit	Mode	Function
7:0	R	**Noise Value of Green Channel in Test Mode after Equal status is triggered.**

Address: DD-23 AUTO_BLACK_LEVEL__Blue_VALUE

Bit	Mode	Function
7:0	R	**Minimum/Average value of B Channel in Test Mode**

Address:DD-24 AUTO_BLACK_LEVEL_NOISE_VALUE_OF_BLUE_CHANNEL

Bit	Mode	Function
7:0	R	**Noise Value of Blue Channel in Test Mode after Equal status is triggered.**

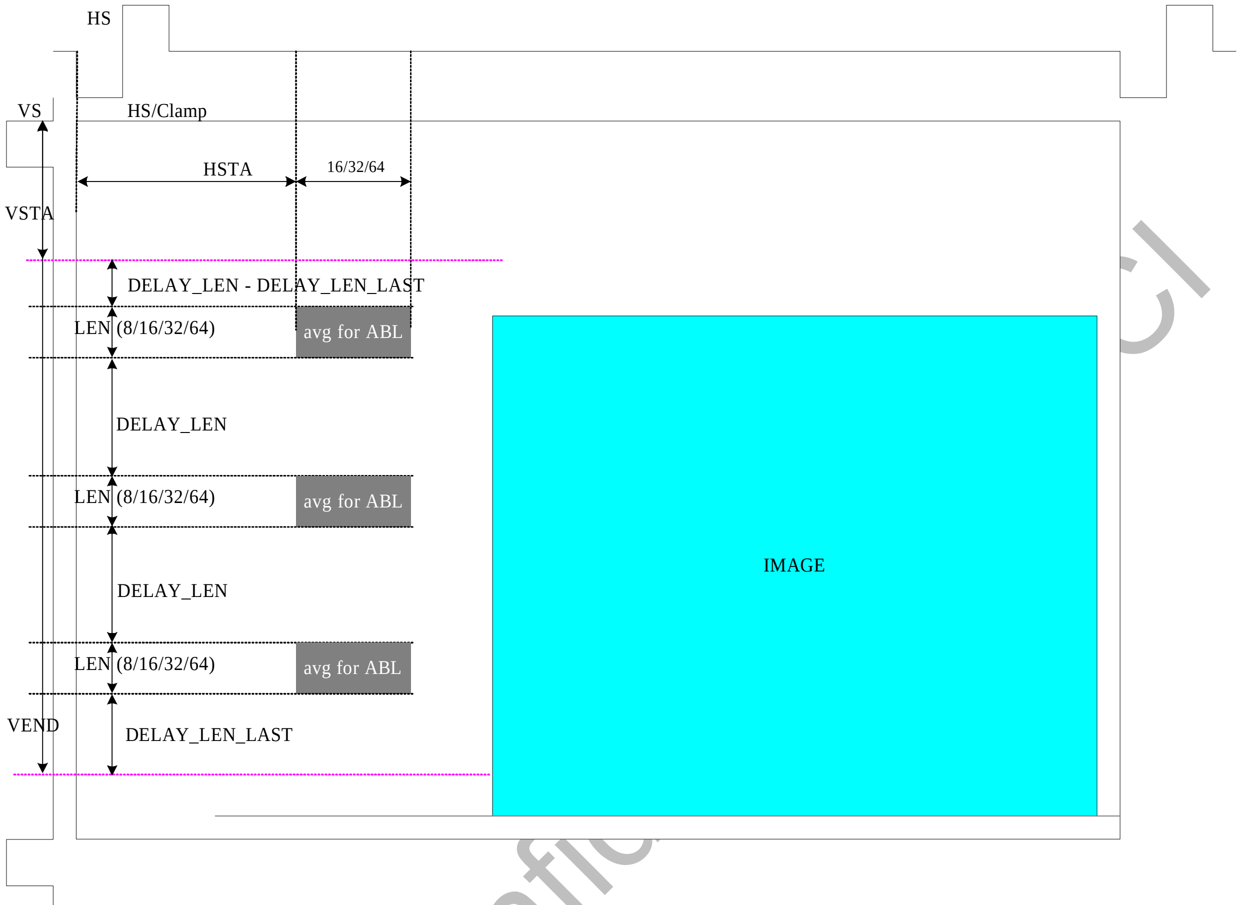


Figure 3 Auto Black Level active region – case 1

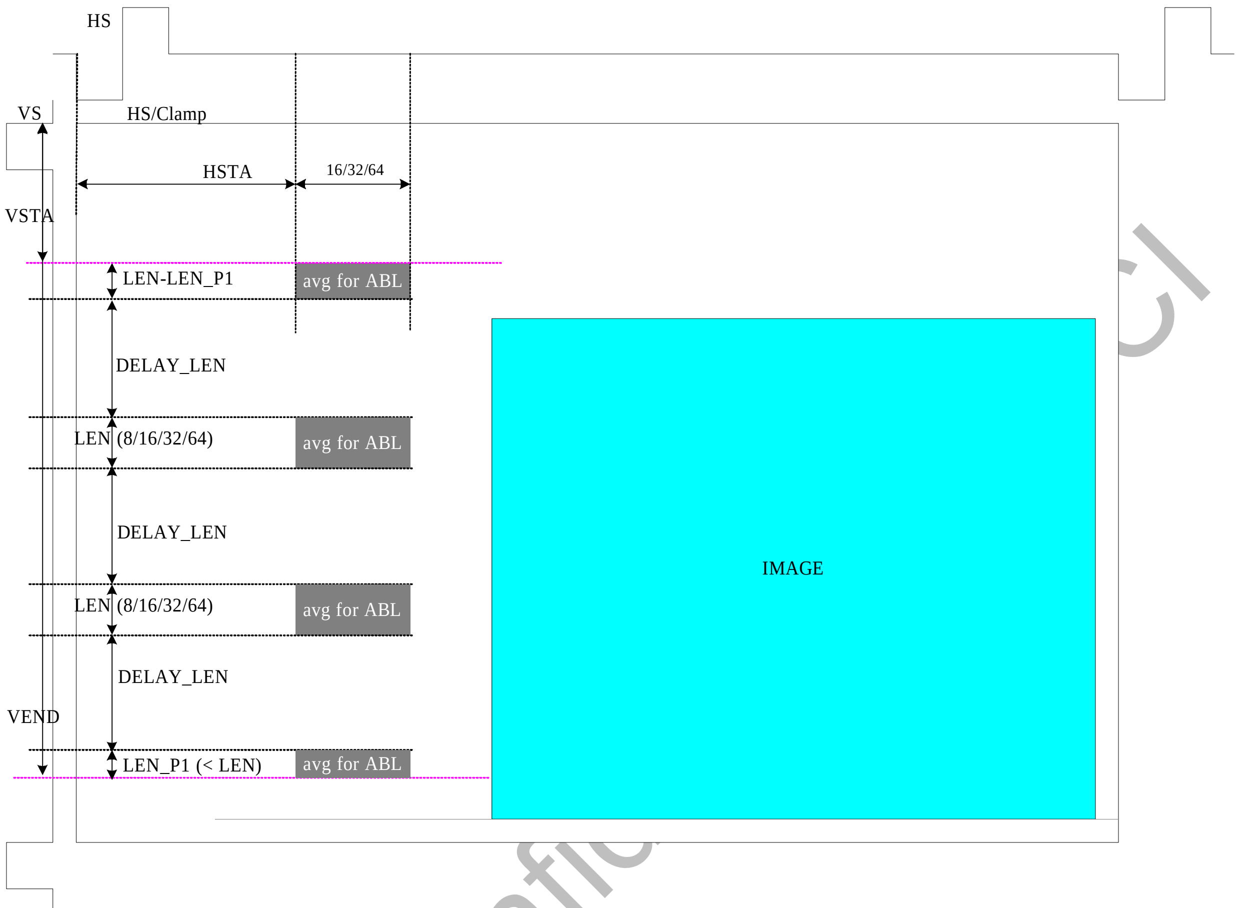


Figure 4 Auto Black Level active region – case 2

ICM (Independent Color Management)

Address: E0 **ICM Control** **Default: 00h**

Bit	Mode	Function
7	R/W	**ICM Enable** 0: Disable 1: Enable
6	R/W	**Y Correction Mode** 0: dY = (8dU+dV)/8 1: dY = (6dU+dV)/8
5	R/W	**ICM U/V Delta Range:** 0: Original -128~+127 1: Double -256~254
4	R/W	**CM0 Enable** 0: Disable 1: Enable
3	R/W	**CM1 Enable** 0: Disable 1: Enable
2	R/W	**CM2 Enable** 0: Disable 1: Enable

Bit	Mode	Function
1	R/W	**CM3 Enable** 0: Disable 1: Enable
0	R/W	**CM4 Enable** 0: Disable 1: Enable

Address:E1 **ICM_SEL** **Default: 00h**

Bit	Mode	Function
7:5	R/W	**ICM Test Mode** 000: disable 001: bypass U, V result 010: bypass hue/saturation result 011: bypass dU, dV value 1xx: R,B as LUT input, and bypass LUT output to R/G/B output
4	--	**reserved**
3	R/W	**CM5 Enable** 0: Disbale 1: Enable
2:0	R/W	**CM Select** 000: Select Chroma Modifier 0 for Accessing Through Data Port 001: Select Chroma Modifier 1 for Accessing Through Data Port 010: Select Chroma Modifier 2 for Accessing Through Data Port 011: Select Chroma Modifier 3 for Accessing Through Data Port 100: Select Chroma Modifier 4 for Accessing Through Data Port 101: Select Chroma Modifier 5 for Accessing Through Data Port 110~111: reserved

Address:E2 **ICM_ADDR** **Default: 00h**

Bit	Mode	Function
7:0	R/W	**ICM port address**

Address:E3 **ICM_Data**

Bit	Mode	Function
7:0	R/W	**ICM port data**

ICM_ADDR will be increased automatically after each byte of ICM_DATA has been accessed.

Address: E3-00 **MST_HUE_HB** **Default: x0h**

Bit	Mode	Function
7:4	--	**Reserved**
3:0	W	**High Byte[11:8] of Master Hue for Chroma Modifier N.**

Address: E3-01 **MST_HUE_LB** **Default: 00h**

Bit	Mode	Function
7:0	W	**Low Byte[7:0] of Master Hue for Chroma Modifier N.**

Address: E3-02 **HUE_SET** **Default: 00h**

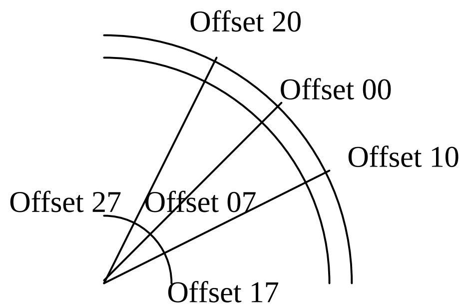
Bit	Mode	Function
7:6	W	**CM[N]_LWID** 00: CM[N] left width = 64 01: CM[N] left width = 128 10: CM[N] left width = 256 11: CM[N] left width = 512
5:4	W	**CM[N]_LBUF** 00: CM[N] left Buffer = 0 01: CM[N] left Buffer = 64 10: CM[N] left Buffer = 128 11: CM[N] left Buffer = 256
3:2	W	**CM[N]_RWID** 00: CM[N] right width = 64

		01: CM[N] right width = 128 10: CM[N] right width = 256 11: CM[N] right width = 512
1:0	**W**	**CM[N]_RBUF** 00: CM[N] right Buffer = 0 01: CM[N] right Buffer = 64 10: CM[N] right Buffer = 128 11: CM[N] right Buffer = 256

Address: E3-03~32 U/V Offset Default: 00h

Bit	Mode	Function
7:0	W	**Addr 03: U Offset 00, -128~127** **Addr 04: V Offset 00, -128~127** **Addr 05: U Offset 01, -128~127** **Addr 06: V Offset 01, -128~127** **Addr 07: U Offset 02, -128~127** **Addr 08: V Offset 02, -128~127** **Addr 09: U Offset 03, -128~127** **Addr 0A: V Offset 03, -128~127** **Addr 0B: U Offset 04, -128~127** **Addr 0C: V Offset 04, -128~127** **Addr 0D: U Offset 05, -128~127** **Addr 0E: V Offset 05, -128~127** **Addr 0F: U Offset 06, -128~127** **Addr 10: V Offset 06, -128~127** **Addr 11: U Offset 07, -128~127** **Addr 12: V Offset 07, -128~127** **Addr 13: U Offset 10, -128~127** **Addr 14: V Offset 10, -128~127** **Addr 15: U Offset 11, -128~127** **Addr 16: V Offset 11, -128~127** **Addr 17: U Offset 12, -128~127** **Addr 18: V Offset 12, -128~127** **Addr 19: U Offset 13, -128~127** **Addr 1A: V Offset 13, -128~127** **Addr 1B: U Offset 14, -128~127** **Addr 1C: V Offset 14, -128~127** **Addr 1D: U Offset 15, -128~127** **Addr 1E: V Offset 15, -128~127** **Addr 1F: U Offset 16, -128~127** **Addr 20: V Offset 16, -128~127** **Addr 21: U Offset 17, -128~127** **Addr 22: V Offset 17, -128~127** **Addr 23: U Offset 20, -128~127** **Addr 24: V Offset 20, -128~127** **Addr 25: U Offset 21, -128~127** **Addr 26: V Offset 21, -128~127** **Addr 27: U Offset 22, -128~127** **Addr 28: V Offset 22, -128~127** **Addr 29: U Offset 23, -128~127** **Addr 2A: V Offset 23, -128~127** **Addr 2B: U Offset 24, -128~127** **Addr 2C: V Offset 24, -128~127** **Addr 2D: U Offset 25, -128~127** **Addr 2E: V Offset 25, -128~127** **Addr 2F: U Offset 26, -128~127** **Addr 30: V Offset 26, -128~127**

		Addr 31: U Offset 27, -128~127 **Addr 32: V Offset 27, -128~127**



DCC (Dynamic Contrast Control)

Address: E4 **DCC_CTRL0** **Default: 00h**

Bit	Mode	Function
7	R/W	**DCC_ENABLE** 0: Disable 1: Enable
6	R/W	**Y_FORMULA** 0: Y = (2R+5G+B)/8 1: Y = (5R+8G+3B)/16
5	R/W	**SOFT_CLAMP** 0: Disable 1: Enable
4	R/W	**DCC_MODE** 0: Auto Mode 1: Manual Mode
3	R/W	**SCENE_CHANGE** 0: Disable Scene-Change Function 1: Enable Scene-Change Function in Auto Mode
2	R/W	**BWL_EXP** 0: Disable Black/White Level Expansion 1: Enable Black/White Level Expansion in Auto Mode
1:0	R/W	**DCC_PAGE_SEL** 00: Page 0 (for Histogram / Ymin-max / Soft-Clamping / Scene-Change) 01: Page 1 (for Y-Curve / WBL Expansion) 10: Page 2 (for Calculation Parameter) 11: Page 3 (for Testing and Debug)

Address: E5 **DCC_CTRL1** **Default: 00h**

Bit	Mode	Function
7	R/W	**DCC gain control enable** 0: Disable 1: Enable Note: DCC gain control enable must delay MOV_AVG_LEN frame after DCC enable.
6	R	1: time to write highlight window position & normalized factor, write to clear
5	R/W	**Saturation Compensation Enable**

		0: Disable 1: Enable
4	R/W	**Blending Factor Control Mode** 0: old mode 1: new mode (diff. regions have diff. blending factor)
3:0	--	**Reserved 0**

Address: E6 DCC Address Port

Bit	Mode	Function
7:0	R/W	**DCC Address**

Address: E7 DCC Data Port

Bit	Mode	Function
7:0	R/W	**DCC Data**

DCC_ADDR will be increased automatically after each byte of DCC_DATA has been accessed.

Address: E7-00 (page0) NOR_FACTOR_H

Bit	Mode	Function
7:6	--	**Reserved**
5:0	R/W	**Bit[21:16] of Normalized Factor; NF=(255/N)*(2^22)**

Address: E7-01 (page0) NOR_FACTOR_M

Bit	Mode	Function
7:0	R/W	**Bit[15:8] of Normalized Factor; NF=(255/N)*(2^22)**

Address: E7-02 (page0) NOR_FACTOR_L

Bit	Mode	Function
7:0	R/W	**Bit[7:0] of Normalized Factor; NF=(255/N)*(2^22)**

Address: E7-03 (page0) BBE_CTRL default: 04h

Bit	Mode	Function
7	R/W	**BBE_ENA** 0: Disable Black-Background Exception 1: Enable Black-Background Exception
6:4	--	**Reserved**
3:0	R/W	**BBE_THD** 8-bit RGB Threshold for Black-Background Exception

Address: E7-04 (page0) NFLT_CTRL default: 00h

Bit	Mode	Function
7	R/W	**HNFLT_ENA** 0: Disable Histogram Noise Filter 1: Enable Histogram Noise Filter
6:4	R/W	**HNFLT_THD** Threshold for Histogram Noise Filter
3	R/W	**YNFLT_ENA** 0: Disable Ymax / Ymin Noise Filter 1: Enable Ymax / Ymin Noise Filter
2:0	R/W	**YNFLT_THD** Threshold for Ymax/Ymin Noise Filter (= 4*YNFLT_THD)

Address: E7-05 (page0) HIST_CTRL default: 00h

Bit	Mode	Function
7	R/W	**RH0_LIMITER** 0: Disable RH0 Limiter 1: Enable RH0 Limiter
6	R/W	**RH1_LIMITER** 0: Disable RH1 Limiter 1: Enable RH1 Limiter
5:3	R	**Real MOV_AVG_LEN** may be different with MOV_AVG_LEN, if SCG enable
2:0	R/W	**MOV_AVG_LEN**

		000: Histogram Moving Average Length = 1 001: Histogram Moving Average Length = 2 010: Histogram Moving Average Length = 4 011: Histogram Moving Average Length = 8 100: Histogram Moving Average Length = 16 101~111: reserved

Address: E7-06 (page0) **SOFT_CLAMP** **default: B0h**

Bit	Mode	Function
7:0	R/W	Slope of Soft-Clamping (= SOFT_CLAMP / 256)

Address: E7-07 (page0) **Y_MAX_LB** **default: FFh**

Bit	Mode	Function
7:0	R/W	Lower Bound of Y_MAX (= 4*Y_MAX_LB) (effect only if this register set from 0xF0~0xFF)

Address: E7-08 (page0) **Y_MIN_HB** **default: 00h**

Bit	Mode	Function
7:0	R/W	Higher Bound of Y_MIN (= 4*Y_MIN_HB) (effect only if this register set from 0x00~0x0F)

Address: E7-09 (page0) **SCG_PERIOD** **default: xxx10000b**

Bit	Mode	Function
7	R/W	**Scene-Change Control Mode** 0: old mode (2553V) 1: new mode (2622)
6:5	--	**Reserved**
4:0	R/W	**Scene-Change Mode Period = 1~32.** Note: SCG_PERIOD >= MOV_AVG_LEN, CRE7-05[2:0](page0)

Address: E7-0A (page0) **SCG_LB** **default: 00h**

Bit	Mode	Function
7:0	R/W	SCG_DIFF Lower Bound for Exiting Scene-Change Mode

Address: E7-0B (page0) **SCG_HB** **default: FFh**

Bit	Mode	Function
7:0	R/W	SCG_DIFF Higher Bound for Exiting Scene-Change Mode

Address: E7-0C (page0) **POPUP_CTRL**

Bit	Mode	Function
7:1		Reserved
0	R	Reg[0D]~Reg[16] are updated every frame. Once POPUP_BIT is read, the value of Reg[0D] ~ Reg[16] will not be updated until Reg[16] is read.

Address: E7-0D (page0) **SCG_DIFF**

Bit	Mode	Function
7:0	R	= (Histogram Difference between Current Frame and Average) / 8

Address: E7-0E (page0) **Y_MAX_VAL**

Bit	Mode	Function
7:0	R	= Max { Y_MAX_LB, (Y Maximum in Current Frame / 4) }

Address: E7-0F (page0) **Y_MIN_VAL**

Bit	Mode	Function
7:0	R	= Min { Y_MIN_HB, (Y Minimum in Current Frame / 4) }

Address: E7-10 (page0) **S0_VALUE**

Bit	Mode	Function
7:0	R	Normalized Histogram S0 Value

Address: E7-11 (page0) **S1_VALUE**

Bit	Mode	Function
7:0	R	Normalized Histogram S1 Value

Address: E7-12 (page0) **S2_VALUE**

Bit	Mode	Function
7:0	R	Normalized Histogram S2 Value

Address: E7-13 (page0) S3_VALUE

Bit	Mode	Function
7:0	R	Normalized Histogram S3 Value

Address: E7-14 (page0) S4_VALUE

Bit	Mode	Function
7:0	R	Normalized Histogram S4 Value

Address: E7-15 (page0) S5_VALUE

Bit	Mode	Function
7:0	R	Normalized Histogram S5 Value

Address: E7-16 (page0) S6_VALUE

Bit	Mode	Function
7:0	R	Normalized Histogram S6 Value

Address: E7-00 (page1) DEF_CRV[01] default:10h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-01 (page1) DEF_CRV[02] default:20h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-02 (page1) DEF_CRV[03] default:30h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-03 (page1) DEF_CRV[04] default:40h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-04 (page1) DEF_CRV[05] default:50h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-05 (page1) DEF_CRV[06] default:60h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-06 (page1) DEF_CRV[07] default:70h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-07 (page1) DEF_CRV[08] default:80h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-08 (page1) DEF_CRV[09] default:90h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-09 (page1) DEF_CRV[10] default:A0h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-0A (page1) DEF_CRV[11] default:B0h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-0B (page1) DEF_CRV[12] default:C0h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-0C (page1) DEF_CRV[13] default:D0h

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-0D (page1) DEF_CRV[14] default:E0h

Bit	Mode	Function

7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-0E (page1) **DEF_CRV[15]** **default:F0h**

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Address: E7-0F (page1) **DEF_CRV[16]** **default:00h**

Bit	Mode	Function
7:0	R/W	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1] Note : default = 0x00 means 0x100 (256)

Registers below is effective only when auto mode is disable and black/white level expansion is enabled.

When auto mode is enabled (DCC_MODE=0), Y_BL_BIAS and Y_WL_BIAS are read-only.

Address: E7-10 (page1) **Y_BL_BIAS** **default:00h**

Bit	Mode	Function
7:0	R/W	Y Offset for Black-Level Expansion (Y_L' = 4*Y_BL_BIAS)

Load double buffer CRE7-00 ~ CRE7-10 (page1) after write CRE7-10 when DCC enable

Address: E7-11 (page1) **Y_WL_BIAS** **default:00h**

Bit	Mode	Function
7:0	R/W	Y Offset for While-Level Expansion (1023-Y_H' = 4*Y_WL_BIAS)

Address: E7-12 (page1) **SAT_COM_FACTOR** **default:00h**

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Saturation Compensation Factor = 0~32 (default=0x00)

Registers below is effective only when auto mode is enabled.

In manual mode (DCC_MODE=1), BLD_VAL will be fixed to 0. It means Y-curve is fully determined by DEF_CUR[01~15]

Address: E7-13 (page1) **BLD_UB** **default:00h**

Bit	Mode	Function
7:0	R/W	Upper Bound of Blending Factor

Address: E7-14 (page1) **BLD_LB** **default:00h**

Bit	Mode	Function
7:0	R/W	Lower Bound of Blending Factor

Address: E7-15 (page1) **DEV_FACTOR** **default:00h**

Bit	Mode	Function
7:0	R/W	Deviation Weighting Factor

Address: E7-16 (page1) **BLD_VAL_SEL** **default:00h**

Bit	Mode	Function
7:6	R/W	**White-Level Range** 00: Yi = 512 (Z8) (Default) 01: Yi = 576 (Z9) 10: Yi = 640 (Z10) 11: Yi = 704 (Z11)
5:4	R/W	**White-Level Blending Factor** 00: 0 (user-defined curve) 01: R/2 10: R 11: 2R
3:2	R/W	**Black-Level Range** 00: Yi = 448 (Z7) 01: Yi = 384 (Z6) 10: Yi = 320 (Z5) 11: Yi = 256 (Z4)
1:0	R/W	**Black-Level Blending Factor** 00: 0 (user-defined curve)

		01: R/2 10: R 11: 2R

Address: E7-17 (page1) **BLD_VAL**

Bit	Mode	Function
7:0	R	= Max{ BLD_UB – [(DEV_VAL*DEV_FACTOR)/256], BLD_LB}

Address: E7-18 (page1) **DEV_VAL_HI**

Bit	Mode	Function
7:0	R	Bit[8:1] of Deviation Value

Address: E7-19 (page1) **DEV_VAL_LO**

Bit	Mode	Function
7	R	Bit[0] of Deviation Value
6:0	--	Reserved

Address: E7-00~8F (page2) **SRAM initial value**

Bit	Mode	Function
7:0	W	Addr 00: SRAM_00 Addr 00: SRAM_01 …. Addr 8F : SRAM_8F

Address: E7-00 (page3) **SRAM_BIST** **default: 00h**

Bit	Mode	Function
7	R/W	**BIST_EN** 0: disable 1: enable
6	R/W	**RAM_Mode** 0: dclk domain mode (normal mode, BIST) 1: MCU domain mode (SCG test)
5:2	--	Reserved
1	R	**BIST_Period** 0: BIST is done 1: BIST is running
0	R	**BIST_OK** 0: SRAM fail 1: SRAM ok

Cyclic-Redundant-Check

Address: F2 **OP_CRC_CTRL (Output CRC Control Register)** **Default: 00h**

Bit	Mode	Function
7:1	--	**Reserved to 0**
0	R/W	**Output CRC Control:** 0: Stop or finish (Auto-stop after checked a completed display frame) (Default) 1: Start

CRC function = X^24 + X^7 + X^2 + X + 1.

Address: F3 **OP _CRC_CHECKSUM (Output CRC Checksum)**

Bit	Mode	Function
7:0	R/W	**1st read=> Output CRC-24 bit 23~16** **2nd read=> Output CRC-24 bit 15~8**

		3rd read=> Out put CRC-24 bit 7~0

- The read pointer should be reset when 1. OP_CRC_BYTE is written 2. Output CRC Control starts.
- The read back CRC value address should be auto-increase, the sequence is shown above

DDC Special Function Access (DDC/CI)

Address: F4 **DDC_SET_SLAVE** **Default: 6E**

Bit	Mode	Function
7:1	R/W	**DDC Slave Address to decode**
0	R/W	**Sample clk select** 0: xclk/2 (default) 1: xclk

Address: F5 **DDC_SUB_IN**

Bit	Mode	Function
7:0	R	**DDC Sub-Address Received**

Address: F6 **DDC_DATA_IN**

Bit	Mode	Function
7:0	R/W	**Read: DDC Data Received (16-bytes buffer)** **Write: DDC Data Received (16-bytes buffer)** Every Read/Write access, the buffer index is auto-decreased/increased.

Address: F7 **DDC_CTRL** **Default: 00h**

Bit	Mode	Function
7:5	--	**Reserved**
4	R/W	**Force DDC2B** 0: disable 1: enable
3	R/W	**Auto reset DDC_DATA Buffer** 0: disable 1: enable In host (pc) write enable, when DDC write (No START after DDC_SUB), reset DDC_DATA buffer.
2	R/W	**Reset DDC_DATA buffer** 0: Finish 1: Reset
1	R/W	**DDC_DATA buffer write enable** 0: host (pc) write enable 1: slave (mcu) write enable Both PC and MCU can read DDC_DATA buffer, but only one can write DDC_DATA buffer.
0	--	**Reserved**

Address: F8 **DDC_STATUS**

Bit	Mode	Function
7	R	**DDC_DATA_BUFFER Full** If DDC_DATA buffer is full, this bit is set to "1". (On-line monitor) The DDC_DATA buffer Full status will be on-line-monitor the condition, once it becomes full, it kept high, if it is not-full, then it goes low.
6	R	**DDC_DATA_BUFFER Empty** If DDC_DATA buffer is empty, this bit is set to "1". (On-line monitor) The DDC_DATA buffer Empty status will be on-line-monitor the condition, once it becomes empty, it kept high, if it is not-empty, then it goes low.
5	--	**Reserved to 0**
4	R	If **DDC_STOP** signal occurs, this bit is set to "1" . Write clear.
3	R	If **DDC_DATA_OUT** loaded to serial-out-byte, this bit is set to "1". Write clear
2	R	If **DDC_DATA_IN** latched, this bit is set to "1" . Write clear
1	R	If **DDC_SUB** latched, this bit is set to "1" Write clear
0	R	If **DDC_SLAVE** latched, this bit is set to "1" Write clear

When DDC Start, clear DDC_Stop flag, CRF8[4].

Address: F9 **DDC_IRQ_CTRL** **Default: 00h**

Bit	Mode	Function
7	R/W	0: Disable the **DDC_DATA_BUFFER Full** signal as an interrupt source 1: Enable the **DDC_DATA_BUFFER Full** signal as an interrupt source
6	R/W	0: Disable the **DDC_DATA_BUFFER Empty** signal as an interrupt source 1: Enable the **DDC_DATA_BUFFER Empty** signal as an interrupt source
5	R/W	**Start/Stop code debounce** 0: Disable 1: Enable t
4	R/W	0: Disable the **DDC_STOP** signal as an interrupt source 1: Enable the **DDC_STOP** signal as an interrupt source
3	R/W	0: Disable the **DDC_DATA_OUT** loaded to serial-out-byte as an interrupt source 1: Enable the **DDC_DATA_OUT** loaded to serial-out-byte as an interrupt source
2	R/W	0: Disable the **DDC_DATA_IN** latched as an interrupt source 1: Enable the **DDC_DATA_IN** latched as an interrupt source
1	R/W	0: Disable the **DDC_SUB** latched as an interrupt source 1: Enable the **DDC_SUB** latched as an interrupt source
0	R/W	0: Disable the **DDC_SLAVE** latched as an interrupt source 1: Enable the **DDC_SLAVE** latched as an interrupt source

Address: FA Reserved

Address: FB Reserved

Address: FC Reserved

Address: FD **DDC__DVI_ENABLE (DDC Channel Enable Register)** **Default: 00h**

Bit	Mode	Function
7:5	R/W	**DVI DDC Channel Address Least Significant 3 Bits** (The default DDC channel address MSB 4 Bits is "A")
4	R/W	**DVI DDC Write Status (for external DDC access only)** It is cleared after write.
3	R/W	**DVI DDC SRAM Write Enable (for external DDC access only)** 0: Disable 1: Enable
2	R/W	**DVI DDC De-bounce Enable (Remember to attribute the pad as Schmitt trigger pad)** 0: Disable 1: Enable
1	R/W	**DVI DDC Channel RAM Size** 0: 128 bytes 1: 256 bytes
0	R/W	**DVI DDC Channel Enable Bit** 0: MCU access Enable 1: DDC channel Enable

Address: FE **DVI DDC_INDEX (DDC SRAM R/W Index Register)**

Bit	Mode	Function
7:0	R/W	**DVI DDC SRAM Read/Write Index Register [7:0]**

The DDC channel index register will be auto increased one by one after each read or write cycle.

Address: FF **DVI DDC_ACCESS_PORT (DDC Channel ACCESS Port)**

Bit	Mode	Function
7:0	R/W	**DVI DDC SRAM Read/Write Port**

** The DDC function can still work when Power_Down & Power_Save.

** After reset, the register will be set to default value, but the SRAM will keep original data.

Embedded OSD

Addressing and Accessing Register

ADDRESS	BIT							
	7	6	5	4	3	2	1	0
High Byte	A15	A14	A13	A12	A11	A10	A9	A8
Low Byte	A7	A6	A5	A4	A3	A2	A1	A0

Figure 5. Addressing and Accessing Registers

Date	BIT							
Byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2. Data Registers

All kind of registers can be controlled and accessed by these 2 bytes, and each address contains 3-byte data, details are described as follows:

Write mode: **[A15:A14] select which byte to write**

-00: Byte 0 -01:Byte 1 -10: Byte 2 –11: All

****All data are sorted by these three Bytes (Byte0~Byte2)***

[A13] Auto Load (Double Buffer)

[A12] Address indicator

-0: Window and frame control registers.

-1: Font Select and font map SRAM

[A11:A0] Address mapping

- Font Select and font map SRAM address: 000~15FF

-Frame control register address: 000~0xx **(Latch)**

-Window control register address: 100~1xx **(Latch)**

**** Selection of SRAM address or Latch address selection is determined by A12!***

Example:

Bit [15:14]=00

-All data followed are written to byte0 and address increases.

*Byte0 **à** Byte0 **à** Byte0… (Address will auto increase)*

Bit [15:14] =01

-All data followed are written to byte1 and address increases.

*Byte1 **à** Byte1 **à** Byte1… (Address will auto increase)*

Bit [15:14] =11

- Address will be increased after each 3-byte data written.

*Byte0 **à** Byte1 **à** Byte2 **à** Byte0 **à** Byte1 **à** Byte2… (Address will auto increase)*

Window control registers

- Windows all support shadow/border/3D button
- Window0, 5, 6, 7 support gradient functions.
- Window 4, 5, 6, 7 start/end resolution are 1line(pixel), Window 0, 1, 2, 3 start/end resolution are 4line(pixel),
- All window start and end position include the ***special effect (border/shadow/3D button)*** been assigned
- Font comes after windows by 10 pixels, so you should compensate 10 pixels on windows to meet font position

Window 0 Shadow/Border/Gradient

Address: 100h

Byte 0

Bit	Mode	Function
7:6	--	**Reserved**
5:3	W	**Window 0 shadow/border width or 3D button thickness in pixel unit** 000~111: 1 ~ 8 pixel
2:0	W	Window 0 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 0 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 0 border color index in 16-color LUT

		For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 0 start position

Address: 101h

Byte 0

Bit	Mode	Function
7:2	W	Window 0 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 0 vertical start [2:0] line
4:0	W	Window 0 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical start [10:3] line

Start position must be increments of four.

Window 0 end position

Address: 102h

Byte 0

Bit	Mode	Function
7:2	W	Window 0 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 0 vertical end [2:0] line
4:0	W	Window 0 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical end [10:3] line

- End position must be increments of four.

Window 0 control

Address: 103h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved

6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 0 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 0 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 0 Enable 0: Disable 1: Enable

Window 1 Shadow/Border/Gradient

Address: 104h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 1 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 1 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1 start position

Address: 105h

Byte 0

Bit	Mode	Function
7:2	W	Window 1 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 1 vertical start [2:0] line
4:0	W	Window 1 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical start [10:3] line

Start position must be increments of four.

Window 1 end position

Address: 106h

Byte 0

Bit	Mode	Function
7:2	W	Window 1 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 1 vertical end [2:0] line
4:0	W	Window 1 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical end [10:3] line

End position must be increments of four.

Window 1 control

Address: 107h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 1 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 1 Enable 0: Disable 1: Enable

Window 2 Shadow/Border/Gradient

Address: 108h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 2 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 2 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2 start position

Address: 109h

Byte 0

Bit	Mode	Function
7:2	W	Window 2 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 2 vertical start [2:0] line
4:0	W	Window 2 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical start [10:3] line

Start position must be increments of four.

Window 2 end position

Address: 10Ah

Byte 0

Bit	Mode	Function
7:2	W	Window 2 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 2 vertical end [2:0] line
4:0	W	Window 2 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function

7:0	W	Window 2 vertical end [10:3] line

End position must be increments of four.

Window 2 control

Address: 10Bh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 2 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 2 Enable 0: Disable 1: Enable

Window 3 Shadow/Border/Gradient

Address: 10Ch

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 3 shadow/border height in line unit

		000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 3 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 3 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3 start position

Address: 10Dh

Byte 0

Bit	Mode	Function
7:2	W	Window 3 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 3 vertical start [2:0] line
4:0	W	Window 3 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical start [10:3] line

Start position must be increments of four.

Window 3 end position

Address: 10Eh

Byte 0

Bit	Mode	Function
7:2	W	Window 3 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 3 vertical end [2:0] line
4:0	W	Window 3 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical end [10:3] line

End position must be increments of four.

Window 3 control

Address: 10Fh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 3 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 3 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 3 Enable 0: Disable 1: Enable

Window 4 Shadow/Border/Gradient

Address: 110h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 4 shadow/border width or 3D button thickness in pixel unit

		000~111: 1 ~ 8 pixel
2:0	W	Window 4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4 shadow color index in 16-color LUT For 3D window, it is the left-top/ bottom border color
3:0	W	Window 4 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4 start position

Address: 111h

Byte 0

Bit	Mode	Function
7:2	W	Window 4 horizontal start [5:0]
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 4 vertical start [2:0] line
4:0	W	Window 4 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical start [10:3] line

Window 4 end position

Address: 112h

Byte 0

Bit	Mode	Function
7:2	W	Window 4 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 4 vertical end [2:0] line
4:0	W	Window 4 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical end [10:3] line

Window 4 control

Address: 113h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 4 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4 Enable 0: Disable 1: Enable

Window 5 Shadow/Border/Gradient

Address: 114h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel

2:0	W	Window 5 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 5 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 5 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 5 start position

Address: 115h

Byte 0

Bit	Mode	Function
7:2	W	Window 5 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function

7:5	W	Window 5 vertical start [2:0] line
4:0	W	Window 5 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical start [10:3] line

Window 5 end position

Address: 116h

Byte 0

Bit	Mode	Function
7:2	W	Window 5 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 5 vertical end [2:0] line
4:0	W	Window 5 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical end [10:3] line

Window 5 control

Address: 117h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 5 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 5 Enable 0: Disable 1: Enable

Window 6 Shadow/Border/Gradient

Address: 118h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 6 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function

7:4	W	Window 6 shadow color index in 16-color LUT For 3D window, it is the left-top/ bottom border color
3:0	W	Window 6 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 6 start position

Address: 119h

Byte 0

Bit	Mode	Function
7:2	W	Window 6 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 6 vertical start [2:0] line
4:0	W	Window 6 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical start [10:3] line

Window 6 end position

Address: 11Ah

Byte 0

Bit	Mode	Function
7:2	W	Window 6 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 6 vertical end [2:0] line
4:0	W	Window 6 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical end [10:3] line

Window 6 control

Address: 11Bh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 6 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable

5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 6 Enable 0: Disable 1: Enable

Window 7 Shadow/Border/Gradient

Address: 11Ch

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 7 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 7 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function

7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 7 start position

Address: 11Dh

Byte 0

Bit	Mode	Function
7:2	W	Window 7 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 7 vertical start [2:0] line
4:0	W	Window 7 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical start [10:3] line

Window 7 end position

Address: 11Eh

Byte 0

Bit	Mode	Function
7:2	W	Window 7 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 7 vertical end [2:0] line
4:0	W	Window 7 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical end [10:3] line

Window 7 control

Address: 11Fh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

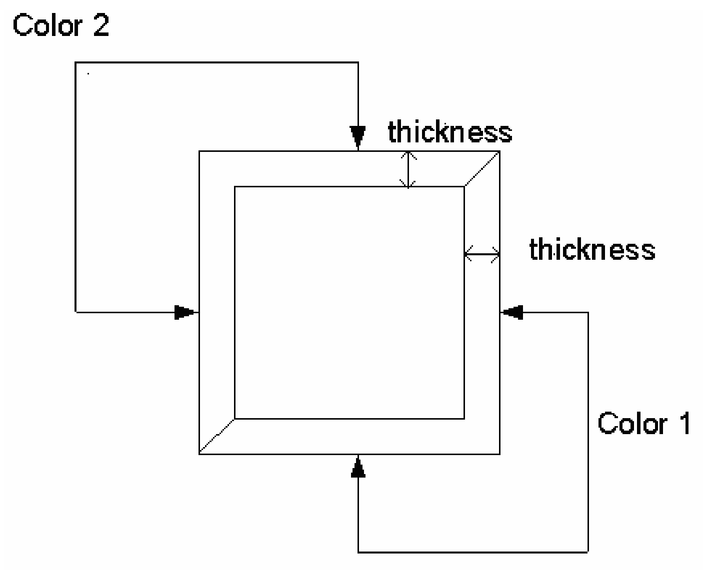
Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 7 color index in 16-color LUT

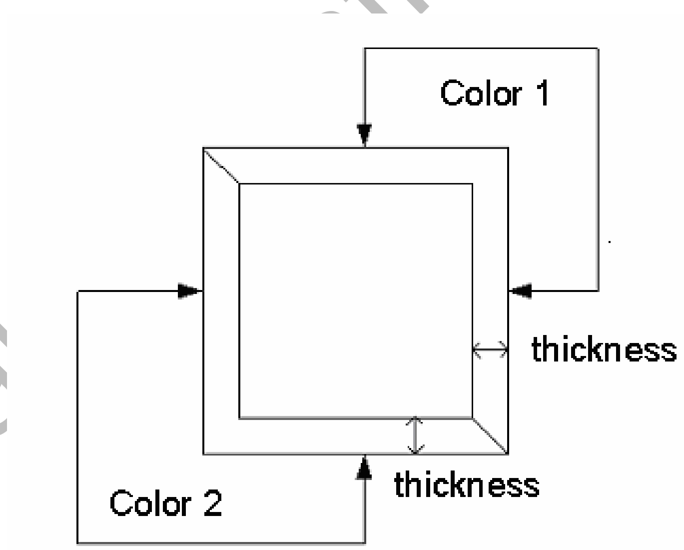
Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 7 Type

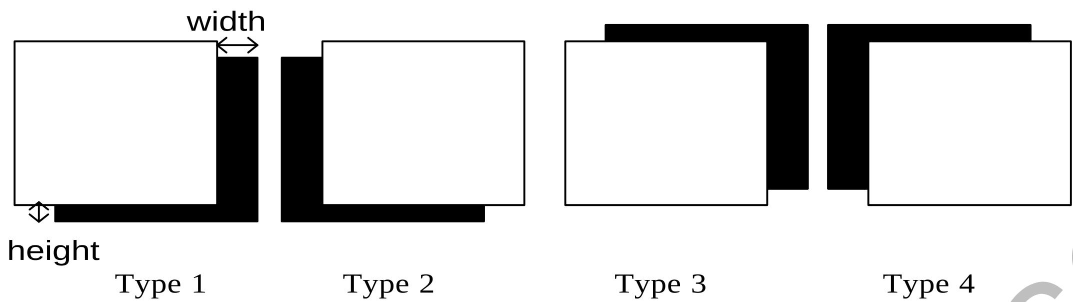
		000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 7 Enable 0: Disable 1: Enable



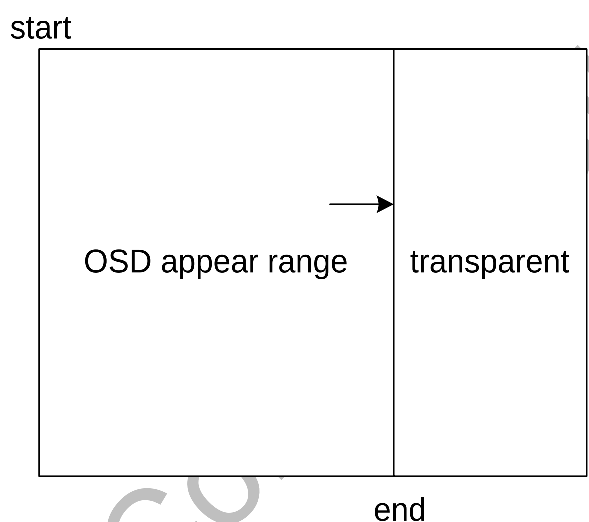
3D Button Type 1



3D Button Type 2



Shadow in all direction



Window mask fade/in out function

Frame control registers

Address: 000h

Byte 0

Bit	Mode	Function
7:0	R/W	Vertical Delay [10:3] The bits define the vertical starting address. Total 2048 step unit: 1 line

Vertical delay minimum should set 1

Byte 1

Bit	Mode	Function
7:0	R/W	Horizontal Delay [9:2] The bits define the horizontal starting address. Total 1024 step unit:4 pixels

Horizontal delay minimum should set 2

Byte 2 default: xxxx_xxx0b

Bit	Mode	Function
7:6	R/W	Horizontal Delay bit [1:0]
5:3	R/W	Vertical Delay [2:0]
2:1	R/W	Display zone, for smaller character width 00: middle 01: left 10: right 11: reserved
0	R/W	OSD enable 0: OSD circuit is inactivated 1: OSD circuit is activated

When OSD is disabled, Double Width (address 0x002 Byte1[1]) must be disabled to save power.

These three bytes have their own double buffer.

PWM Duty Width

Address: 001h

Byte 0 Default: 00h

Bit	Mode	Function
7:0	R/W	PWM_0 8bits decides the output duty width and waveform of PWM at PWM channel

Byte 1 Default: 00h

Bit	Mode	Function
7:0	R/W	PWM_1 8bits decides the output duty width and waveform of PWM at PWM channel

Byte 2 Default: 00h

Bit	Mode	Function
7:0	--	Reserved

Address: 002h

Byte 0 Default: 00h

Bit	Mode	Function
7:0	R/W	PWM0 First stage clock divider N[7:0] N=0-255, 1st F= F/2(N+1)

Byte 1 Default: 00h

Bit	Mode	Function
7	R/W	PWM0 First stage clock divider Enable 0: Disable 1: Enable
6	R/W	PWM1 First stage clock divider Enable 0: Disable 1: Enable
5	--	Reserved
4	R/W	Enable PWM Output
3:2	R/W	Crystal Clock Divider 00: Crystal 01: Crystal/2 10: Crystal/4 11: Crystal/8
1	R/W	PWM0 reset by DVS enable 0: Disable

		1: Enable
0	R/W	PWM1 reset by DVS enable 0: Disable 1: Enable

Byte 2 Default: 00h

Bit	Mode	Function
7:0	R/W	PWM1 First stage clock divider N[7:0] N=0-255, 1^{st} F= F/2(N+1)

Address: 003h

Byte 0 Default: 00h

Bit	Mode	Function
7	R/W	Specific color blending (blending type 2) bit[3:0] 0: Disable 1: Enable
6:5	R/W	Window 7special function 00: disable 01: blending (blending type 3) 10: window 7 mask region appear 11: window 7 mask region transparent
4	R/W	OSD vertical start input signal source select 0: Select DVS as OSD VSYNC input 1: Select ENA as OSD VSYNC input
3:0	R/W	Blending color from 16-color LUT (blending type 2)

Byte 1

Bit	Mode	Function
7:4	R/W	Char shadow/border color
3: 2	R/W	Alpha blending type (blending type 1) 00: Disable alpha blending 01: Only window blending 10: All blending 11: Window and Character background blending
1	R/W	Double width enable (For all OSD including windows and characters) 0: Normal 1: Double
0	R/W	Double Height enable (For all OSD including windows and characters) 0: Normal 1: Double

Total blending area = blending type1 area + blending type 2 area + blending type 3 area

Byte 2 **Default: 00h**

Bit	Mode	Function
7:6	R/W	**Font downloaded swap control** 0x: No swap 10: CCW 11: CW
5	R	**Buffer Empty** 0: empty rotation-font buffer 1: non-empty rotation-font buffer
4	R	**Buffer Valid** 0: buffer job done 1: buffer is writing to SRAM
3	R/W	**Reset buffer** 0: Normal (Default) 1: reset non-full rotation-font buffer
2	R/W	**Hardware Rotation Enable** 0: Disable (Default) 1: Enable
1	R/W	**Global Blinking Enable** 0: Disable 1: Enable
0	R/W	**Rotation** 0: Normal (data latch 24 bit per 24 bit) 1: Rotation (data latch 18 bit per 24 bit)

Bit	7	6	5	4	3	2	1	0
Firmware	A	B	C	D	E	F	G	H
CW	A	E	B	F	C	G	D	H
CCW	E	A	F	B	G	C	H	D

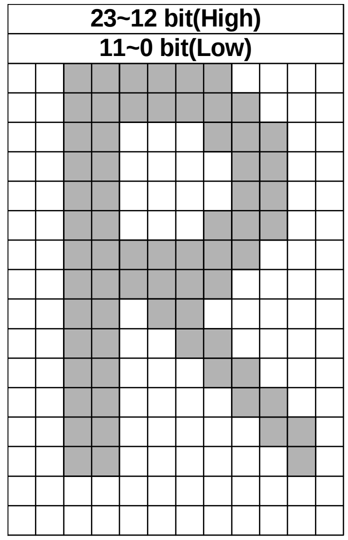


Figure 3 Non-rotated memory alignments

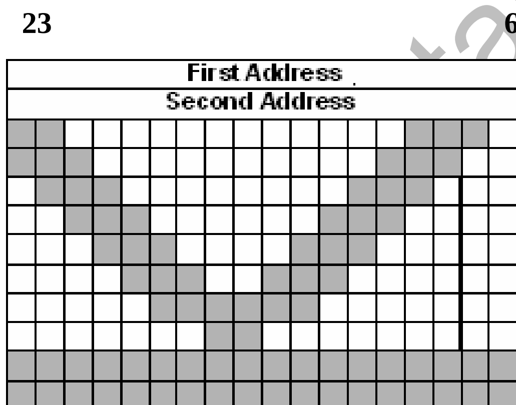


Figure 4 Rotated memory alignments

Base address offset

Address: 004h

Byte 0

Bit	Mode	Function
7:0	R/W	Font Select Base Address[7:0]

Byte 1

Bit	Mode	Function
7:4	R/W	Font Select Base Address[11:8]
3:0	R/W	Font Base Address[3:0]

Byte 2

Bit	Mode	Function
7:0	R/W	Font Base Address[11:4]

When OSD function for PON-ON is enabled (OSD[008]), Font Select Base Address here will not be effective.

OSD compression

Address: 005h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 0
3:0	R/W	4-bit value for VLC code 100

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1010
3:0	R/W	4-bit value for VLC code 1011

Byte 2

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1100
3:0	R/W	4-bit value for VLC code 1101 0

Address: 006h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1101 1
3:0	R/W	4-bit value for VLC code 1110 0

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1110 10
3:0	R/W	4-bit value for VLC code 1110 11

Byte 2

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 00
3:0	R/W	4-bit value for VLC code 1111 01

Address: 007h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 100

3:0	R/W	4-bit value for VLC code 1111 101

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 110
3:0	R/W	4-bit value for VLC code 1111 1110

Byte 2 default: xxxx_xxx0b

Bit	Mode	Function
7:1	--	reserved
0	R/W	OSD compression (4bit/symbol, VLC code 1111_1111 represents the end of data) (only for SRAM) 0: disable 1: enable

Note:

1. If enable OSD compression or auto load (double buffer), only one byte can be read after writing address at 0x90, 0x91.
2. For OSD compression, MSB 4 bits of original byte is first transferred to corresponding VLC code, and then LSB 4 bits is transferred. VLC code is placed from LSB to MSB of compression font. For example, 4-bit value for VLC code 1100 is 4’b0101, and 4-bit value for VLC code 100 is 4’b0001. Original data 0x15 is transferred to compression x0011001.
3. OSD double buffer and compression can’t be enabled simultaneous.
4. When power-down mode or lack of crystal clock, OSD compression font can’t be write.
5. After OSD enable, it is better to delay 1 DVS to start writing OSD compression data.

OSD Special Function

Address: 008h

Byte 0 Default: 0x00

Bit	Mode	Function
7	R/W	OSD Special Function Enable 0: Disable 1: Enable
6	R/W	OSD Special Function Select (Effective only when Bit[7]=1) 0: ROLL-UP 1: POP-ON
5	R/W	OSD Vertical Boundary Function Enable 0: Disable 1: Enable
4:1	R/W	Reserved to 0
0	R/W	Display Base Select (Effective only when Bit[7:6]=11`b)

		0: Base 0 1: Base 1

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	Row Command Base 0 [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	Row Command Base 1 [7:0]

Address: 009h

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	Font Select Base 0 [11:8]
3:0	R/W	Font Select Base 1 [11:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	Font Select Base 0 [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	Font Select Base 1 [7:0]

Address: 00Ah

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	OSD Vertical Upper Boundary [10:8]
3:0	R/W	OSD Vertical Lower Boundary [10:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	OSD Vertical Upper Boundary [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	OSD Vertical Lower Boundary [7:0]

Note:

1. When OSD Special Function for POP-ON is enabled, Font Select Base Address in OSD[004] will not be effective anymore.
2. When OSD Vertical Boundary Function is enabled, OSD image above upper boundary and below lower boundary will be invisible.
3. When ROLL-UP function is enabled, OSD will always start from the row-command pointed by Base0, and after

the row-command pointed by Base1 has been dealt with, the next row-command will be the first one in OSD SRAM. Row-command processing will terminate in the row-command before the one pointed by Base0. (For example, R1 is pointed by Base0, and R5 is pointed by Base1. OSD will show R1 as the first row, followed by R2, R3, R4, R5, and R0 as last row.)

4. When POP-ON function is enabled, OSD will start from the row command pointed by the base selected as display base(selected by OSD[008][0.0]), and terminate when end-command is encountered. That is, all row-command will be separated into two non-overlay subset which is enclosed by the row-command pointed by base and end-command.

OSD SRAM (Map and font registers)

<table>
<tr><td>R0</td><td>R1</td><td>R2</td><td colspan="4">….</td><td>Rn</td><td>End</td><td colspan="3"></td></tr>
<tr><td>C01</td><td>C02</td><td>B03</td><td>C04</td><td colspan="3">…</td><td>C11</td><td>C12</td><td>C13</td><td colspan="2">…</td></tr>
<tr><td colspan="12">…</td></tr>
<tr><td colspan="12">…</td></tr>
<tr><td colspan="3">…</td><td>Cn1</td><td>Cn2</td><td colspan="3">…</td><td colspan="3">1-bit font start</td><td>…</td></tr>
<tr><td colspan="12">…</td></tr>
<tr><td colspan="3">…</td><td colspan="3">2-bit font start</td><td colspan="6">…</td></tr>
<tr><td colspan="12">…</td></tr>
<tr><td colspan="3">4-bit font start</td><td colspan="9">…</td></tr>
<tr><td colspan="12">…</td></tr>
<tr><td colspan="12">…</td></tr>
</table>

16.5k bytes SRAM

1. Row Command

R0	R1	R2	R3	R….	Rn	End

Row Command R0~Rn represent the start of new row. Each command contains 3 bytes data which define the length of a row and other attributes. OSD End Command represent the end of OSD. R0 is set in address 0 of SRAM.

2. Character/Blank Command (Font Select)

Character Command is used to select which character font is show. Each command contains three bytes which specify its attribute and 1,2 or 4bit per pixel. Blank Command represents blank pixel to separate the preceding character and following character. Use two or more Blank Command if the character distance exceeds 255 pixel.

The Font Select Base Address in Frame Control Register represents the address of the first character in Row 0, that is, C01 in the above figure. The following character/blank is write in the next address. C11 represents the first character in Row1, C12 represents the second character in Row1, and so on.

The address of the first character Cn1 in Row n = Font Select Base Address + Row 0 font base length + Row 1 font base length + …+Row n-1 font base length.

3. Font

User fonts are stored as bit map data. For normal font, one font has 12x18 pixel, and for rotation font, one has 18x12 pixel. One pixel use 1, 2 or 4 bits.

For 12x18 font,

One 1-bit font requires 9 * 24bit SRAM

One 2-bit font requires 18 * 24bit SRAM

One 4-bit font requires 36 * 24bit SRAM

For 18x12 font,

One 1-bit font requires 12 * 24bit SRAM

One 2-bit font requires 24 * 24bit SRAM

One 4-bit font requires 48 * 24bit SRAM

Font Base Address in Frame Control Register point to the start of 1-bit font.

For normal (12x18) font:

1-bit Font, if CS = 128, Real Address of Font = Font Base Address + 9 * 128

2-bit Font, if CS = 128, Real Address of Font = Font Base Address + 18 * 128

4-bit Font, if CS = 128, Real Address of Font = Font Base Address + 36 * 128

For rotational (18x12) font:

1-bit Font, if CS = 128, Real Address of Font = Font Base Address + 12 * 128

2-bit Font, if CS = 128, Real Address of Font = Font Base Address + 24 * 128

4-bit Font, if CS = 128, Real Address of Font = Font Base Address + 48 * 128

where CS is Character Selector in Character Command.

Note that Row Command, Font Select and Font share the same OSD SRAM.

When we download the font, we have to set the Frame control 002h byte1 [1:0] to set the method of hardware bit swap. If the OSD is Counter-Clock-Wise rotated, we have to set to 0x01 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of “7 5 3 1 6 4 2 0” (from MSB to LSB) and should be rearranged to “7 6 5 4 3 2 1 0” by hardware). If it is Clock-Wise rotated, we have to set to 0x10 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of “6 4 2 0 7 5 3 1” (from MSB to LSB) and should be rearranged to “7 6 5 4 3 2 1 0” by hardware). After we finish the downloading or if we don’t have to rotate the OSD, we have to set it to 0x00.

Row Command

Byte 0

Bit	Mode	Function
7	W	1: Row Start Command 0: OSD End Command Each row must start with row-command, last word of OSD map must be end-command
6	R/W	VBI OSD function enable 0: normal OSD function as usual 1: support VBI OSD functions like underline, B/F separated blink and 512 fonts select
5	W	Reserved
4:2	W	Character border/shadow 000: None 001: Border 100: Shadow (left-top) 101: Shadow (left-bottom) 110: Shadow (right-top) 111: Shadow (right-bottom)
1	W	Double character width 0: x1 1: x2
0	W	Double character height 0: x1 1: x2

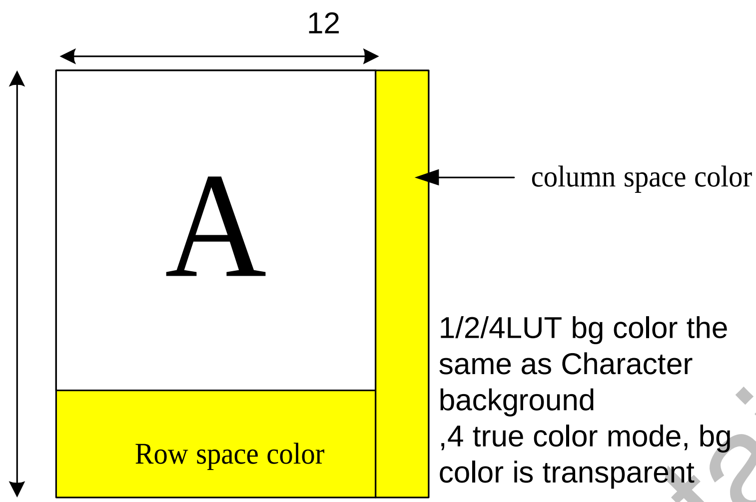
Byte 1

Bit	Mode	Function
7:3	W	Row height (1~32)
2:0	W	Column space 0~7 pixel column space When Char is doubled, so is column space.

Notice:

When character height/width is doubled, the row height/column space definition also twice. If the row height is larger than character height, the effect is just like space between rows. If it is smaller than character height, it will drop last several bottom line of character.

When using 1/2/4LUT font, column space and font smaller than row height, the color of column space and row space is the same as font background color, only 4 bit true color font mode, the color is transparent



Byte 2

Bit	Mode	Function
7:0	W	Row length unit: font base

Character Command (For blank)

Byte 0

Bit	**Mode**	**Function**
7	W	0
6	W	Blinking effect 0: Disable 1: Enable
5:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Blank pixel length

At least 3 pixels, and can't exceed 255 pixels.

Byte 2

Bit	Mode	Function

7:5	W	Reserved
4	W	Reserved
3:0	W	Blank color – select one of 16-color LUT (0 is special for transparent)

Character Command (For 1-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	00 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	VBI OSD disable: Character width (only for 1-pixel font, doubled when specifying double-width in Row/Blank command register) For 12x18 font: 0100: 4-pixel 0101: 5-pixel 0110: 6-pixel 0111: 7-pixel 1000: 8-pixel 1001: 9-pixel 1010: 10-pixel 1011:11-pixel 1100: 12-pixel For 18x12 Font (rotated) 0000: 4-pixel 0001: 5-pixel 0010: 6-pixel 0011: 7-pixel 0100: 8-pixel 0101: 9-pixel 0110: 10-pixel 0111: 11-pixel 1000: 12-pixel 1001:13-pixel 1010:14-pixel 1011:15-pixel 1100: 16-pixel 1101:17-pixel 1110:18-pixel VBI OSD enable: While VBI OSD enable, 1 bit font will be NO rotated and 12-pixel fonts always. Then the [3:0] setting will be as following: [3]: character select[8] support 512 font while VBI OSD enable [2]: additional blinking effect {[6], [2]}

		00: NO blink for both F/B 01: Only blink for Foreground 10: Only blink for Background 11: Both blink for F/B [1]: Underline enable underline will be at 17th & 18th line and got the same color with foreground [0]: Reserved

When using border/shadow/ effect, the width of the 1-bit font should at least 6 pixel.

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:4	W	Foreground color Select one of 16-color from color LUT
3:0	W	Background color Select one of 16-color from color LUT (0 is special for transparent)

Character command (For 2-bit RAM Font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	MSB of Foreground color 11, Background 00
5	W	1
4	W	MSB of Foreground color 10, Foreground 01
3:1	W	Foreground color 11 Select one of 8 color from color LUT Add Byte0 [6] as MSB for 16-color LUT.
0	W	Background color 00 Bit[2] Select one of 8 color from color LUT

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:6	W	Background color 00 Bit[1:0] Select one of 8 color from color LUT While 0 is special for transparent Add Byte0 [6] as MSB for 16-color LUT. Once we fill 0000 or 1000(MSB follow Byte0[6]), BG appears transparent.
5:3	W	Foreground color 10 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.
2:0	W	Foreground color 01 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.

Character command (For 4-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	01 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	(for Byte1[7] = 0) select one color from 16-color LUT as background (for Byte1[7] = 1) Red color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)

Byte 1

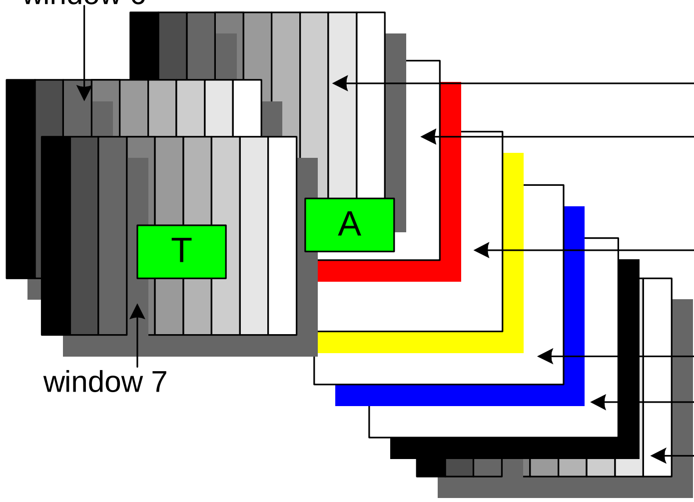
Bit	Mode	Function
7	W	0: 4bit Look Up Table, 0000'b is transparent. 1: 3bit specify R,G,B pattern, color level defined in Byte0[3:0],Byte2. One mask bit defines foreground or background.
6:0	W	Character Select [6:0]

- When 4-bit look-up table mode，color of column space is the same as background.

- When 4-bit look-up table mode and pixel value is 0000, and byte0[3:0]=0000 means transparent.
- When true color mode and pixel value is 0000，it is transparent。

Byte 2

Bit	Mode	Function
7:4	W	(for Byte1[7] = 1) Green color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)
3:0	W	(for Byte1[7] = 1) Blue color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)

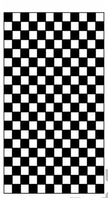


Display Priority

We have four windows with gradient and four windows without gradient, the window priority is as above, character should be always on the top layer of the window.

Pattern gen.
Use OSD to replace display pattern generator.

Chess Board: make a font as below



If we want to fill to the full 1280x1024 screen with character, we need 1280*1024 pixels. Required character is:

Using 12*18 font

1280/12 = 106.7 -> 107

1024/18 = 56.9 -> 57

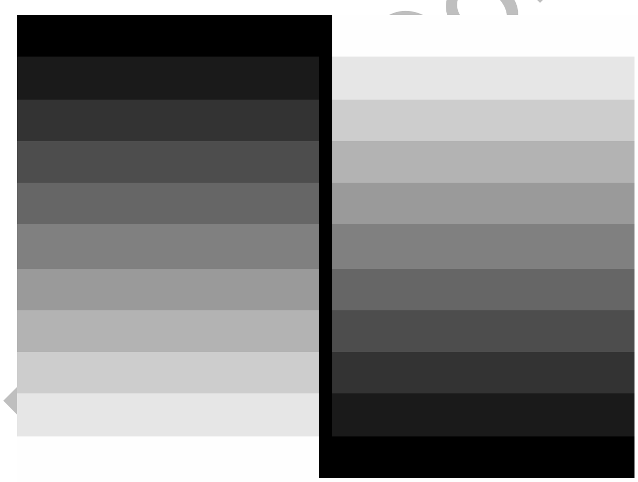
107*57 = 6099 character

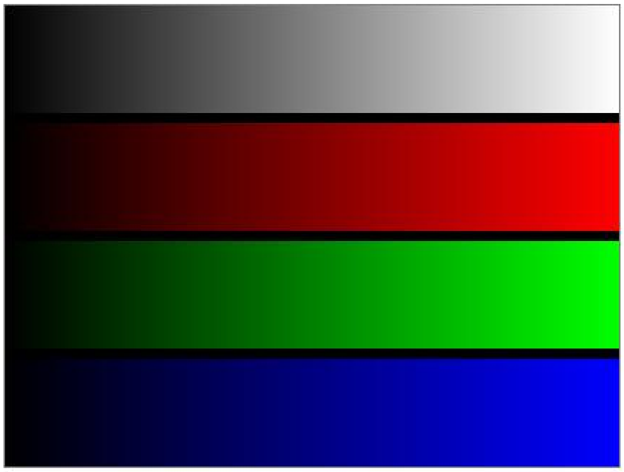
The required number of character map is larger than RAM size. We must turn on double width or double height function to reduce the half of character map.

So the basic unit to chessboard is 2x2 pixel. You can use larger chessboard instead of 2x2 pixels unit, such as 4x4 and so on.

Gray level

We can display 256 gray level by gradient window, 8 and 16 gray level by character map. 32 and 64 gray level is not supported.





7. Electric Specification

DC Characteristics

Table 2 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerant)	V_{IN}	-1		5.5	V
Voltage on Output or I/O or NC	V_{IO}	-1		4.6	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Junction Acceptable Temperature	T_j			125	ºC
Storage temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	θ_{JA}			47.4 ＊	ºC/W

＊

Under 2-layer PCB

Dimension 50 x 70 mm,

Thickness: 1.6mm

Top layer: 65% coverage of Cu, 0.5oz thickness

Bottom layer: 95% coverage of Cu, 0.5oz thickness

Via Underneath Package: 12 (Diameter: 12 mil)

Table 3 DC Characteristics/Operating Condition

(0℃<TA<70℃ ; VDD = 3.3V ± 0.3V)

WSXGA Panel

VGA IN:1600*1200@75Hz

DVI IN:1280*1024@85Hz

Display Clock:168MHz

Regulators=1.94V

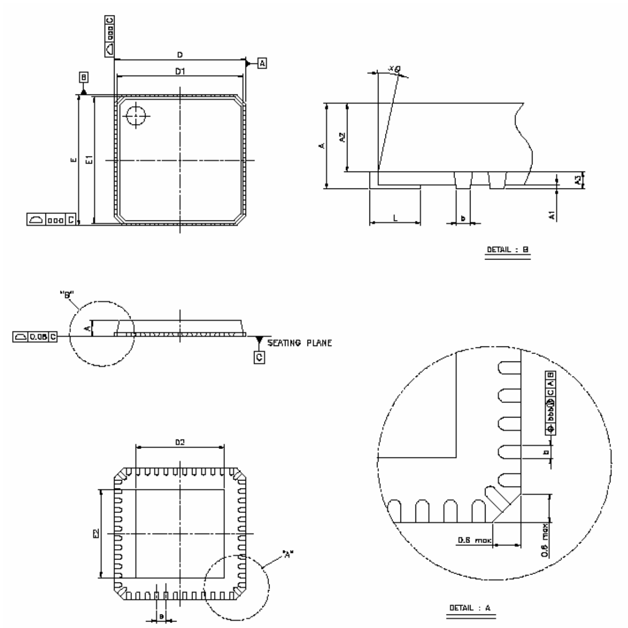
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	VDD	3.0	3.3	3.6	V
Supply Current(All function on at 168M)					mA
● Digital Power	I_{DVCC}		340(LVDS)		
● ADC Power	I_{ADC_VDD}		113.5		
● TMDS Power(VGA input)	$I_{TMDS\_VDD\_V}$		38.2		
● TMDS Power(DVI input)	$I_{TMDS\_VDD\_D}$		137.6		
Supply Current(Power Saving)					mA
● Digital Power	I_{DVCC}		3.0		

● ADC Power ● TMDS Power(VGA input) ● TMDS Power(DVI input)	I_{ADC_VDD} $I_{TMDS\_VDD\_V}$ $I_{TMDS\_VDD\_D}$		1.7 13.1 (Z0-ON) 1.5 (Z0-OFF) 13.1 (Z0-ON)		
Output High Voltage	V_{OH}	2.4		VDD	V
Output Low Voltage	V_{OL}	GND		0.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
I/O Pull-up resistance	R_{PU}	100		300	Ω
I/O Pull-down resistance	R_{PD}	50		150	Ω
Input Leakage Current(VI=VCC or GND)	I_{LI}	-10		+10	μA
Output Leakage Current(VO=VCC or GND)	I_{LO}	-20		+20	μA

.

8. Mechanical Specification

48 Pin QFN



SSYMBO	MILLIMETER			INCH		
L	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	---	0.20	---	---	0.008	---
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
D2	2.25	4.70	5.25	0.089	0.185	0.207
E	7.00 BSC			0.276 BSC		
E1	6.75BSC			0.266 BSC		
E2	2.25	4.70	5.25	0.089	0.185	0.207
b	0.18	0.23	0.30	0.007	0.009	0.012
e	0.50 BSC			0.020 BSC		
TH	0o	---	12o	0o	---	12o
L	0.3	0.4	0.5	0.012	0.016	0.020
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
Chamfer	---	---	0.60	---	---	0.024

TITLE: QFN-48 (7.0x7.0x1.6mm)		
PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	
CHECK	DWG NO	
	DATE	
REALTEK SEMICONDUCTOR CORP.		

9. Ordering Information

The available RTD2545L series pin compatible products listed below:

Part Number	ADC	DVI	HDCP	Resolution	Output	Package
RTD2545L-LF	210MHz	Yes	No	UXGA/WSXGA+	LVDS	48 QFN
RTD2045L-LF	210MHz	No	No	UXGA/WSXGA+	LVDS	48 QFN
RTD2545LH-LF	210MHz	Yes	Yes	UXGA/WSXGA+	LVDS	48 QFN
RTD2525LH-LF	165MHz	Yes	Yes	SXGA/WXGA+	LVDS	48 QFN

* lead free packages are available for above items with suffix –LF.