Discrete Controller Design for High Voltage DC-DC Converter

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Mechanical Engineering

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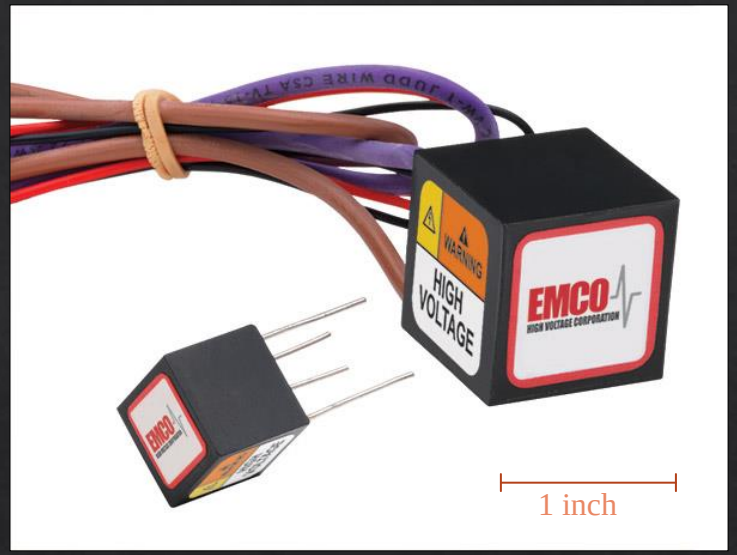
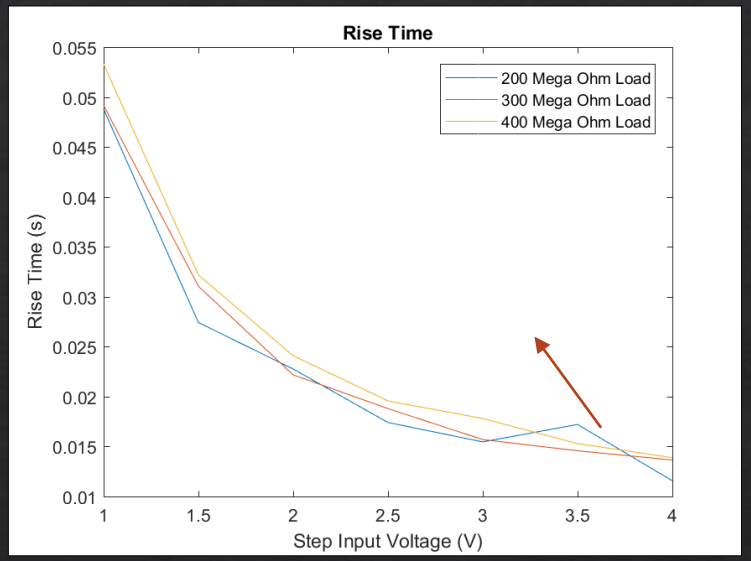
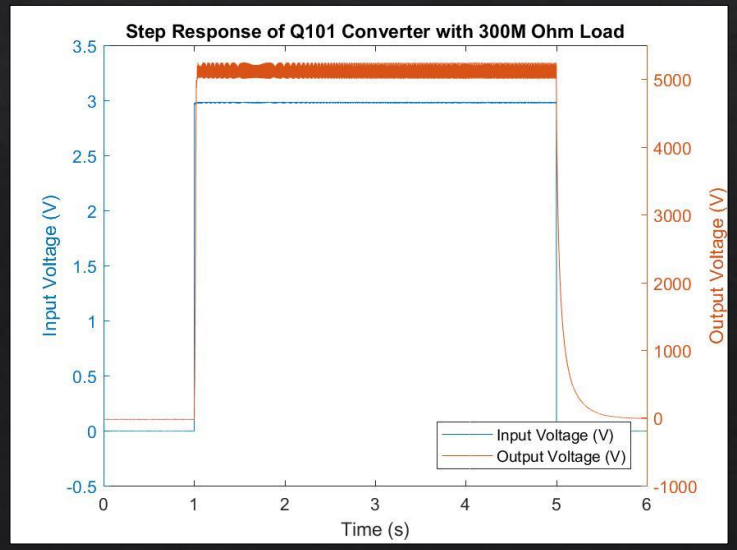
Open-loop Step Response for Q101 Converter

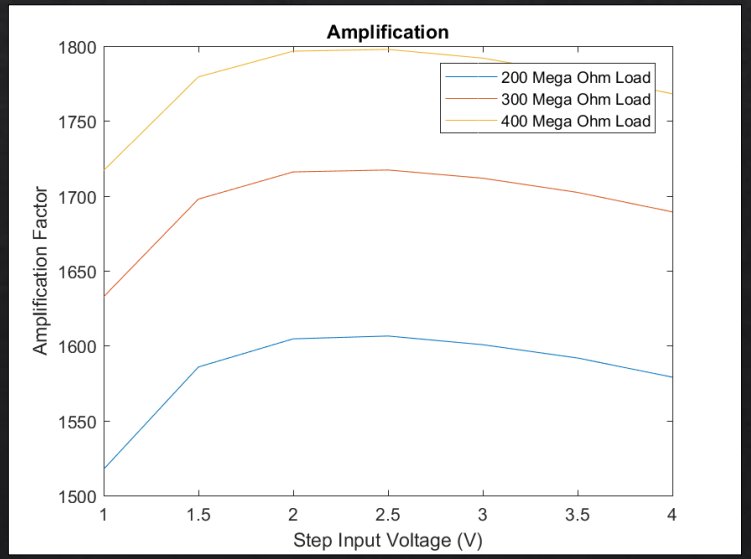
Conclusion:

1. Converter never achieves amplification factor of 2000
2. The more current drawn, the smaller the amplification factor
3. DC-DC converter behaves nonlinearly, and worse when the input voltage is less than 1.5V









Controller Design Requirement

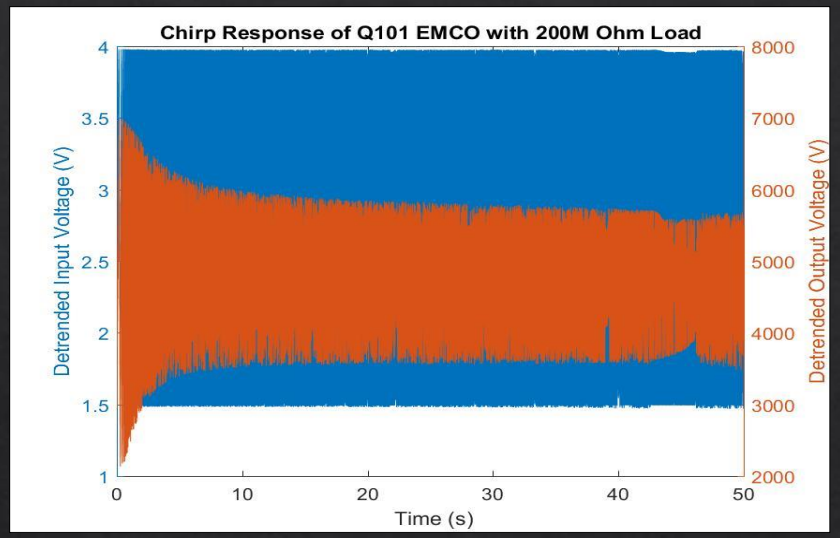
Desired step response characteristics:

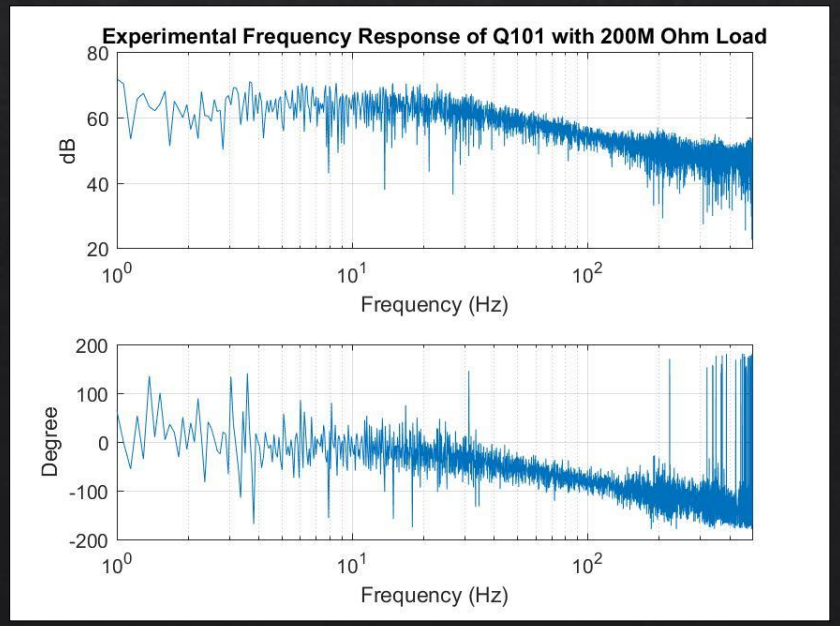
- HASEL actuator must be able to operate at 5Hz, so the converter rise time < 50ms
- Voltage arcing and charge built-up in HASEL must be completely avoided, so the closed loop overshoot <1%
- Precision control of the actuator's stretch state, so steady state error must be < 1%

Assumption:

- DC-DC Converter is an LTI system
- Load is only resistive load, no capacitive load concerned
- Voltage Ripple is not modelled

Dynamical Response of Q101 Converter





Information:

- Sampling Frequency: 4000Hz
- Chirp Range: 0.1Hz – 1000Hz
- Chirp Duration: 50 second
- PK-PK input signal: 1.5-4V Sine Wave
- Data collected for both 200M Ohm and 300M Ohm loads

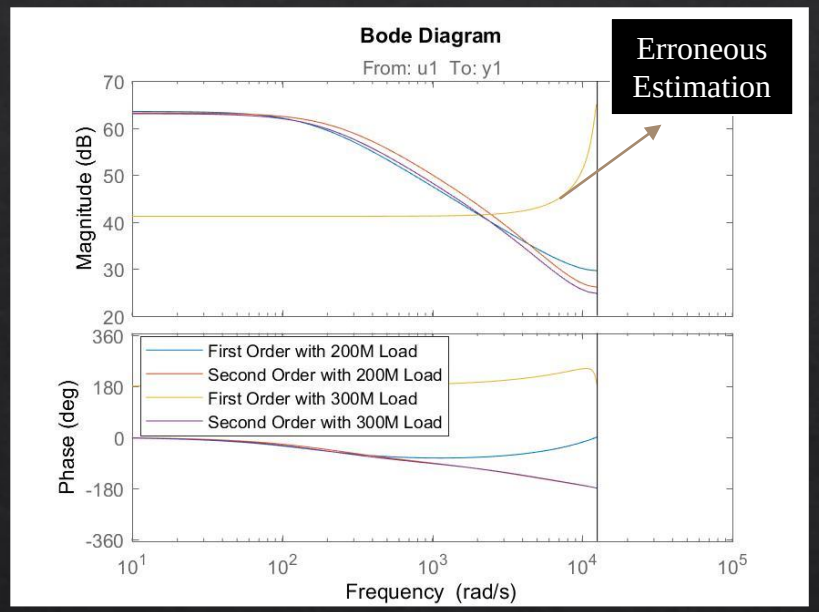
Observation

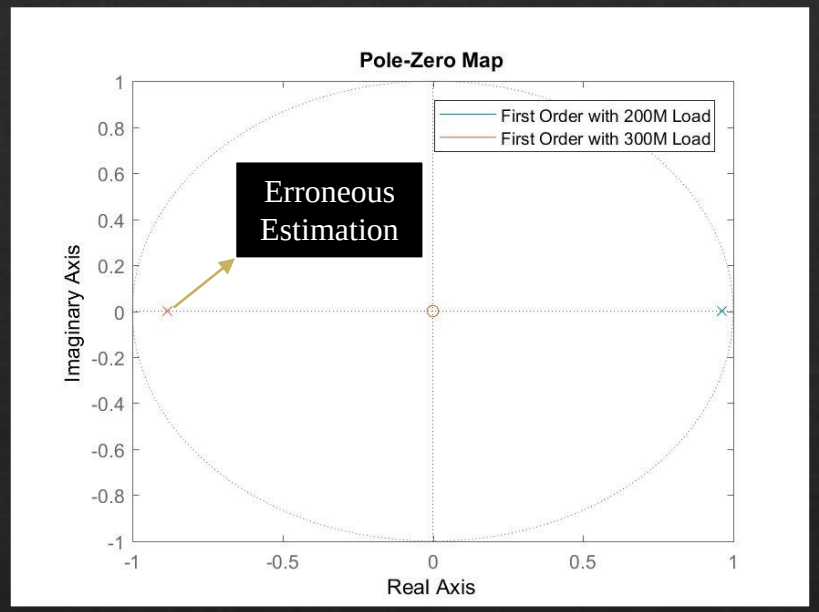
- Relatively flat magnitude bode at low Hz
- Roll-off rate is approximately 15dB/Decade
- Staring Phase: 0 degree
- Ending Phase: 120 degree

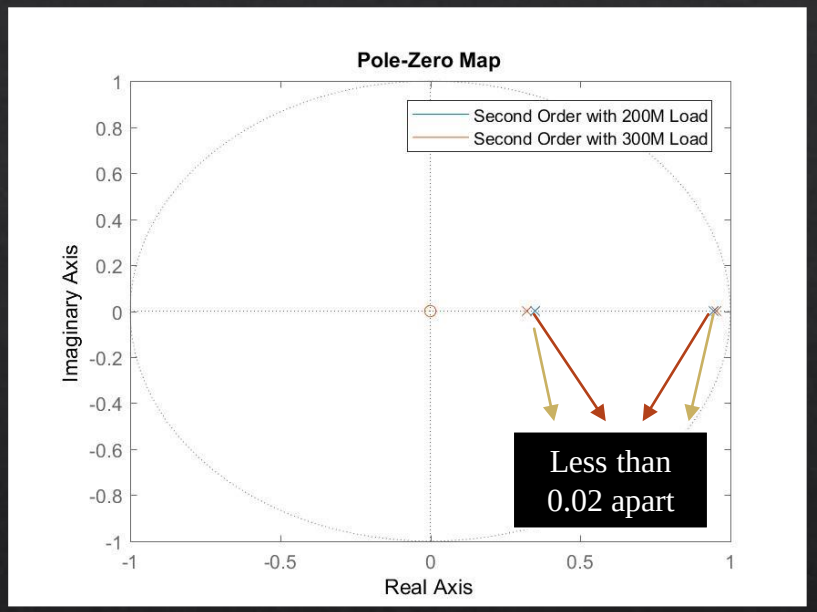
→ Prediction in continuous time:

- First order system with no zero
- Overdamped second order System with one zero

Discrete Estimated Bode Diagram and Pole-Zero Map







Observation:

Matlab discrete bode estimation is accurate for all cases except the first order system with 300M Ohm load.

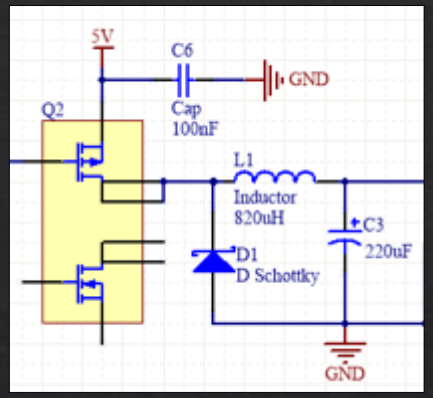
This leads to erroneous pole mapping on pzmap

There are no significant distinction between the pole and zero locations for both loading configuration

➡ Use estimated 1st and 2nd order transfer functions of the Q101 converter under 200M Ohm load

Mathematical Models of Converters

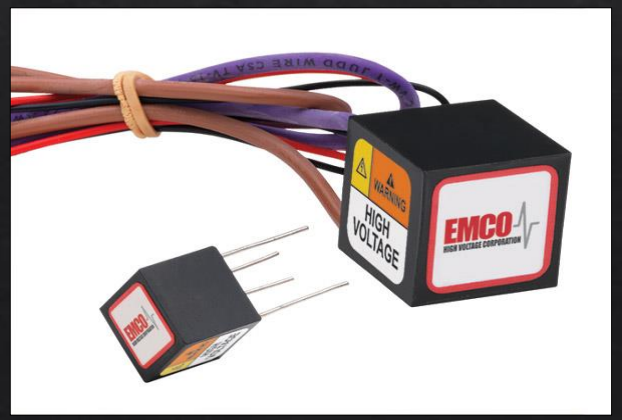
Buck Converter



$$\begin{bmatrix} \frac{d}{dt}u_c \\ \frac{d}{dt}i_L \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{c} \\ -\frac{1}{L} & -\frac{R_C + R_L}{L} \end{bmatrix} * \begin{bmatrix} u_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{c} \\ \frac{Vg}{L} & \frac{R_c}{L} \end{bmatrix} * \begin{bmatrix} d \\ i_R \end{bmatrix}$$

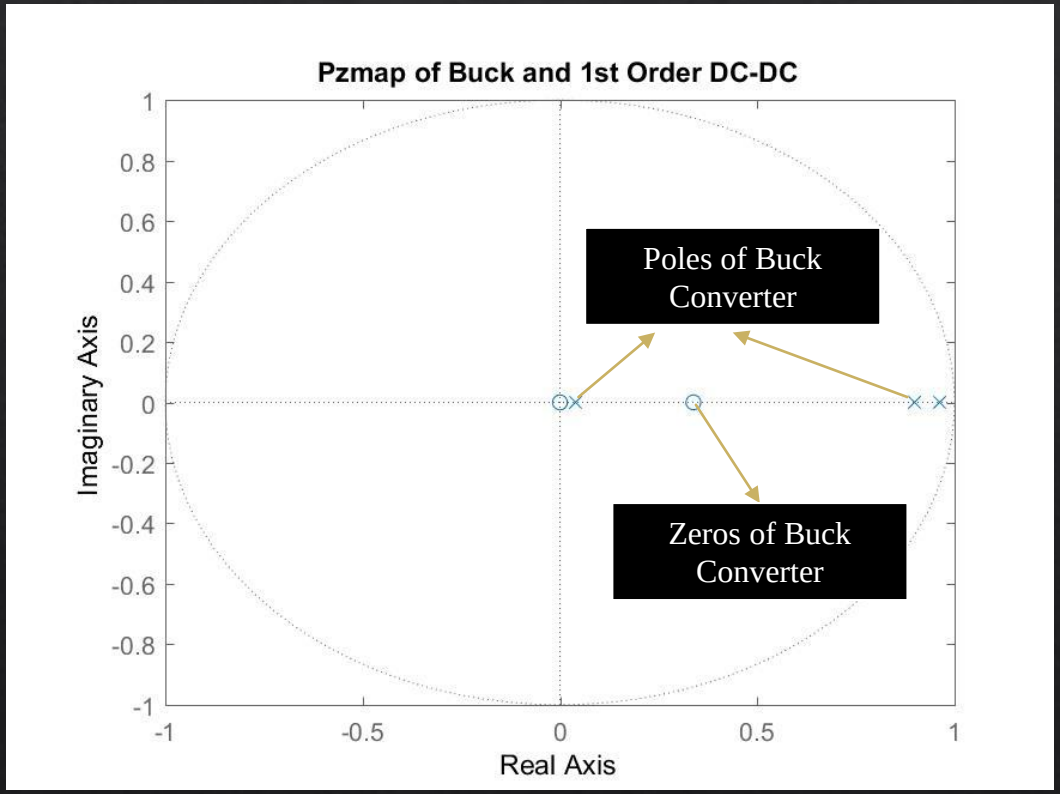
$$\begin{bmatrix} u_0 \\ i_L \end{bmatrix} = \begin{bmatrix} 1 & R_c \\ 0 & 1 \end{bmatrix} * \begin{bmatrix} u_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & -R_c \\ 0 & 0 \end{bmatrix} * \begin{bmatrix} d \\ i_R \end{bmatrix}$$

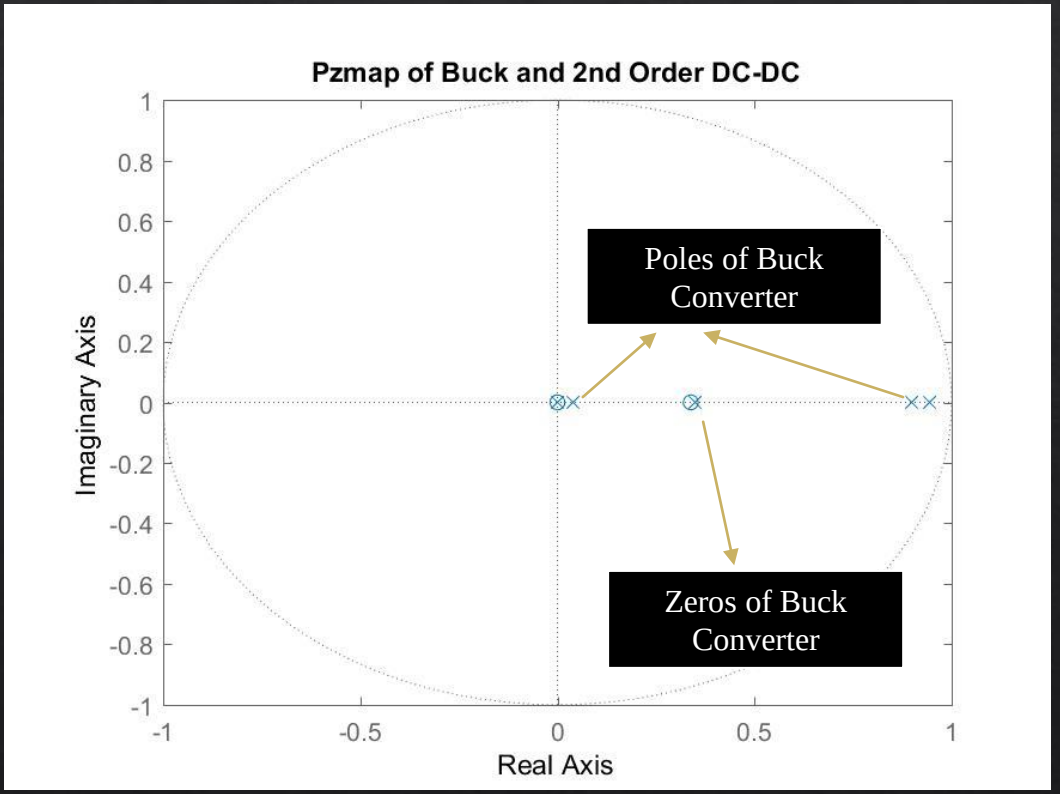
Q101 DC-DC Converter



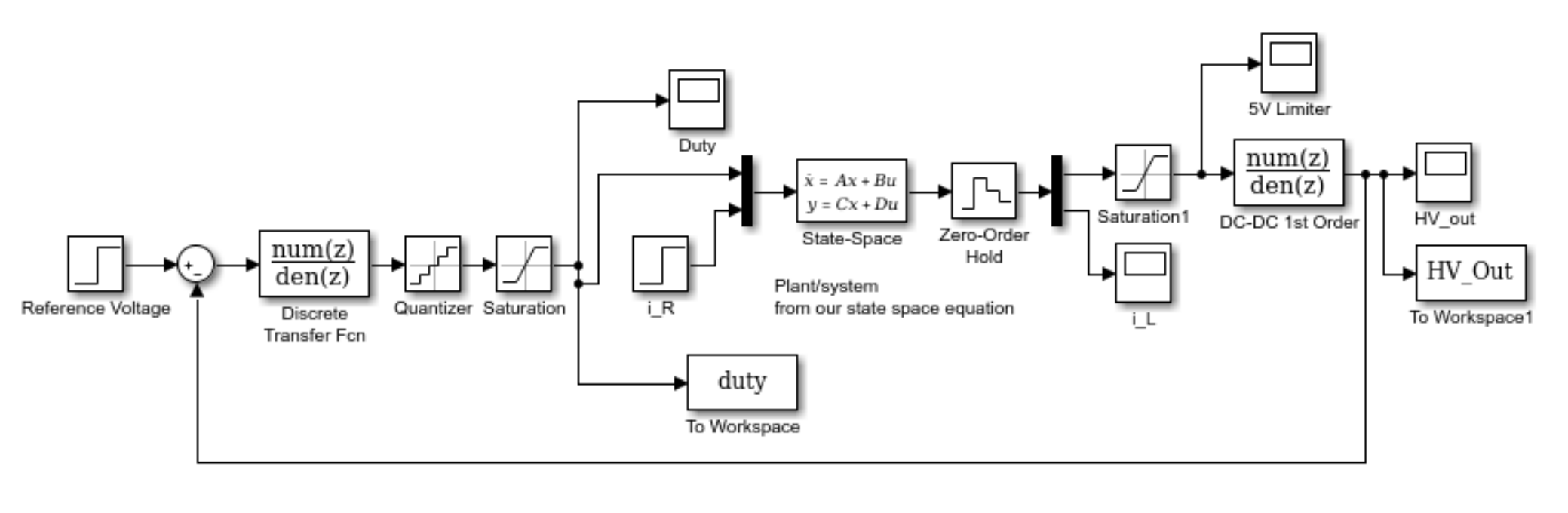
- DC-DC Converter 1st Order Approximated Transfer Function $\frac{59.11z}{z - 0.9606}$
- DC-DC Converter 2nd Order Approximated Transfer Function $\frac{52.71z^3}{z^4 - 1.292z^3 + 0.3287z^2}$

Pole-Zero Map of the Combined DC-DC Converter





Simulink Block Diagram



- Controller Saturation: duty cycle has the saturation range of 0-1
- Quantizer: microcontroller's duty cycle has 512 discrete steps between 0 and 1
- Buck Converter Output Saturation: 0-5V

Discrete Controller Design

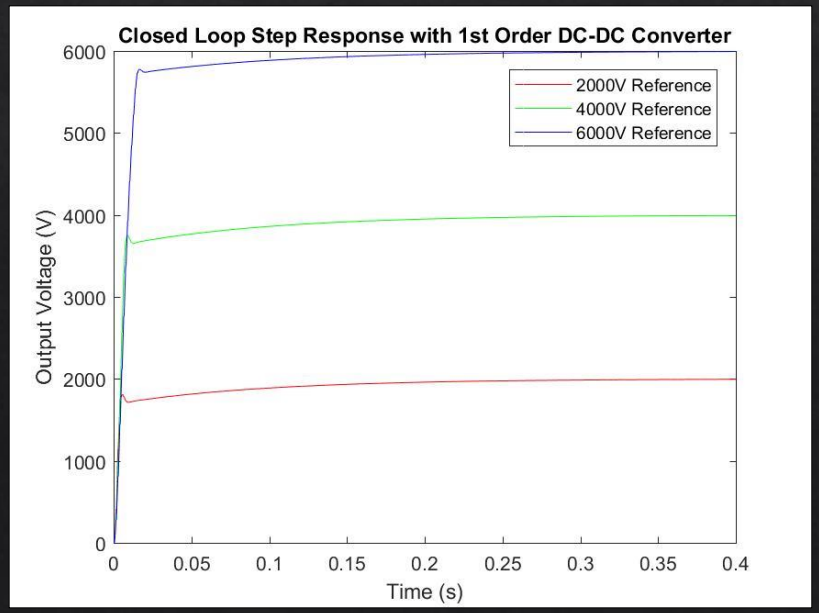
Conclusion:

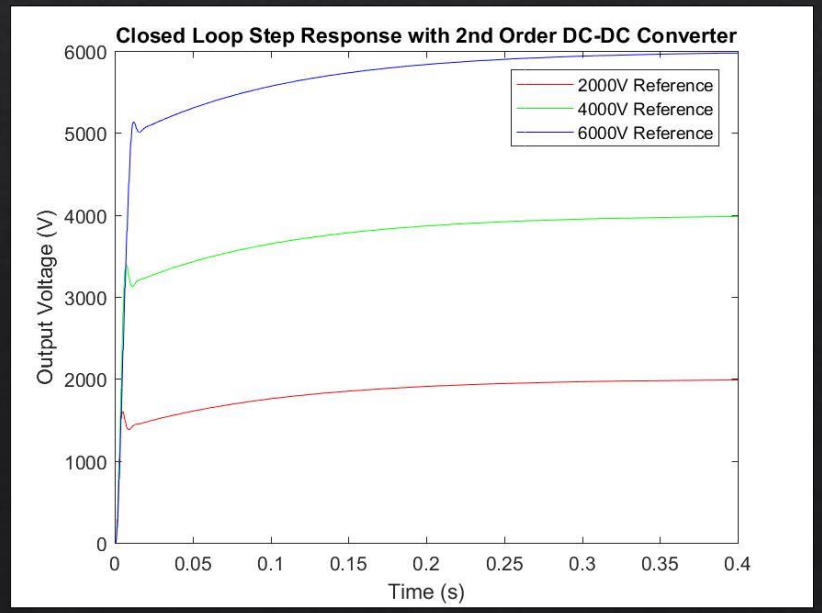
1. K was chosen first to stabilize the system
2. PD Controller decreases overshoot
3. PI Controller decreases steady state error

Controller Terms

1. K = 0.004 for 1st Order and 0.002 for 2nd Order
2. PD = $\frac{z - 0.7}{z}$
3. PI = $\frac{z - 0.9964}{z - 1}$

Closed Loop Characterization

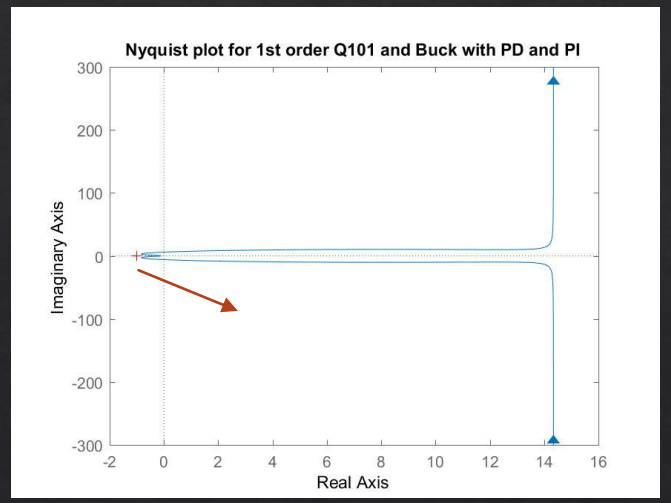


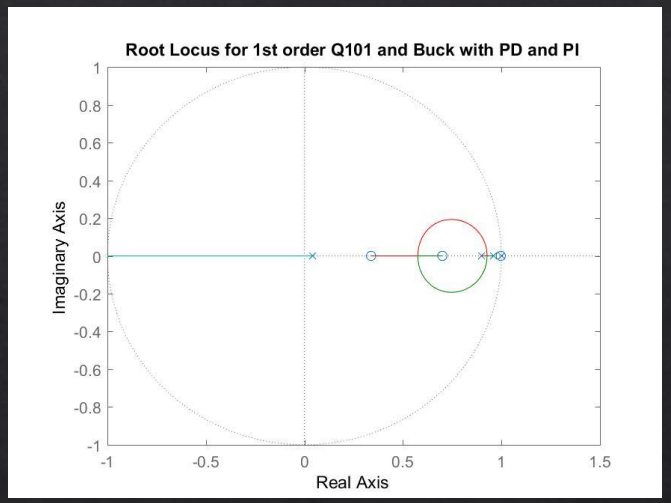


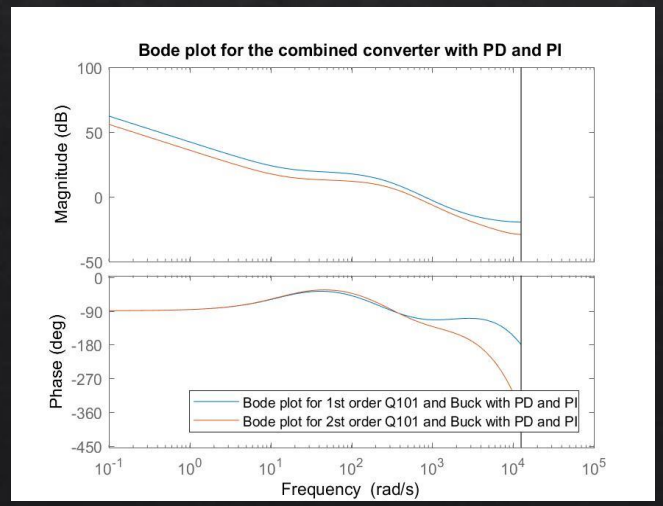
Stability and Control Analysis

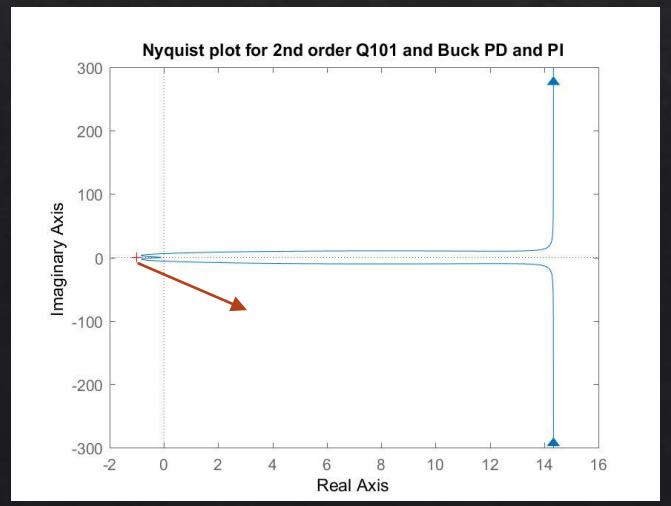
Controller Terms

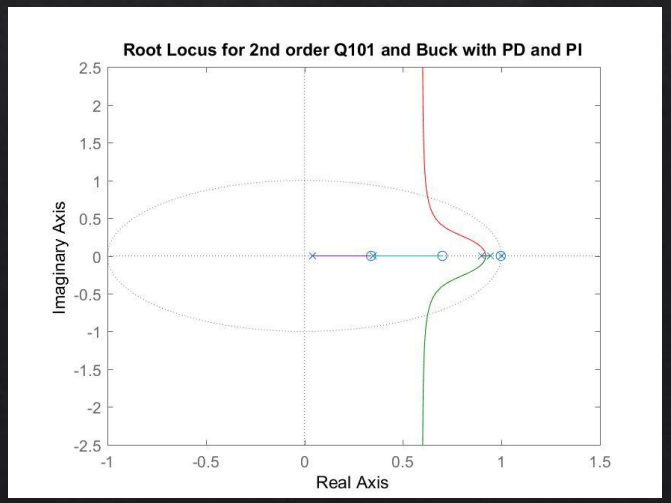
1. K = 0.004 for 1st Order and 0.002 for 2nd Order
2. PD = $\frac{z - 0.7}{z}$
3. PI = $\frac{z - 0.9964}{z - 1}$



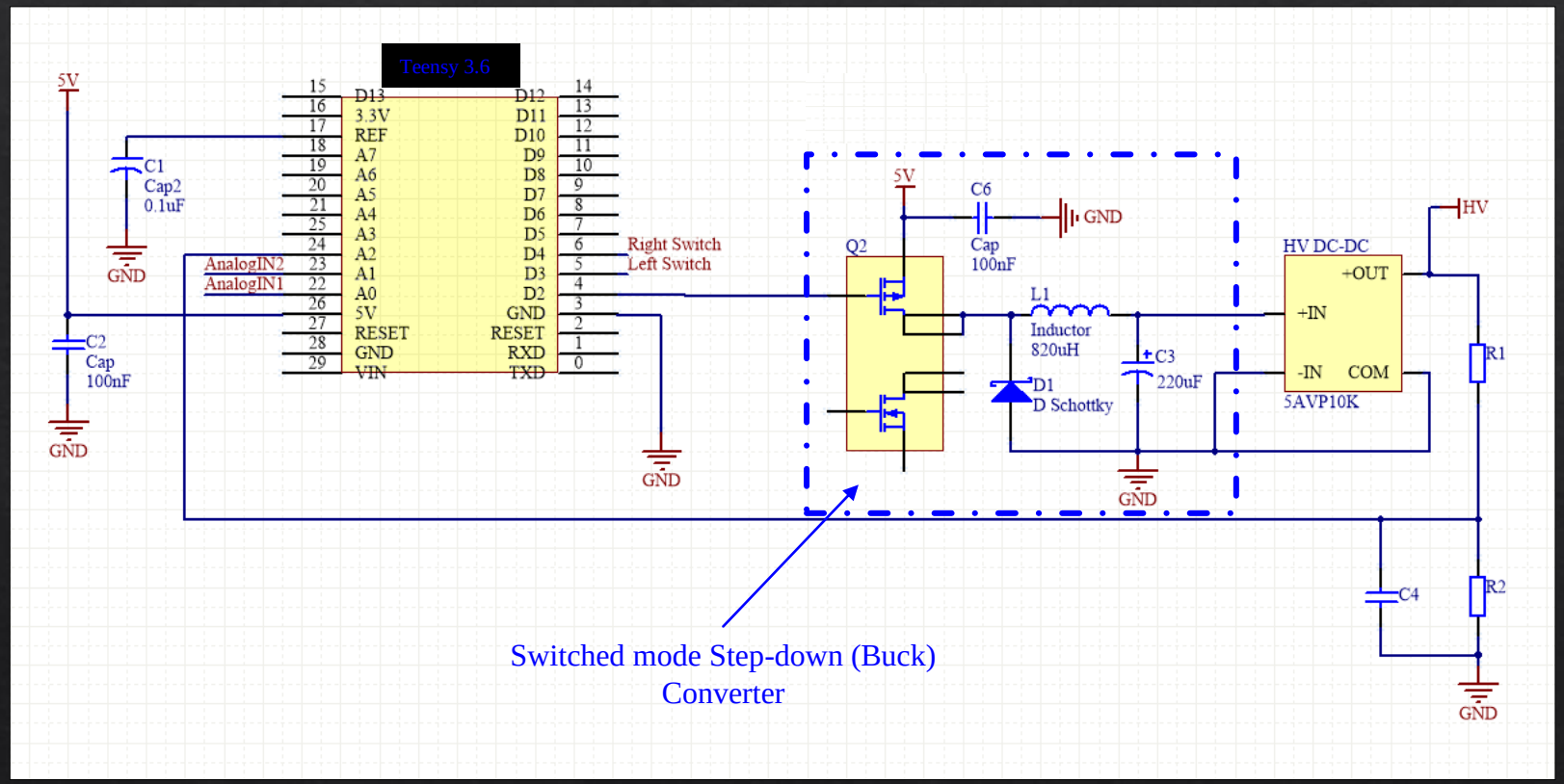








High Voltage Converter Controller Design



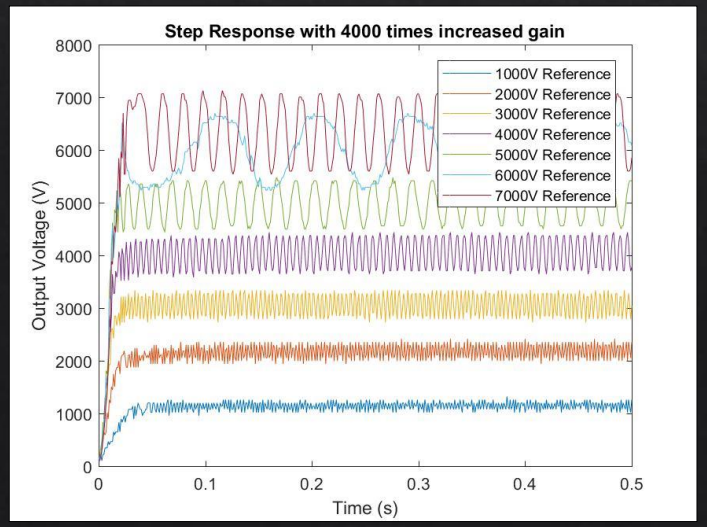
Information:

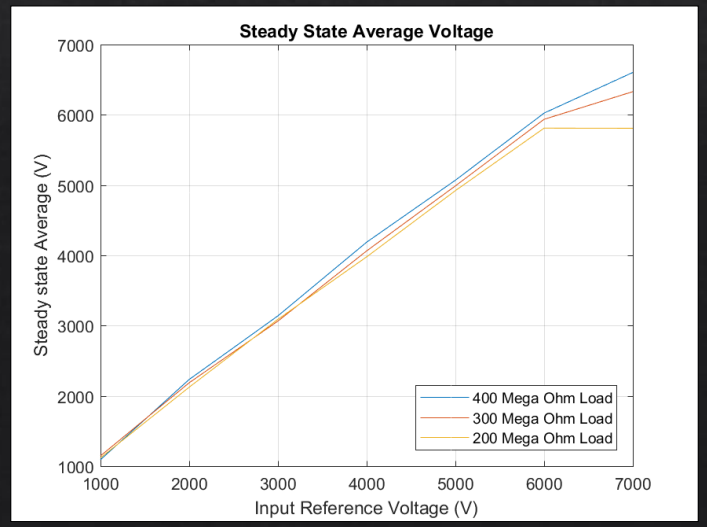
- ADC Sampling Rate: 4000Hz
- ADC Resolution: 512 steps
- PWM Quantization: 512 steps
- PWM Frequency: 100kHz

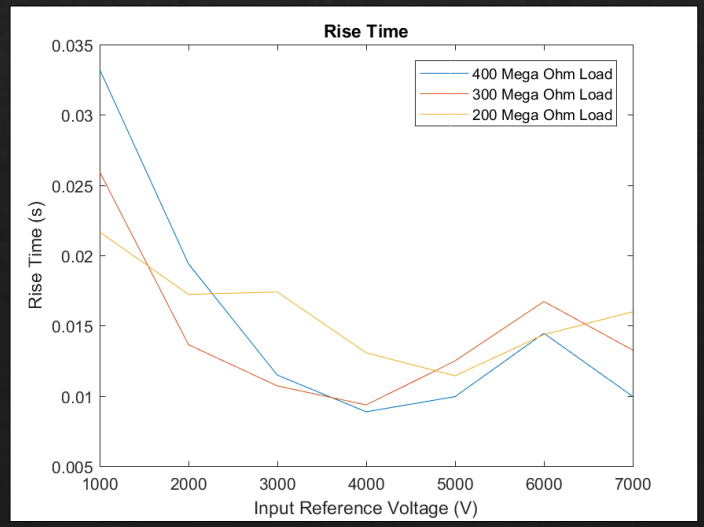
Experimental Closed Loop Step Response Analysis

Observation:

1. The higher the output voltage, the larger the voltage ripple
2. As predicted, maximum achievable output voltage for all load cases is 6kV
3. Steady state error is approximately 0
4. Overshoot is approximately 0
5. Rise time is less than 35 ms for all cases
6. Settling time is affected by voltage ripple. Need fast sampling and ripple filtering







Future Works

- Repeating chirp analysis to obtain better estimated mathematical model for the DC-DC converter
- Output voltage ripple rejection design
- Rise time, overshoot and steady state error closed loop analysis with capacitive load (HASEL actuator)