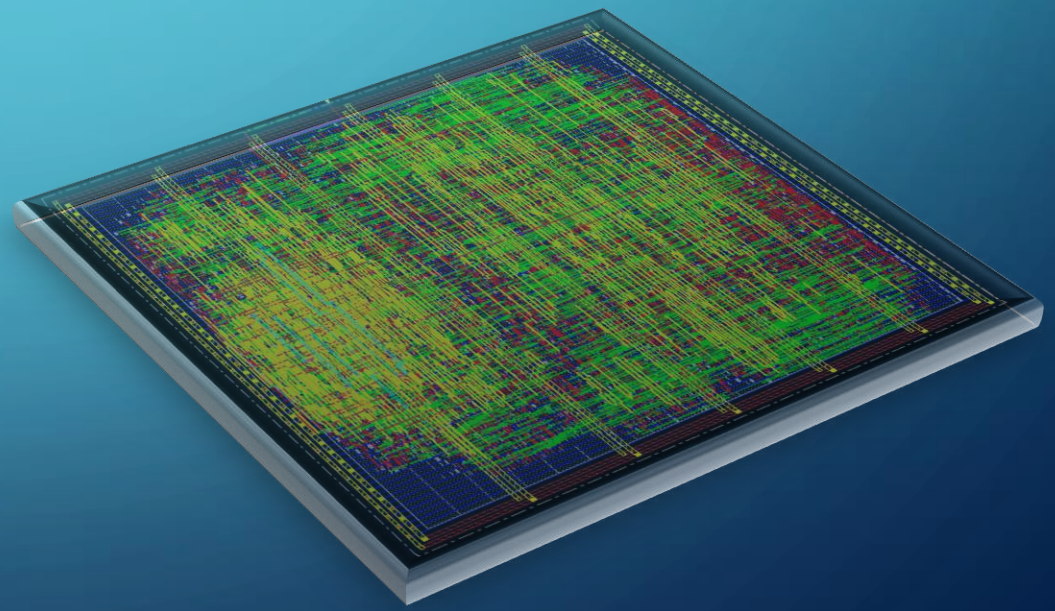
DLX MICROPROCESSOR

DALMASSO LUCA

GAI OMAR



OVERVIEW

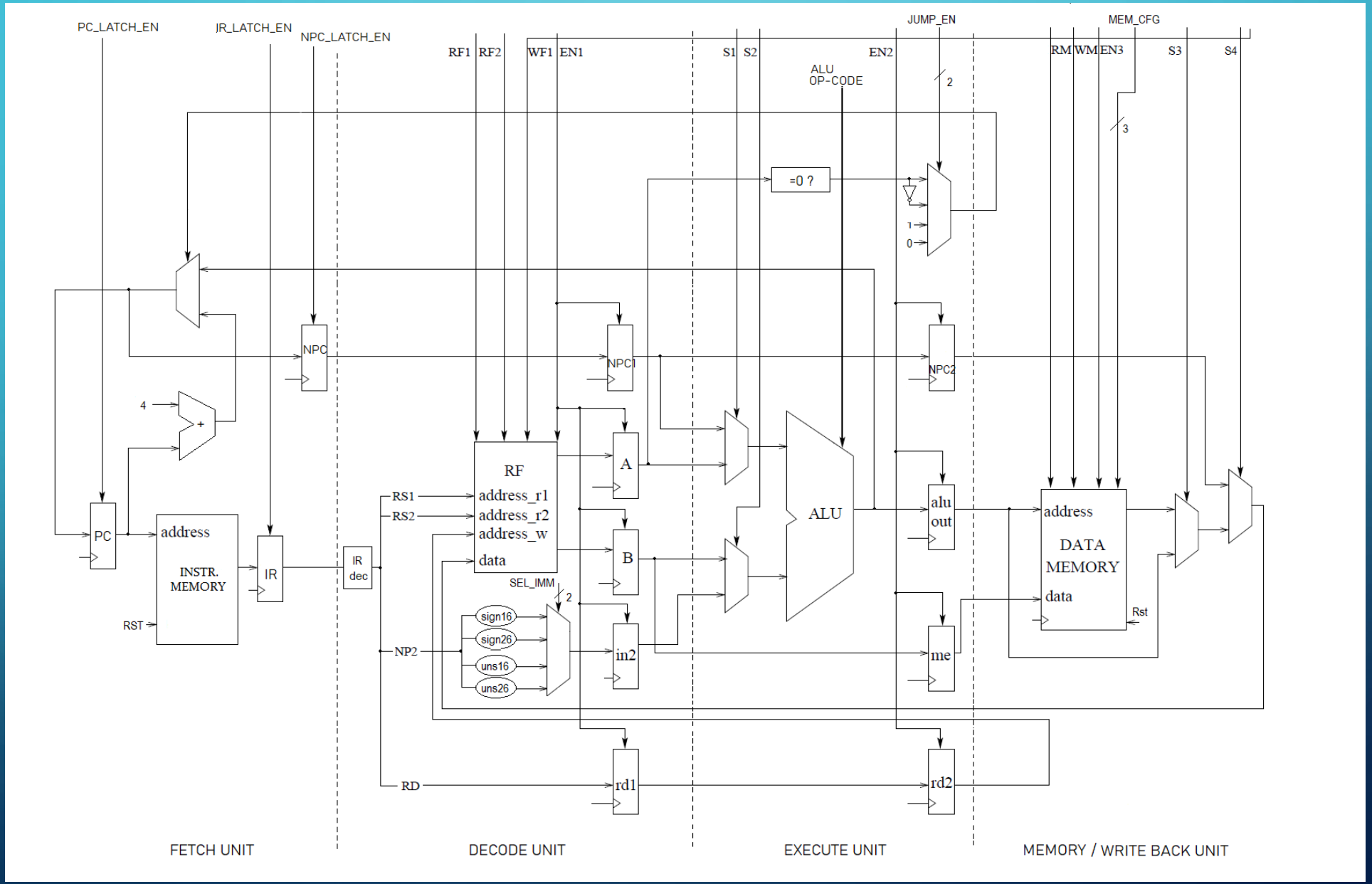
32-bit RISC Microprocessor

Pipelined Datapath with 4 stages

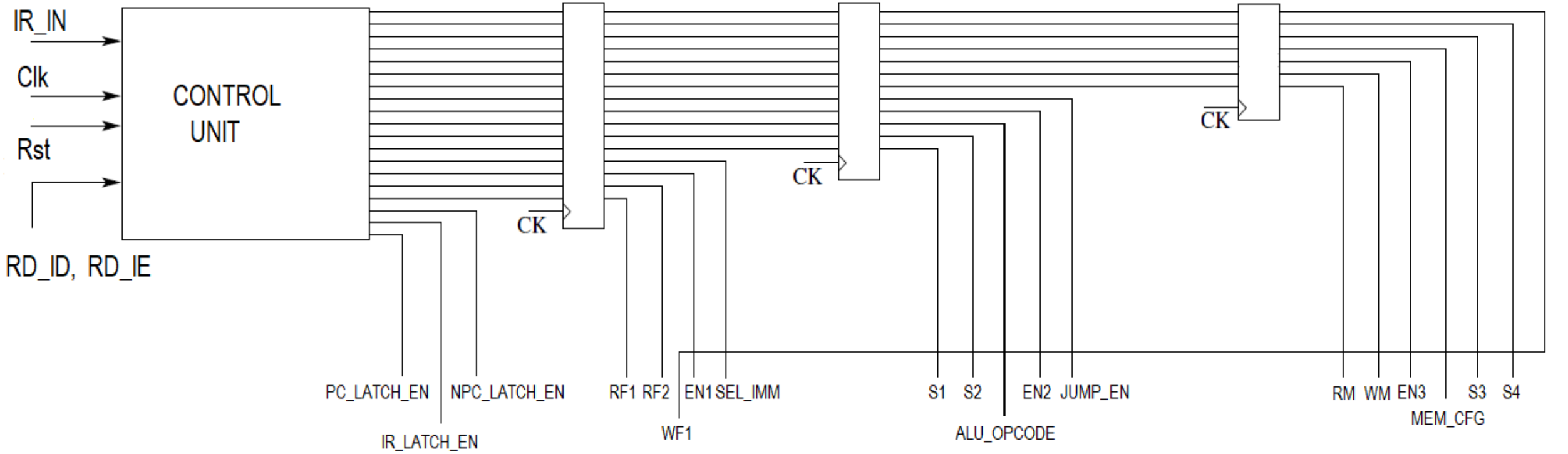
Hardwired Control Unit

Hazard detection FSM inside Control Unit for solving RAW Hazards

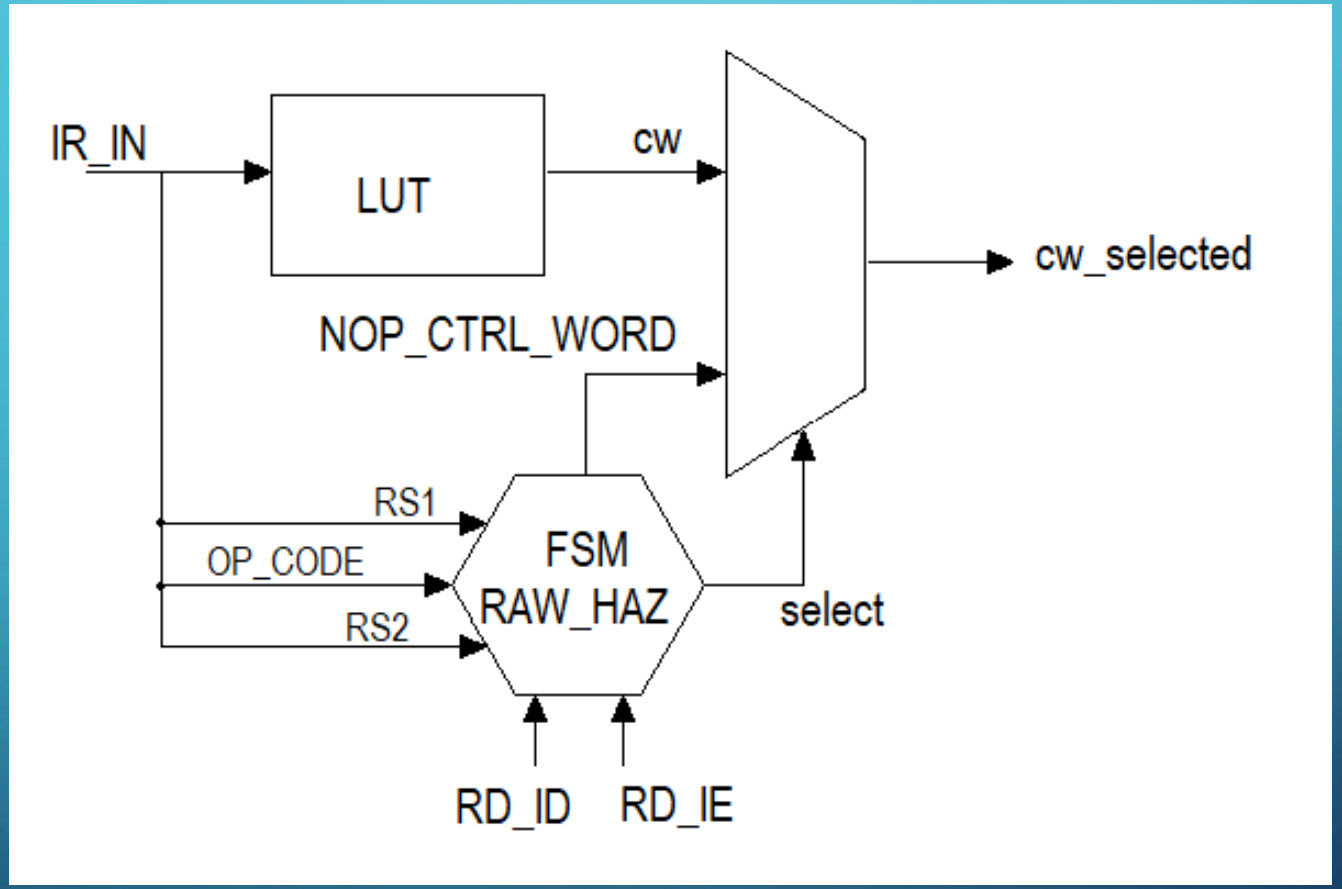
DATAPATH


PC_LATCH_EN
IR_LATCH_EN
NPC_LATCH_EN
RF1
RF2
WF1
EN1
S1
S2
ALU OP-CODE
EN2
JUMP_EN
2
MEM_CFG
RM
WM
EN3
3
S3
S4
=0 ?
1
0
NPC
NPC1
NPC2
4
+
RF
address_r1
address_r2
address_w
data
A
B
RS1
RS2
ALU
alu out
address
DATA MEMORY
data
Rst
PC
address
INSTR. MEMORY
RST
IR
IR dec
SEL_IMM
2
sign16
sign26
uns16
uns26
NP2
in2
me
RD
rd1
rd2
FETCH UNIT
DECODE UNIT
EXECUTE UNIT
MEMORY / WRITE BACK UNIT

CONTROL UNIT



INSIDE THE CONTROL UNIT



ADDITIONAL FEATURES W.R.T BASIC PROJECT

Management of unsigned operations

Addition of some jump instructions

Different load and store operations (byte and halfword)

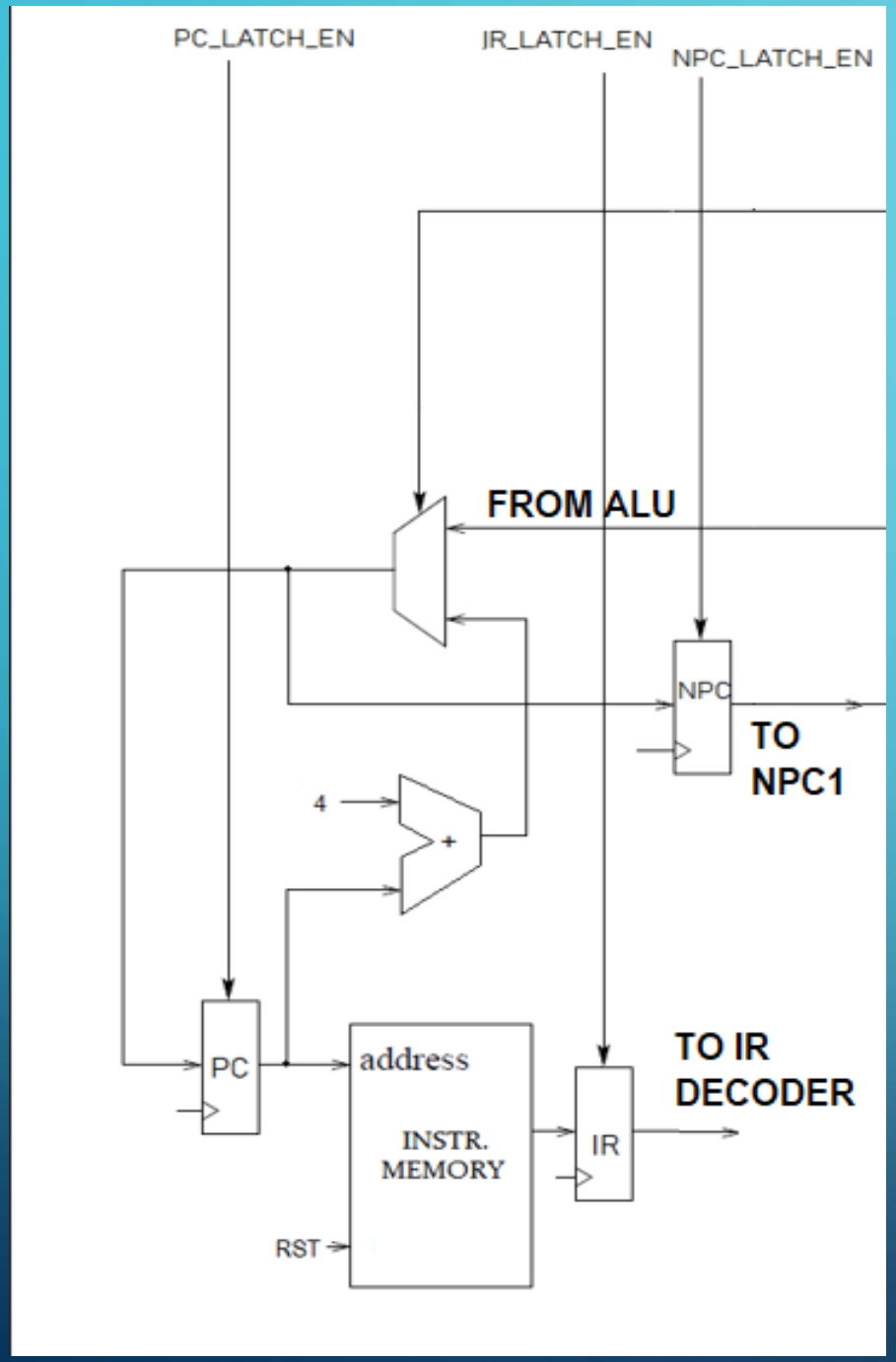
Additional arithmetic operations

ALU is optimized

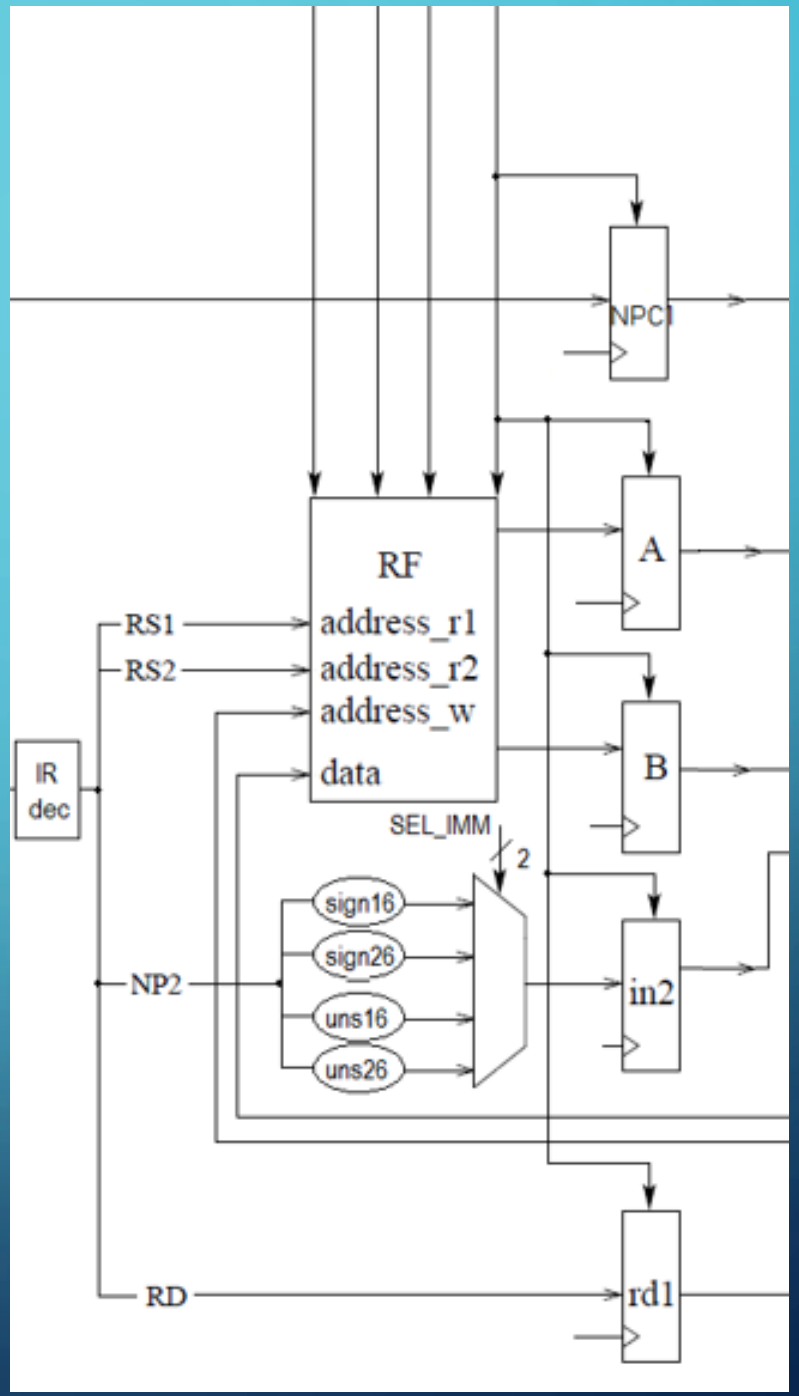
RAW Hazards detection

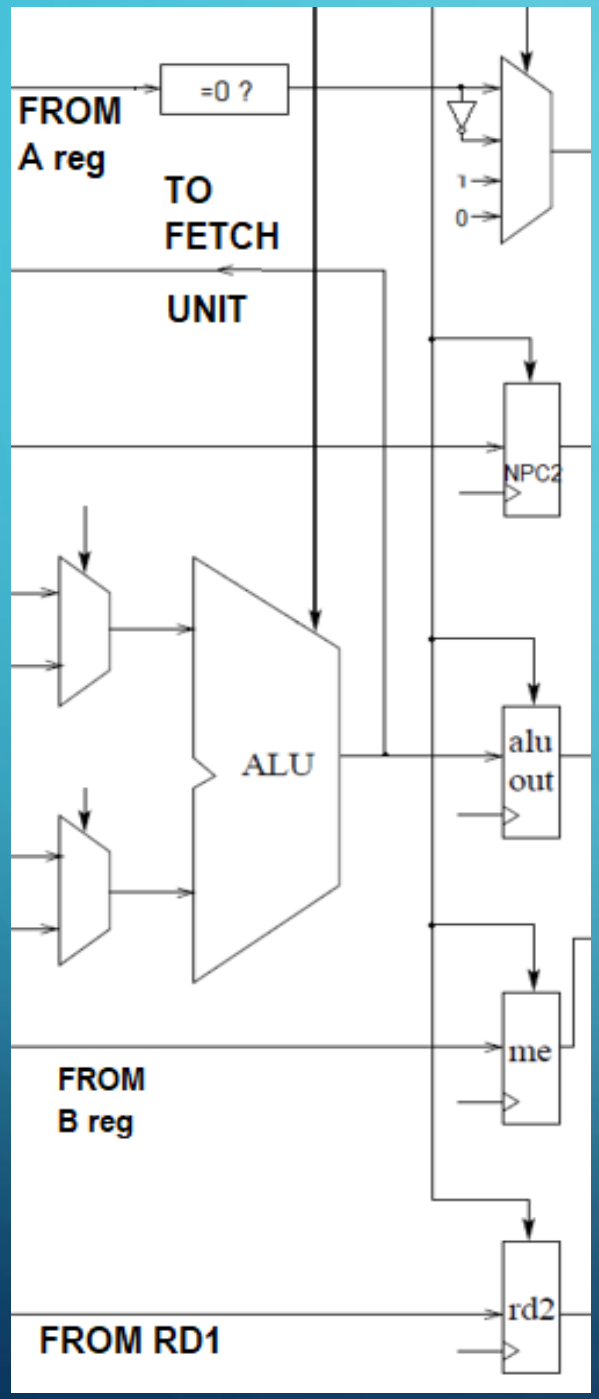
Scripts for automatic Compilation and Synthesis

FETCH UNIT


PC_LATCH_EN
IR_LATCH_EN
NPC_LATCH_EN
FROM ALU
NPC
TO
NPC1
4
+
PC
address
INSTR.
MEMORY
IR
TO IR
DECODER
RST

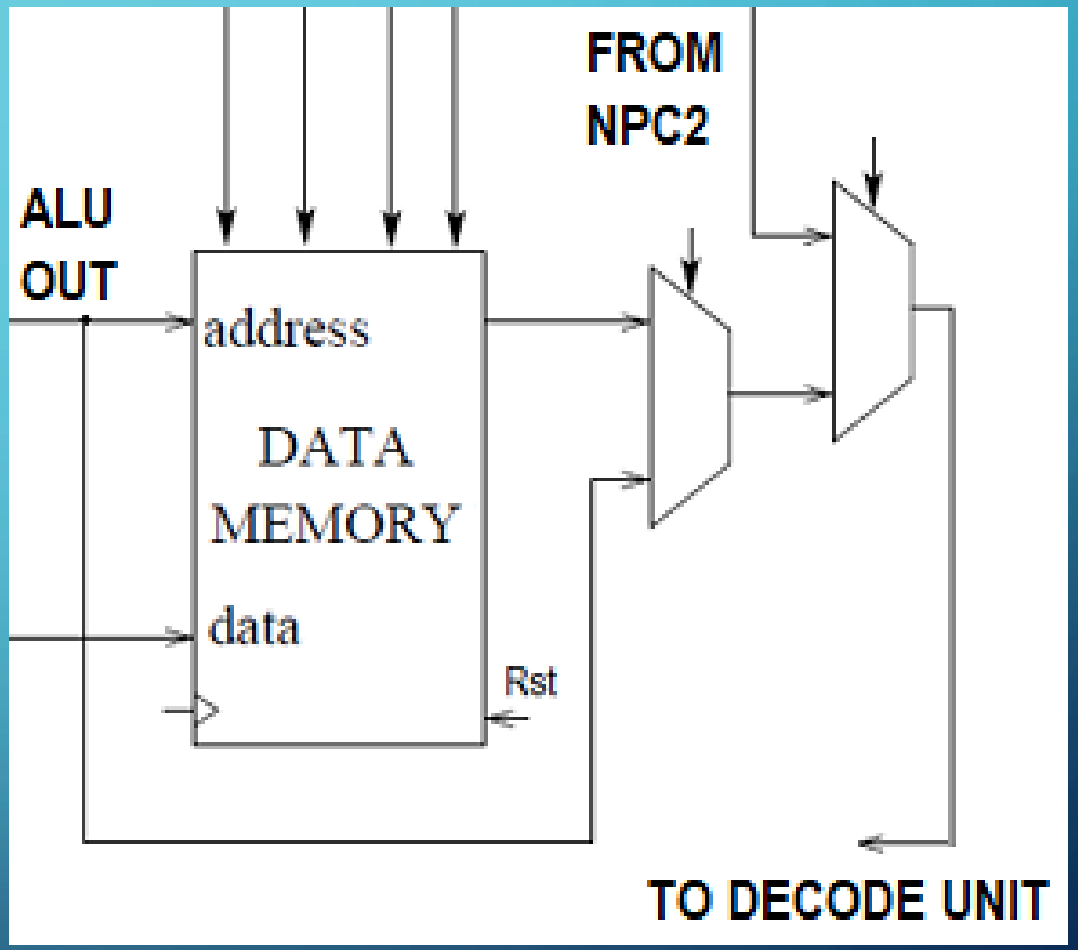
DECODE UNIT


NPC1
RF
address_r1
address_r2
address_w
data
A
B
RS1
RS2
IR
dec
SEL_IMM
2
sign16
sign26
uns16
uns26
NP2
in2
RD
rd1



EXECUTION UNIT

MEMORY UNIT


FROM
NPC2
ALU
OUT
address
DATA
MEMORY
data
Rst
TO DECODE UNIT