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**Lab YP1**

**The Serial Loader Flow**

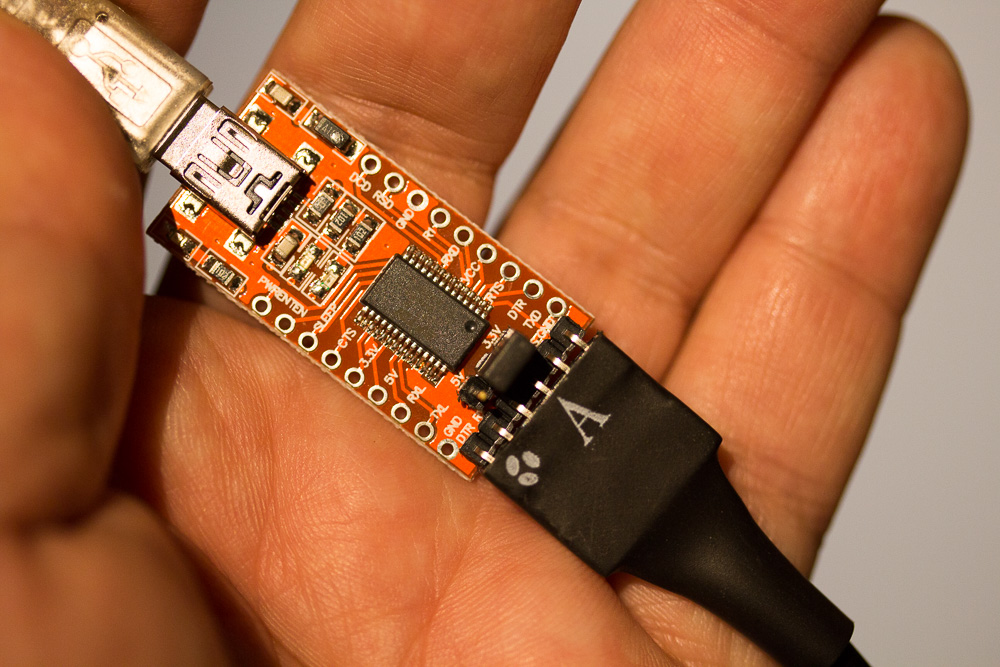


Loader Flow". This alternative flow does not require using [BusBlaster debugger board and OpenOCD software](http://blog.imgtec.com/mips-processors/bus-blaster-v3c-is-an-affordable-debug-probe-for-mips-cpus). While BusBlaster / OpenOCD

**Appendix A. More pictures for setting up Terasic boards with Altera Cyclone II, III, IV and V FPGA**

Some Terasic boards have USB-to-UART connector, for some other boards it is possible to use other interfaces, but for simplicity this lab uses external USB-to-UART connectors attached to general purpose I/O pins.

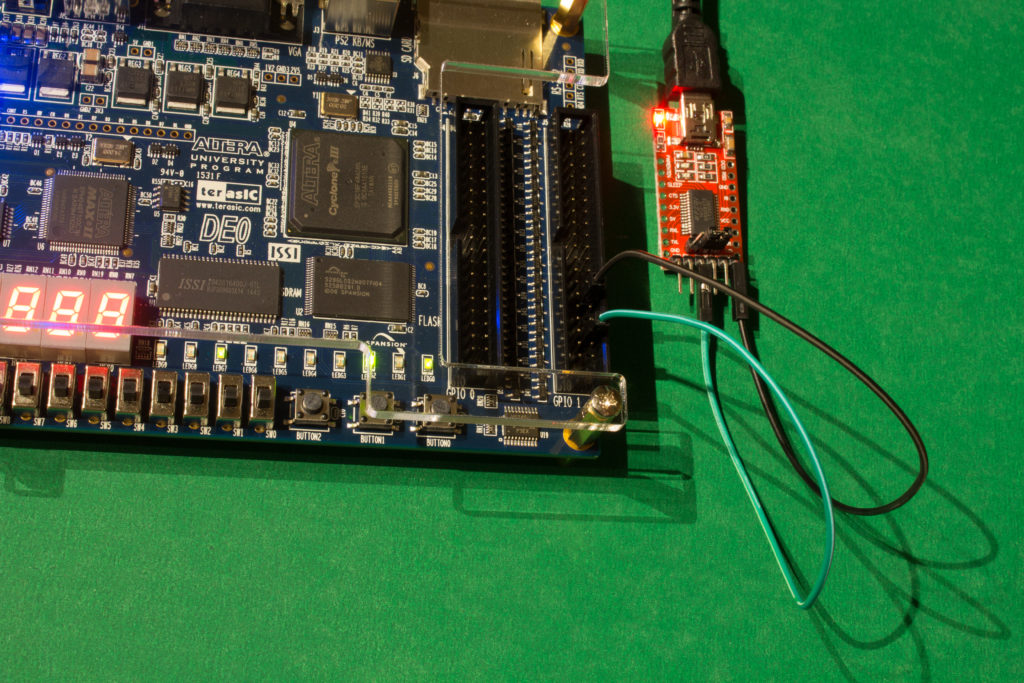
**Picture A.1.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/02/IMG_1423.jpg)

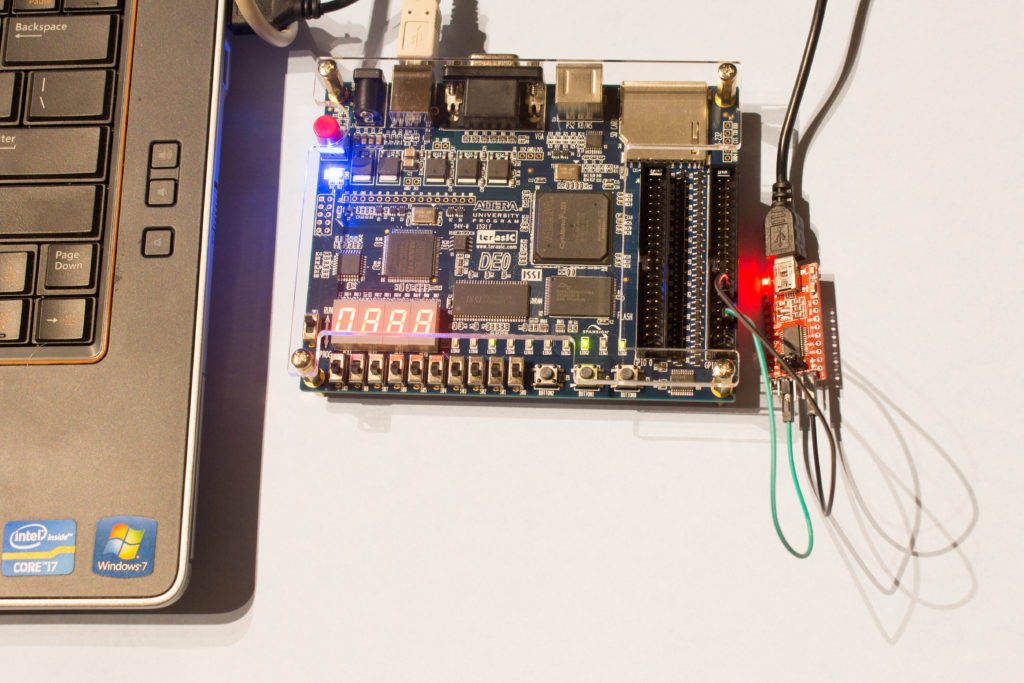
**Picture A.2.** Serial Loader is also compatible with [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable). There is another, alternative cable, based on [PL2303HX chip](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182718&SearchText=PL2303HX) however this cable has more compatibility problems with Windows 8.x and we recommend to use cables based on PL2303TA instead:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/pl2303ta_160926_175832.jpg)

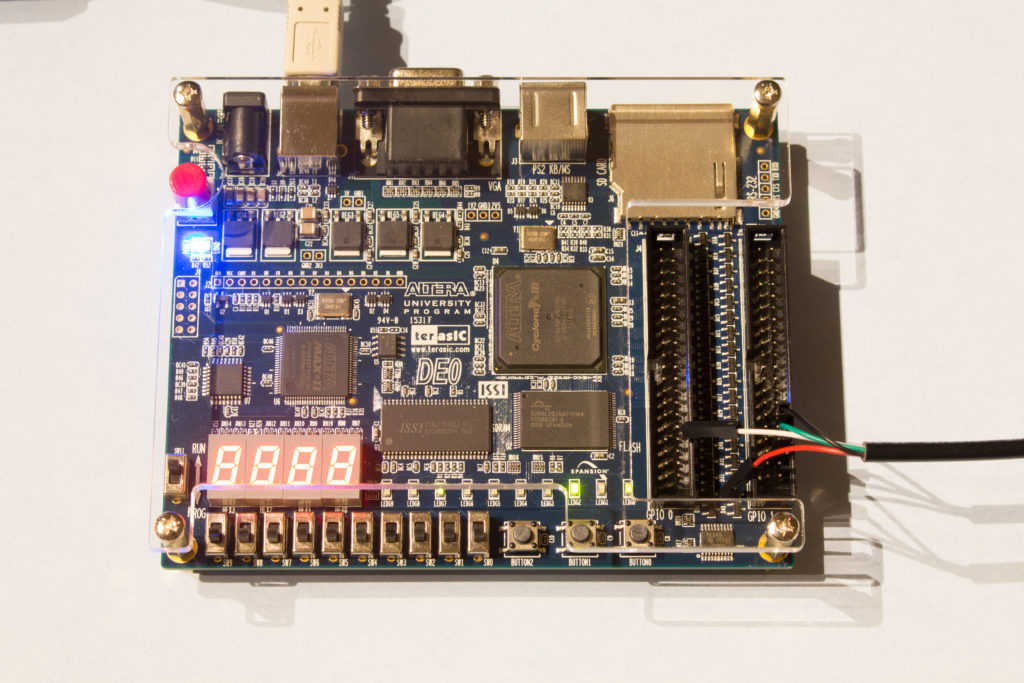
**Picture A.3.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0](http://de0.terasic.com) with Altera Cyclone III FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_and_ft232rl_160926_213603.jpg)

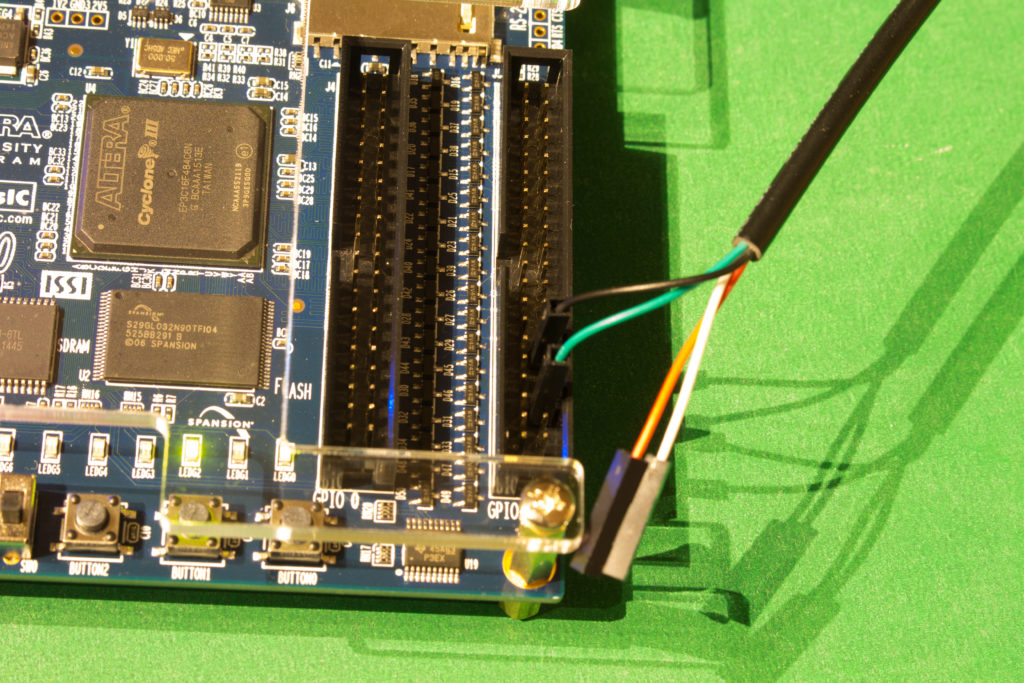
**Picture A.4.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0](http://de0.terasic.com) with Altera Cyclone III FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_and_ft232rl_160926_213705.jpg)

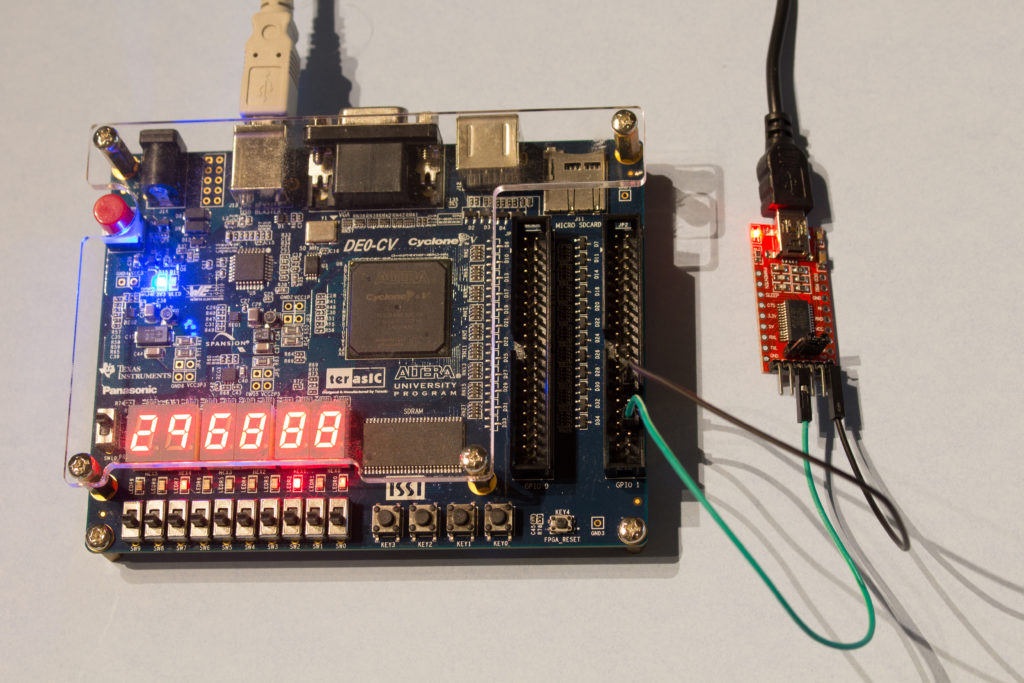
**Picture A.5.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE0](http://de0.terasic.com) with Altera Cyclone III FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_and_pl2303ta_160926_213033.jpg)

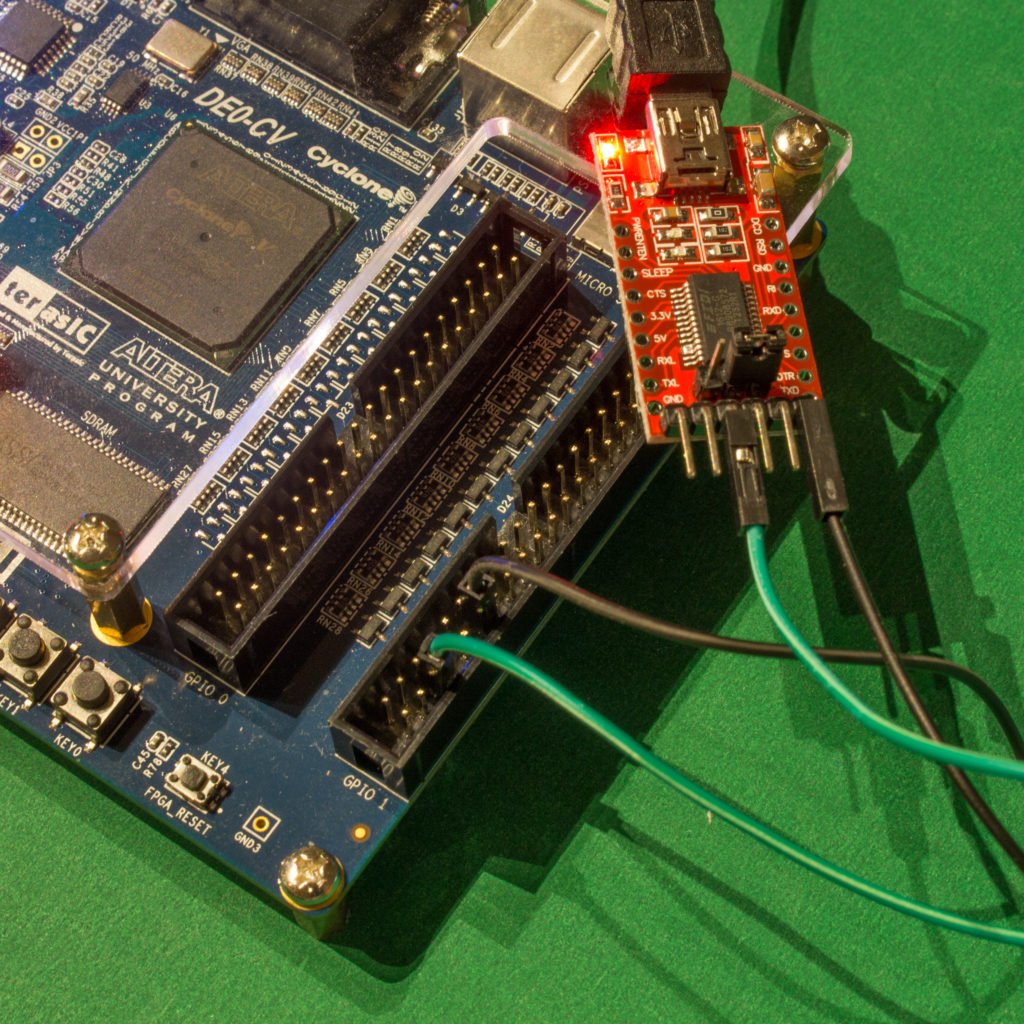
**Picture A.6.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE0](http://de0.terasic.com) with Altera Cyclone III FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_and_pl2303ta_160926_213338.jpg)

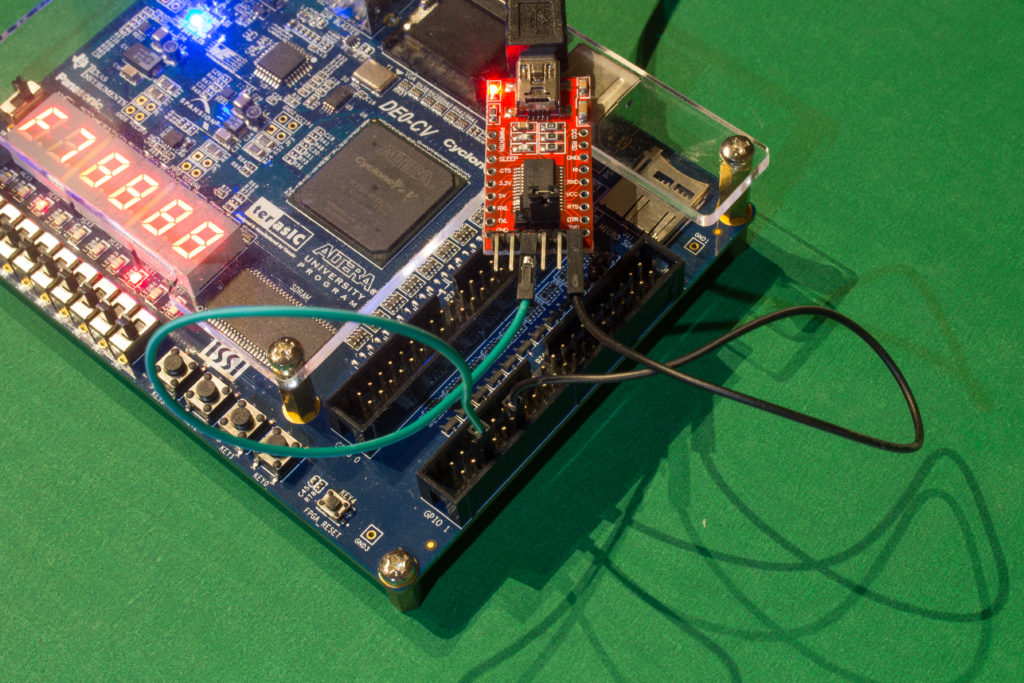
**Picture A.7.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0-CV](http://de0-cv.terasic.com.tw) with Altera Cyclone V FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_cv_and_ft232rl_160926_160527.jpg)

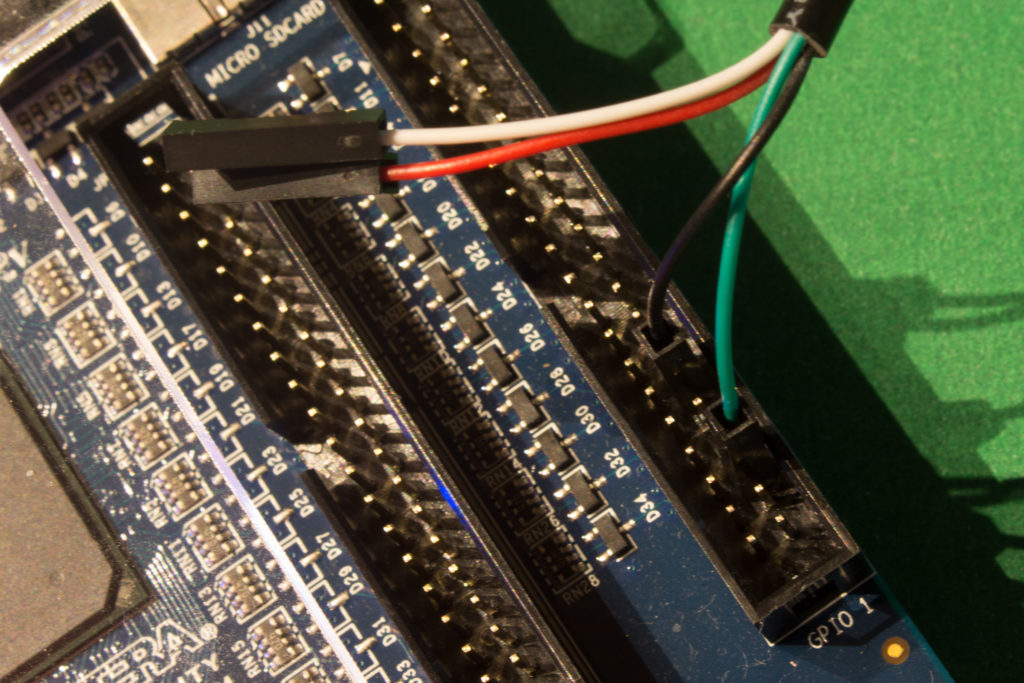
**Picture A.8.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0-CV](http://de0-cv.terasic.com.tw) with Altera Cyclone V FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_cv_and_ft232rl_160926_171948.jpg)

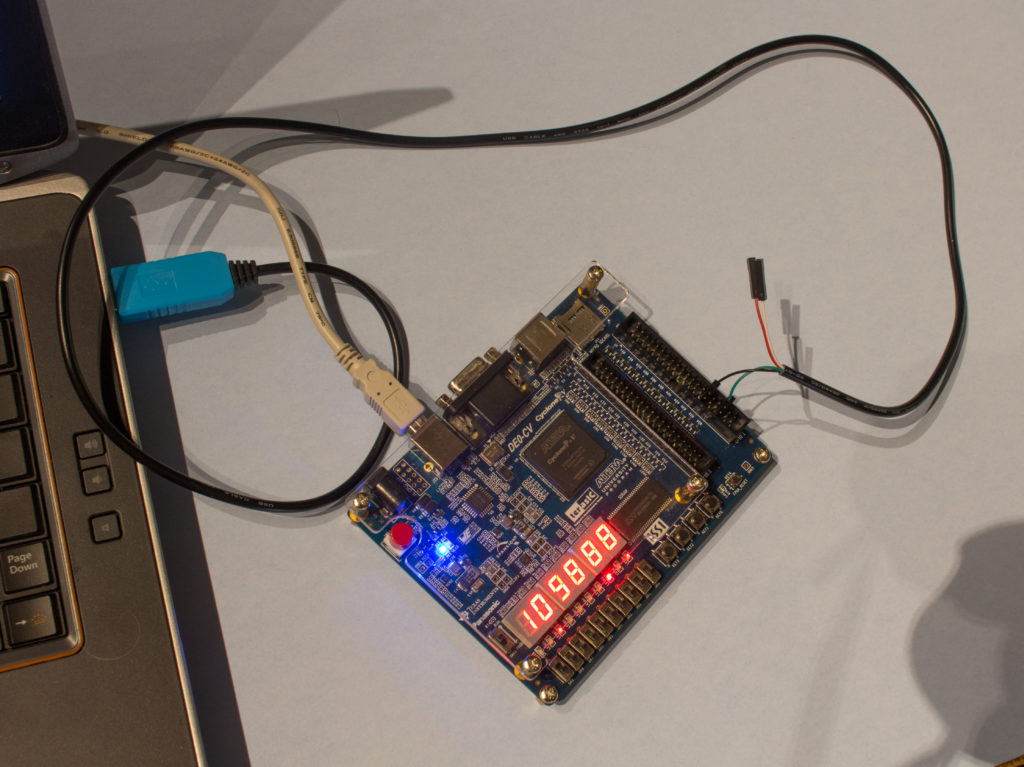
**Picture A.9.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0-CV](http://de0-cv.terasic.com.tw) with Altera Cyclone V FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_cv_and_ft232rl_160926_175703.jpg)

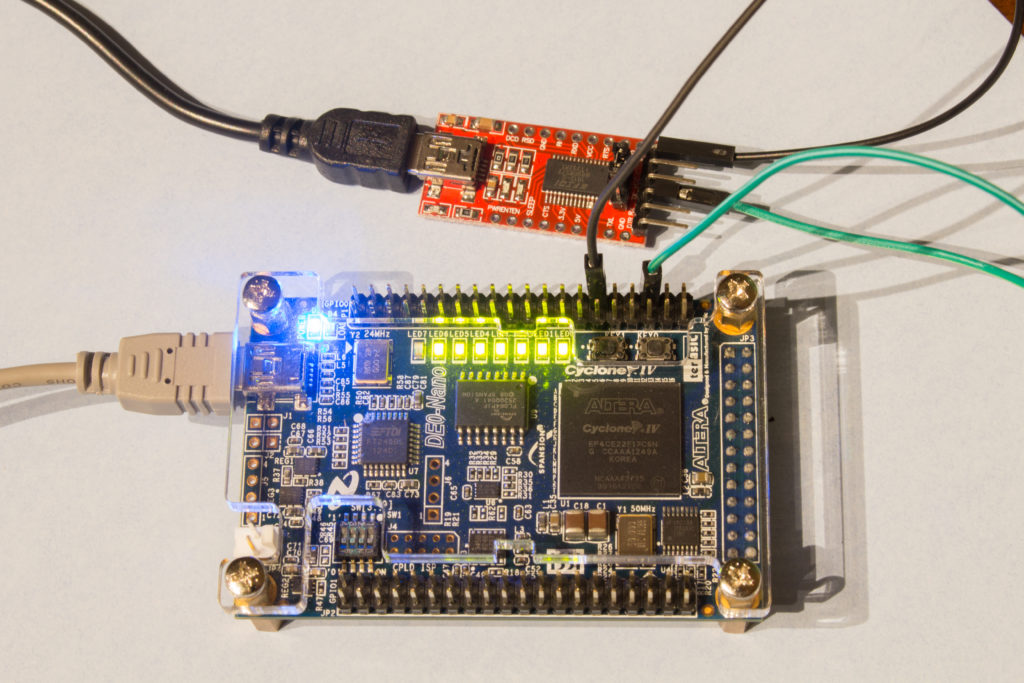
**Picture A.10.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE0-CV](http://de0-cv.terasic.com.tw) with Altera Cyclone V FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_cv_and_pl2303ta_160926_163235.jpg)

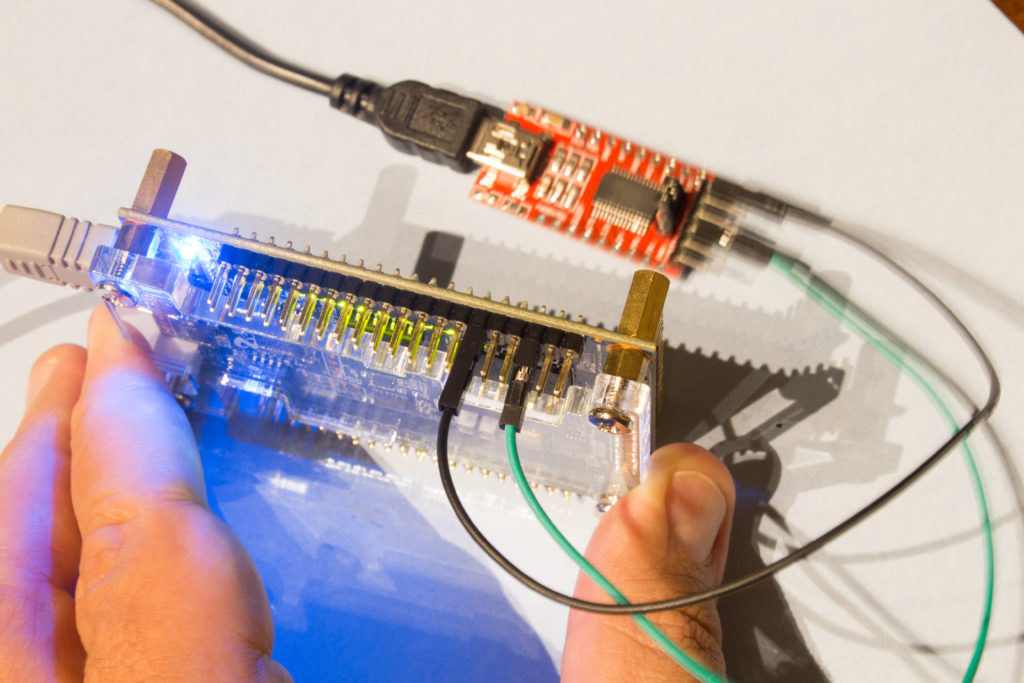
**Picture A.11.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE0-CV](http://de0-cv.terasic.com.tw) with Altera Cyclone V FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_cv_and_pl2303ta_160926_163515.jpg)

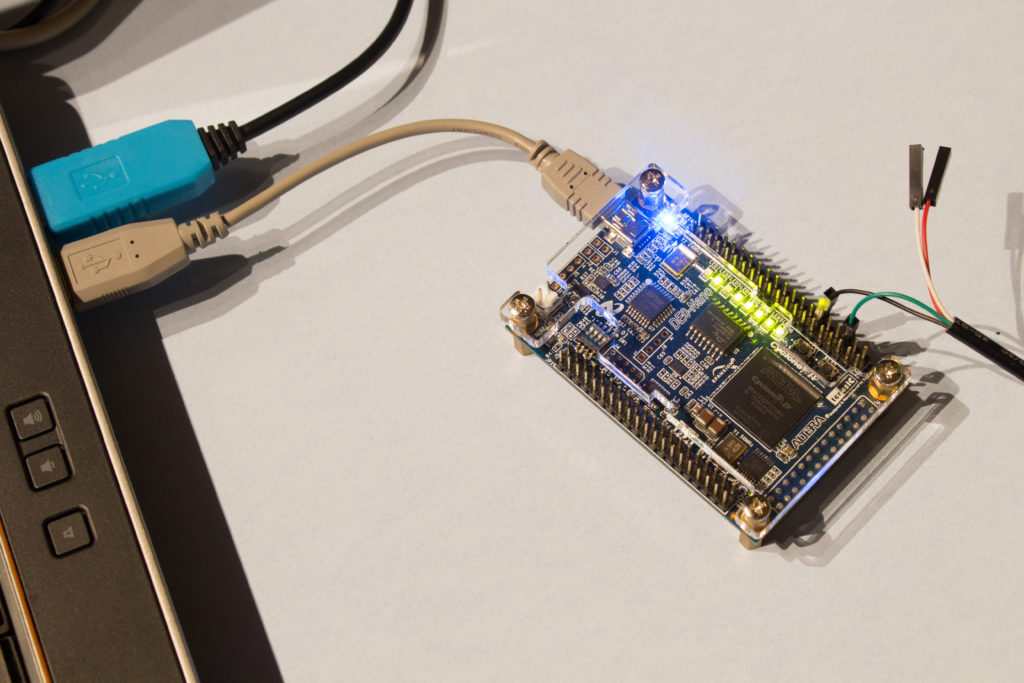
**Picture A.12.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0-Nano](http://de0-nano.terasic.com.tw) board with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_nano_and_ft232rl_160926_200247.jpg)

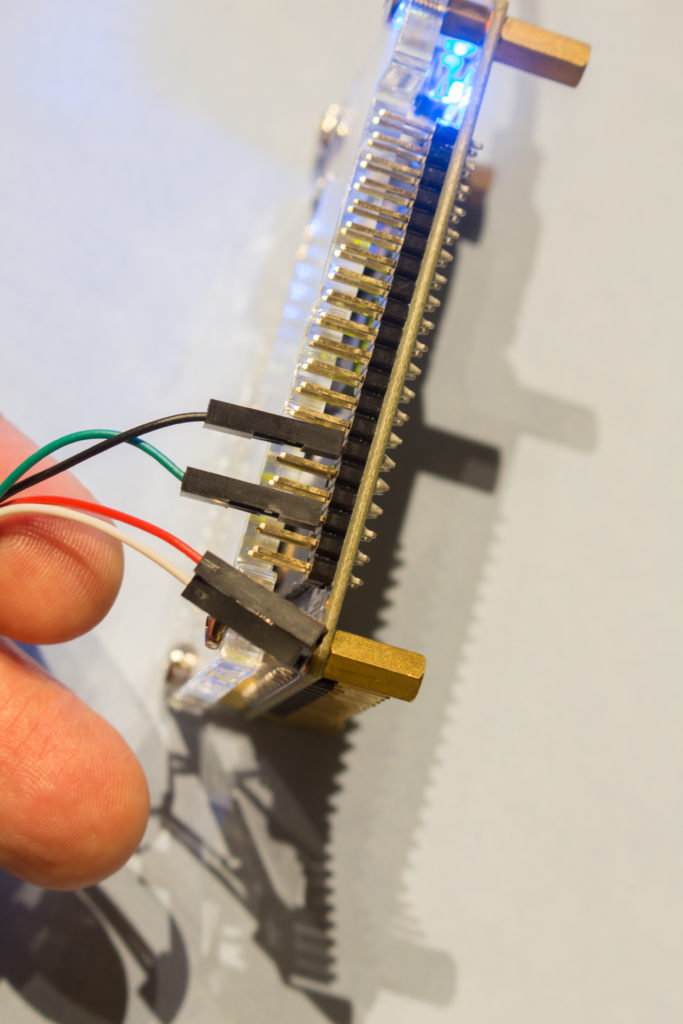
**Picture A.13.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE0-Nano](http://de0-nano.terasic.com.tw) board with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_nano_and_ft232rl_160926_200325.jpg)

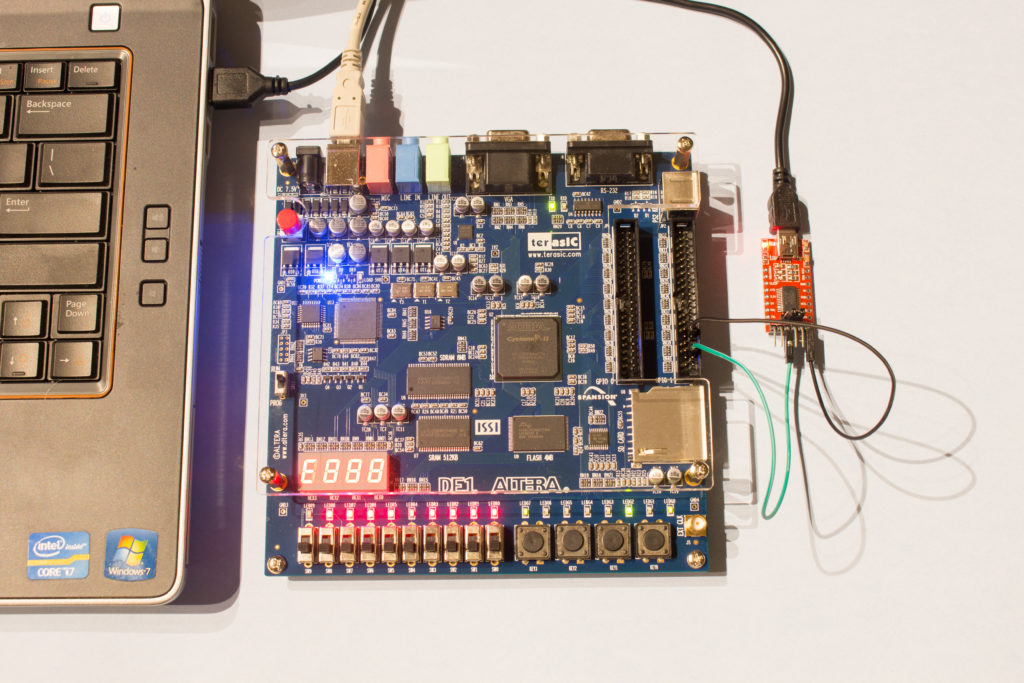
**Picture A.14.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE0-Nano](http://de0-nano.terasic.com.tw) board with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_nano_and_pl2303ta_160926_195706.jpg)

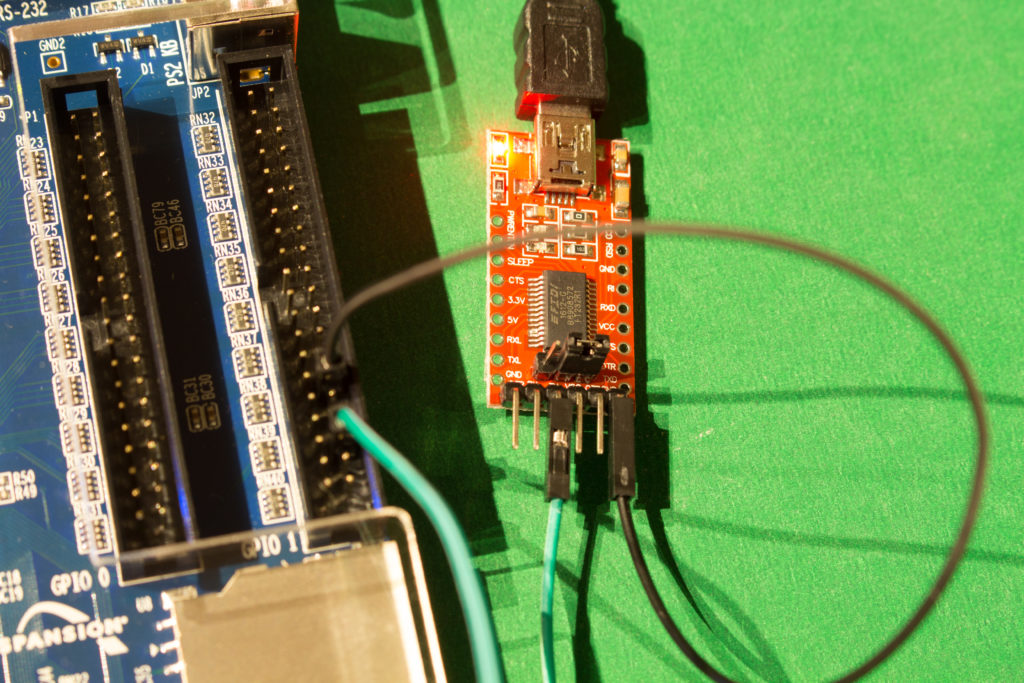
**Picture A.15.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE0-Nano](http://de0-nano.terasic.com.tw) board with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de0_nano_and_pl2303ta_160926_200109.jpg)

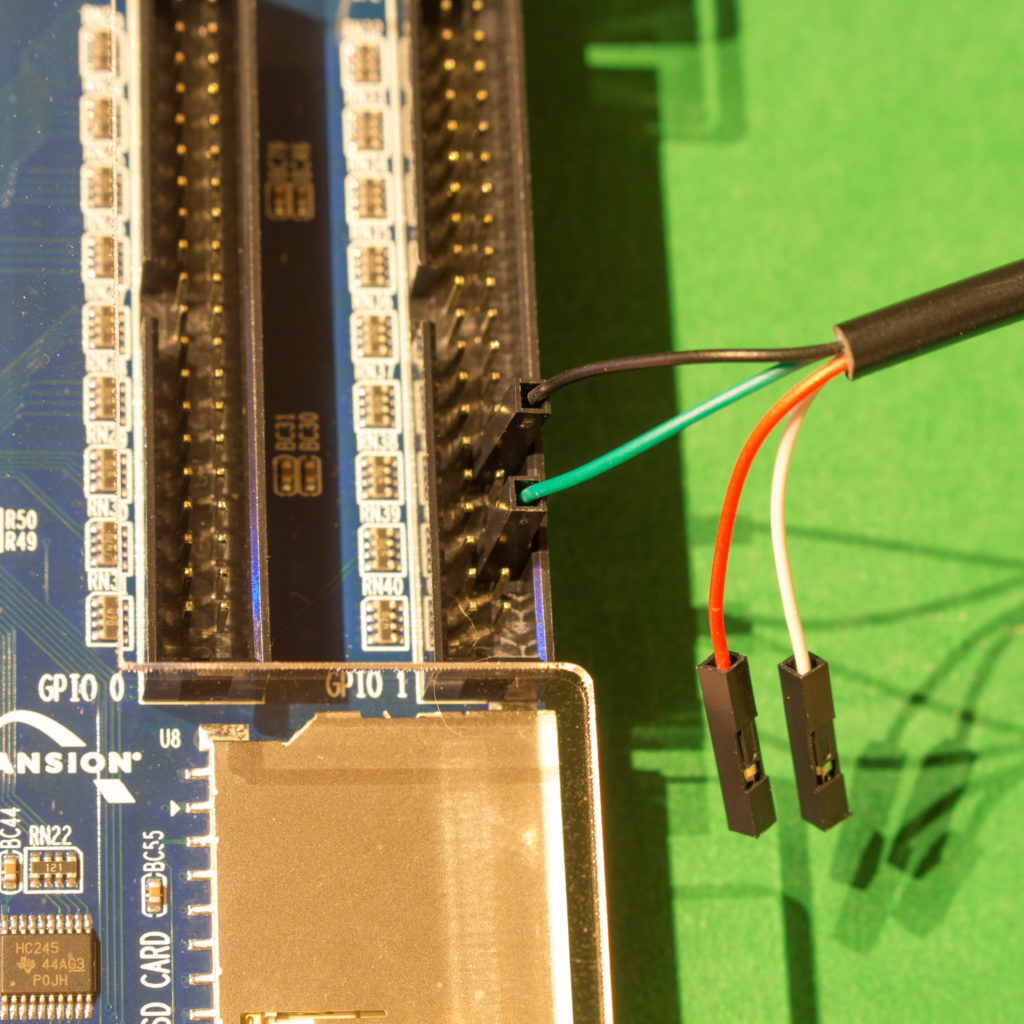
**Picture A.16.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE1](http://de1.terasic.com) with Altera Cyclone II FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de1_and_ft232rl_160926_202017.jpg)

**Picture A.17.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE1](http://de1.terasic.com) with Altera Cyclone II FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de1_and_ft232rl_160926_202330.jpg)

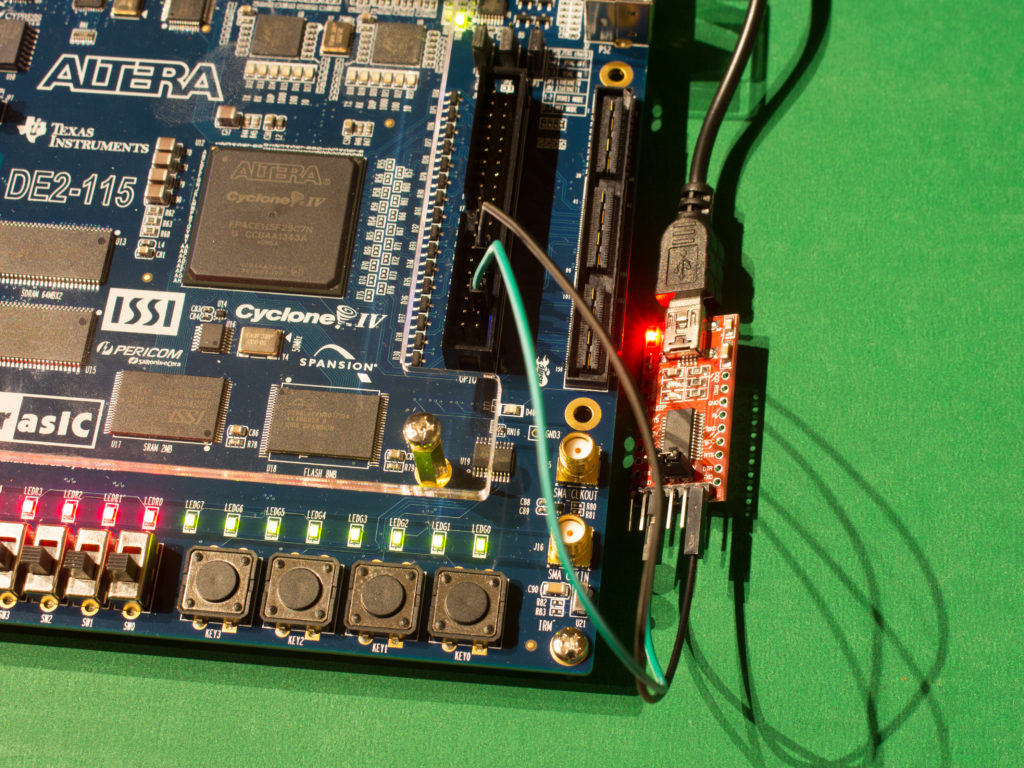
**Picture A.18.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE1](http://de1.terasic.com) with Altera Cyclone II FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de1_and_pl2303ta_160926_202449.jpg)

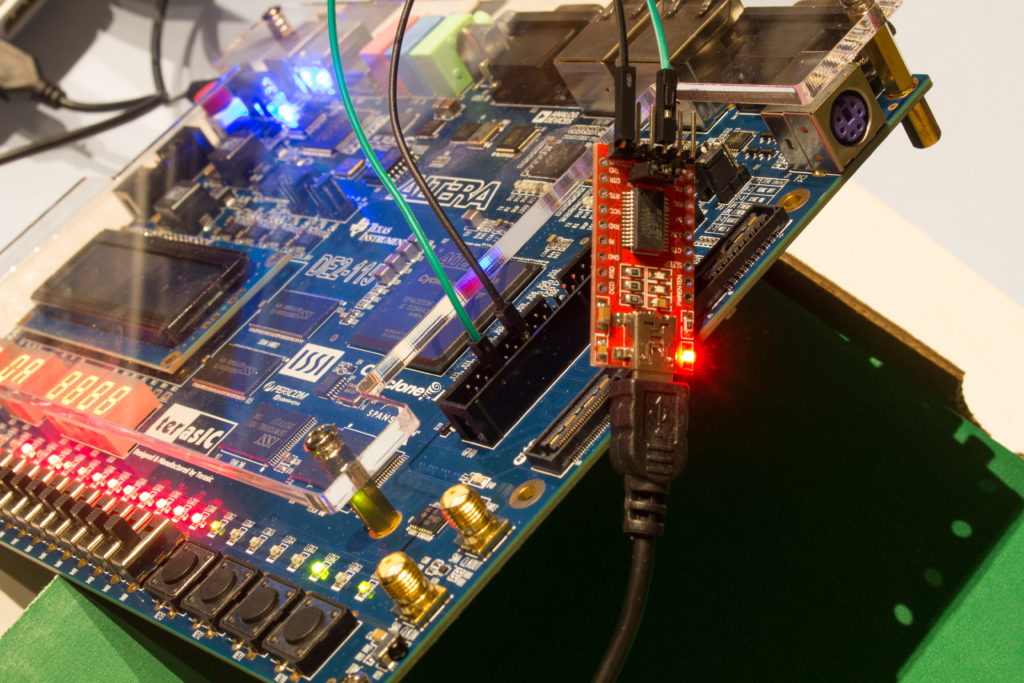
**Picture A.19.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE1](http://de1.terasic.com) with Altera Cyclone II FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de1_and_pl2303ta_160926_202733.jpg)

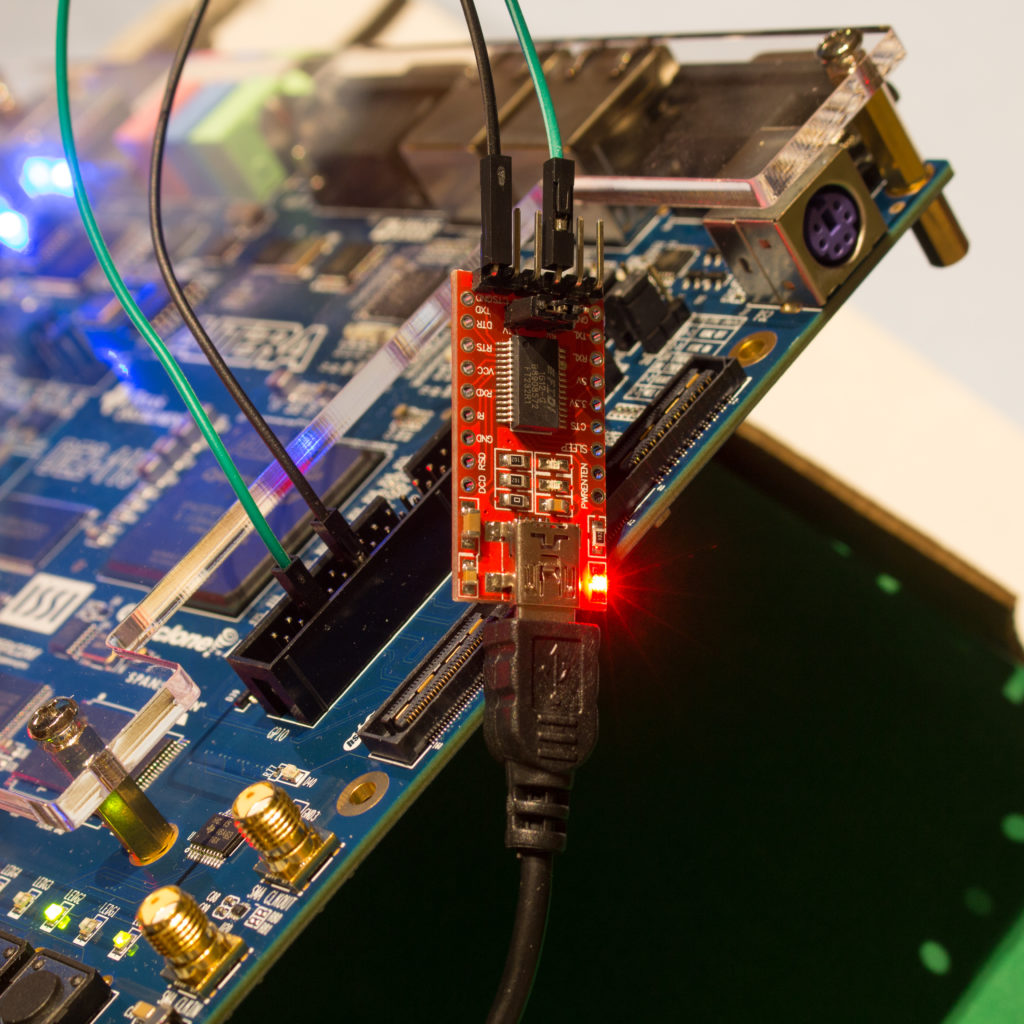
**Picture A.20.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_ft232rl_160926_215000.jpg)

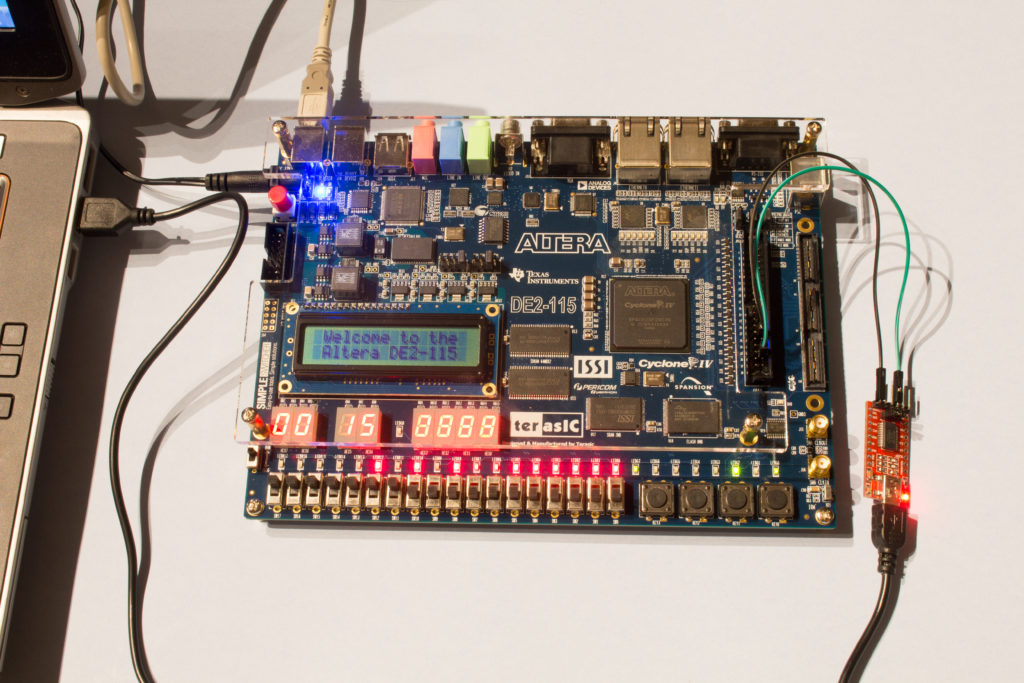
**Picture A.21.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_ft232rl_160926_232001.jpg)

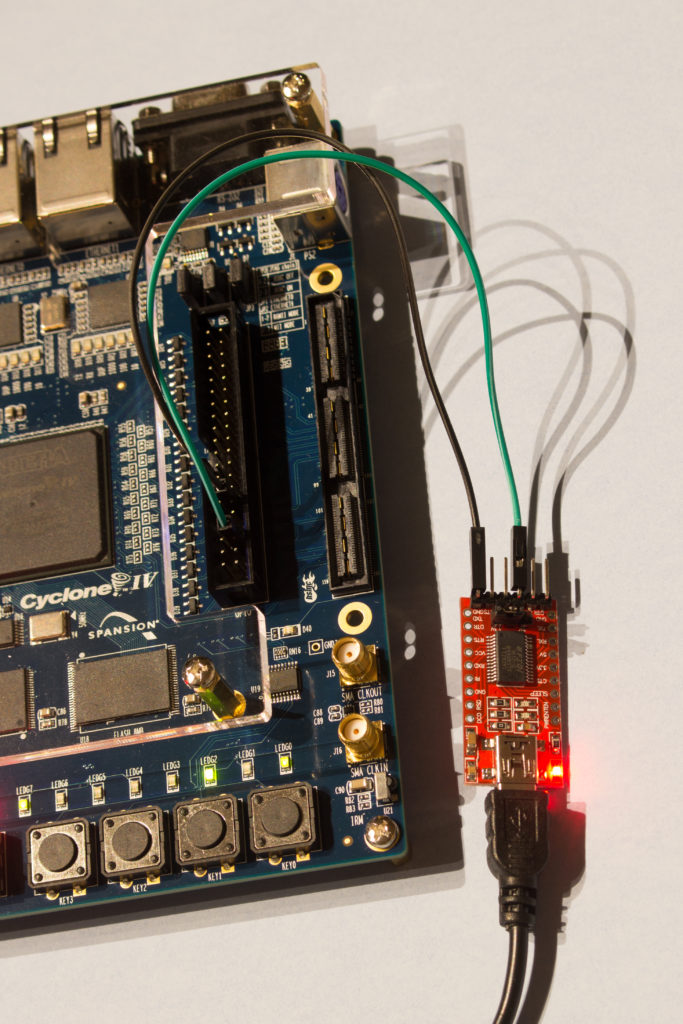
**Picture A.22.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_ft232rl_160926_232040.jpg)

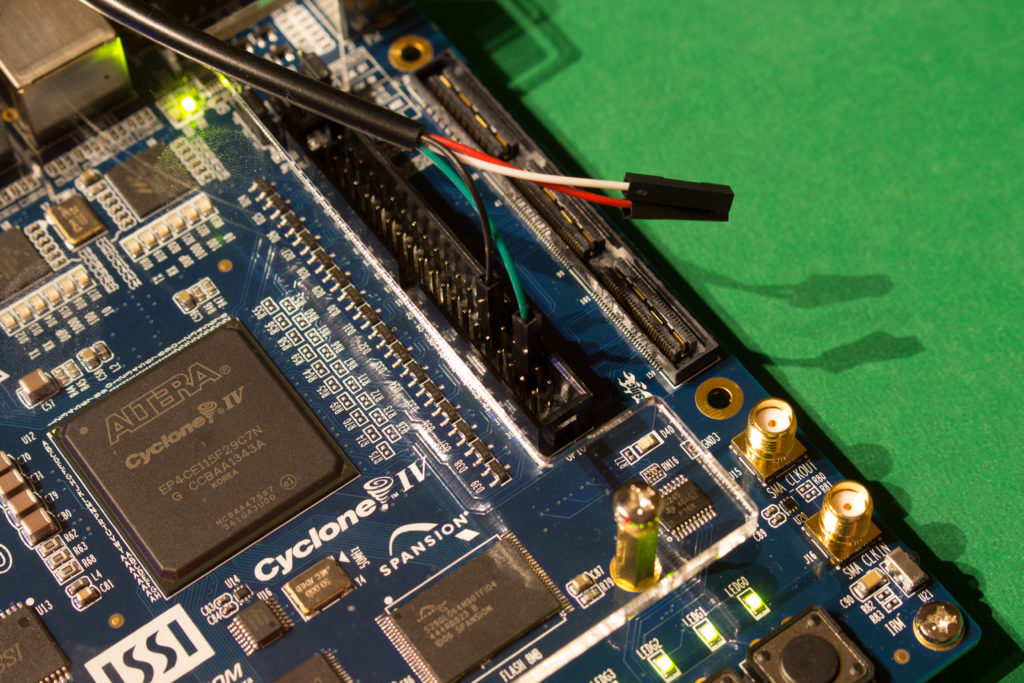
**Picture A.23.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_ft232rl_160926_232207.jpg)

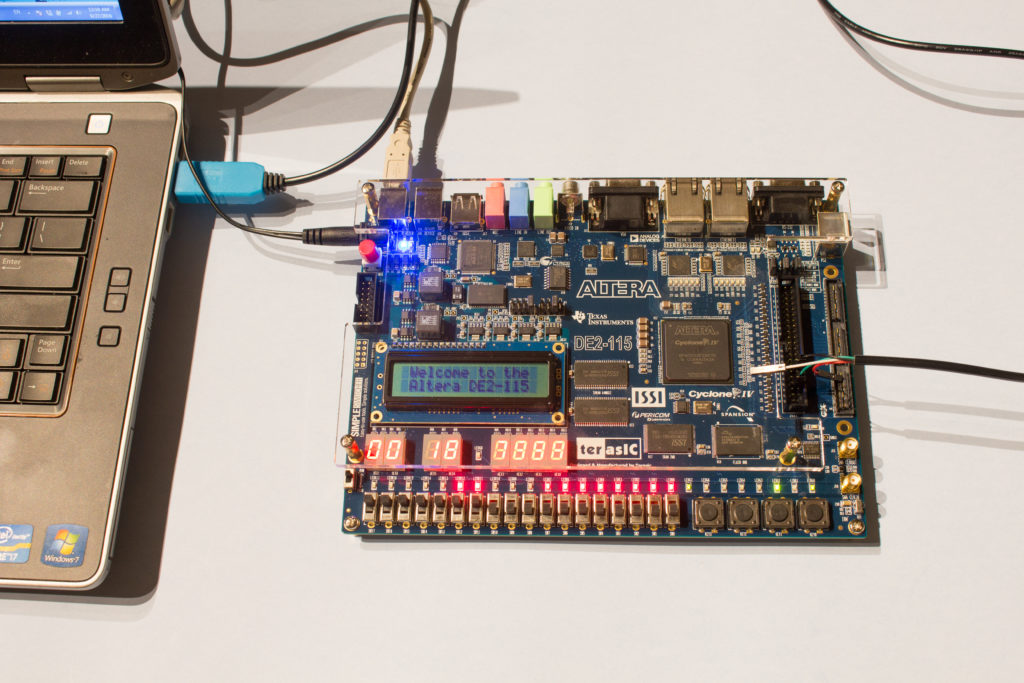
**Picture A.24.** A picture of FTDI-based USB-to-UART connector with [FT232RL](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231000536&SearchText=FT232RL+FTDI+USB) chip connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground is connected to pin 6 from right bottom. Note that you need to setup 3.3V/5V jumper on this connector into 3.3V position to avoid potential damage to some sensitive FPGAs:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_ft232rl_160926_232333.jpg)

**Picture A.25.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_pl2303ta_160926_215112.jpg)

**Picture A.26.** A picture of [PL2303TA USB TTL to RS232 Converter Serial Cable module for win XP/VISTA/7/8/8.1](http://www.aliexpress.com/wholesale?catId=0&initiative_id=SB_20151231182357&SearchText=PL2303TA+cable) connected to GPIO pins of [Terasic DE2-115](http://de2-115.terasic.com) with Altera Cyclone IV FPGA. UART TX (green) is connected to the pin 3 from right bottom and the ground (black) is connected to pin 6 from right bottom:

[](http://www.silicon-russia.com/wp-content/uploads/2016/09/terasic_de2_115_and_pl2303ta_160926_231019.jpg)