SCLD (TS2068/PAL) I/O Function Pin Definitions Rev. 0.2

based on TS2068 Technical Manual and validated for TC2048/2068 by Mark Smith (2020)

Pin no.	Symbol	Name	Direction of SCLD	Function	TC2048 application
1, 2, 60, 62, 64, 66, 67, 68 25, 27, 30	A0-A7 A13-A15	Address Buss	In	Address Bus line inputs from Z80A	
3, 4, 5, 6, 43	KB0-BD4	Keyboard Outputs	In	Input from 5 lines of keyboard matrix – goes low at one of 8 address line (active low) sequences on I/O Request	
7	BC1	Bus Control to Sound Chip	Out	A bus control signal to the PSG. When high the sound chip either is read to data bud or latches addresses from the data bus	Not connected
8	MUX	Mux Control of RAM Address	Out	Multiplexer control to 74LS157 (U13 & U14) to multiplex the row and column addresses to all dynamic RAM's	
9	CSYNC	Composite Sync	Out	Produce composite synchronisation signals to RGB monitor (TTL Level)	
10	TPIN	Tape In	In	Magnetic tape signal input	
11, 13, 17, 19, 52, 56, 58, 59	D0-D7	Data Bus	In/Out	Data Bus inputs/outputs from/to Z80A through U4 – 74LS245 or inputs from display RAM (16K) – U6 and U7	
12	TPOUT	Speaker and Tape Output	Out	Digital output to magnetic tape and to sound amplifier for speaker output	
14	CPUCLK	Clock to CPU	Out	CLK – Clock to Z80A CPLU which is interrupted to stop CPU when CPU wants to address display RAM at the same time as display controller	
15, 16, 21, 49, 53, 54, 55, 57	MA0-MA7	Muxed Address Bus	Out	Display memory multiplexed address bus and refresh	
18	GND	Ground	In	Ground return of SCLD	
20	BRIGHT	Brightness	Out	Produce brightness signals to RGB monitor (TTL Level)	
22	/CAS	Column Address Strobe #1	Out	To activate column address strobe for display memory only (2nd 16K) during memory read/write and display read	
23	A7RB	A7 + Refresh	Out	To refresh and address 8th bit address line input of RAM memory (not display) of 32K of 4416 RAM's (Home Bank 0x8000 to 0xFFFF)	
25	/RD	Read to CPU	In	CPU is reading from a memory or I/O location	
26	50_60Hz		In	50/60Hz Select	
28	/RFSH	Refresh	In	CPU is generating a refresh address to refresh dynamic RAM's	
29	AYCLK	PSG Clock	Out	Clock for sound chip @ 1.75MHz	Not connected
31	/MREQ	Memory Request	In	CPU is requesting access to a memory location to read or write	
32	/IORQ	I/O Request	In	CPU is requesting access to an I/O location to read or write	
33	/INT	Interrupt to CPU	Out	Interrupts CPU to handle keyboard strobing and timer for PAUSE command. Oped drain N channel with internal pull-up	
34	/BE	Bank Enable	In	When active low, indicated that internal memory is disabled (Home, Extension and Dock Banks) and an external memory is in use	Not connected
35	/ROMCS	Home ROM Chip Select	Out	To activate the 16k Home ROM (first 16K) when memory selection (MS) is set to Home Bank	
36	XOUT	Oscillator Out	Out	Xtal Oscillator amplifier output to drive crystal	
37	XIN	Oscillator In	In	Xtal Oscillator amplifier input to sense crystal signal	
38	/ROSCS	ROS Chip Select	Out	ROM-Oriented Software (Cartridge Bank) Chip Select	Not connected
39	/EXROM	Extension ROM Select	Out	Active low chip select signal for Extension ROM	Not connected
40	G	Green Colour Output	Out	Produce colour signals to RGB monitor (TTL Level)	
41	B	Blue Colour Output	Out	Produce colour signals to RGB monitor (TTL Level)	
42	/WR	Write from CPU	In	CPU is writing to a memory or I/O location	
44	R	Red Colour Output	Out	Produce colour signals to RGB monitor (TTL Level)	
45	/RAS	Row Address Strobe #1	Out	To activate row address strobe for display memory only during memory read/write, refresh and display read	
46	/CAS1	Column Address Strobe #2	Out	To activate column address strobe for Home Bank RAM (3rd 16K)	
47	/TS	Tri-State Display Memory Control	Out	Tri-State control form address and data buffers when CPI is addressing display memory at same time display controller is addressing the display memory	
48	/CAS2	Column Address Strobe #3	Out	To activate column address strobe for Home Bank RAM (4th 16K)	
50	/WE	Dynamic RAM Write Enable	Out	When active low, enables a write into the display RAM only	
51	Vcc	+5V Power	In	Power (+5V) input to SCLD	
61	/RDN	Read Direction Control to SCLD	Out	To control read/writ direction of 74LS245 (U4) Data Bus Buffer between CPU and SCLD	
63	BDIR	Bus Direction to Sound Chip	Out	A bus direction control signal to the PSG. When high the sound chip either receives a write to PSG or latches addresses from the data bus	Not connected
65	/CPUCLKB	Inverted clock	Out	CPU Clock signal inverted and buffered	Not connected

Notes:

1 IC chip references are applicable to TC2048 only