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CSC 230 Assignment 4 Questions

1. a) R = 1/P 1 / 200,000,000 Hz * 10^9 = 5 ns

b) 8*1 + 4*3 + 4*2 + 4*3 = 40M cycles. 40M cycles / 200M cycles per second = 0.2s = 200 ms

c) 10*1 + 8*2 + 2*4 + 4*3 = 46M cycles. 46M cycles / 200M cycles per second = 0.23s = 230 ms

d) Performance(A) / Performance(B) = T(B) / T(A) = 230 ms / 200 ms = 1.15. Machine A is about 1.15 times as fast as machine B. (i.e. machine A is better)

e) CPI = CPU clock cycles / instruction count

CPI(A) = 40M cycles / 20M instructions = 2 cycles per instruction

CPI(B) = 46M cycles / 24M instructions = 1.916666667 cycles per instruction

f) Machine A increased clock rate = 200 MHz * 1.2 = 240 MHz

New execution time = 40M cycles / 240M cycles per second = 0.166666667 s

Speedup is difference in time = 0.2s / 0.167s = 1.2 times

g) new cycles = 6*1 + 8*2 + 2*4 + 4*3 = 42M

new execution time: 42M cycles / 200M cycles per second = 0.21s = 210 ms

h) MIPS(A) = 200,000,000 Hz / 2x10^6 cycles per instruction = 100

MIPS(B) = 200,000,000 Hz / 1.9167x10^6 cycles per instruction = 104.347826087

2. a) Each instruction requires 4 clock cycles since there are 4 different stages. Each stage executes in one clock cycle. 3.2*10^9 ns

b) (1.25*10^9) / 4 = 312.5 x 10^6 instructions per second

c) Throughput is instructions per second. n instructions divided by time for n instructions with pipelining i.e. n / T(k,n) = n / ([k + (n-1)]*Pi) = n / ([4 + (n-1)]*(1/1.25*10^9)). The exact number depends the number of instructions being executed.

d) Sk = T(1,n) / T(k,n) = nk / (k + n - 1) = 500,000*4 / (4 + 500,000 - 1) = 3.999976

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e) Sk = T(1,n) / T(k,n) = nk / (k + n - 1) = 1,000,000*4 / (4 + 1,000,000 - 1) = 3.999988

f) The limit as n approaches infinity of Sk = k / 1 (by l'Hopital's rule) = 4

g) CPI(avg) = 1 + b*Pb*Pt = 1 + 10*0.15*0.5 = 1.75 cycles per instruction

Execution efficiency = 1 / CPI = 1 / 1.75 = 4 / 7 = 57.1428571%

3. a) log2(16,000,000) = 23.93 so 24 lines

b) Number of blocks is 16M / 32 = 500,000. Bits needed to address these blocks is

log2(500,000) =18.93 so 19

c) Number of lines is 16K / 32 = 500. Bits needed to address these blocks is log2(500) = 8.97 so

9.

d) 19 - 9 = 10. Need 10 bits for tag in direct mapped cache.

e) Need 19 bits for tag in fully-associative cache.

f) 19 - 8 = 11. Need 11 bits for tag in 2-way set-associative cache.

g) 19-7 = 12. Need 12 bits for tag in 4-way set-associative cache.

h) T(avg) = h*C + (1-h)*M

C = 1 cycle / 16M cycles per second = 0.000000062 s = 62 ns

M = 16 cycles / 16M cycles per second = 0.000001 s = 1000 ns

0.9*62 + (1 - 0.9)* 1000 = 155.8 ns

i) speedup = no cache / with cache

1*16 / 16000000 / 0.0000001558 = 6.418485237 times speedup

j) new T(avg) with 50% hit ratio = 0.5*62 + (1 - 0.5)* 1000 = 531 ns

new speedup = 1*16 / 16000000 / 0.000000531 = 1.883239171 times speedup