Experiment 2 - FPGA Realization of Radix-4 Multiplier

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***Abstract*— This document is a student report for the 2nd experiment of the Digital Logic Laboratory course (ECE 045) at University of Tehran, Department of Electrical and Computer Engineering.**

***Keywords*— Radix-4 Multiplier, RTL Design, RTL Simulation, FPGA Implementation, Altera Cyclone II, Quartus, ModelSim**

I. RTL Design and Simulation

A. Datapath

Fig. 1 shows the circuit's datapath. A flip-flop is added to the design to save the adder's carryout in order to prevent the multiplication overflow.

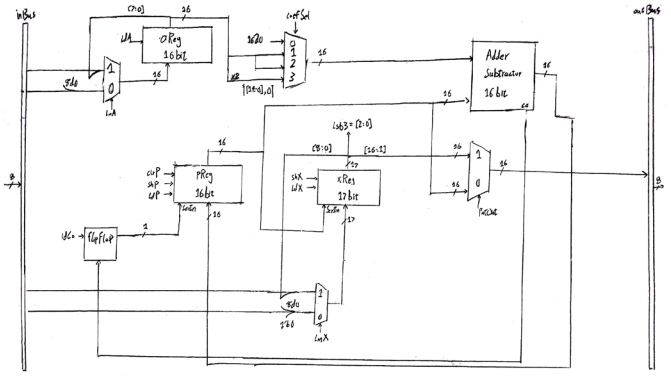

Fig. 1 Datapath design

B. Controller

The controller's state diagram is presented in Fig. 2.

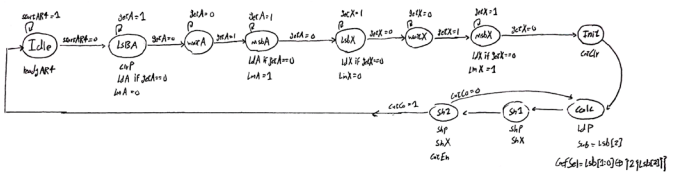

Fig. 2 Controller state diagram

C. Simulation Results

In order to verify the design, the following testbench is provided. The chosen multiplicand is -54 which is represented as 0b1111_1111_1100_1010 and the multiplier is -26 which is represented as 0b1111_1111_1110_0110. The multiplication result is 1404 which can be represented as 0x0000_057C.

Fig. 3 shows the simulation waveform for the mentioned values.

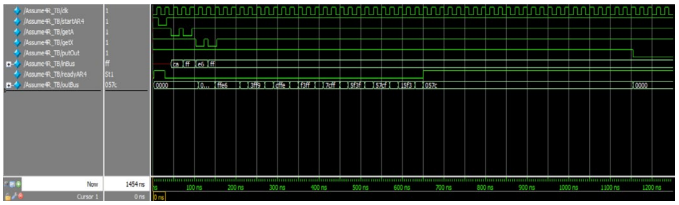

Fig. 3 Simulation waveform

Fig. 4 shows a zoomed in version of the above waveform.

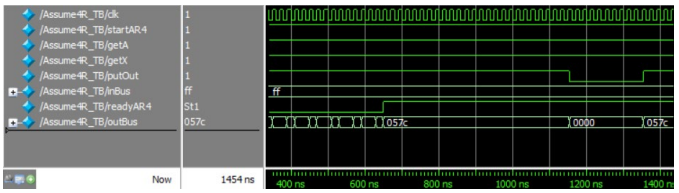

Fig. 4 Simulation waveform with relatively better visibility

D. ***Bonus Part***

As discussed in class, there is a bonus point if the design is able to handle the overflow which occurs in the multiplication process for some particular values. The following values lead to overflow if the adder's carryout is not used:

Multiplicand: 28 (0b011_100)
Multiplier: 11 (0b001_011)
Correct Result: 308 (0b000100_110100)

Fig. 5 shows the simulation waveform for the above values while Fig. 6 shows the same waveform with better visibility.

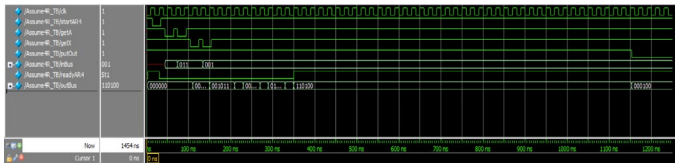

Fig. 5 Simulation waveform

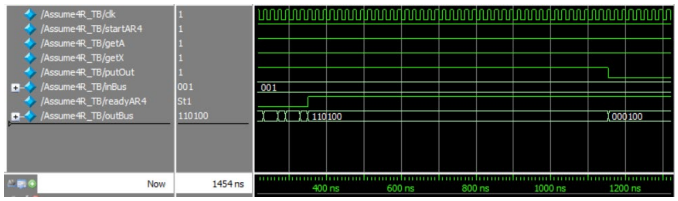

Fig. 6 Simulation waveform with relatively better visibility

II. FPGA Implementation

A. Pin Planning

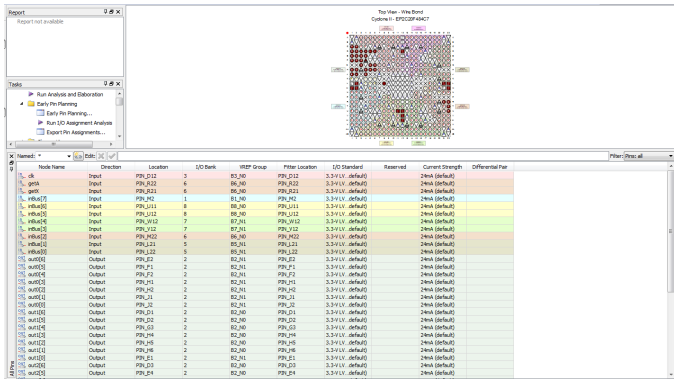

Fig. 7 Quartus pin planner

B. RTL View

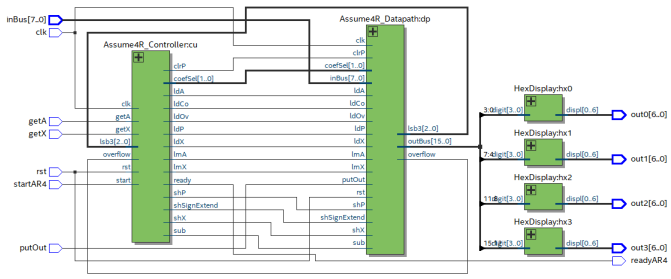

Fig. 8 Circuit's RTL view

C. Results

Fig. 9 shows the programmed Cyclone II using Quartus. The values provided to verify the circuit are the same values which were used in part 1.C (ModelSim). Fig. 10 shows the result's LSB while Fig. 11 shows its MSB. The values are as presented below:

Multiplicand: -54 (0b1111_1111_1100_1010)
Multiplier: -26 (0b1111_1111_1110_0110)
Result: 1404 (0x0000_057C)

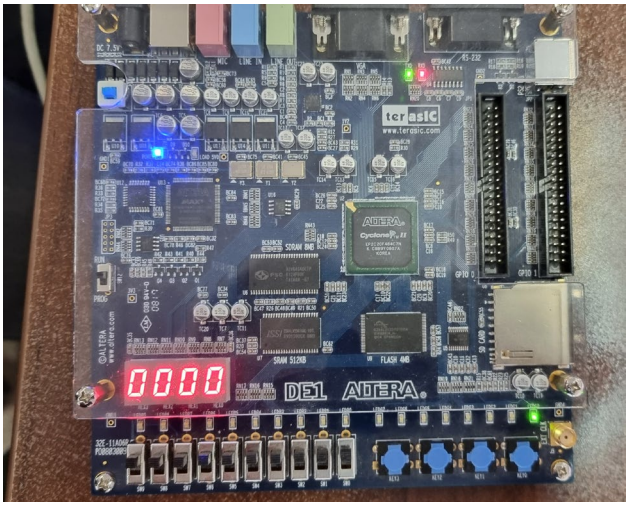

Fig. 9 A Cyclone II board with AssumeR4 programmed using Quartus.

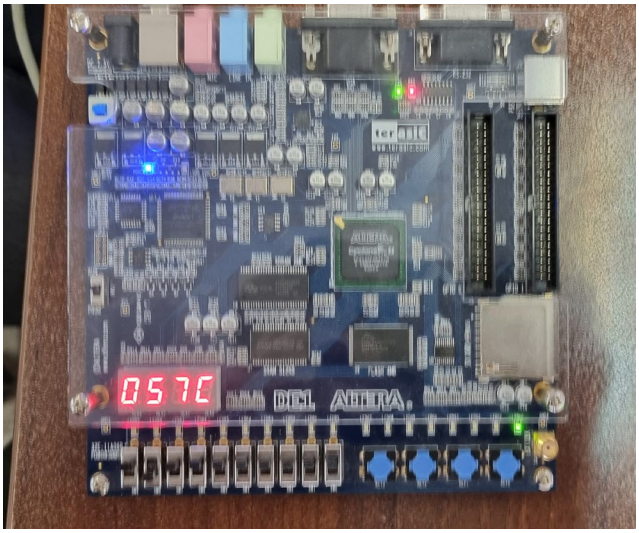

Fig. 10 The test result's LSB.

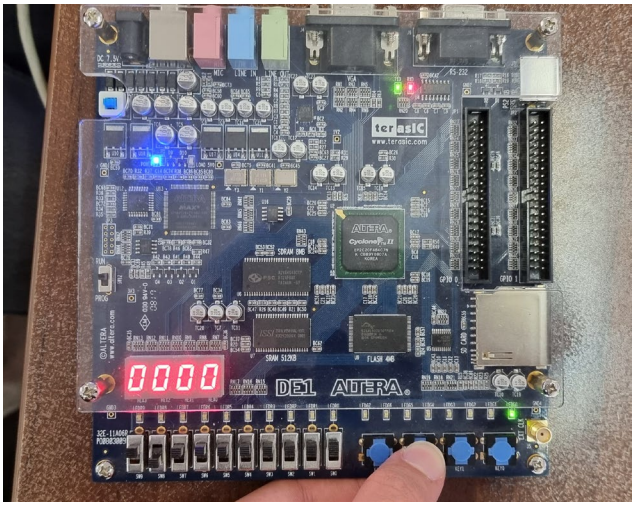

Fig. 11 The test result's MSB shown after holding the pushdown button.