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Quadrature Phase Shift Keying Modulator & Demodulator for Wireless Modem

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Abstract— ***Digital modulation is a process that impresses a digital symbol on to a signal suitable for transmission on a wired or wireless medium in order to receive that signal at receiving end correctly with out any loss of information. Quadratic phase shift keying (QPSK) modulation technique is the most widely used modulation scheme in modern digital communication system; it provides high performance on bandwidth efficiency and bit error rate. In this paper the complete model of Quadrature Phase Shift Keying (QPSK) modulator and demodulator has been developed. The model has been simulated in Matlab using Simulink. Complete results are tested and verified. In final hardware design and implementation of QPSK for Wireless Modem has been proposed. QPSK modulation has various applications particularly in the design of wireless modem, cellular CDMA communication.***

***Key Terms*—QPSK, Wireless Modem, QPSK Hardware Implementation, MATLAB Simulation of QPSK.**

I. INTRODUCTION

Internet has converted this world into global village. Now people want to communicate while on move. Wireless is the technology that makes it possible. In last few years, the mobile radio communication industry has grown exponentially. By the fabrication of high density low power, low noise, small size and reliable digital and RF chips make radio equipment smaller, cheaper and more reliable. Due to this explosive growth of mobile and wireless users there are so many problems created, the most critical problem is frequency spectrum, Bit Error Rate (BER) and Bandwidth. In this paper the Quadrature Phase Shift Keying is addressed as modulator and demodulator for the wireless modem.

II. DIGITAL MODULATION

A. Overview

Digital modulation is a process that impresses a digital symbol on to a signal suitable for transmission on a wired or wireless medium in order to receive that signal at receiving end correctly with out any loss of information [1].

For short distance transmissions, base band modulation is usually used, which is referred as line coding.

In long distance and wireless transmission band pass modulation (carrier modulation) is used. In band pass modulation a base band signal is modulated over a high frequency sinusoidal carrier signal. The bandwidth of this modulated signal depends upon the base band signal and modulation scheme to be used. A sequence of digital symbols is used to alter the parameters of high frequency carrier signal. There are three parameters that can be changed, which are amplitude, phase and frequency. In this way three basic digital modulation schemes are amplitude shift keying (ASK), frequency shift keying (FAK), and phase shift keying (PSK). Besides on these basic digital modulation schemes a variety of digital modulation schemes can be derived from their combination. For example combination of two orthogonal BPSK modulated signals form quadrature Phase Shift Keying (QPSK). The combination of amplitude modulated signal and phase modulated signal form a quadrature amplitude modulation (QAM). These both modulated techniques i.e. QAM and QPSK are used in IEEE 802.11 (Wi-Fi), IEEE 802.16 (WiMAX) and 3G (WCDMA/HSDPA) Wireless technologies, including Wireless Modem [6]. Another advantage of these techniques is to reduce the utilized bandwidth PSK or QAM are highly useful [2].

B. Quadrature Phase Shift Keying (QPSK)

QPSK can be stated as a method for transmitting digital information across an analog channel. Data bits are grouped into pairs, and each pair is represented by a particular waveform, called a symbol, to be sent across the channel after modulating the carrier [3].

The most commonly used modulation scheme for wireless and cellular systems is Quadrature Phase Shift Keying (QPSK). It's because it does not suffer from BER degradation while the band width efficiency is increased [1]. The QPSK The QPSK signals are mathematically defined as [4]:

$$Si(t) = A\cos(2\pi f_c t + \theta_i) \quad 0 \le t \le T, \qquad \textbf{(1)}$$

Where

$$\theta_i = \frac{(2i-1)\pi}{4} \qquad \textbf{(2)}$$

The carrier frequency is chosen as integer multiple of the symbol rate, there fore in any symbol interval, the signal initial phase is also one of the four phases ($\frac{\pi}{4}, \frac{3\pi}{4}, \frac{5\pi}{4}, \frac{7\pi}{4}$).

The above expression can be written as:

$$s_t(t) = A\cos\theta_i \cos 2\pi f_c t - A\sin\theta_i \sin 2\pi f_c t \quad \textbf{(3)}$$

$$s_t = s_{i1}\phi_1(t) + s_{i2}\phi_2(t)$$

Where

$$\phi_1 = \sqrt{\frac{2}{T}}\cos 2\pi f_c t, \quad 0 \le t \le T \quad \textbf{(4)}$$

$$\phi_2 = -\sqrt{\frac{2}{T}}\cos 2\pi f_c t, \quad 0 \le t \le T \quad \textbf{(5)}$$

$$s_{i1} = \sqrt{E}\cos\theta_i \quad \textbf{(6)}$$

$$s_{i2} = \sqrt{E}\sin\theta_i \quad \textbf{(7)}$$

$$\theta_i = \tan^{-1}\frac{s_{i2}}{s_{i1}} \quad \textbf{(8)}$$

There fore the QPSK signal can be entirely written as:

$$S(t) = \frac{A}{\sqrt{2}}[I(t)\cos 2\pi f_c t - Q(t)\sin 2\pi f_c t] \quad -\infty < t < \infty \ \textbf{(9)}$$

The constellation diagram of QPSK signal is shown in fig.1.

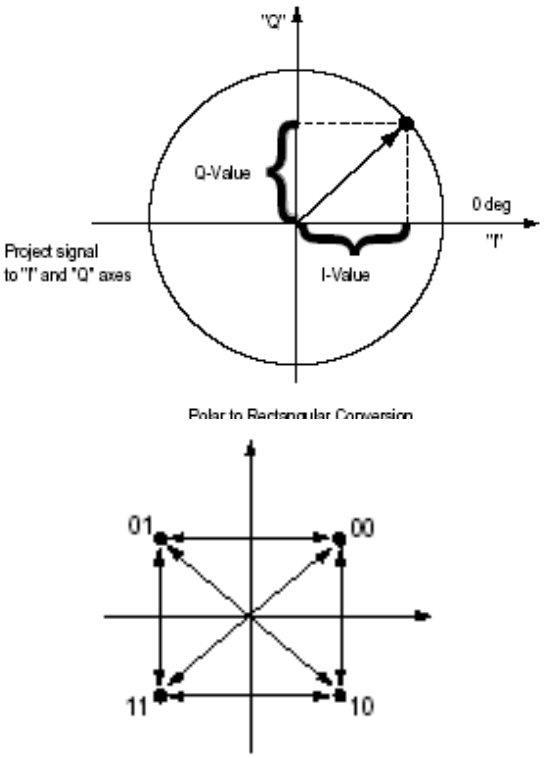

Fig. 1: Constellation diagram of QPSK modulation

III. Model Block Diagram

A. QPSK Modulator

QPSK modulator consists of two binary phase shift keying (BPSK) modulators, serial to parallel converter shift register, oscillator and 90^0 phase shifter [5]. The binary serial bit sequence with bit rate R_b applied to modulator is converted into two bit parallel sequence I-bit and Q-bit each of having bit rate $R_b/2$ [8]. These I and Q bits are applied to BPSK modulators, whose carrier frequency is orthogonal to each other. This orthogonal signal is achieved through phase shifter; which shift the applied signal to 90 degrees. The out put from both BPSK modulators is added by summing amplifier; which results QPSK modulated signal. The block diagram of QPSK modulator is given in fig.2.

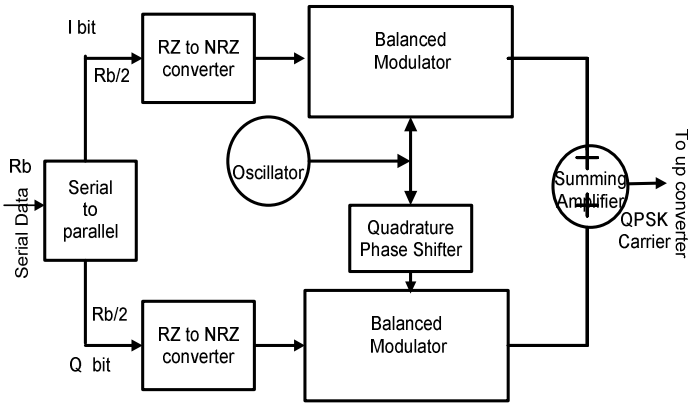

Fig.2. Block Diagram of QPSK Modulator.

B. QPSK Demodulator

The design of the coherent carrier recovery circuit for the demodulation of suppressed carrier PSK signals is very critical and involves several performance considerations and tradeoffs. The digitally modulated signal (QPSK) is fed to the demodulator. And it is applied to the I mixer, which is driven with 0o carrier phase, and to the Q mixer with the 90o carrier phase. The carrier recovery circuit regenerates the coherent reference for the demodulation and is routed to the balance modulators (multipliers). The multipliers extracts the in-phase (I) and quadrature-phase (Q) data streams, which are low pass filtered and fed to the corresponding plug-in of the bit-synchronizer and signal conditioner NRZ converter unit. The block diagram of QPSK demodulator is given in fig.3.

IV. Software Implementation

A. QPSK Modulator

The QPSK modulator is simulated in Matlab, using Simulink tool boxes. The simulation model in given in fig. 4 and the resulting wave forms are given in fig. 5.

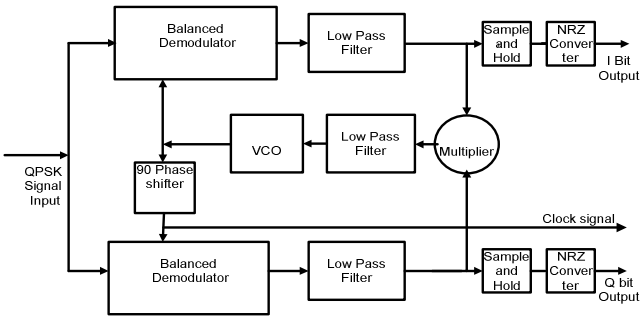

Fig. 3. QPSK Demodulator

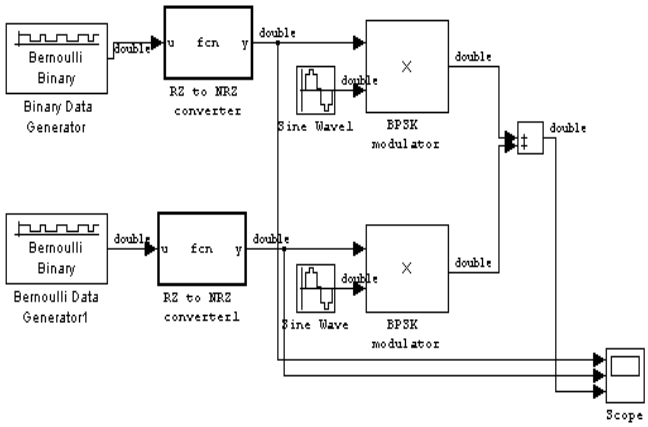

Fig.4. QPSK Matlab Modulator Model.

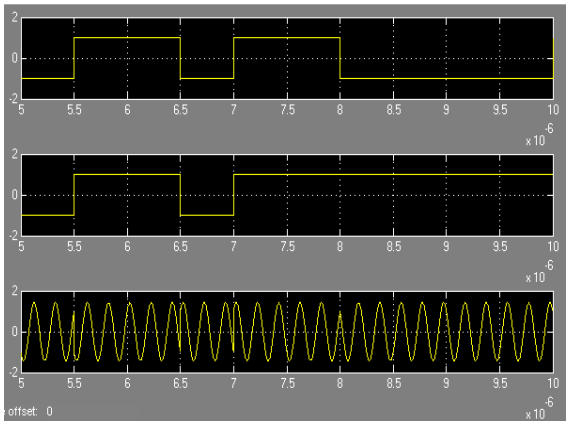

Fig. 5. Modulation Results

B. QPSK Demodulation

The Matlab Simulink demodulation model of QPSK is given in fig.6. The simulation results of Matlab model are given in fig.7.

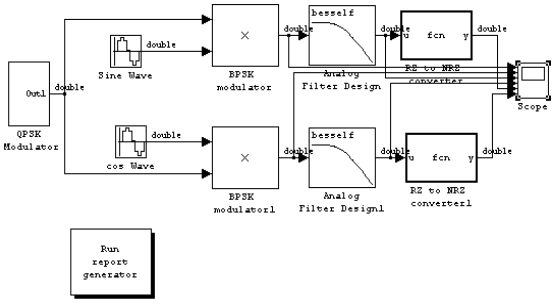

Fig.6. OPSK Demodulation in Matlab

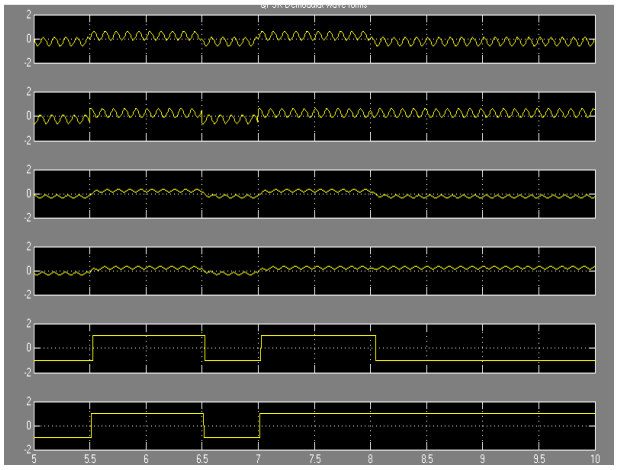

Fig.7. QPSK Demodulation Matlab Results

V. HARDWARE IMPLEMENTATION: QPSK MODULATOR

A. Proposed Balanced Modulator

The MC1496 IC [7] is used as a balanced modulator; because it makes an excellent building block for high frequency communications equipment. The device functions as a broadband; double–sideband suppressed carrier balanced modulator without a requirement for transformers or tuned circuits. In addition to its basic application as a balanced modulator/demodulator, the device offers excellent performance as an SSB product detector, AM modulator/detector, FM detector, mixer, frequency doublers, phase detector, and more. The schematic of MC1496 is shown in fig. 8.

The operation of the MC1496 consists of applying a high level input signal to the dual differential amplifiers, Q1, Q2, Q3, and Q4, (carrier input port) and a low level input signal to the lower differential amplifier, Q5 and Q6, (modulating signal input port) [7]. This results in saturated switching operation of carrier dual differential amplifiers, and linear operation of the modulating differential amplifier. The resulting output signal contains only the sum and difference frequency components and amplitude information of the modulating signal. This is the

desired condition for our applications. The Spectrum of double balanced modulator is shown in fig. 9.

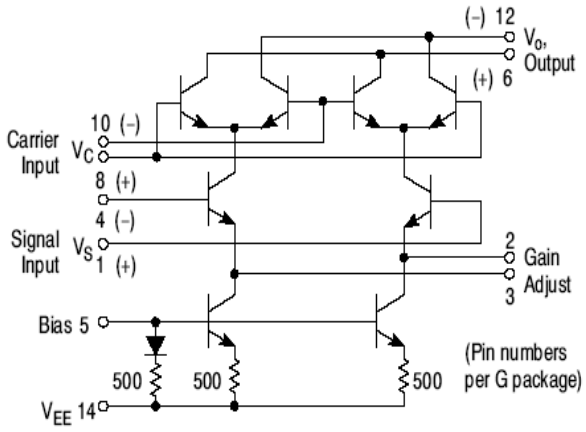

Fig.8. Schematic of Balanced Modulator

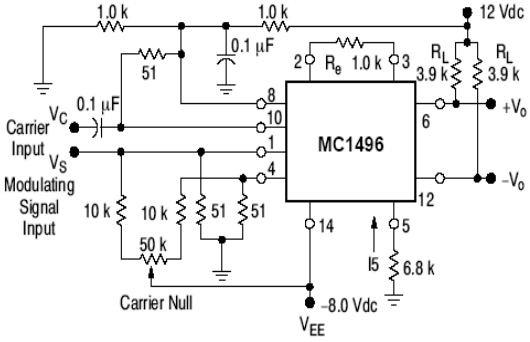

Fig.9. Balanced Modulator-Demodulator typical Circuit.

B. Quadrature Phase Shifter

The quadrature phase shifter is designed by differential circuit. As our carrier is a sinusoidal signal, and derivative of sin is cos; which is 90° out of phase with sin wave. The circuit diagram of phase shifter is given in fig 9 and its result is shown in fig. 11. The values of circuit components are only for the 10 MHz carrier frequency.

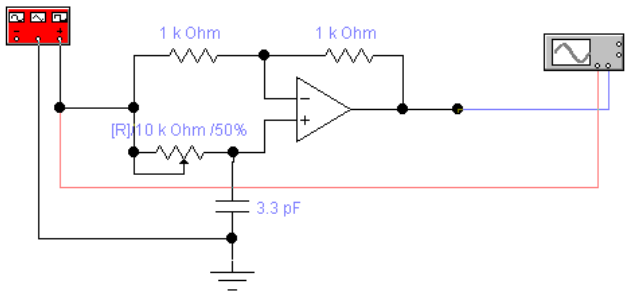

Fig.11. Phase Shifter Diagram

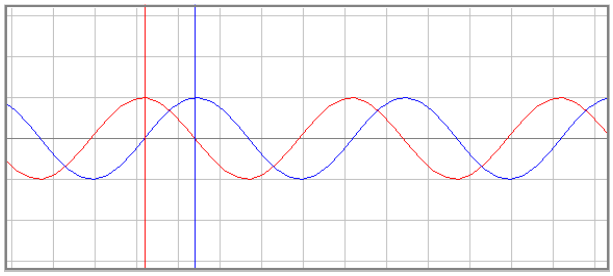

Fig.12.Phase Shifter Output

C. Summing amplifier

The I bit modulated signal from BPSK 1 modulator is applied to the I input of summing amplifier and the Q bit modulated signal from BPSK 2 modulator is applied to the Q input of summing amplifier where these are linearly added to generate complex QPSK modulated signal. The circuit diagram of summing amplifier is given in fig. 13.

D. RZ to NRZ converter

The digital signal applied to BPSK modulator is non-return-to-zero coded. But signal from serial to parallel shift register is return to zero. This circuit shown in fig 14 is used to convert RZ coding to NRZ coded signal.

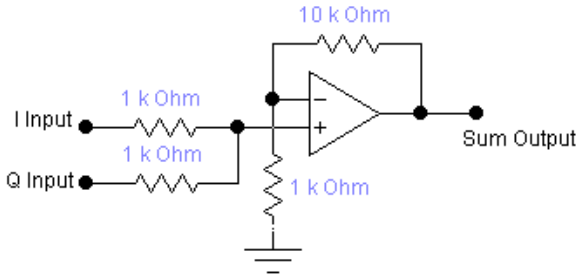

Fig. 13. Summing Amplifier

E. Carrier signal generator

The carrier frequency is generated using a crystal oscillator, to get stable phase response as desired in communication systems. The oscillator is designed around a BJT transistor. It operates at 10 MHz frequency. The output of oscillator is applied to balance modulator BPSK1 and phase shifter. The schematic is shown in fig 14.

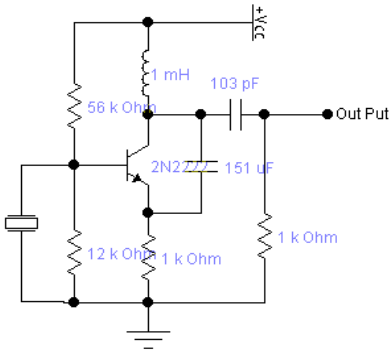

Fig. 14. Carrier Signal Generator

F. Serial to parallel Converter

Data sent to QPSK modulator is a sequence to serial bits; which is converted to two bit parallel sequence called I and Q bits. The schematic diagram of serial to parallel converter is shown in fig. 15.

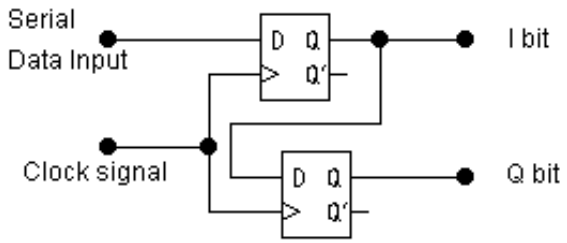

Fig.15. Serial to Parallel Conversion

VI. Hardware Implementation QPSK Demodulator

A. Proposed Demodulator

In demodulation section the most of the circuit parts are same; that described in modulator section; which are balanced modulator/Demodulator, low pass filter, phase shifter and NRZ converter. Only the new components are voltage controlled oscillator, parallel to serial converter and sample and hold circuit.

B. Voltage controlled oscillator (VCO)

Two requirements must be fulfilled in order to obtain oscillation in the closed loop circuit:

1. The closed loop gain must be greater than or equal to one.
2. The phase shift around the loop is N*360E, where N is an integer.

VCO, or voltage controlled oscillators, can have the output frequency change with a change in voltage at a control pin of the oscillator. The amount of frequency shift with a given voltage change is highly dependent on the oscillator circuit. 35% to 50% frequency variation per volt can common be achieved and higher ranges can be obtained by adding an inductor to "de-Q" the crystal. Most VCOs use varactor diodes to vary the frequency. The varactor diode changes the capacitance across its terminals based on the DC (or low frequency AC) voltage across the same terminals. A common transistor circuit is shown in fig 16.

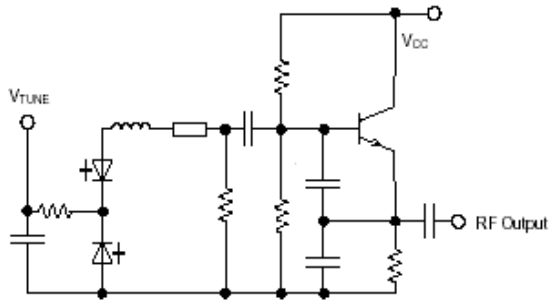

Fig. 16. Voltage Controlled Oscillator

C. Sample and Hold Circuit

Signal from BPSK demodulators is applied to the in put of sample and hold circuit; which takes the sample of signal at proper interval determined by clock signal and holds that signal information till next sample. The holding time depends upon the capacitor value used in the circuit. And sampling time depends upon the clock signal applied to Vs pin. The schematic circuit diagram of sample and hold circuit in shown in fig. 18.

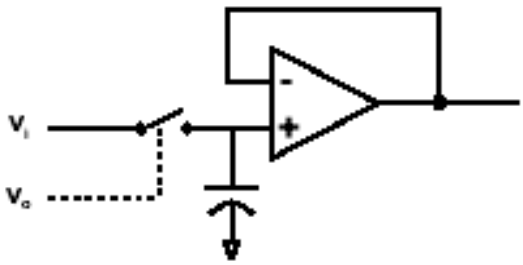

Fig.18. Sample & Hold Circuit

VII. Conclusion

At first stage the digital modulation has been reviewed followed by Quadrature Phase Shift Modulation (QPSK). In second stage the QPSK Modulator & Demodulator block diagrams are discussed & Matlab Simulink simulation of both (modulator & demodulator) has been presented. In final stage the complete hardware implementation of QPSK Modulator-Demodulator using MC1496 has been proposed.

In this paper the complete software model of QPSK Modulator- Demodulator has been designed, simulated, and tested using Simulink MATLAB. Hardware of QPSK Modulator-Demodulator has been proposed using MC1496 (balanced Modulator-Demodulator).

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