EECS 140: Lab 10

Scrolling Display

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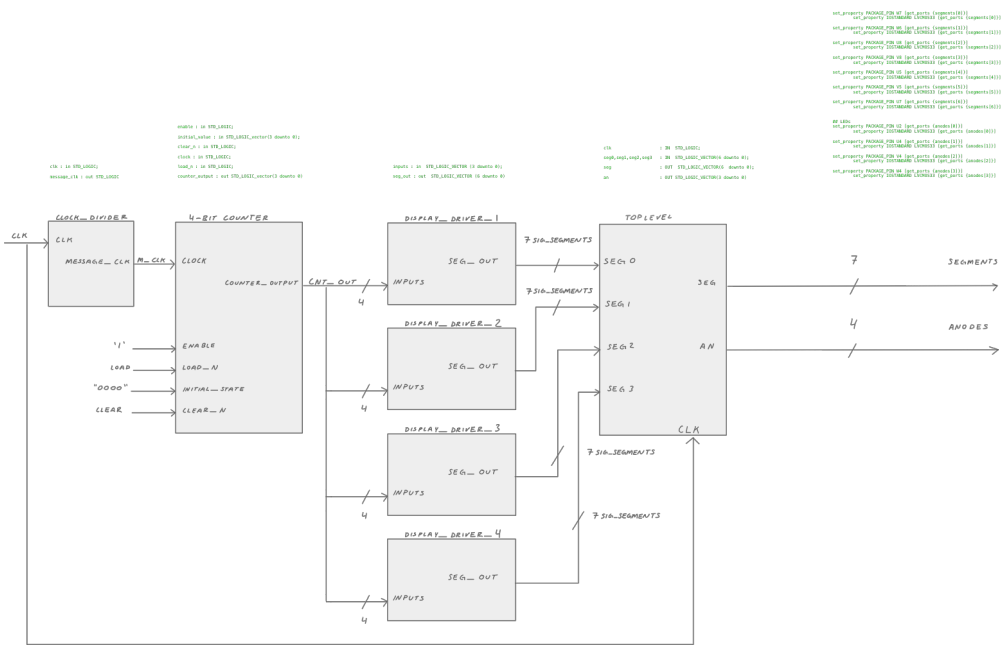
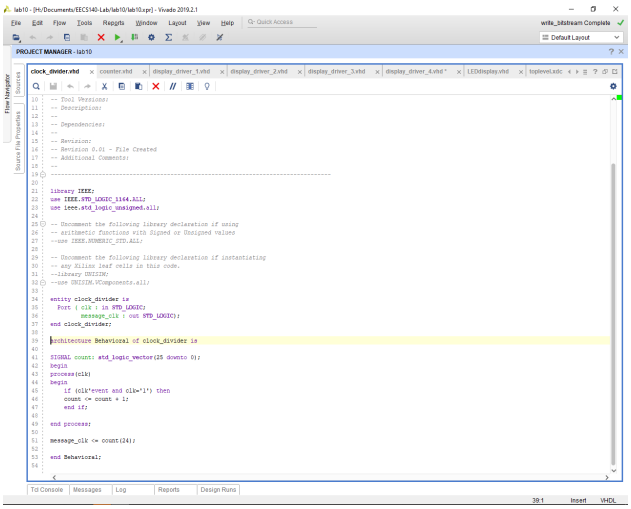
1. Introduction and Background

The objective of this laboratory exercise is to learn how to use modular design in VHDL to display a scrolling phrase up to 16 characters long on the 4 7-segment displays on the Basys 3 board. The components that were used in completing this lab are the following,

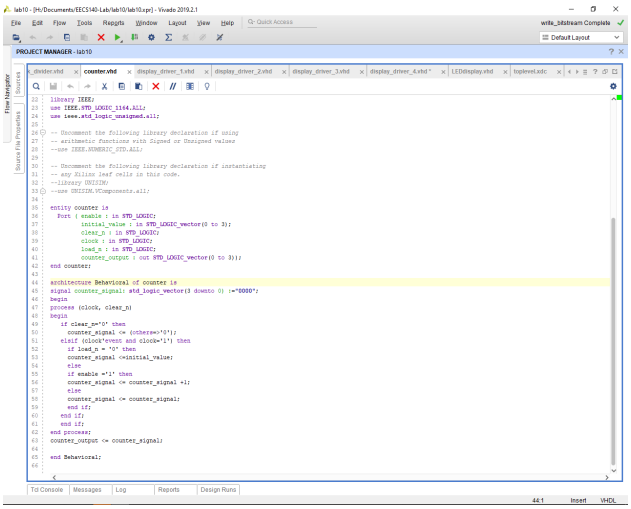
clock_divider.vhd
counter.vhd
display_driver_1.vhd
display_driver_2.vhd
display_driver_3.vhd
display_driver_4.vhd
LEDdisplay.vhd
toplevel.vhd
toplevel.xcd
All of the pictures comprising the code to these modules can be found on page 3, 4, & 5.

The total amount of connections (signals) that connected to the counter will have 4 signals connecting to each of the display drivers, the variable for the signals is a vector of length 4. The following shows the block diagram of how this lab was structured.

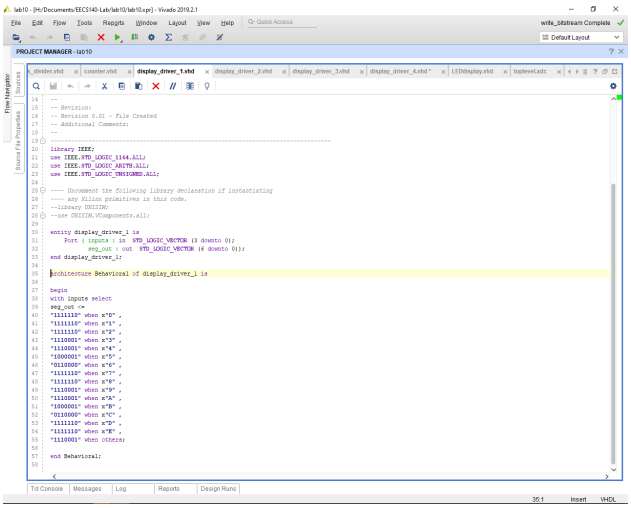




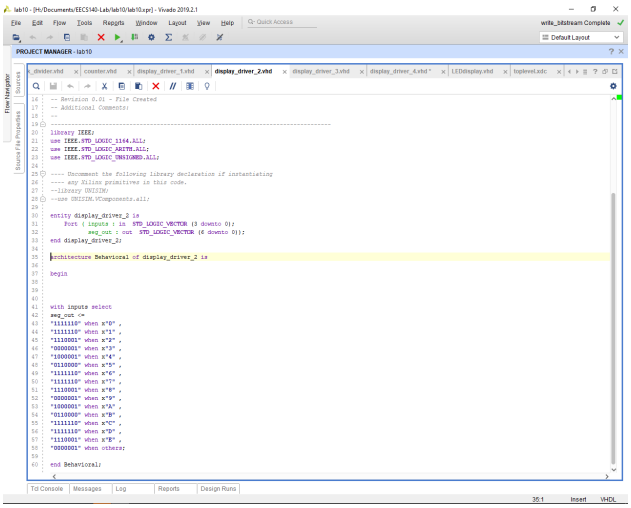
clock_divider.vhd



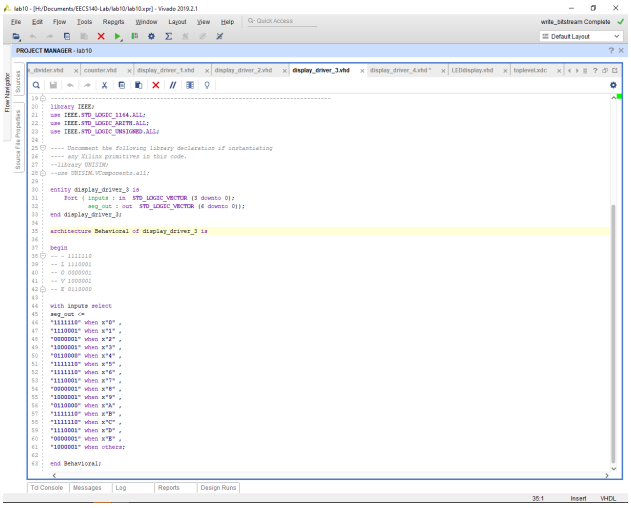
counter.vhd



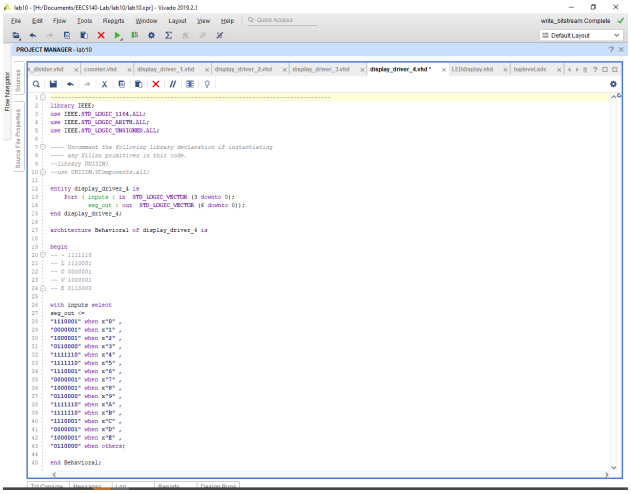
display_driver_1.vhd



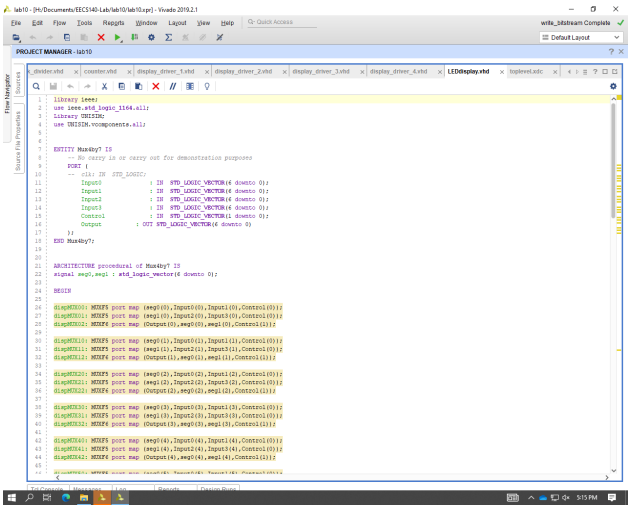
display_driver_2.vhd



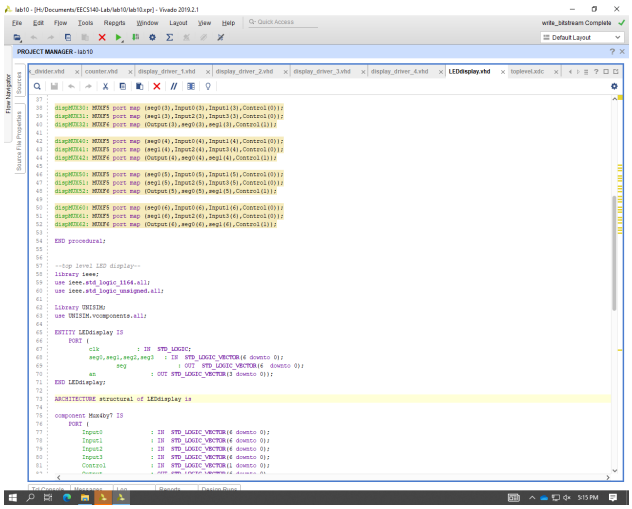
display_driver_3.vhd



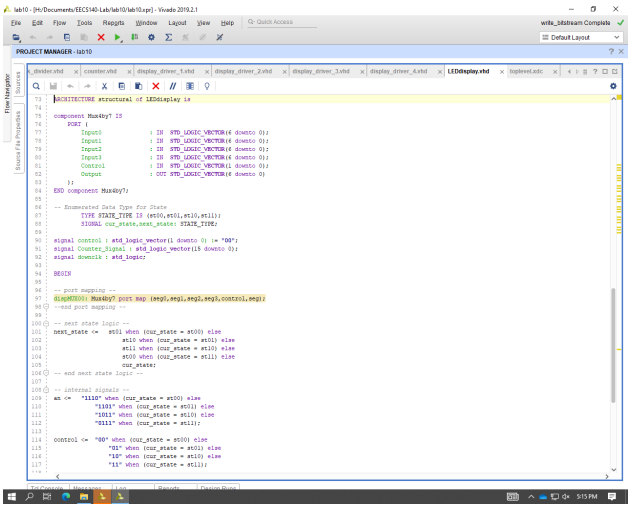
display_driver_4.vhd



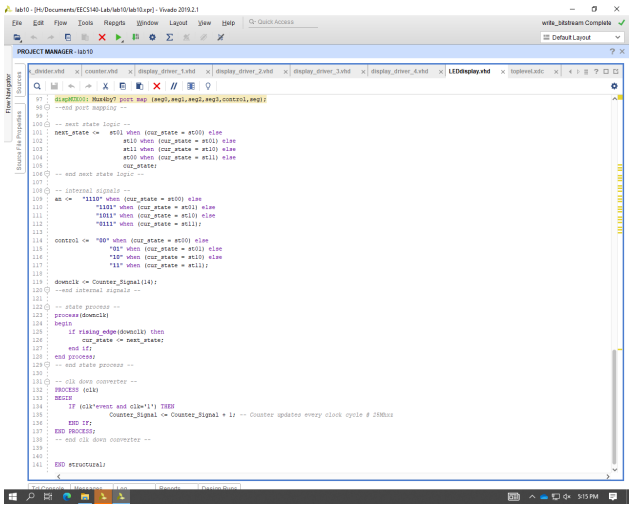
LEDdisplay.vhd



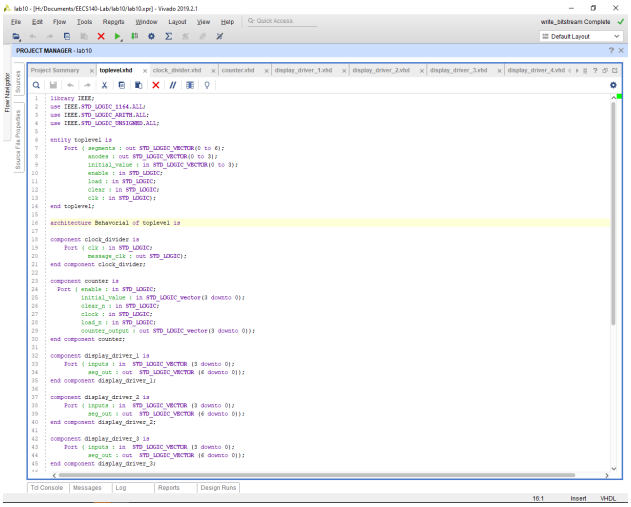
LEDdisplay.vhd



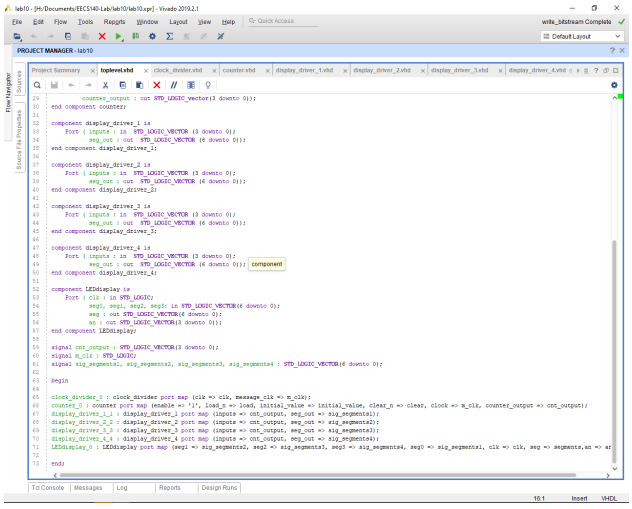
LEDdisplay.vhd



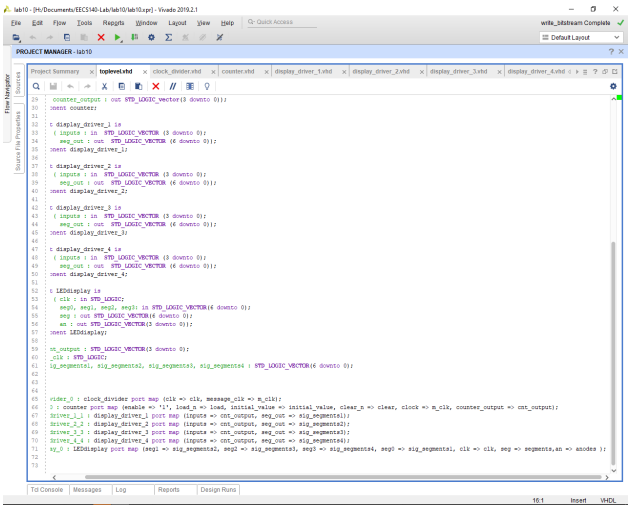
LEDdisplay.vhd



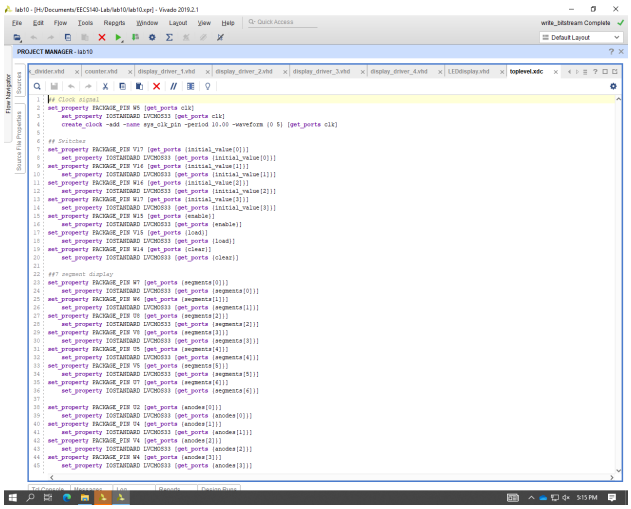
toplevel.vhd



toplevel.vhd



toplevel.xcd



toplevel.xcd

2. Implementation Process

Our first task was to define the clock_divider.vhd. This component is responsible to take the on-board 450MHz clock input and divide it so that the period of the resulting clock is about 1 second. The name of this clock was message_clk and it controlled the speed at which my message will scroll on the 4 7-segment displays. And I was able to test component by hooking it up to an LED (say LD0) and make sure it blinks every 1 second or so). Next was to define, source 2 counter.vhd. I then designed a 4-bit counter that ran at the rate of message_clk which is the output of the clock divider, that was now the clock input of the counter). The output was a 4-bit vector called counter_output. The counter also has extra inputs: enable, initial_value, clear_n, load_n. Then there after was the 4 display drivers (analogous to the display_driver.vhd display_driver_1.vhd display_driver_2.vhd display_driver_3.vhd display_driver_4.vhd. All of which need to be defined so that the output could look as follows,

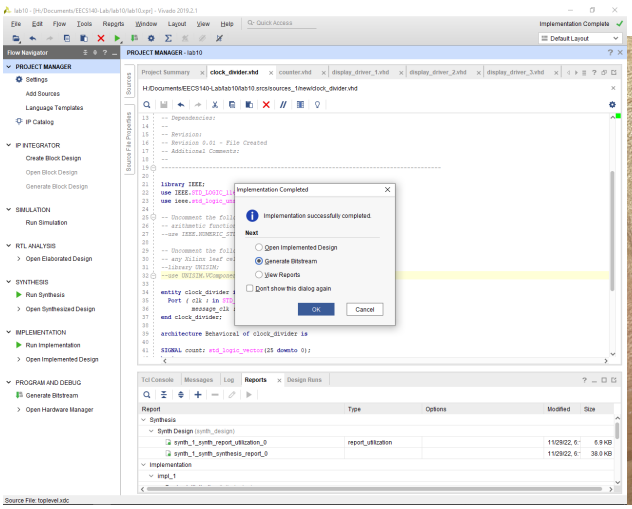
```
L O V E
1 2 3 4  display_drivers each column is 1 driver

- - - L
- - L O
- L O V
L O V E
L V E -
V E - -
E - - L
- - L O
- L O V
L O V E
L V E -
V E - -
E - - L
- - L O
- L O V
L O V E

L = "1110001" = "abcdefg"
O = "0000001" = "abcdefg"
V = "1000001" = "abcdefg"
E = "0110000" = "abcdefg"
```

Next was defining the LEDdsiplay, then the The toplevel structural VHDL module for the block diagram is provided below, I declared the components and instantiated (port map =>) them to reflect the interconnections from the diagram above. toplevel entity with required input and output ports: clk, segments(7 bits), anodes(4 bits), enable, load, clear, initial_value, declare components clock divider, counter, display_driver_1, display_driver_2, display_driver_3, display_driver_4, LEDdisplay I declared signals m_clk, cn_out, sig_segments1, sig_segments2, sig_segments3, sig_segments4. The component instantiation / port mapping had all ports defined in toplevel.vhd should be mapped using constraints file to implement the design.

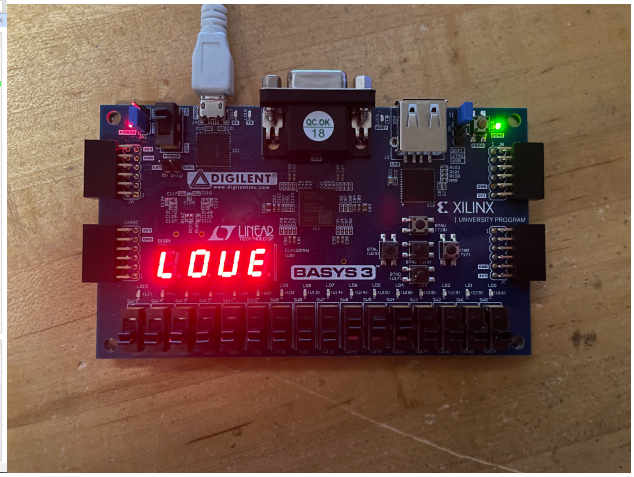
Finally was the constants, toplevel.xdc. However before creating constraints file, I needed to ensure that hierarchical design is established over all other sources so to pull from the following constraints and modify variable so the defined Toplevel entity matches with the declared constraints file as well.

3. Evaluation Process

Lastly, in order to evaluate and test the lab we need to check the accuracy of the result of this lab will be tested by using the Basys 3 board and the Xilinx Vivado software. The Basys 3 board will be used to display the scrolling phrase on the 4 7-segment displays. The Xilinx Vivado software will be used to simulate the scrolling phrase on the 4 7-segment displays. I displayed ‘love’ and to looked as follows.



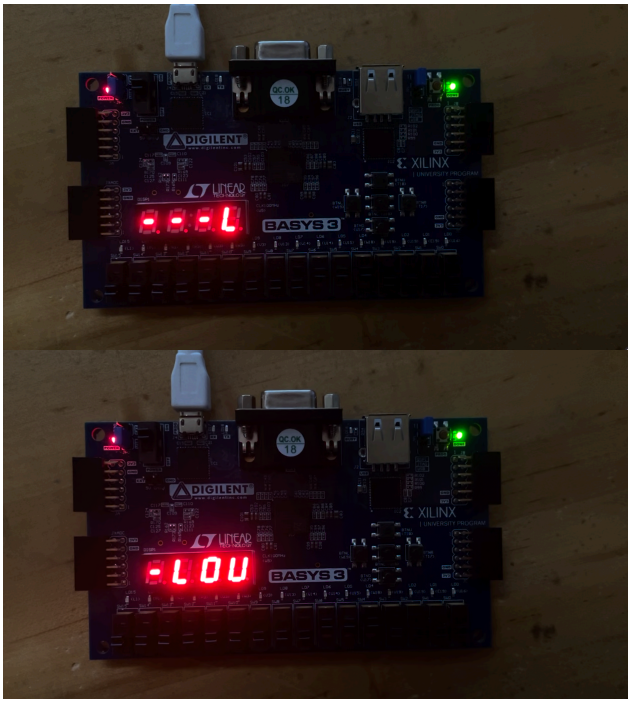
successful implementation

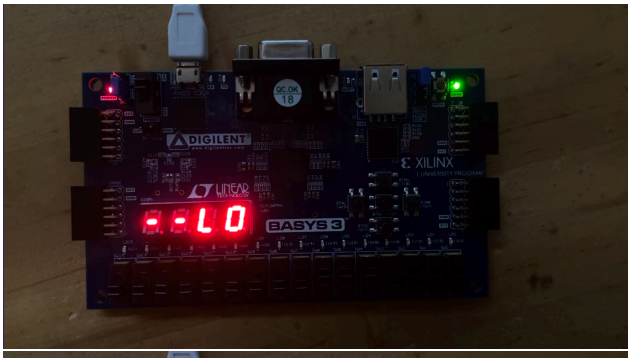


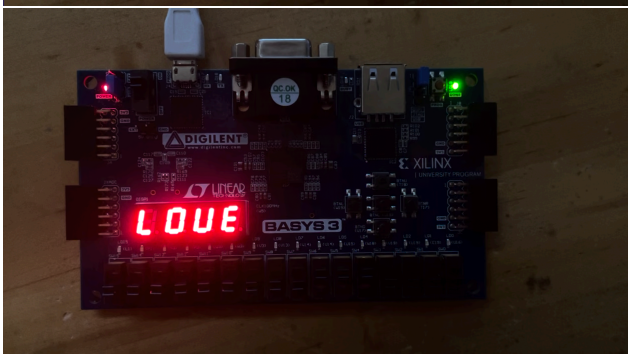
scrolling display

4. Results and Discussion

The result was a scrolling segment display, with the word love. The display driver definitions were the most important component to the output.







5. Conclusion and Recommendations

I properly learned how to use modular design in VHDL in order to display a scrolling phrase that was all the way p to 16 characters long on the board. I really enjoyed this lab and it was the most exciting output I have generated.