1. Draw the Boolean Logic Network for the following problem statement

Adam is delighted!!! He secured a job as a “Digital Design Engineer” in a Nuclear Power Plant. The nuclear plant has four sensors placed in four dangerous zones. These sensors indicate any impending danger which enables the maintenance officer to shut down the plant. Out of the four, three major sensors are namely X, Y, and Z. If any of the two-out of three major sensors-sense some danger, they actuate an alarm that notifies the maintenance officer for a plant shutdown. However, there is a small caveat. If sensor Z is one of the two major sensors that triggered an alarm, the maintenance officer shuts the plant only if another sensor (minor), “sensor B”, associated with sensor Z also sounds the alarm.

Adam had to dust his Boolean algebra skills to design the truth table that outputs a variable S which indicates when the plant has to shut down. He also has to provide a schematic capture of the same that helps the maintenance officer to understand the conditions for the plant shutdown. Imagine “U” were Adam, and provide a viable solution.

Major Sensors X, Y, Z
Minor Sensor B

(X AND Y) OR (X AND Z AND B) OR (Y AND Z AND B) = True
S = X.Y + X.Y.Z + B.Y.Z + B.X.Z + B.X.Y + B.X.Y.Z
S = X.Y + B.X(X+Y)
. AND
+ OR
‘ NOT

'AND' keyword in VHDL is to represent '.' (and gate) operation in Boolean Expression.
'OR' keyword in VHDL is to represent '+' (or gate) operation in Boolean Expression.
'NOT' keyword in VHDL is to represent 'Apostrophe' (not gate) operation in Boolean Expression.

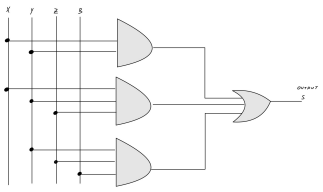
The alarm will shut down if and only if Z and or any other major sensor is switched on.
If Z and B are turned on, then the alarm will turn on. Otherwise the alarm will not be on.

The following output for variable S is True if and only if:

S = X’.Y’ + X’.Z’.B’ + B’ + Y’.Z’.B’

X == 1 & Y == 1 or X == 1 & Z == 1 & B == 1 OR Y == 1 & Z == 1 & B == 1
The variable S is thus False if Otherwise

S <= X.Y + B.X.Z + B.Y.Z



2. Write the truth table for the same.

Inputs				Outputs
X	Y	Z	B	S
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

3. Specify the type of gate and quantity for question 1

The circuit required in the inputs as variables X, Y, Z, and B and the Output required was the Variable S. And gate implementation was required.
2 - input AND Gate - 1 NOT
3 - input AND gate - 2 NOT
3 - input AND gate 1 NOT

4. What does Parse Error in VHDL mean?
Parse errors happen when the code you've written doesn't conform to the syntax or language rules for the language in which you're working. Confronted with the syntax error, the compiler can't make sense of that segment of the program and so refuses to work with it.