EECS 140: Lab 2 Report

# Introduction to VHDL

*Morgan Bergen*

**KUID: 3073682**

*Date submitted: 09/06/2022*

## 1. Introduction and Background

The purpose of this experiment is to increase familiarity with the VHDL-VHSIC Hardware Description Language by implementing basic digital logic that describes what functionalities that the hardware must compute and what components are to be connected for such computation. By utilizing simple circuits and applying syntax for scripting AND and OR gate implementation this lab increases one familiarity with Vivado and Adept software.

The behavior that was coded for this experiment was Y = A'.B' + B.C' + B'.C this assignment statement provided the basis design of the Basys3 Board and generalized that assigned inputs and outputs of the FPGA board.

## 2. Implementation Process

The project required creating a new VHDL scripting during entry wizard, write behavioral code to implement the the assignment statement Y = A'.B' + B.C' + B'.C (Read As: Y equals A not and B not, or B and C not, or B not and C. This assignment statement scripted as the following string literal,

```
Y <= ((NOT A) AND (NOT B)) OR ((B) AND (NOT C)) OR ((NOT B) AND (C))
```

After such code was scripted using VHDL, the design for the Basys3 Board required creating an Xilinx Design constraints file which contained the extension XDC (.xdc). This design constraints file ensured that the proper inputs and outputs of the design were affiliated to the correct pins ion the FPGA board. Generating the designing the constraints file, writing the following script as the following string literal was required as follows,

```
 ## Switches
set_property PACKAGE_PIN V17 [get_ports {A}]
      set_property IOSTANDARD LVCMOS33 [get_ports {A}]
set_property PACKAGE_PIN V16 [get_ports {B}]
      set_property IOSTANDARD LVCMOS33 [get_ports {B}]
set_property PACKAGE_PIN W16 [get_ports {C}]
      set_property IOSTANDARD LVCMOS33 [get_ports {C}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {Y}]
      set_property IOSTANDARD LVCMOS33 [get_ports {Y}]
```

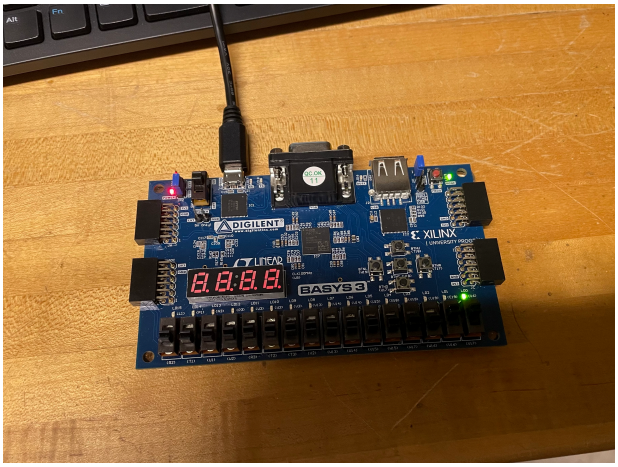
Uncommenting the corresponding lines to use the pins and renaming the ports after (get_imports) accorded to the top level sign names in the project. These Assigned names were A, B, and C to slide switches V17, V16, and W16. A == V17

B == V16

C ==W16

Y==U16

Thus assigning the outputs as well, after setting up the architecture of the project from scripting to the correct files, the design was then synthesized (with no errors or warnings) and implemented. On successful completion of implementation Bitstream generation was executed, the target was assigned to the BASYS3 Board (specifically as device ID XC7A35T-1CPG236C) and the programed into the hardware. Upon completion the following output was displayed with such configuration. (Figure 1.1)




**(Figure 1.1)**

### 3. Evaluation Process

The evaluation process entailed checking for the correct LED output onto the board, this output if correct would reflect the logic as shown in the following truth table of the assignment expression. **(Figure 1.2)**

| A | B | C | A' | B' | C' | A' . B' | B . C' | B . C' | B' . C | Y = A' . B' + B . C' + B' . C |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**(Figure 1.2)**

## 4. Results & Discussion

The results of the project were the return values of the sequential assignment statement. If the Boolean network was described correctly in the hardware and the direct relationship between the inputs and output would directly reflect the truth table upon testing for switches.

```
Y <= ((NOT A) AND (NOT B)) OR ((B) AND (NOT C)) OR ((NOT B) AND (C))
```

This is the VHDL syntax, syntax is the arrangement of words and phrases to create well-formed sentences in a language or a set of rules for or an analysis of the syntax of a language it helps ensure that the correct signals and ports are assigned within the output function. This would be written within the BEGIN and END Behavior of the implementation file. For example if A, B, and C were all switched on which corresponds to the value 1 on the truth table, the LED output would be turned off. If A, B, C were all switched off then the LED output at port W16 would one turned on.

## 5. Conclusions and Recommendations

The ending of this lab increased familiarity and re assured exposure to the development environment of the Vivado HLx Edition suit for scripting VHDL logic. The purpose of this project was to again verify the functional correctness of the Boolean logic as presented in the Assignment statement that was scripted into the implementation file. Upon successful scripting, synthesis, implementation, and bitstream generation the correct output verified the logic of the syntactical specifications. All output was sound and diligently verified.