EECS 140 Encoder and Decoder

Implementation of Decoder and Encoder

Contents

PreLab

No prelab for Lab

Objective

In this Lab we will look at decoder and encoder circuits. Decoder circuits have n inputs and up to 2n outputs. One output is associated with each possible binary input. Encoders are the opposite of decoders. They have 2n inputs and n outputs. For this lab, we design and implement a 3-to-8 decoder and 8-to-3 encoder.

Discussion

- A decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different e.g. n-to-2n , binary-coded decimal decoders. Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address decoding.

Encoders are combinational logic circuits and they are exactly opposite of decoders. They accept one or more inputs and generate a multibit output code. An encoder has M input and N output lines. Out of M input lines only one is activated at a time and produces equivalent code on output N lines. If a device output code has fewer bits than the input code has, the device is usually called an encoder. The logic circuit of a 8-to-3 encoder and 3-to-8 decoder is presented below

1. EncoderDecoder (http://www.ittc.ku.edu/EECS/EECS_140/wiki/EncoderDecoder.pdf)

Tasks

Step 1:

1. Write the truth table (must be included in Lab Report) for 3-to-8 Decoder shown in the figure above (attachment in discussion section)
2. Input: X which is a 3 bit vector
3. Output: Y which is a 8 bit vector
4. To describe the behavior of the circuit, write the logical equations governing the outputs. You should have eight such equations.
5. How do you verify the correctness of the design on the FPGA board?

Step 2:

Create a new Vivado project for the 3-to-8 Decoder circuit as follows:

1. Create a new project for the Decoder on your H:// drive.
2. Generate a VHDL file for the above schematic provided and include it in the project.
3. Implement the 3-to-8 Decoder onto Basys3 Board.

XDC File Basys3_Constraints

Step 3:

1. Write the truth table (must be included in Lab Report) for 8-to-3 Encoder shown in the figure above (attachment in discussion section)
2. Input: X which is a 8 bit vector
3. Output: Y which is a 3 bit vector
4. To describe the behavior of the circuit, write the logical equations governing the outputs. You should have three such equations.
5. How do you verify the correctness of the design on the FPGA board?

Step 4:

1. Create a new .vhd file for the Encoder
2. Implement the 8-to-3 Encoder onto Basys3 Board.

Step 5: (2:1) Multiplexer(Honors)

1. Data inputs as (a & b) and Select input as (S)
2. Output Y: select Y = a when S = 0 and select Y = b when S = 1
3. Create a new .vhd file for the Multiplexer
4. You can use either one of IF statement, CASE statement, WITH-SELECT-WHEN or direct relationship statements
5. Assign a, b, and s to slide switches
6. Assign Y to LED0
7. Implement the 2:1 Multiplexer onto Basys3 Board.

XDC File Basys3_Constraints (https://www.ittc.ku.edu/EECS/EECS_140/wiki/Basys3_Master.txt)

Multiplexer [1] (https://wiki.ittc.ku.edu/ittc_wiki/images/2/23/2to1_Mux.jpg)

Lab Report

Now write your lab report according the format outlined by your TA. Your lab report should include any suggestions of improvements or ways you believe this lab exercise could have been implemented better.

Acknowledgment

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