EECS 140: Lab 3 Report

Implementation of Nuclear Power Plant Control Circuit

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1. Introduction and Background

The purpose of this experiment was to not only design a logic circuit in VHDL, but also to derive a Boolean logic Network from a problem statement, that of which applied to the implementation of a nuclear power plant control circuit. The nuclear power plant required two types of gate and quantities the sensors alarm the sound system. The alarm will shut down if and only if Z and or any other major sensor was switched on, if Z and B are turned on then the alarm would be turned on as well, otherwise the alarm would be off. The way in which this project tied in with previous projects is that it still utilized the same program environment which was the Vivado test suit.
The expression that was derived from the problem statement is as follows

```
S <= X.Y + B.X.Z + B.Y.Z
```

Additionally the following truth table and scheme are provided below. The table essentially outlines all of the possible configurations of the control system. Where by the S would indicate an alarm. The circuits required in the input as variable, X, Y, Z, and B and the output required was the variable. And and Not gates were used for the implementation. Specifically 1 2 - input AND gates, and 2 3-input AND gates, to one no gate

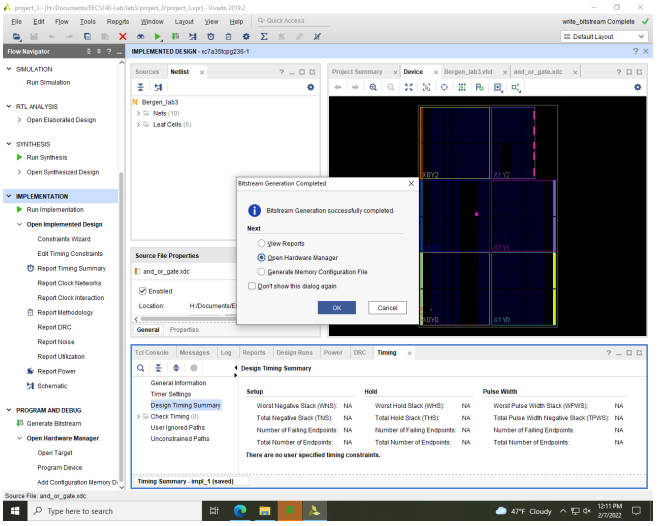
INPUT				OUTPUT
X	Y	Z	B	S
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

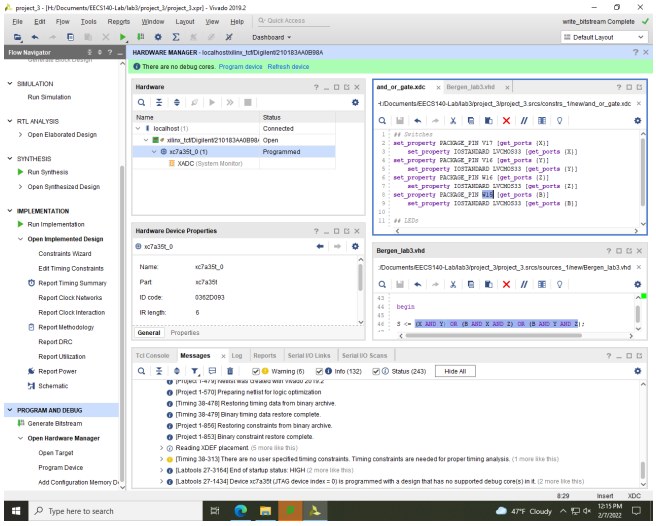
2. Implementation Process

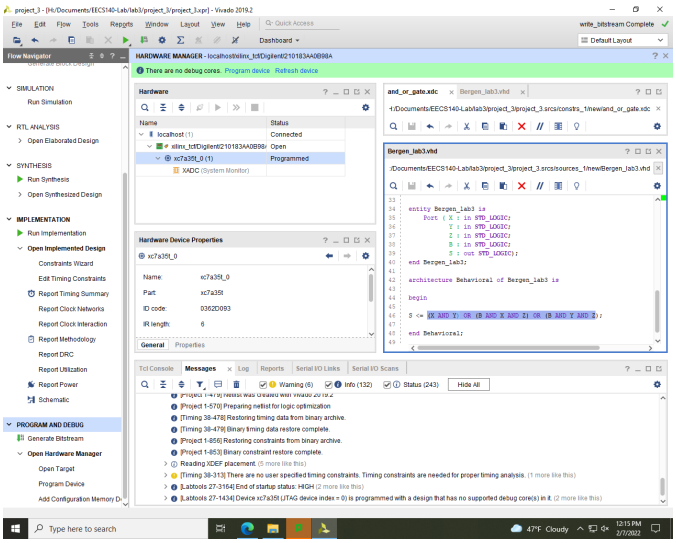
The implementation process consisted of writing up the {} into the begin and end Behavioral of the .vhd file which, specifically the script

```
S <= X.Y + B.X.Z + B.Y.Z
S <= (X AND Y) OR (B AND X AND Z) OR (B AND Y AND Z);
```

Then setting the switch and led properties that corresponded to the constraints file for the .xdc file these ports were labeled as the variables X, Y, and Z for the inputs and S for the outputs. Because there were no faults or syntax errors affiliated with these two files the hierarchy of designs were prepared to be synthesized, implemented, generated into bitstreams, and programmed into the hardware of the device.

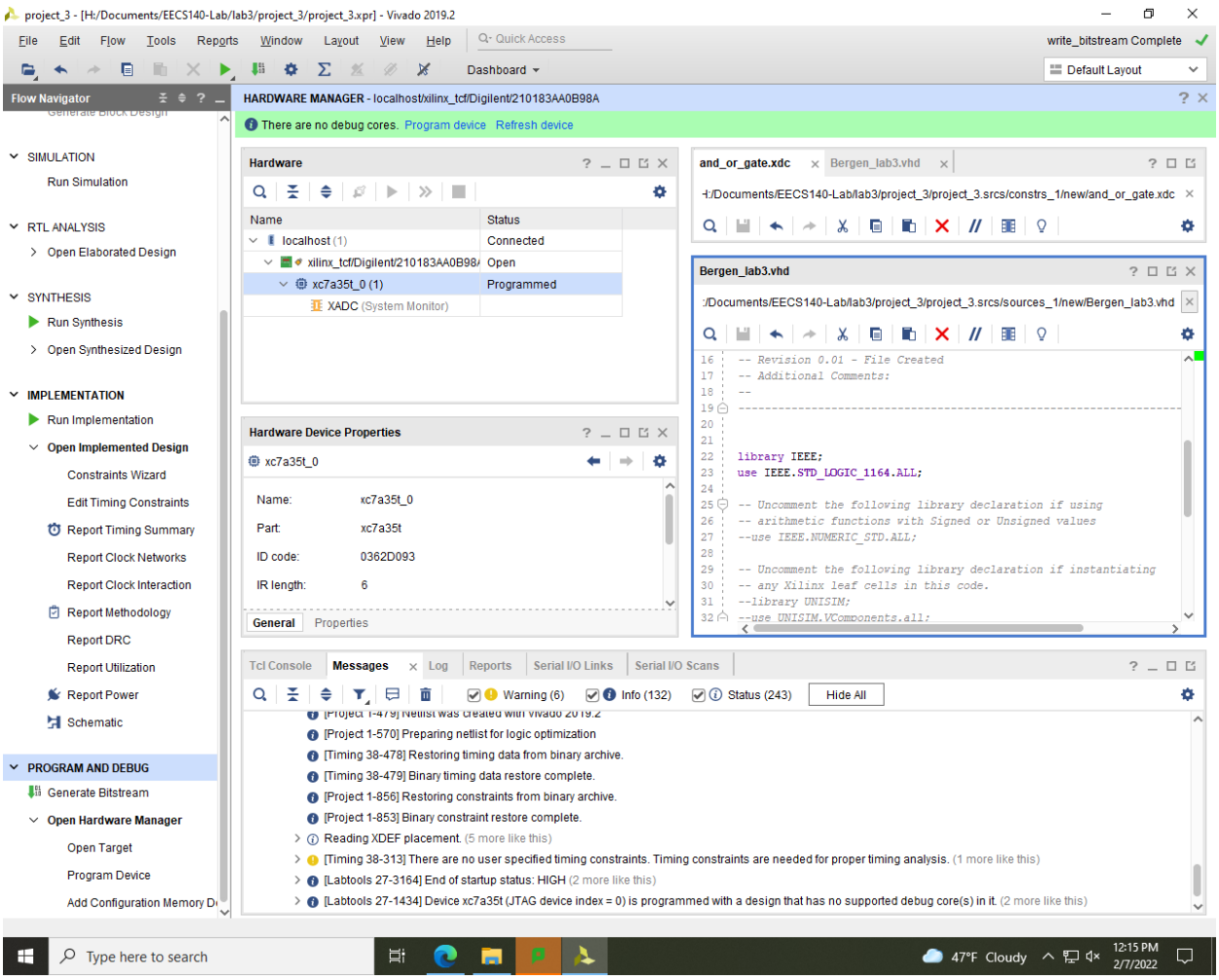






3. Evaluation Process

The evaluation process required making sure that all of the outputs on the device corresponded to the outputs that the truth table as outlined in Part 1 outputted. The binding operations of and and or gates evaluated the output of the function.



4. Results & Discussion

The results of this project consisted of the LED indicating on and then indicating off corresponding to the truth table. These results must have followed the logical operations from the final S output.

5. Conclusions and Recommendations

The final conclusion of this project taught out to implemented functions within the program and help build a more robust familiarity with the program.