

EECS 140: Lab 5 Report

Implementing a SOP Expression on Prototyping board

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1. Introduction and Background

The purpose of this experiment is to solder IC sockets, bypass capacitors, power, ground buses, and interconnections headers in order to implement a SOP expression. That expression being specially the following line,

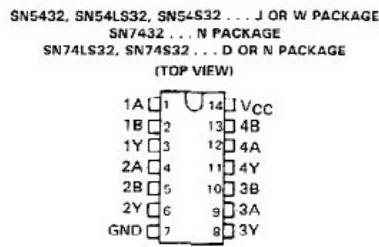
$$f = A \cdot \bar{B} \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot D$$

The preceding lab, Lab 4: Introduction to prototype board ensured that we had a solid foundation in order to be able to run simple boolean computations onto the hardware. That lab ensured that we had properly installed three main sections onto the prototyping board Power, Input Circuit Section, Switch Circuit Section, LED Display Section built and prepared in order to implement our expression. That lab additionally ensured that we had a minimally viable and functioning board and tested that viability by performing a first board test, specifically the LED display of the components presenting negative logic. The previous lab was quintessential and tied in directly to this currently lab for which the main activities taken place was installing the bypass capacitors, IC society, 7400 series ICs, power and ground buses, IC connection headers, and interconnection headers properly to perform the expression.

2. Implementation Process

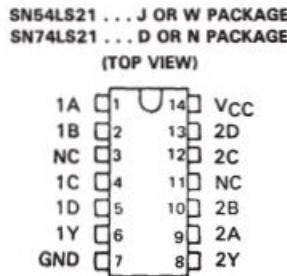
The process to initial set-up the experiment entailed installing physical components into the board and connecting those components with jumpers. The following list outlines the equipment, location, functional, and soldering action for each component of the board,

1. 3x Bypass Capacitors: At locations C2, C3, C4. The purpose of this capacitor is top shorts AC signs to the ground.
2. 3x 16-pin IC Sockets: At locations U1, U4, U7. The purpose of the IC sockets were deigned specifically top provide an interconnection between the component leads and the printed circuit board.
3. 1x 74LS32 2 Input OR Gate: At location U1 a top of the IC Socket specifically in the top left socket where the orientation faced inward, where the cut out notice in the IC faced the bypass capacitor. The purpose of this device is to provide an independent 2-input OR gate. Illustrated in (figure 1).



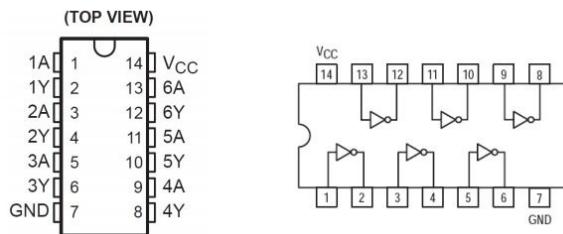
(Figure 1)

4. 1x 74LS21 Input AND Gate: At location U4 a top of the IC Socket, specifically in the middle row, where the orientation faced inward, where the cut out notice in the IC faced the bypass capacitor.. The purpose of this device was to contain a two independent 4-input AND gate. Illustrated in (figure 2).



(Figure 2)

5. 1x 74LS32 Input NOT Gate also known to be (HEX Inverter): At location U7 a top of the IC Socket, specially in the bottom socket, where the orientation faced inward, where the cut out notice in the IC faced the bypass capacitor. The purpose of this NOT gate was to perform functional inversion to basic logic. This gate has only one input and one output. Illustrated in (figure 3).

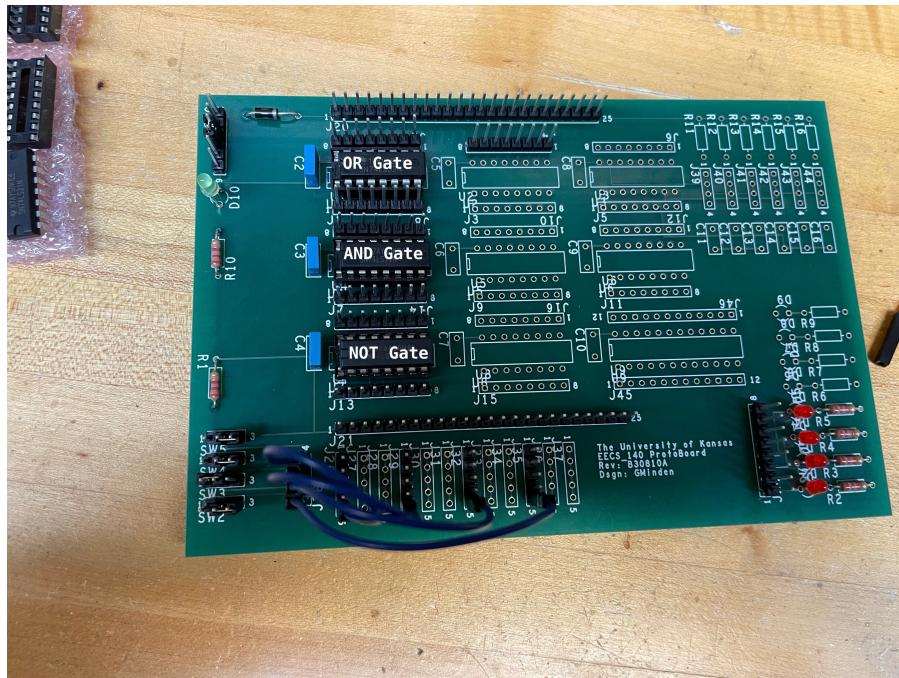


(Figure 3)

6. 1x Power Bus: At location J20. The purpose of at the power bus is to be the horizontal line at which the several components of the power system are connected. The power bus will be used in this context to provide the VCC to ICs or to the logic ‘1’ level.
7. 1x Ground Bus: At location J21. The purpose of the ground bus is the ground bus in this implementation context is to be used to ground the ICs or logic ‘0’ level.
8. 4x IC 5-pin Connection Headers: At locations J35, J32, J29, and J26. These headers were used to extend the switch inputs or in other words duplicate the IC pins.
9. 6x IC 8-pin Connection Headers: At locations J2, J1, J8, J7, J14, and J13. These are used as connection headers for the top and bottom pins of the IC.

After successful sobering and placement of the individual units in their corresponding locations. The board is ready to be connected using jumpers and adhering to the following boolean expression. (Figure 4)

$$f = A \cdot \bar{B} \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot D$$



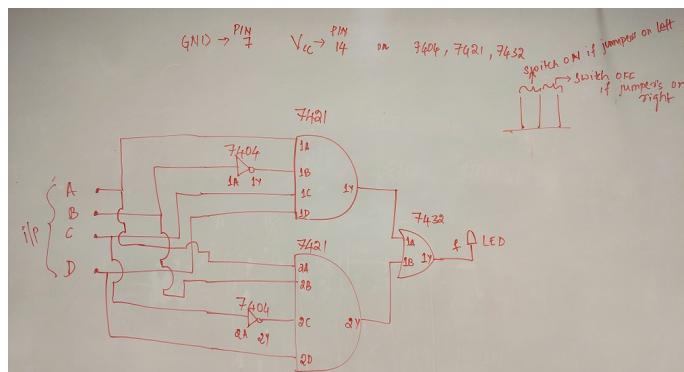
(Figure 4)

3. Evaluation Process

The evaluation process consisted of connecting the SW2, SW3, SW4, SW5 duplicated inputs with jumpers to the J38 4-pin header (figure 4 illustrates this connection). The next step was to follow the boolean expression,

$$f = A \cdot \bar{B} \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot D$$

And abide to the logic diagram outlined in figure 5.



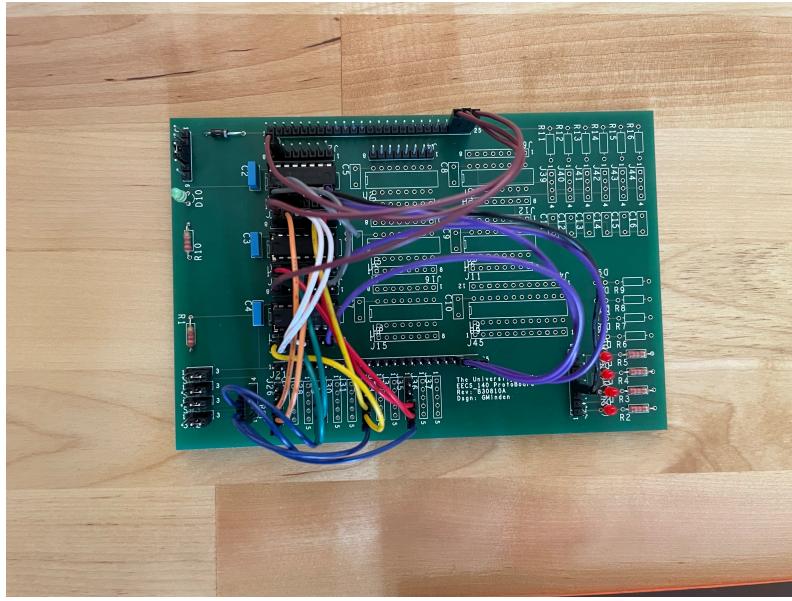
(Figure 5)

By connecting all of the correct corresponding jumpers to the NOT, AND, and OR gates to the inputs. The truth table must be written whereby logic 0 input: Jumper to Right 2 pins of header strip and Logic 1 input: Jumper to the Left 2 pins of header strip indicate that output F \rightarrow True logic 1/LED OFF or an output of F \rightarrow False logic 0/LED on.

$$F = A \cdot B' \cdot C \cdot D + A \cdot B \cdot C' \cdot D = AD(B'C + BC')$$

Truth Table is as follows.

<u>SW5</u>	<u>SW4</u>	<u>SW3</u>	<u>SW2</u>	<u>F</u>
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



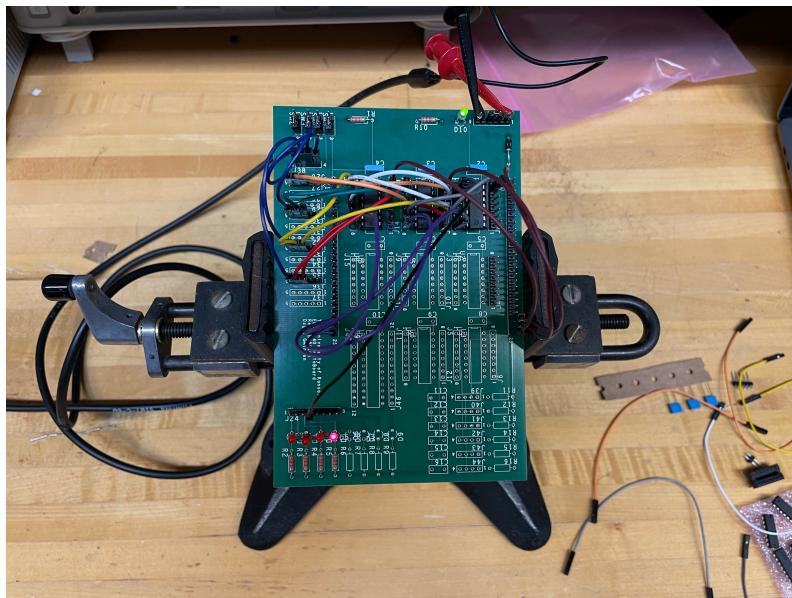
(Figure 6)

The final jumper connections provide the basis necessarily for us to run the logic onto. (Illustrated in Figure 6)

4. Results & Discussion

With the correct configurations in place the LED green light should incite ON if the output is 0 and OFF if the output is 1. The truth table that was outlined provided a grounds for demonstrating this, now because there are only two possible permutations of the switch inputs in which to indicate an output for F that is 1. I tested the board with the following configuration set. Illustrated as the final result in figure 7.

<u>SW5</u>	<u>SW4</u>	<u>SW3</u>	<u>SW2</u>	<u>F</u>
1	0	1	1	1



(Figure 7)

5. Conclusions and Recommendations

The final implementation provides a solid foundation for programmers (Computer Science Undergraduates) to understand how hardware outputs map onto boolean expressions.