EECS 140: Lab 8

Lab08: Four Bit Adder with Double 7-Segment Display

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1. Introduction and Background

The purpose of this lab is to create a binary 4-bit adder and display the result on two 7-segment outputs and a multiplier. This is done by using Xilinx, and from the previous lab, we then connect the result of the adder to the input of your display drivers. Then there after we programmed the circuit design to the board and tested proper functionality of the circuit, to find out the equation we used K-mapping and Sum of Products that led us to the output, specially the S and C outputs. We also learned about VHDL code modularization.

2. Implementation Process

The implementation process entailed

step 1: vhdl tutorial

we needed to defined the VHDL modular design and starting with the component definitions

step 2: ripple carry adder design

we used the source files to define the

bit_full_adder.vhd

display_driver.vhd

led_display.vhd

top_level.vhd

step 3: 7 segment display

step 4: top-level.vhd

- we made sure to use the 1-bit full adder to create the signal assent for the sum and carry
- defined the 4-bit inputs and 7-bit controlling 7 segment output for the 7-segment display
- defined the LED display, this was defined by the display_driver
- we then provided a toplevel.vhd file and port map for the components

step 5: XDC file for top level

- we declared and defined the ports in the entity declared in the constraints file.

step 6: download the board

step 7: evaluate and correct

The following screenshots demonstrate the implementation details of the full_bit_adder.vhd, constraints.vhd, display_driver.vhd, LED_display.vhd, and top_level.vhd from page 4 - 12.

The equipment that was required was the basics of what we have been using in the previous labs which were the vivado software and the basys 3 board. Family: Artix-7, Package: CPG236, Speed: -1 Part: xc7a35tcpg236-1

3. Evaluation Process

We needed to change inputs using the slide switches and make sure that we have the correct corresponding outlet. If we found that we did not have the correct output we probably would have to verify that our in assignments are correct.

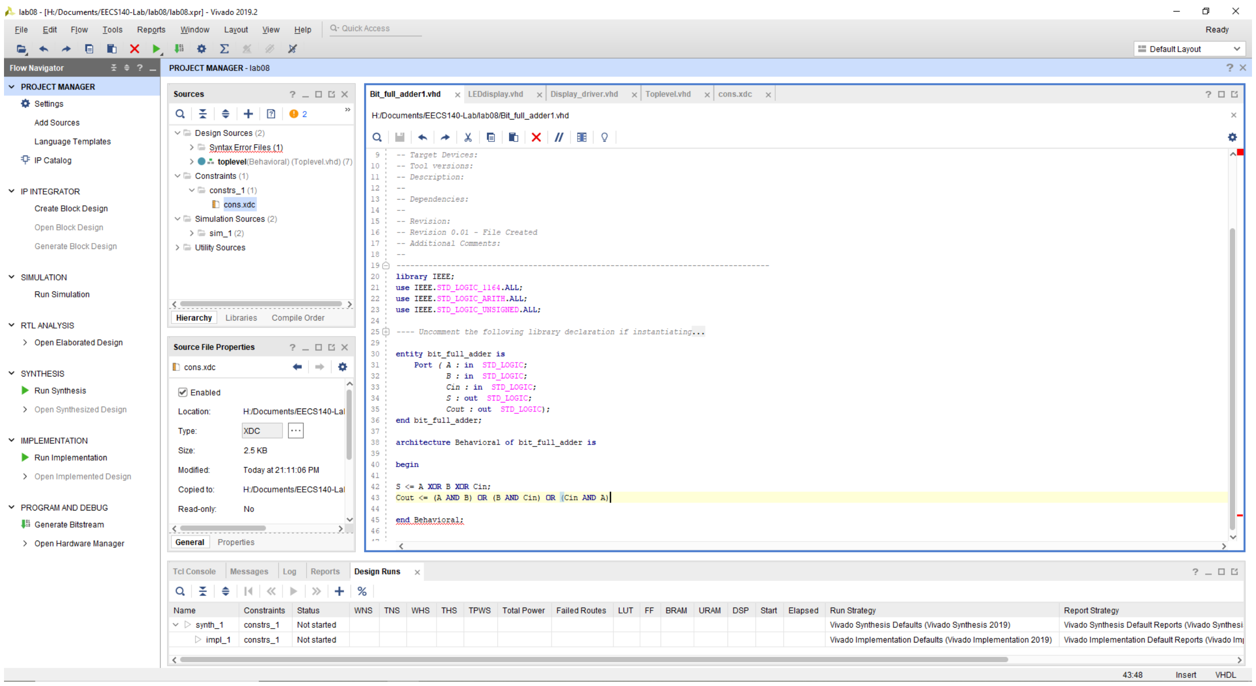
4. Results & Discussion

Switches were set to all 1s and 7-segment display was finally showing an E1.

5. Conclusions and Recommendations

This lab helps me learn the modularity design practices of VHDL to create a real world application and implement an adder unit into the FPGA chip and display the addition results. Upon using the 4-bit adder circuit I learned how to connect the result of the adder to the input of my display driver and deign the circuit design to ensure the functionality is working properly.

Note: You will need to create new project in H:// (as in the earlier labs) and provide these details: Family: Artix-7, Package: CPG236, Speed: -1 Part: xc7a35tcpg236-1 bit_full_adder1.vhd



lab08 - [H:/Documents/EECS140-Lab/lab08/lab08.xpr] - Vivado 2019.2

PROJECT MANAGER - lab08

Sources

- Design Sources (2)
  - Syntax Error Files (1)
  - toplevel(Behavioral) (Toplevel.vhd) (7)
- Constraints (1)
  - constrs_1 (1)
    - cons.xdc
- Simulation Sources (2)
  - sim_1 (2)
- Utility Sources

Source File Properties

cons.xdc

Enabled	✓
Location:	H:/Documents/EECS140-Lal
Type:	XDC
Size:	2.5 KB
Modified:	Today at 21:11:06 PM
Copied to:	H:/Documents/EECS140-Lal
Read-only:	No

H:/Documents/EECS140-Lab/lab08/Bit_full_adder1.vhd

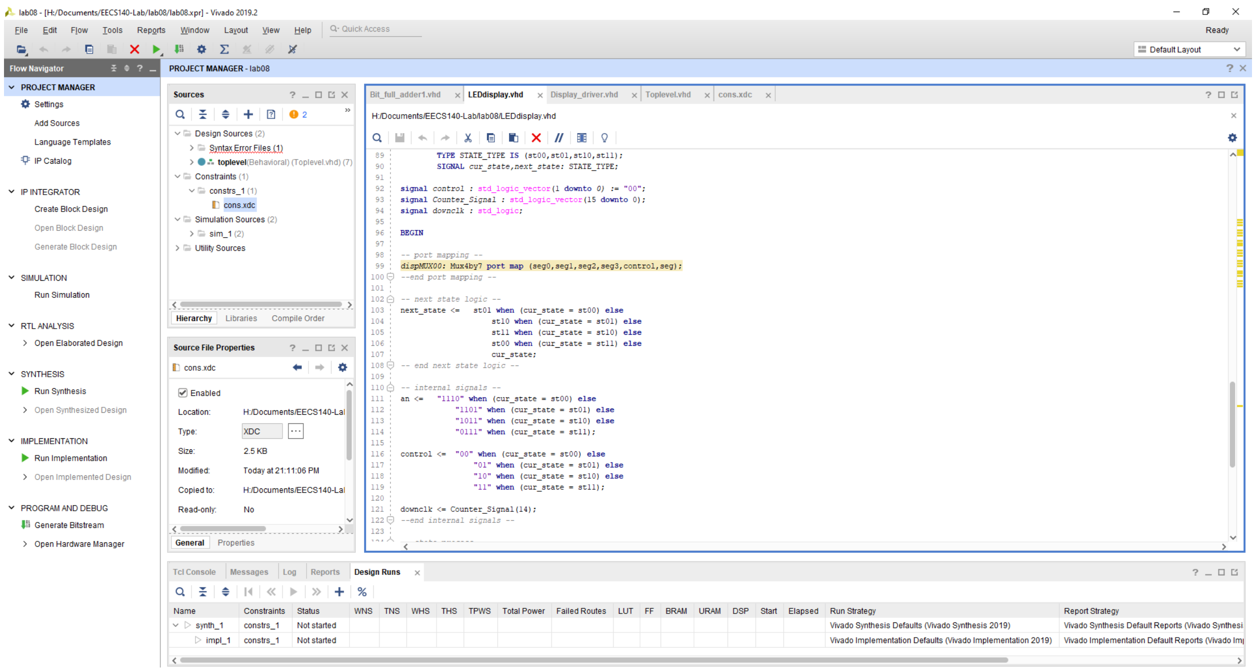
```vhdl
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating...

entity bit_full_adder is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           Cin : in  STD_LOGIC;
           S : out  STD_LOGIC;
           Cout : out  STD_LOGIC);
end bit_full_adder;

architecture Behavioral of bit_full_adder is

begin

S <= A XOR B XOR Cin;
Cout <= (A AND B) OR (B AND Cin) OR (Cin AND A)

end Behavioral;
```

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im

43:48 Insert VHDL

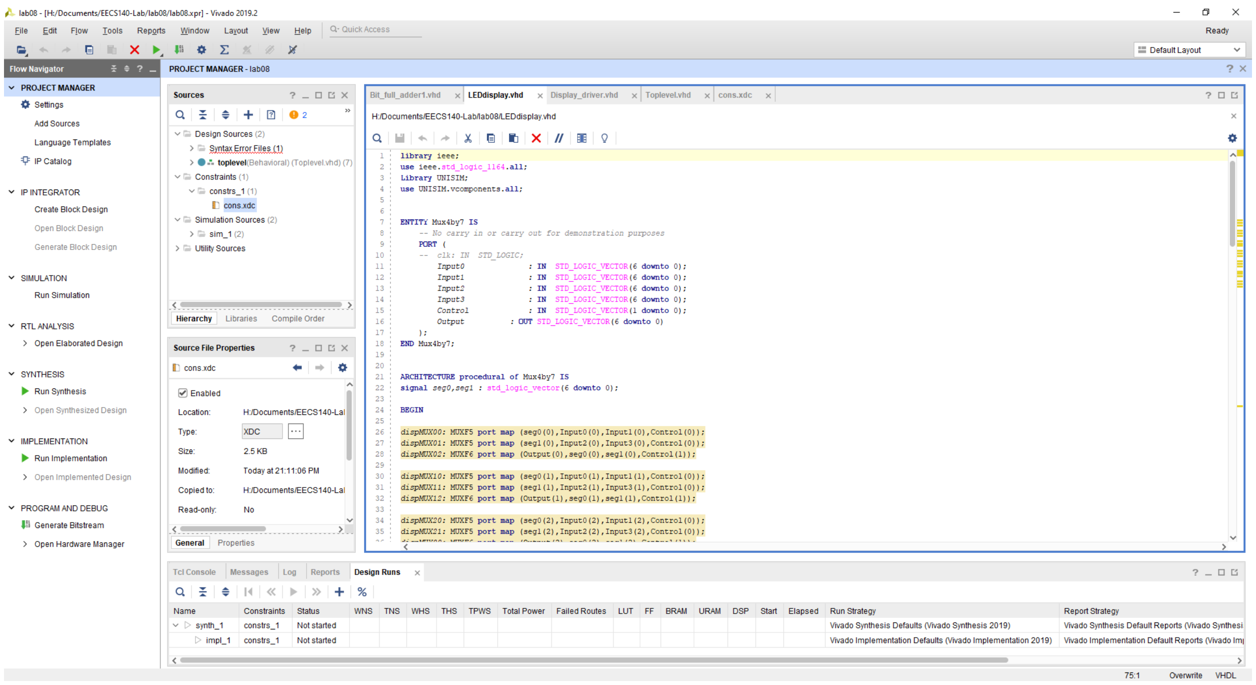
led_display



H:/Documents/EECS140-Lab/lab08/LEDdisplay.vhd

```vhdl
        TYPE STATE_TYPE IS (st00,st01,st10,st11);
        SIGNAL cur_state,next_state: STATE_TYPE;

signal control : std_logic_vector(1 downto 0) := "00";
signal Counter_Signal : std_logic_vector(15 downto 0);
signal downclk : std_logic;

BEGIN

-- port mapping --
dispMUX00: Mux4by7 port map (seg0,seg1,seg2,seg3,control,seg);
--end port mapping --

-- next state logic --
next_state <=   st01 when (cur_state = st00) else
                    st10 when (cur_state = st01) else
                    st11 when (cur_state = st10) else
                    st00 when (cur_state = st11) else
                    cur_state;
-- end next state logic --

-- internal signals --
an <=   "1110" when (cur_state = st00) else
            "1101" when (cur_state = st01) else
            "1011" when (cur_state = st10) else
            "0111" when (cur_state = st11);

control <=  "00" when (cur_state = st00) else
                "01" when (cur_state = st01) else
                "10" when (cur_state = st10) else
                "11" when (cur_state = st11);

downclk <= Counter_Signal(14);
--end internal signals --
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Imp

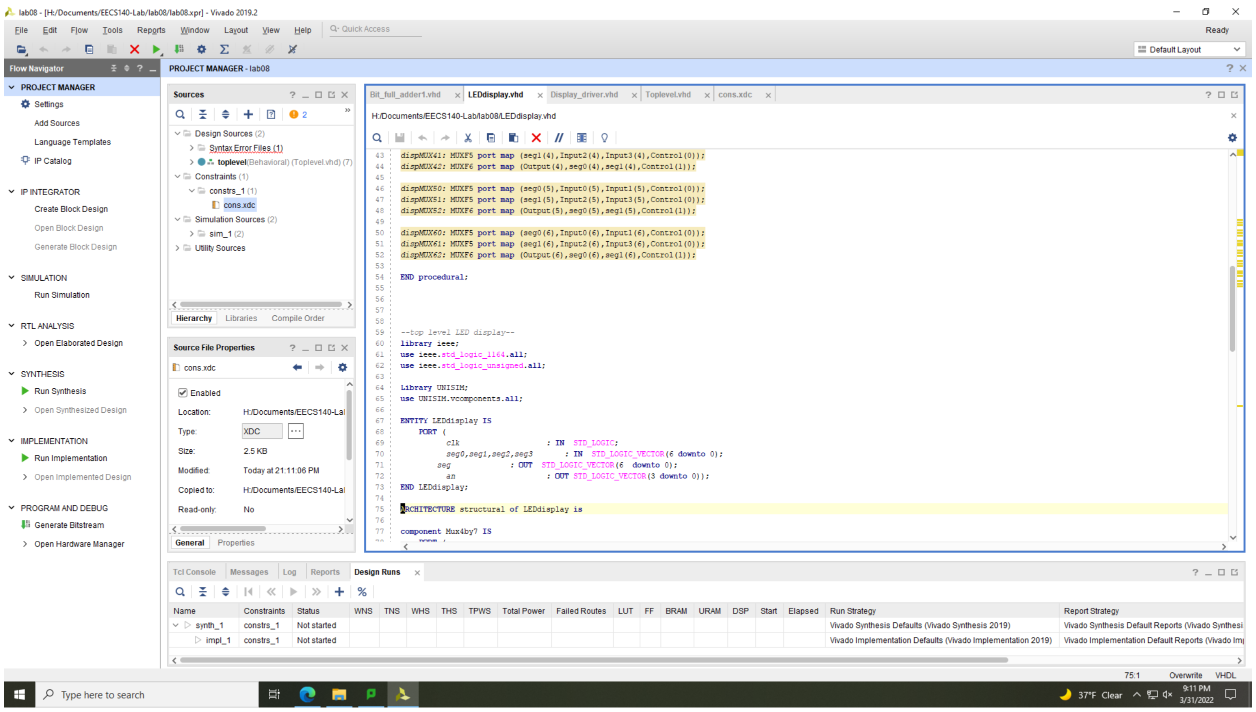


H:/Documents/EECS140-Lab/lab08/LEDdisplay.vhd

```vhdl
library ieee;
use ieee.std_logic_1164.all;
Library UNISIM;
use UNISIM.vcomponents.all;


ENTITY Mux4by7 IS
    -- No carry in or carry out for demonstration purposes
    PORT (
    --  clk: IN  STD_LOGIC;
        Input0              : IN  STD_LOGIC_VECTOR(6 downto 0);
        Input1              : IN  STD_LOGIC_VECTOR(6 downto 0);
        Input2              : IN  STD_LOGIC_VECTOR(6 downto 0);
        Input3              : IN  STD_LOGIC_VECTOR(6 downto 0);
        Control             : IN  STD_LOGIC_VECTOR(1 downto 0);
        Output          : OUT STD_LOGIC_VECTOR(6 downto 0)
    );
END Mux4by7;


ARCHITECTURE procedural of Mux4by7 IS
signal seg0,seg1 : std_logic_vector(6 downto 0);

BEGIN

dispMUX00: MUXF5 port map (seg0(0),Input0(0),Input1(0),Control(0));
dispMUX01: MUXF5 port map (seg1(0),Input2(0),Input3(0),Control(0));
dispMUX02: MUXF6 port map (Output(0),seg0(0),seg1(0),Control(1));

dispMUX10: MUXF5 port map (seg0(1),Input0(1),Input1(1),Control(0));
dispMUX11: MUXF5 port map (seg1(1),Input2(1),Input3(1),Control(0));
dispMUX12: MUXF6 port map (Output(1),seg0(1),seg1(1),Control(1));

dispMUX20: MUXF5 port map (seg0(2),Input0(2),Input1(2),Control(0));
dispMUX21: MUXF5 port map (seg1(2),Input2(2),Input3(2),Control(0));
```

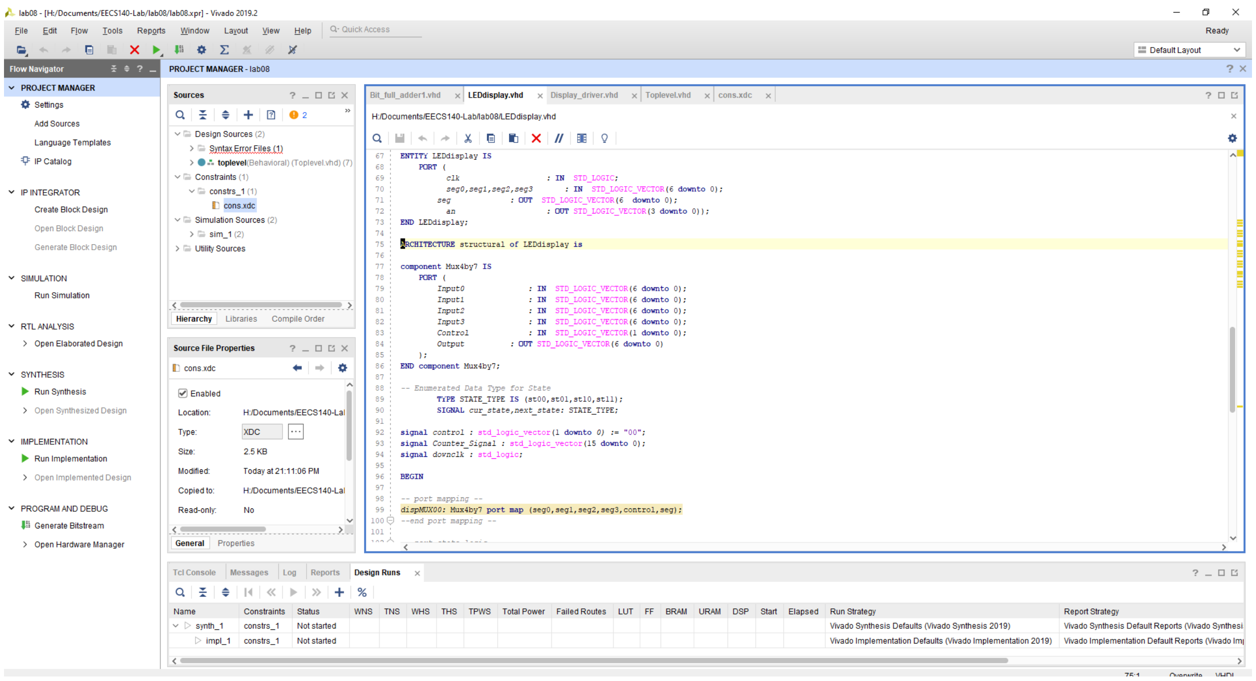
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Imp

led_display continued


H:/Documents/EECS140-Lab/lab08/LEDdisplay.vhd

```vhdl
dispMUX41: MUXF5 port map (seg1(4),Input2(4),Input3(4),Control(0));
dispMUX42: MUXF6 port map (Output(4),seg0(4),seg1(4),Control(1));

dispMUX50: MUXF5 port map (seg0(5),Input0(5),Input1(5),Control(0));
dispMUX51: MUXF5 port map (seg1(5),Input2(5),Input3(5),Control(0));
dispMUX52: MUXF6 port map (Output(5),seg0(5),seg1(5),Control(1));

dispMUX60: MUXF5 port map (seg0(6),Input0(6),Input1(6),Control(0));
dispMUX61: MUXF5 port map (seg1(6),Input2(6),Input3(6),Control(0));
dispMUX62: MUXF6 port map (Output(6),seg0(6),seg1(6),Control(1));

END procedural;




--top level LED display--
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

Library UNISIM;
use UNISIM.vcomponents.all;

ENTITY LEDdisplay IS
    PORT (
          clk                     : IN  STD_LOGIC;
          seg0,seg1,seg2,seg3       : IN  STD_LOGIC_VECTOR(6 downto 0);
        seg             : OUT  STD_LOGIC_VECTOR(6  downto 0);
          an                      : OUT STD_LOGIC_VECTOR(3 downto 0));
END LEDdisplay;

ARCHITECTURE structural of LEDdisplay is

component Mux4by7 IS
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im


H:/Documents/EECS140-Lab/lab08/LEDdisplay.vhd

```vhdl
ENTITY LEDdisplay IS
    PORT (
          clk                     : IN  STD_LOGIC;
          seg0,seg1,seg2,seg3       : IN  STD_LOGIC_VECTOR(6 downto 0);
        seg             : OUT  STD_LOGIC_VECTOR(6  downto 0);
          an                      : OUT STD_LOGIC_VECTOR(3 downto 0));
END LEDdisplay;

ARCHITECTURE structural of LEDdisplay is

component Mux4by7 IS
    PORT (
        Input0                : IN  STD_LOGIC_VECTOR(6 downto 0);
        Input1                : IN  STD_LOGIC_VECTOR(6 downto 0);
        Input2                : IN  STD_LOGIC_VECTOR(6 downto 0);
        Input3                : IN  STD_LOGIC_VECTOR(6 downto 0);
        Control               : IN  STD_LOGIC_VECTOR(1 downto 0);
        Output            : OUT STD_LOGIC_VECTOR(6 downto 0)
    );
END component Mux4by7;

-- Enumerated Data Type for State
        TYPE STATE_TYPE IS (st00,st01,st10,st11);
        SIGNAL cur_state,next_state: STATE_TYPE;

signal control : std_logic_vector(1 downto 0) := "00";
signal Counter_Signal : std_logic_vector(15 downto 0);
signal downclk : std_logic;

BEGIN

-- port mapping --
dispMUX00: Mux4by7 port map (seg0,seg1,seg2,seg3,control,seg);
--end port mapping --
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
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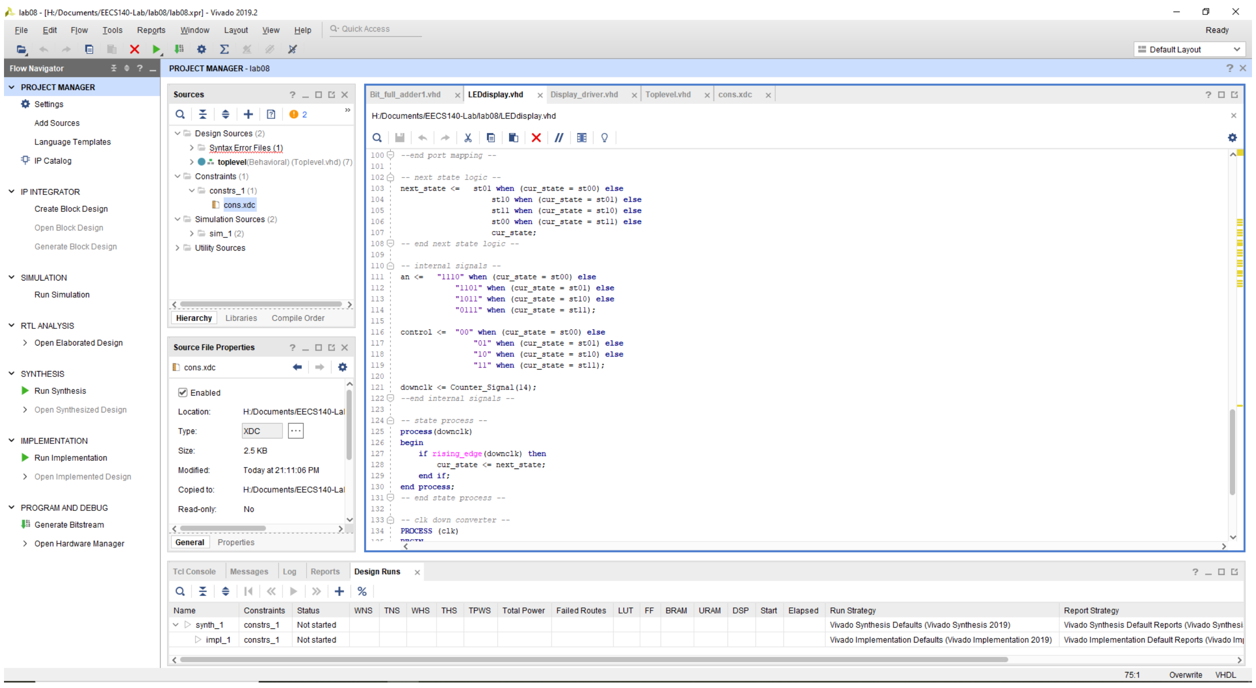
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im

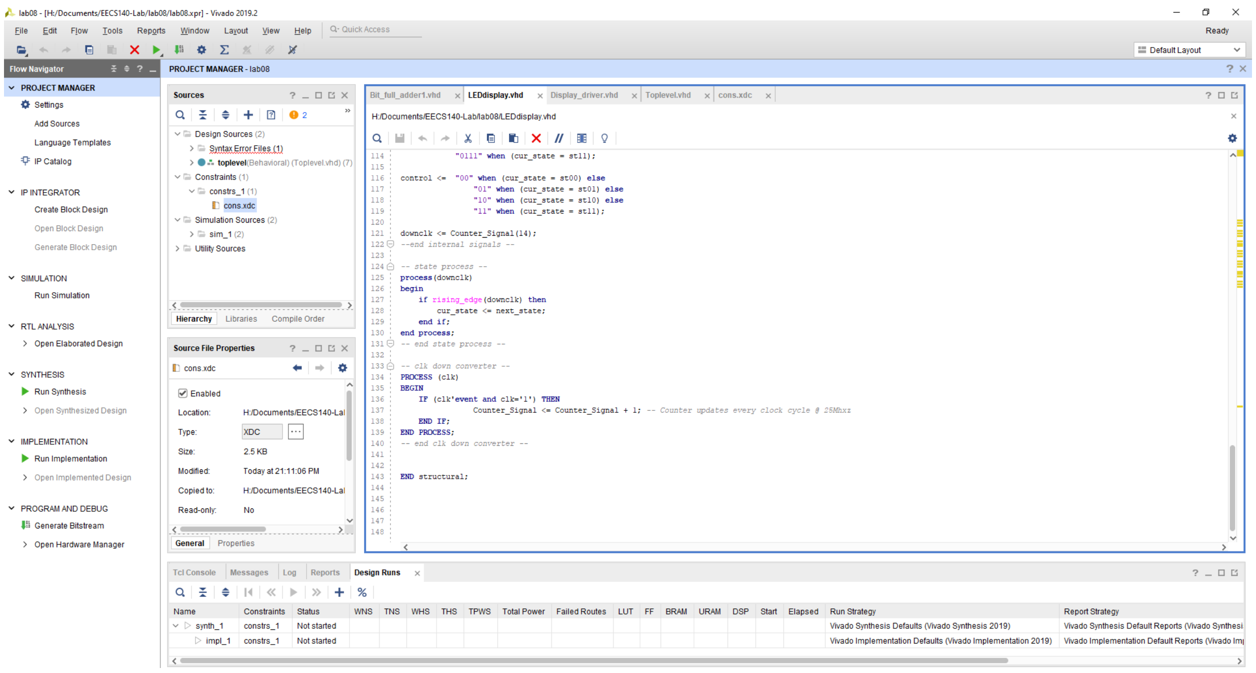
led_display continued



H:/Documents/EECS140-Lab/lab08/LEDdisplay.vhd

```vhdl
--end port mapping --

-- next state logic --
next_state <=   st01 when (cur_state = st00) else
                    st10 when (cur_state = st01) else
                    st11 when (cur_state = st10) else
                    st00 when (cur_state = st11) else
                    cur_state;
-- end next state logic --

-- internal signals --
an <=   "1110" when (cur_state = st00) else
            "1101" when (cur_state = st01) else
            "1011" when (cur_state = st10) else
            "0111" when (cur_state = st11);

control <=  "00" when (cur_state = st00) else
                "01" when (cur_state = st01) else
                "10" when (cur_state = st10) else
                "11" when (cur_state = st11);

downclk <= Counter_Signal(14);
--end internal signals --

-- state process --
process(downclk)
begin
    if rising_edge(downclk) then
        cur_state <= next_state;
    end if;
end process;
-- end state process --

-- clk down converter --
PROCESS (clk)
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Imp

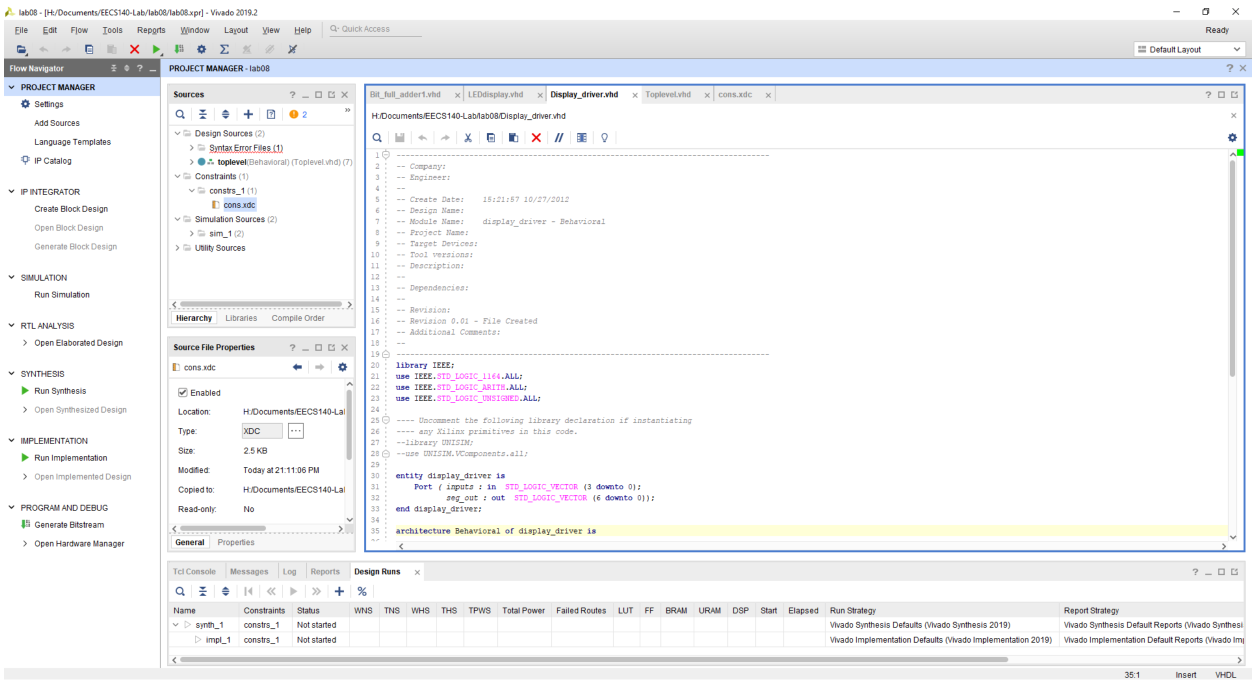

lab08 - [H:/Documents/EECS140-Lab/lab08/lab08.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER - lab08
Sources
Bit_full_adder1.vhd
LEDdisplay.vhd
Display_driver.vhd
Toplevel.vhd
cons.xdc
Hierarchy Libraries Compile Order
Source File Properties
General Properties
Tcl Console Messages Log Reports Design Runs

H:/Documents/EECS140-Lab/lab08/LEDdisplay.vhd

```vhdl
            "0111" when (cur_state = st11);

control <=  "00" when (cur_state = st00) else
                "01" when (cur_state = st01) else
                "10" when (cur_state = st10) else
                "11" when (cur_state = st11);

downclk <= Counter_Signal(14);
--end internal signals --

-- state process --
process(downclk)
begin
    if rising_edge(downclk) then
        cur_state <= next_state;
    end if;
end process;
-- end state process --

-- clk down converter --
PROCESS (clk)
BEGIN
    IF (clk'event and clk='1') THEN
            Counter_Signal <= Counter_Signal + 1; -- Counter updates every clock cycle @ 25Mhxz
    END IF;
END PROCESS;
-- end clk down converter --


END structural;
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Imp

display driver

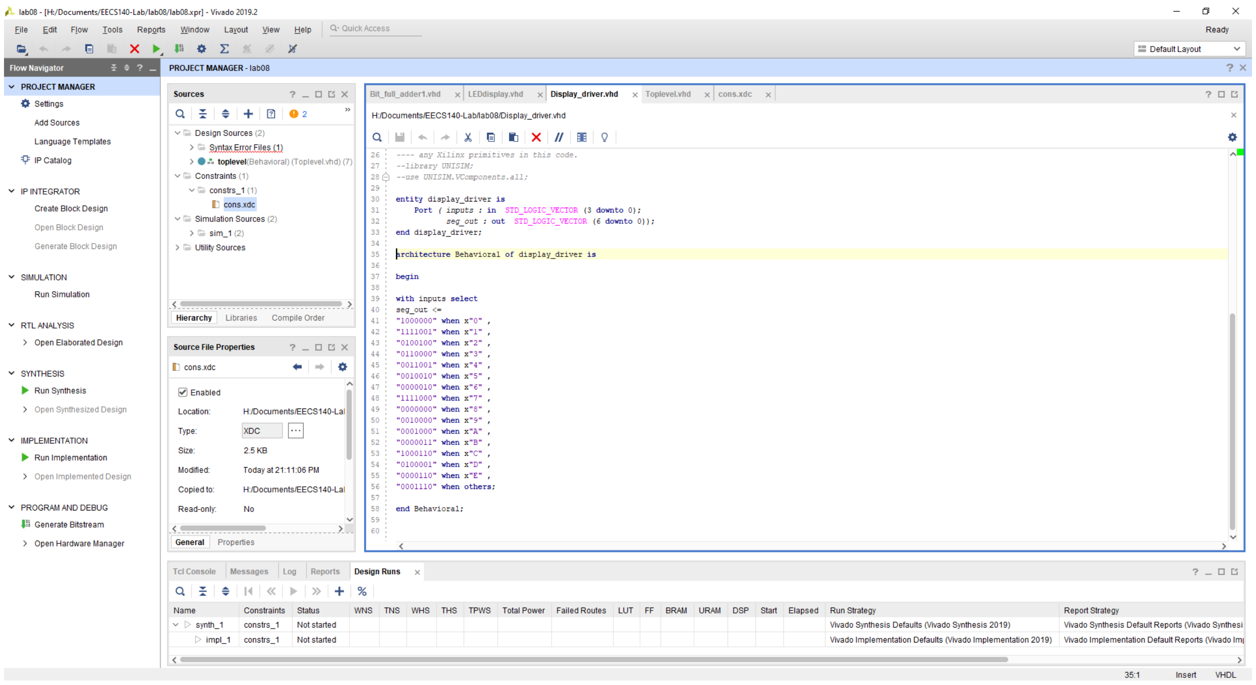


lab08 - [H:/Documents/EECS140-Lab/lab08/lab08.xpr] - Vivado 2019.2

H:/Documents/EECS140-Lab/lab08/Display_driver.vhd

```vhdl
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    15:21:57 10/27/2012
-- Design Name:
-- Module Name:    display_driver - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity display_driver is
    Port ( inputs : in  STD_LOGIC_VECTOR (3 downto 0);
           seg_out : out  STD_LOGIC_VECTOR (6 downto 0));
end display_driver;

architecture Behavioral of display_driver is
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Imp

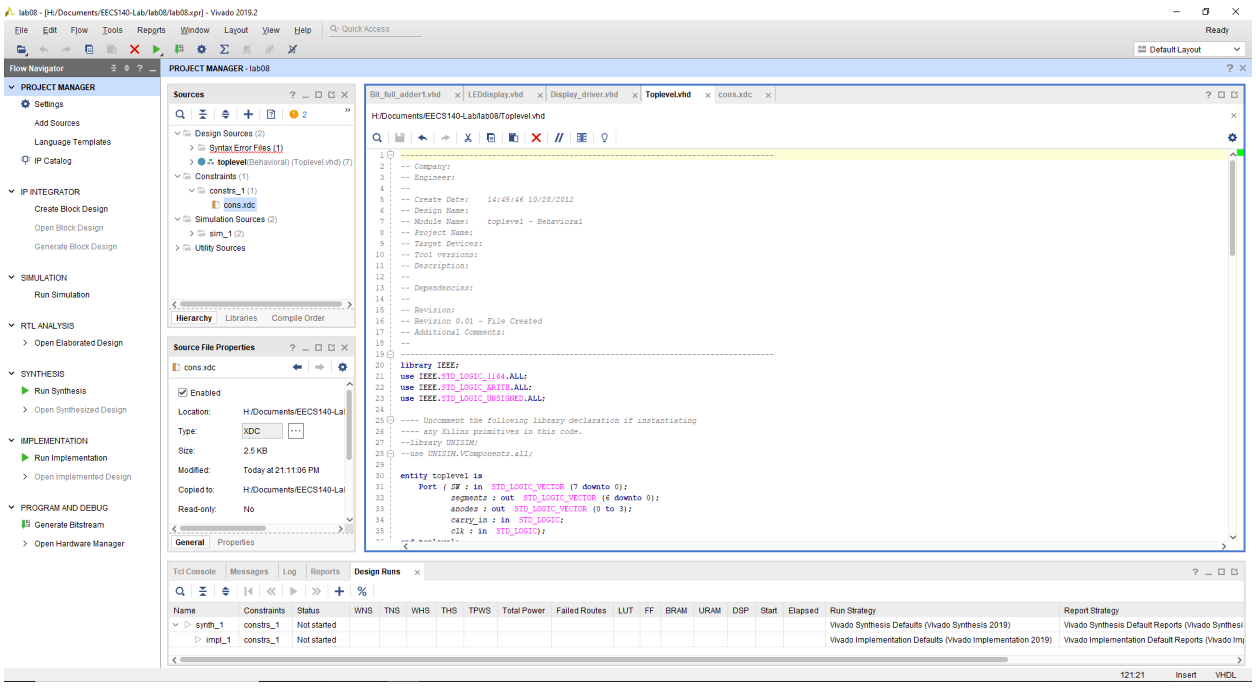


lab08 - [H:/Documents/EECS140-Lab/lab08/lab08.xpr] - Vivado 2019.2

H:/Documents/EECS140-Lab/lab08/Display_driver.vhd

```vhdl
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity display_driver is
    Port ( inputs : in  STD_LOGIC_VECTOR (3 downto 0);
           seg_out : out  STD_LOGIC_VECTOR (6 downto 0));
end display_driver;

architecture Behavioral of display_driver is

begin

with inputs select
seg_out <=
"1000000" when x"0" ,
"1111001" when x"1" ,
"0100100" when x"2" ,
"0110000" when x"3" ,
"0011001" when x"4" ,
"0010010" when x"5" ,
"0000010" when x"6" ,
"1111000" when x"7" ,
"0000000" when x"8" ,
"0010000" when x"9" ,
"0001000" when x"A" ,
"0000011" when x"B" ,
"1000110" when x"C" ,
"0100001" when x"D" ,
"0000110" when x"E" ,
"0001110" when others;

end Behavioral;
```

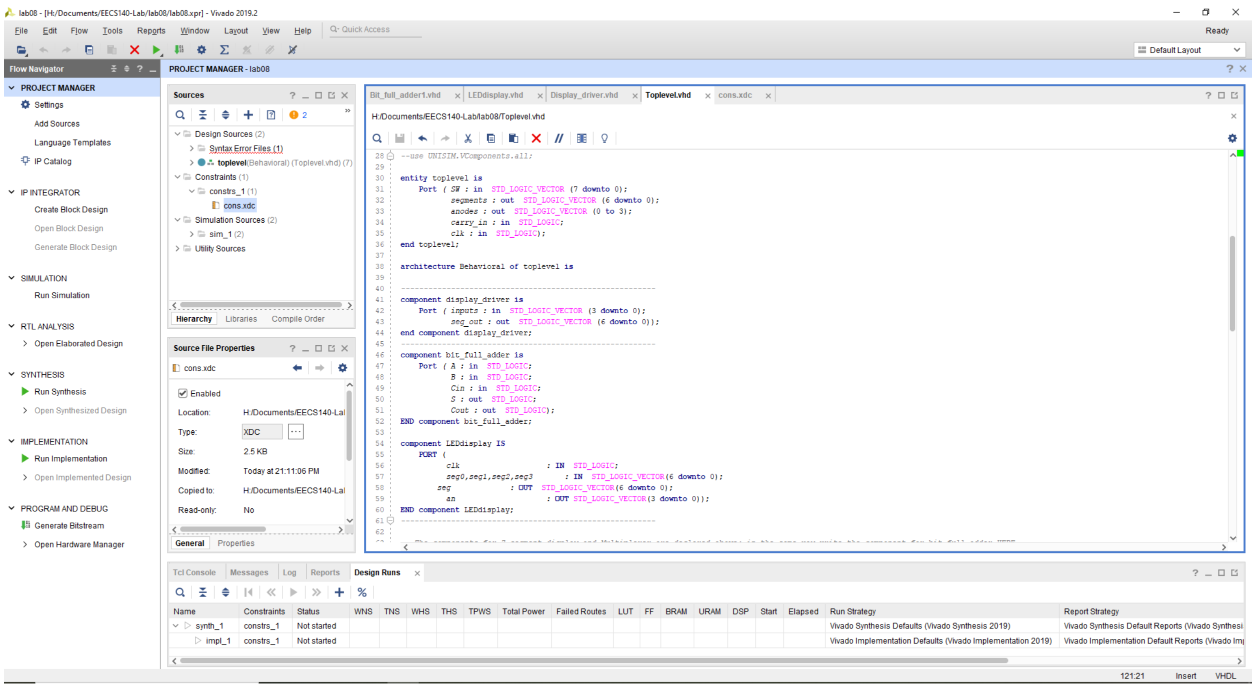
top_level



H:/Documents/EECS140-Lab/lab08/Toplevel.vhd

```vhdl
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    14:45:46 10/28/2012
-- Design Name:
-- Module Name:    toplevel - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity toplevel is
    Port ( SW : in  STD_LOGIC_VECTOR (7 downto 0);
           segments : out  STD_LOGIC_VECTOR (6 downto 0);
           anodes : out  STD_LOGIC_VECTOR (0 to 3);
           carry_in : in  STD_LOGIC;
           clk : in  STD_LOGIC);
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im

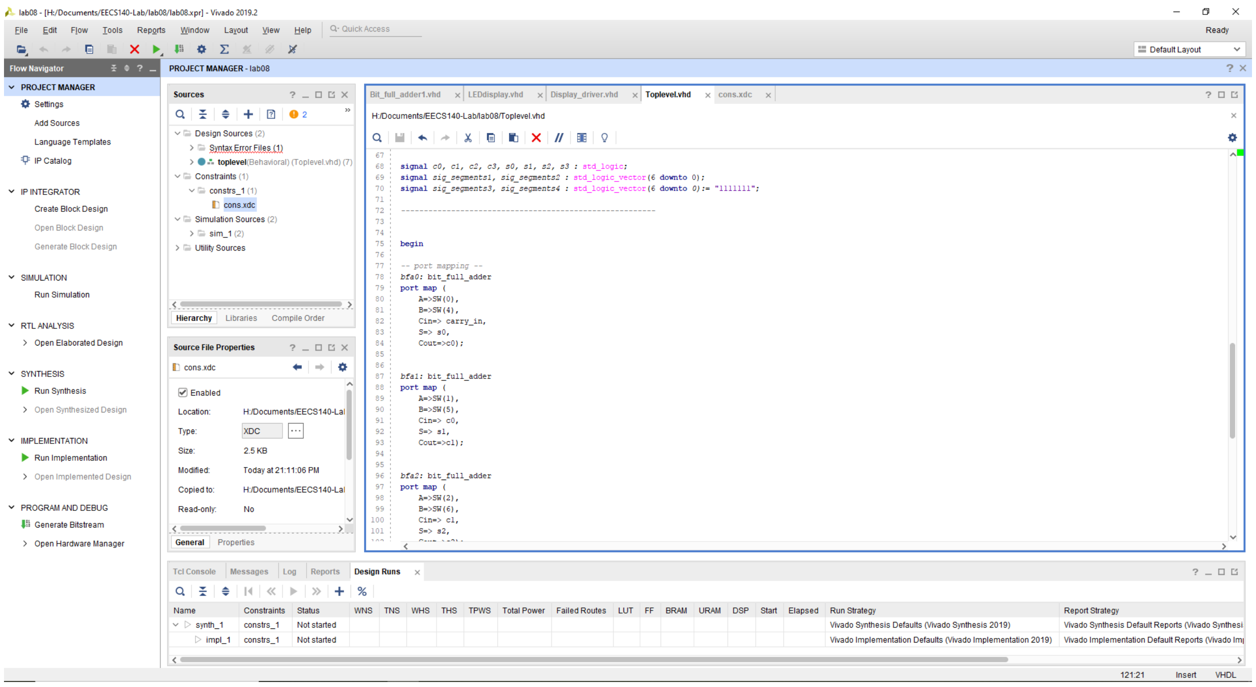


H:/Documents/EECS140-Lab/lab08/Toplevel.vhd

```vhdl
--use UNISIM.VComponents.all;

entity toplevel is
    Port ( SW : in  STD_LOGIC_VECTOR (7 downto 0);
           segments : out  STD_LOGIC_VECTOR (6 downto 0);
           anodes : out  STD_LOGIC_VECTOR (0 to 3);
           carry_in : in  STD_LOGIC;
           clk : in  STD_LOGIC);
end toplevel;

architecture Behavioral of toplevel is

-------------------------------------------------------
component display_driver is
    Port ( inputs : in  STD_LOGIC_VECTOR (3 downto 0);
           seg_out : out  STD_LOGIC_VECTOR (6 downto 0));
end component display_driver;
-------------------------------------------------------
component bit_full_adder is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           Cin : in  STD_LOGIC;
           S : out  STD_LOGIC;
           Cout : out  STD_LOGIC);
END component bit_full_adder;

component LEDdisplay IS
    PORT (
          clk                   : IN  STD_LOGIC;
          seg0,seg1,seg2,seg3       : IN  STD_LOGIC_VECTOR(6 downto 0);
        seg             : OUT  STD_LOGIC_VECTOR(6 downto 0);
          an                    : OUT STD_LOGIC_VECTOR(3 downto 0));
END component LEDdisplay;
-------------------------------------------------------
```

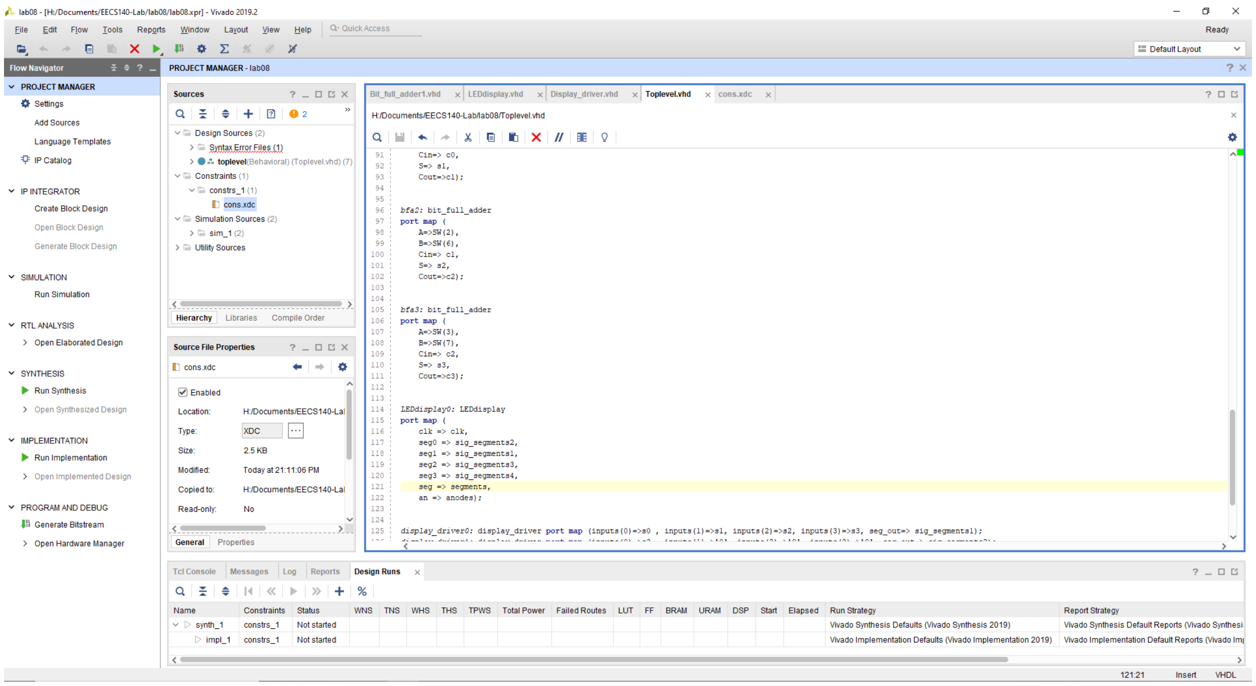
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im

top_level continued



H:/Documents/EECS140-Lab/lab08/Toplevel.vhd

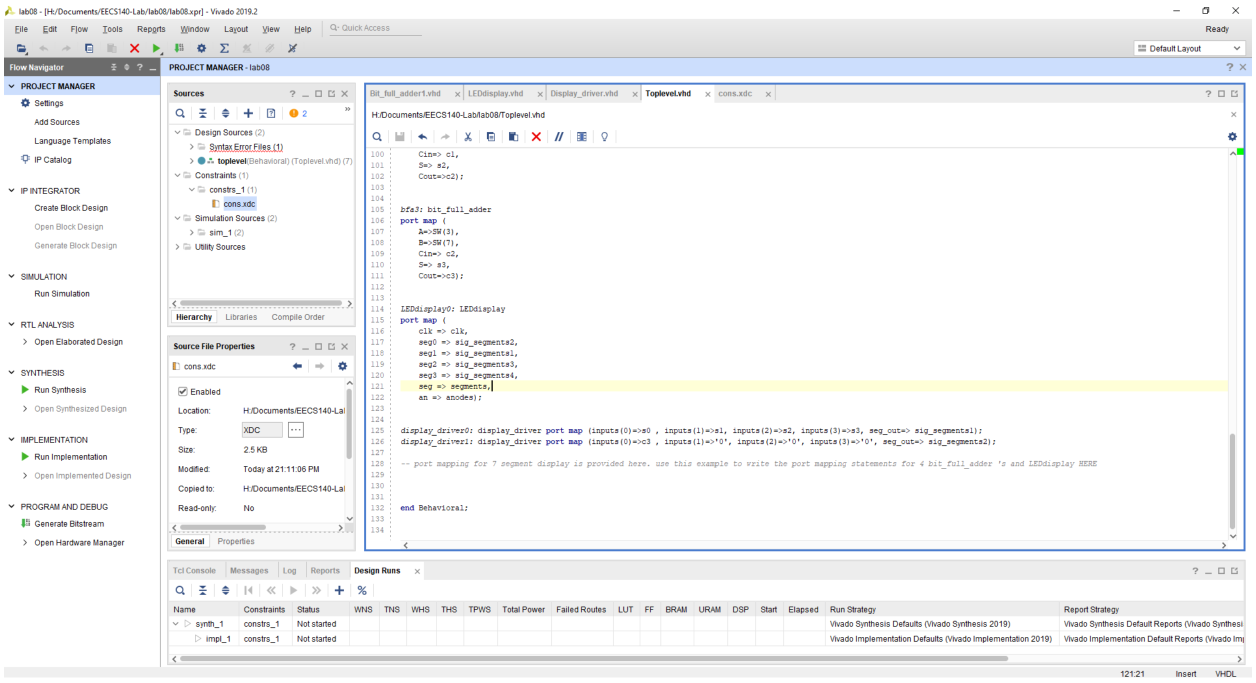
```vhdl

signal c0, c1, c2, c3, s0, s1, s2, s3 : std_logic;
signal sig_segments1, sig_segments2 : std_logic_vector(6 downto 0);
signal sig_segments3, sig_segments4 : std_logic_vector(6 downto 0):= "1111111";

-----------------------------------------------------------------



begin

-- port mapping --
bfa0: bit_full_adder
port map (
    A=>SW(0),
    B=>SW(4),
    Cin=> carry_in,
    S=> s0,
    Cout=>c0);


bfa1: bit_full_adder
port map (
    A=>SW(1),
    B=>SW(5),
    Cin=> c0,
    S=> s1,
    Cout=>c1);


bfa2: bit_full_adder
port map (
    A=>SW(2),
    B=>SW(6),
    Cin=> c1,
    S=> s2,
```



H:/Documents/EECS140-Lab/lab08/Toplevel.vhd

```vhdl
    Cin=> c0,
    S=> s1,
    Cout=>c1);


bfa2: bit_full_adder
port map (
    A=>SW(2),
    B=>SW(6),
    Cin=> c1,
    S=> s2,
    Cout=>c2);


bfa3: bit_full_adder
port map (
    A=>SW(3),
    B=>SW(7),
    Cin=> c2,
    S=> s3,
    Cout=>c3);


LEDdisplay0: LEDdisplay
port map (
    clk => clk,
    seg0 => sig_segments2,
    seg1 => sig_segments1,
    seg2 => sig_segments3,
    seg3 => sig_segments4,
    seg => segments,
    an => anodes);


display_driver0: display_driver port map (inputs(0)=>s0 , inputs(1)=>s1, inputs(2)=>s2, inputs(3)=>s3, seg_out=> sig_segments1);
```

top_level continued

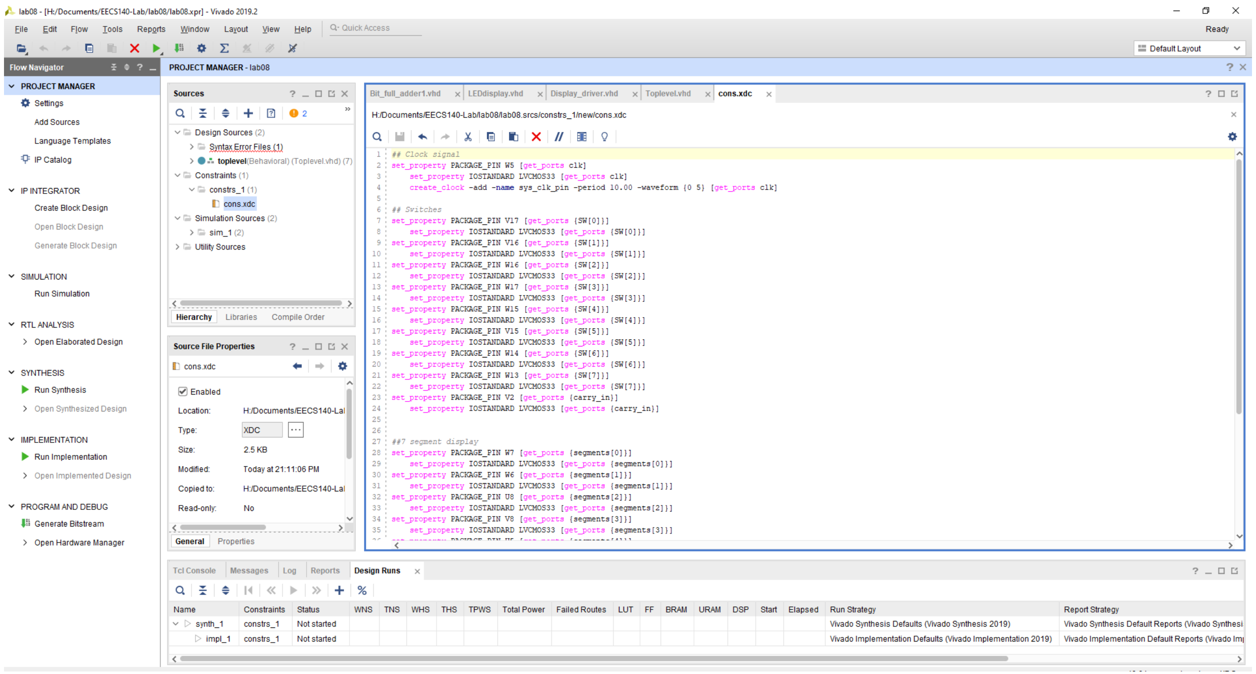


H:/Documents/EECS140-Lab/lab08/Toplevel.vhd

```vhdl
    Cin=> c1,
    S=> s2,
    Cout=>c2);


bfa3: bit_full_adder
port map (
    A=>SW(3),
    B=>SW(7),
    Cin=> c2,
    S=> s3,
    Cout=>c3);


LEDdisplay0: LEDdisplay
port map (
    clk => clk,
    seg0 => sig_segments2,
    seg1 => sig_segments1,
    seg2 => sig_segments3,
    seg3 => sig_segments4,
    seg => segments,
    an => anodes);


display_driver0: display_driver port map (inputs(0)=>s0 , inputs(1)=>s1, inputs(2)=>s2, inputs(3)=>s3, seg_out=> sig_segments1);
display_driver1: display_driver port map (inputs(0)=>c3 , inputs(1)=>'0', inputs(2)=>'0', inputs(3)=>'0', seg_out=> sig_segments2);

-- port mapping for 7 segment display is provided here. use this example to write the port mapping statements for 4 bit_full_adder 's and LEDdisplay HERE



end Behavioral;
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im

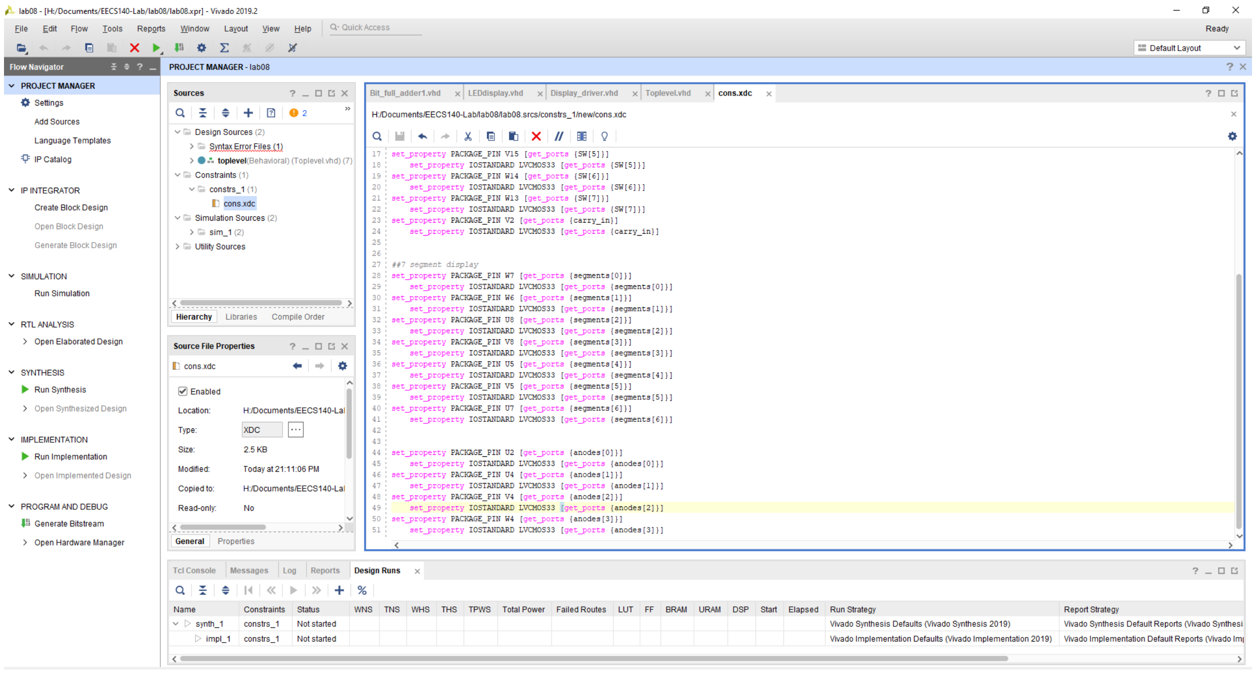
constraints file


lab08 - [H:/Documents/EECS140-Lab/lab08/lab08.xpr] - Vivado 2019.2

H:/Documents/EECS140-Lab/lab08/lab08.srcs/constrs_1/new/cons.xdc

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports clk]
    set_property IOSTANDARD LVCMOS33 [get_ports clk]
    create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {SW[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[0]}]
set_property PACKAGE_PIN V16 [get_ports {SW[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[1]}]
set_property PACKAGE_PIN W16 [get_ports {SW[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[2]}]
set_property PACKAGE_PIN W17 [get_ports {SW[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[3]}]
set_property PACKAGE_PIN W15 [get_ports {SW[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[4]}]
set_property PACKAGE_PIN V15 [get_ports {SW[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[5]}]
set_property PACKAGE_PIN W14 [get_ports {SW[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[6]}]
set_property PACKAGE_PIN W13 [get_ports {SW[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[7]}]
set_property PACKAGE_PIN V2 [get_ports {carry_in}]
    set_property IOSTANDARD LVCMOS33 [get_ports {carry_in}]


##7 segment display
set_property PACKAGE_PIN W7 [get_ports {segments[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[0]}]
set_property PACKAGE_PIN W6 [get_ports {segments[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[1]}]
set_property PACKAGE_PIN U8 [get_ports {segments[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[2]}]
set_property PACKAGE_PIN V8 [get_ports {segments[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[3]}]
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im


lab08 - [H:/Documents/EECS140-Lab/lab08/lab08.xpr] - Vivado 2019.2

H:/Documents/EECS140-Lab/lab08/lab08.srcs/constrs_1/new/cons.xdc

```
set_property PACKAGE_PIN V15 [get_ports {SW[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[5]}]
set_property PACKAGE_PIN W14 [get_ports {SW[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[6]}]
set_property PACKAGE_PIN W13 [get_ports {SW[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {SW[7]}]
set_property PACKAGE_PIN V2 [get_ports {carry_in}]
    set_property IOSTANDARD LVCMOS33 [get_ports {carry_in}]


##7 segment display
set_property PACKAGE_PIN W7 [get_ports {segments[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[0]}]
set_property PACKAGE_PIN W6 [get_ports {segments[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[1]}]
set_property PACKAGE_PIN U8 [get_ports {segments[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[2]}]
set_property PACKAGE_PIN V8 [get_ports {segments[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[3]}]
set_property PACKAGE_PIN U5 [get_ports {segments[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[4]}]
set_property PACKAGE_PIN V5 [get_ports {segments[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[5]}]
set_property PACKAGE_PIN U7 [get_ports {segments[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {segments[6]}]


set_property PACKAGE_PIN U2 [get_ports {anodes[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {anodes[0]}]
set_property PACKAGE_PIN U4 [get_ports {anodes[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {anodes[1]}]
set_property PACKAGE_PIN V4 [get_ports {anodes[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {anodes[2]}]
set_property PACKAGE_PIN W4 [get_ports {anodes[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {anodes[3]}]
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Im