EECS 140: Prelab 7

EECS 140 Introduction Structural VHDL

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1. **Google about VHDL Component Declaration, Signal Declaration and Component Instantiation/port mapping. Submit a summary of your findings.**

Component Declaration

In order to build hierarchical designs to describe the connections in a subsystem a component declaration must be written. It is a the declarative part of the architecture (before the begin statement of the program). And it is an alternative to using entity declarations which defines a real module, as a separate design.

Signal Declaration

Signals are objects with a past history of values. A signal may or may not have multiple drivers each with their current and projected values. A signal declaration contains identifiers and a subtype indicator. Each signal name is an identifier and creates one separate signal. Here is an example,

```
library IEEE;
use IEEE.Std_Logic_1164.all;
entity DataTransm is
  port (Data : Std_Logic_Vector(15 downto 0));
end entity DataTransm;
architecture ExDecl of DataTransm is
signal Temp : Std_Logic;
signal FlagC, FlagZ : Bit;
begin
```

Component Installation / Port Mapping

VHDL components are reusable VHDL modules which can be declared within another digital circuit using component declaration. VHDL port maps is the process of mapping the input and output ports of components in main modules. Here is an example,

```
a: and_gate port map(a, b, out);
```