DDR3 SDRAM controller :: Overview

Project maintainers

- Ecob, Steve

Details

Name: ddr3_sdram
Created: Oct 24, 2012
Updated: Jul 2, 2017
SVN: **No files checked in**

Other project properties

Category: Memory core
Language: Verilog
Development status: Stable
Additional info: Design done, FPGA proven, Specification done
WishBone compliant: No
WishBone version: n/a
License: LGPL

Downloading

The project files are checked in to SVN, available here:
SVN files

Description

This is a controller core for DDR3 SDRAM.

- Default configuration supports one 64 bit UDIMM or SO-DIMM
- Supports DIMM sizes of 1GB, 2GB, 4GB and 8GB
- Works at the minimum DDR3 transfer rate of 600 MT/s
- Heavily optimised for Xilinx Spartan 6 FPGA family
- Implemented in less than 1300 lines of Verilog
- Supports BC4 (Burst chop 4) read and write commands and the refresh command
- Reliable operation verified with XC6SLX25 and XC6SLX75 FPGAs in -2 and -3 speed grades

DDR3 controller working in a Spartan XC6SLX25-2i with a 2GB Corsair UDIMM:

Testbench

The testbench consists of a MicroBlaze MCS microcontroller with one module of glue logic to adapt it to the DRAM controller.
The glue logic module multiplexes the 256 bit data busses of the DRAM controller down to the 32 bit data busses of the MicroBlaze MCS.
The MB MCS only has 1GB of address space available in its IO port interface and the DRAM controller supports DIMMS of up to 8GB. The glue logic accounts for this by using a GPIO port from the MB MCS to provide the high order address bits, allowing SW running on the MB MCS

to use a bank switching scheme to fully access DIMMS larger than 1GB.