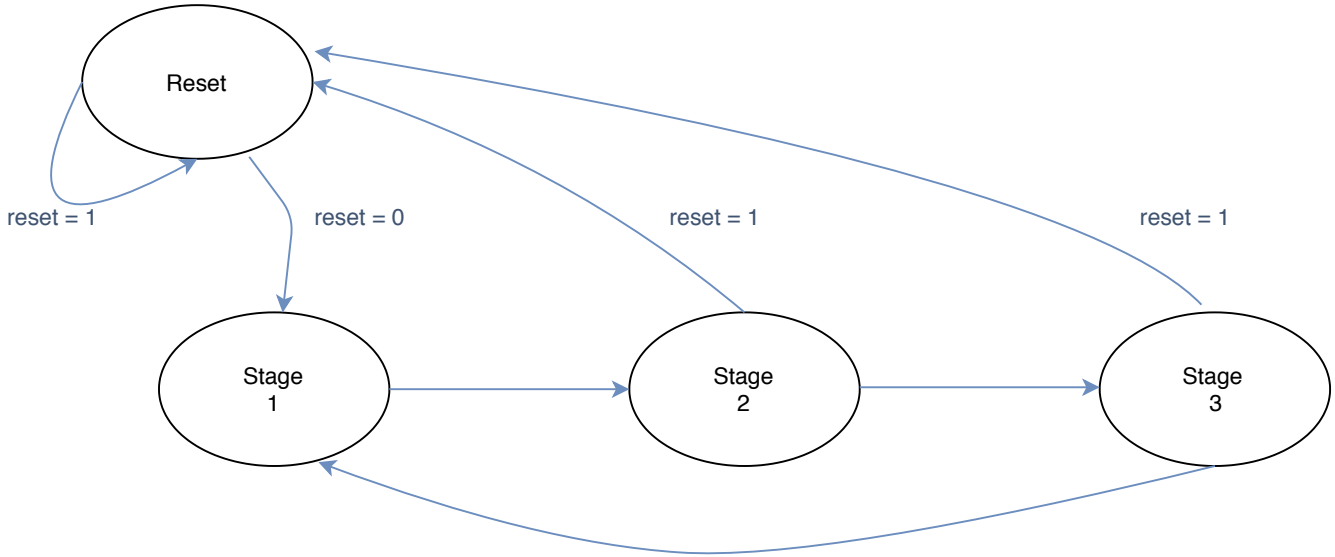


## Stage 1:

Only the control signals related to Stage 1 can change.

The Enable signals for both Stage 2 and Stage 3 are kept at logic state 0, thus, all the control signals related to only these stages are meaningless, no matter the values they assume.

EN1, RF1, RF2, WF1 => can change

---

EN2 = 0

S1, S2, ALU1, ALU2 => keep the previous values

---

EN3 = 0

RM, WM, S3 => keep the previous values

## Stage 2:

Only the control signals related to Stage 2 can change.

The Enable signals for both Stage 1 and Stage 3 are kept at logic state 0, thus, all the control signals related to only these stages are meaningless, no matter the values they assume.

EN1 = 0

RF1, RF2, WF1 =>keep the previous values

---

EN2, S1, S2, ALU1, ALU2 => can change

---

EN3 = 0

RM, WM, S3 => keep the previous values

## Stage 3:

Only the control signals related to Stage 3 can change.

The Enable signals for both Stage 1 and Stage 2 are kept at logic state 0, thus, all the control signals related to only these stages are meaningless, no matter the values they assume.

EN1 = 0

RF1, RF2, WF1 => keep the previous values

---

EN2 = 0

S1, S2, ALU1, ALU2 => keep the previous values

---

EN3, RM, WM, S3 => can change

# CW: std_logic_vector mapping with TLE control signals

| WF1 | S3 | EN3 | WM | RM | EN2 | ALU2 | ALU1 | S2 | S1 | EN1 | RF2 | RF1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |