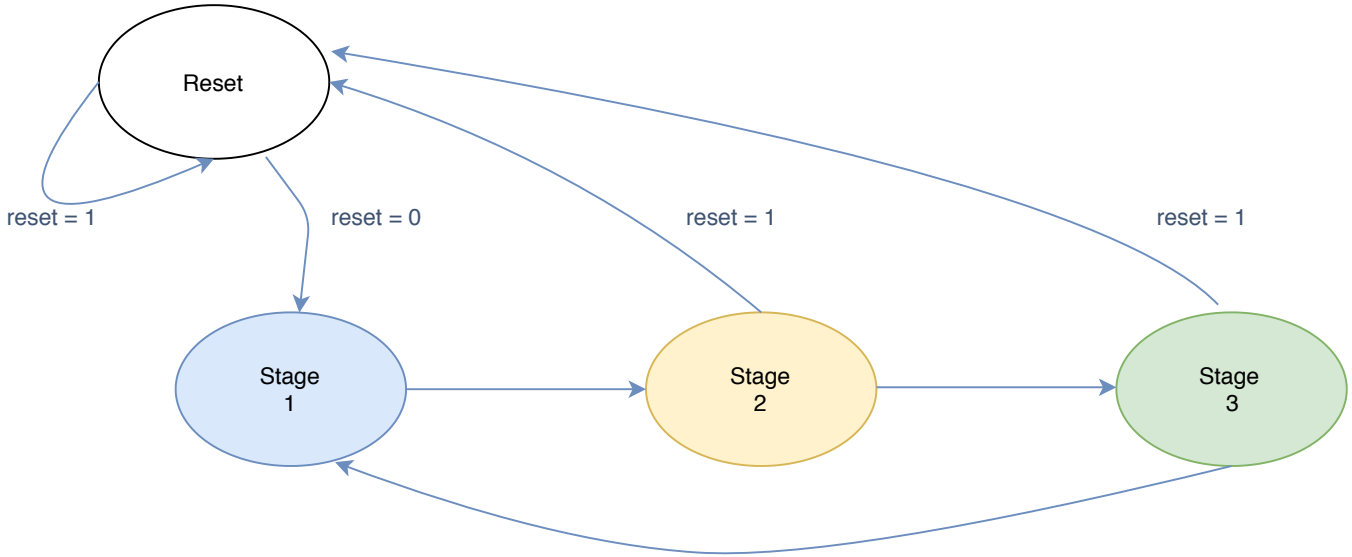
# NOTES:

* The colors indicate which signals "belong" to which stage.

* Each stage modify the EN signals of the remaining stages.

* Stage3 modifies the WF1 signal, even if it "belongs" to Stage1

* The reset state simply disables the EN1, EN2 and EN3 signals.




## Stage 1:

Only the control signals related to Stage 1 can change.

The Enable signals for both Stage 2 and Stage 3 are kept at logic state 0, thus, all the control signals related to only these stages are meaningless, no matter the values they assume.

EN1, RF1, RF2 => can change (assume value from CW)

WF1 = 0

---

EN2 = 0

S1, S2, ALU1, ALU2 => keep the previous values

---

EN3 = 0

RM, WM, S3 => keep the previous values

## Stage 2:

Only the control signals related to Stage 2 can change.

The Enable signals for both Stage 1 and Stage 3 are kept at logic state 0, thus, all the control signals related to only these stages are meaningless, no matter the values they assume.

EN1 = 0

RF1, RF2, WF1 => keep the previous values

---

EN2, S1, S2, ALU1, ALU2 => can change (assume value from CW)

---

EN3 = 0

RM, WM, S3 => keep the previous values

## Stage 3:

Only the control signals related to Stage 3 can change.

The Enable signal of Stage 2 is kept at logic state 0, thus, all the control signals related to this stage are meaningless, no matter the values they assume. The Enable signal of Stage 1 depends on the value assumed by WF1.

EN1 = 1/0 (depending if WF1 = 1/0)

RF1, RF2 => keep the previous values

WF1 = can change (assume value from CW)

---

EN2 = 0

S1, S2, ALU1, ALU2 => keep the previous values

---

EN3, RM, WM, S3 => can change (assume value from CW)

# CW: std_logic_vector mapping with TLE control signals