Product Specification

Product Name: VGM256064A0B01

Product Code: M00160

Customer
Approved by Customer
Approved Date:

Designed By	Checked by	Approved By	
		R&D	QA
2011.12.13	2011.12.15	2011.12.15	2011.12.15

CONTENT

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
Y01	Initial release.	2009-10-29	
Y02	Update the electro-optical characteristics	2010-02-26	Page 9
	Update the module weight in mechanical data		Page 4
A01	Update the TBD	2010-4-15	Page 9 、16、17、19
A02	Modify the value of V_{IH}. Add the value of V_{CI},V_{DDIO}. Modify the application circuit.	2010-05-28	Page 9 Page 9 Page 15,16
A03	Update the Electro-optical Characteristics Update the AC Electrical Characteristics Update the Power ON and Power OFF Sequence Update the Application Circuit(Add the 6800、3-wire、4-wire) Add the External DC-DC application circuit Update the Package Specification	2011-10-08	Page 10 Page 11~16 Page 17 Page 18~22 Page 23 Page 26
A04	Update the Recommended Software Initialization Update the Lifetime(Condition)	2011-12-12	Page 24~25 Page 27

1 Overview

VGM256064A0B01 is a grayscale OLED display module with 256×64 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

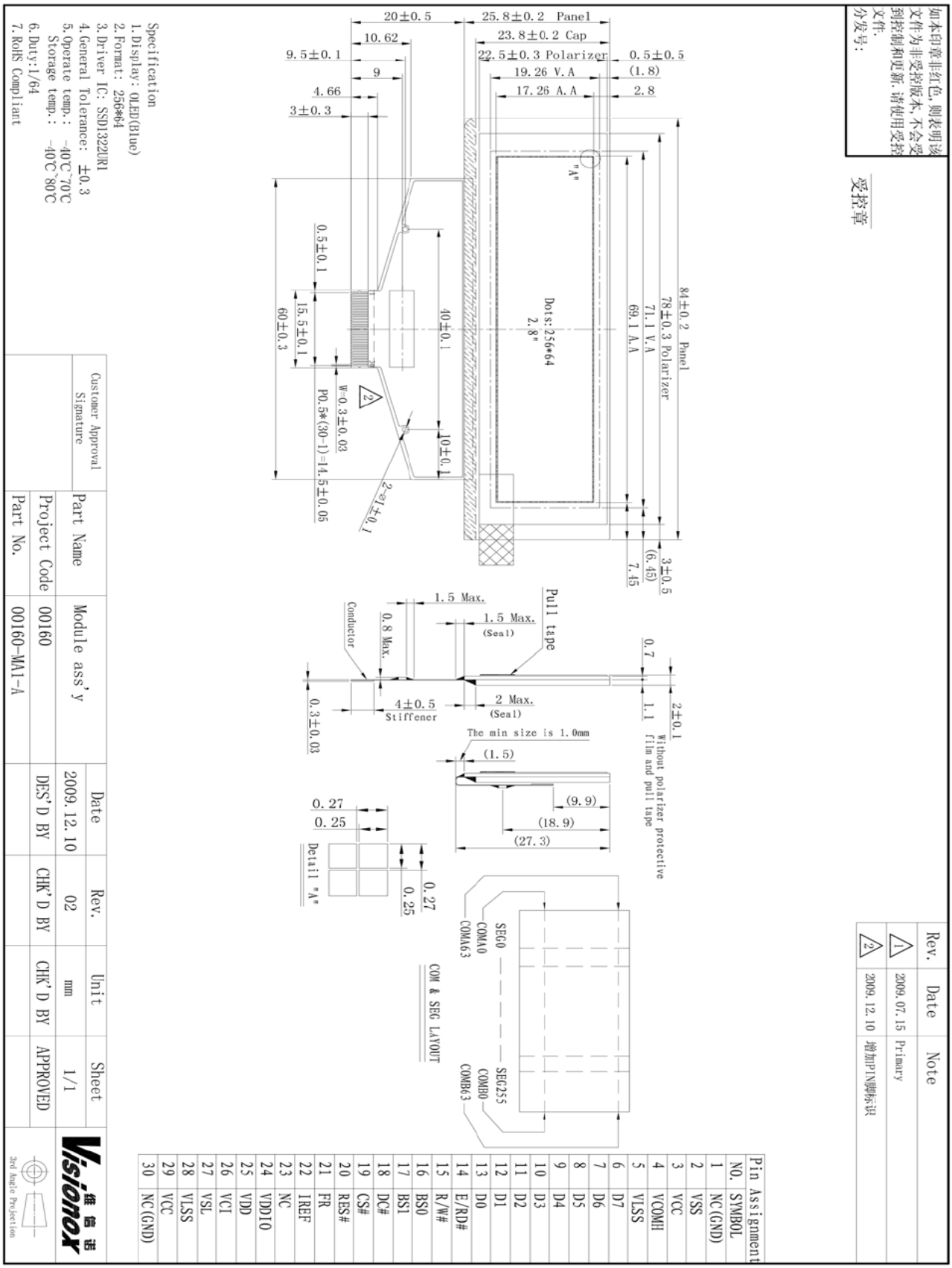
2 Features

- Display Color: Blue
- Dot Matrix:256×64
- Driver IC: SSD1322UR1
- Interface:8-bit 8080,8-bit 6800, SPI
- Wide range of operating temperature: -40℃ to 70℃

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	256(W)×64(H)	-
2	Dot Size	0.25(W)×0.25(H)	mm^2
3	Dot Pitch	0.27(W)×0.27(H)	mm^2
4	Aperture Rate	85	%
5	Active Area	69.1(W)×17.26(H)	mm^2
6	Panel Size	84(W)×25.8(H) ×1.8(T)	mm^3
7	Module Size	84(W)×45.8(H) ×2.0(T)	mm^3
8	Diagonal A/A Size	2.8	inch
9	Module Weight	9.2±10%	gram

4 Mechanical



5 Module Interface

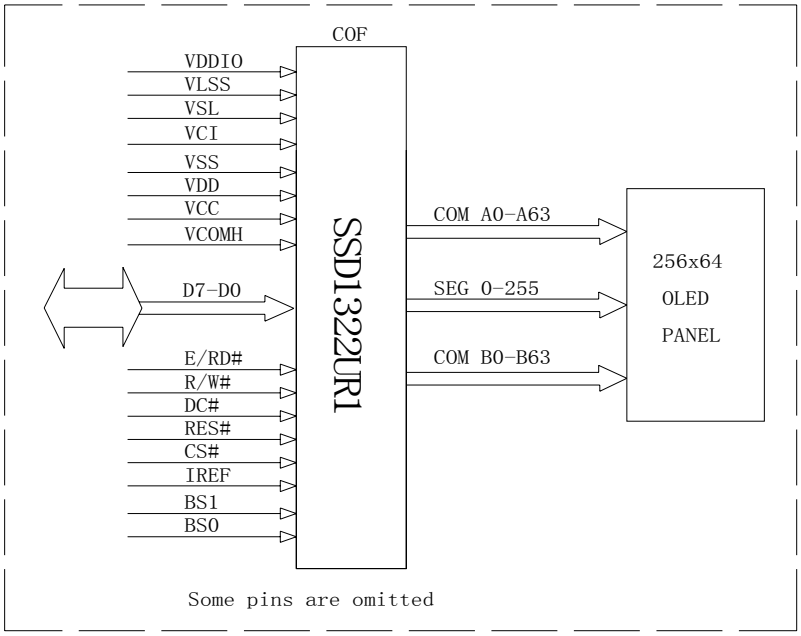
PIN NO.	PIN NAME	DESCRIPTION
1	NC(GND)	No Connection or Ground.
2	VSS	Ground.
3	VCC	OLED drive voltage, it should be supplied externally.
4	VCOMH	This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
5	VLSS	Analog system ground pin.
6~13	D7~D0	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode)
14	E/RD#	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS.
15	R/W#	This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to VSS.
16	BS0	Table 5-1
17	BS1	
18	DC#	Data/Command Select. H: Data; L: Command.
19	CS#	Chip Select, active low.
20	RES#	Reset, active low.
21	FR	No Connection.
22	IREF	This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.
23	NC	No Connection.
24	VDDIO	Power supply for interface logic level.
25	VDD	Power supply pin for core logic operation.
26	VCI	Low voltage power supply
27	VSL	This is segment voltage reference pin.
28	VLSS	Analog system ground pin.
29	VCC	OLED drive voltage, it should be supplied externally.
30	NC(GND)	No Connection or Ground.

Table 5-1

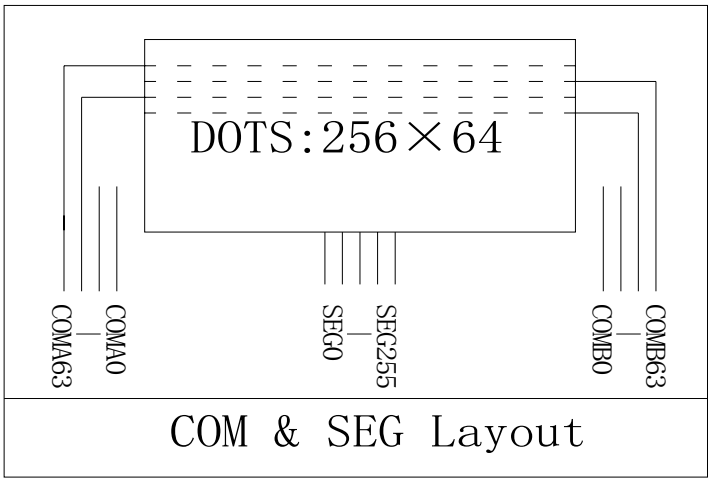
Pin Name	8-bit 6800	8-bit 8080	4 Line SP	3 Line SPI
BS0	1	0	0	1
BS1	1	1	0	0

6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Supply Voltage	V_{DD}	-0.5	2.75	V	IC maximum rating
	V_{CC}	-0.5	21	V	IC maximum rating
	V_{DDIO}	-0.5	V_{CI}	V	IC maximum rating
	V_{CI}	-0.3	4.0	V	IC maximum rating
Operating Temp.	Top	-40	+70	℃	-
Storage Temp	Tstg	-40	+80	℃	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	V_{DD}	22±3°C, 55±15%R.H	2.4	-	2.6	V
Power Supply for I/O pins	V_{DDIO}	22±3°C, 55±15%R.H	1.65	-	V_{CI}	V
Low voltage power supply	V_{CI}	22±3°C, 55±15%R.H	2.4	-	3.5	V
OLED Driver Supply Voltage	V_{CC}	22±3°C, 55±15%R.H	11.5	12	12.5	V
High-level Input Voltage	V_{IH}	-	$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low-level Input Voltage	V_{IL}	-	0	-	$0.2\times V_{DDIO}$	V
High-level Output Voltage	V_{OH}	-	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low-level Output Voltage	V_{OL}	-	0	-	$0.1\times V_{DDIO}$	V

Note : The V_{CC} input must be kept in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Normal Mode Brightness	L_{br}	All pixels ON(1)		70	90	-	cd/m^2
VDD Sleep mode Current	I_{SLP_VDD}	VCI = VDDIO =2.8V, VCC =OFF VDD(external) = 2.5V, Display OFF, No panel attached		-	-	10	uA
V_{DDIO} Sleep mode Current	I_{SLP_VDDIO}	VCI = VDDIO =2.8V, VCC =OFF Display OFF, No panel attached	External VDD =2.5V	-	-	10	uA
			Internal VDD	-	-	10	uA
VCI Sleep mode Current	I_{SLP_VCI}	VCI = VDDIO =2.8V, VCC =OFF Display OFF, No panel attached	External V_{DD} =2.5V	-	-	10	uA
			Enable Internal VDD during Sleep mode	-	-	50	uA
			Disable Internal VDD during Sleep mode	-	-	10	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)		-	492	600	mW
C.I.E(Blue)	(x)	x,y(CIE1931)		0.12	0.16	0.20	-
	(y)			0.28	0.32	0.36	-
Dark Room Contrast	CR	-		≥2000:1	-	-	-
Response Time	-	-		---	10	-	μ s
View Angle	-	-		≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage : 12V
- Contrast setting : 0x9f
- Frame rate : 120Hz
- Duty setting : 1/64

8.3 AC Electrical Characteristics

(1)6800-Series MPU Parallel Interface Timing Characteristics

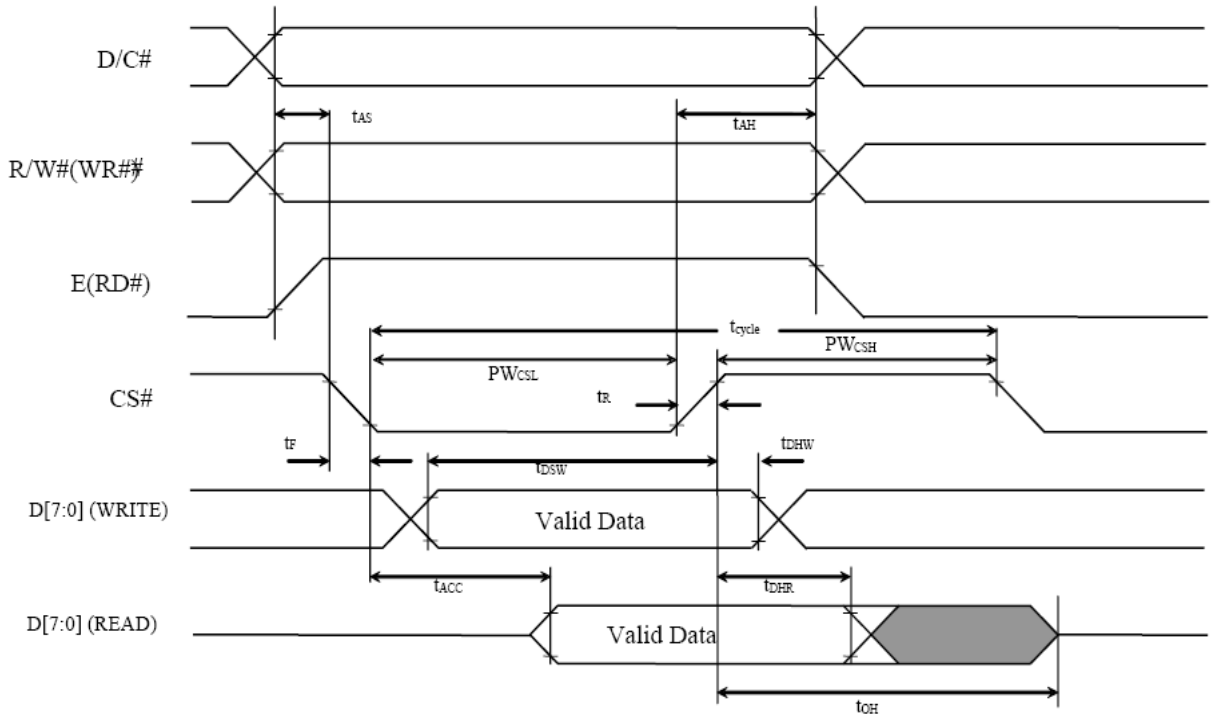
(VDDIO - VSS = 1.65V to 2.1V,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	200	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	450 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

(VDDIO - VSS = 2.1V to VCI,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	300 100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	150 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

6800-series MCU parallel interface characteristics



(2)8080-Series MPU Parallel Interface Timing Characteristics

(VDDIO - VSS = 1.65V to 2.1V,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

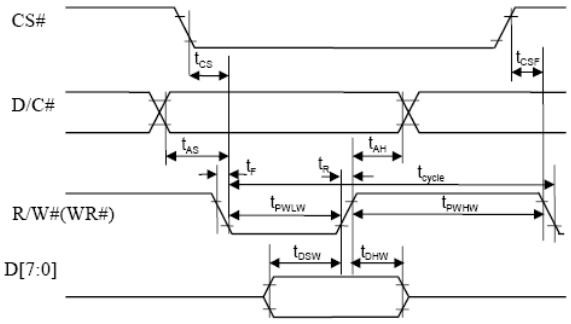
Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	400 100	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	220	ns
t_{PWLR}	Read Low Time	200	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

(VDDIO - VSS = 2.1V to VCI,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

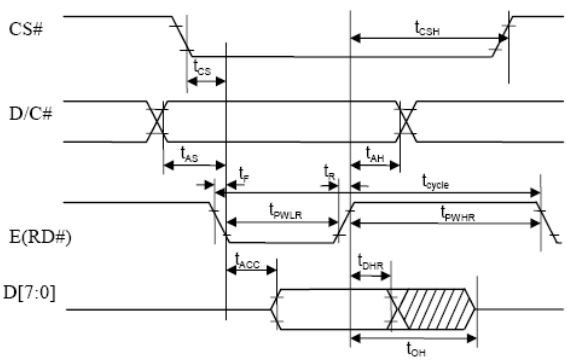
Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	300 100	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MPU parallel interface characteristics

Write cycle



Read cycle



(3)Serial Interface Timing Characteristics (4-wire SPI)

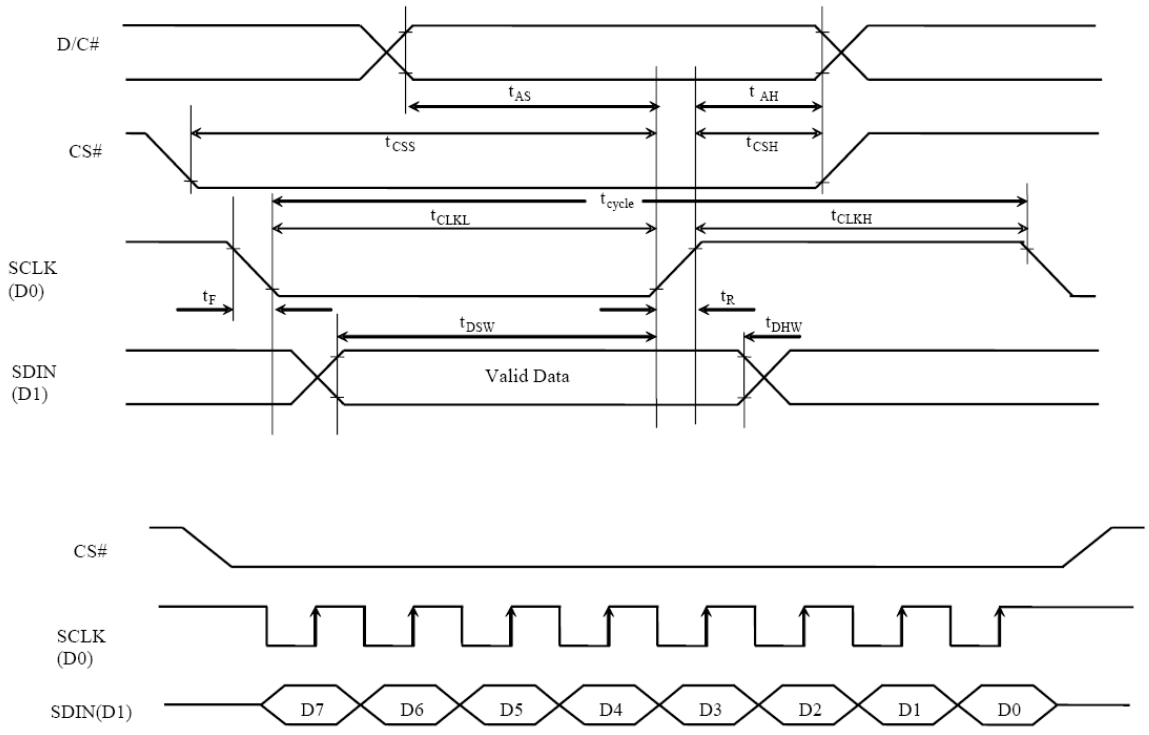
(VDDIO - VSS = 1.65V to 2.1V,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	35	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	40	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

(VDDIO - VSS = 2.1V to VCI,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	25	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	40	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (4-wire SPI)



(4)Serial Interface Timing Characteristics (3-wire SPI)

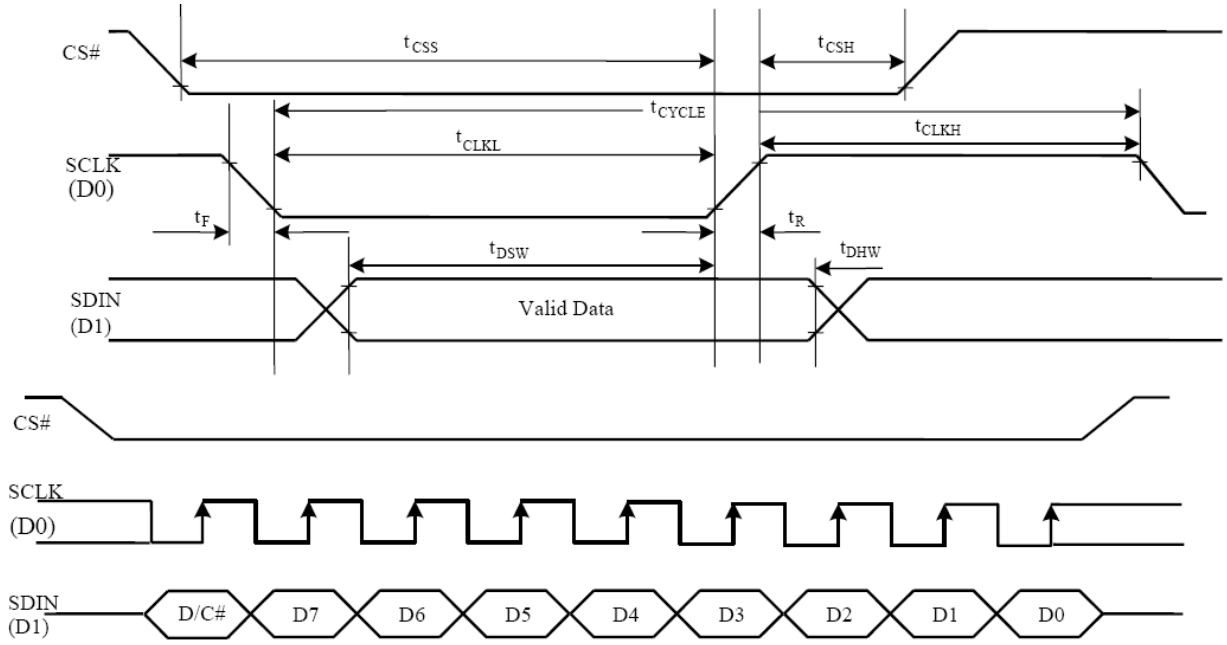
(VDDIO - VSS = 1.65V to 2.1V,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	35	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	40	-	-	ns
t_{CLKH}	Clock High Time	25	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

(VDDIO - VSS = 2.1V to VCI,VCI - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	25	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	25	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics (3-wire SPI)

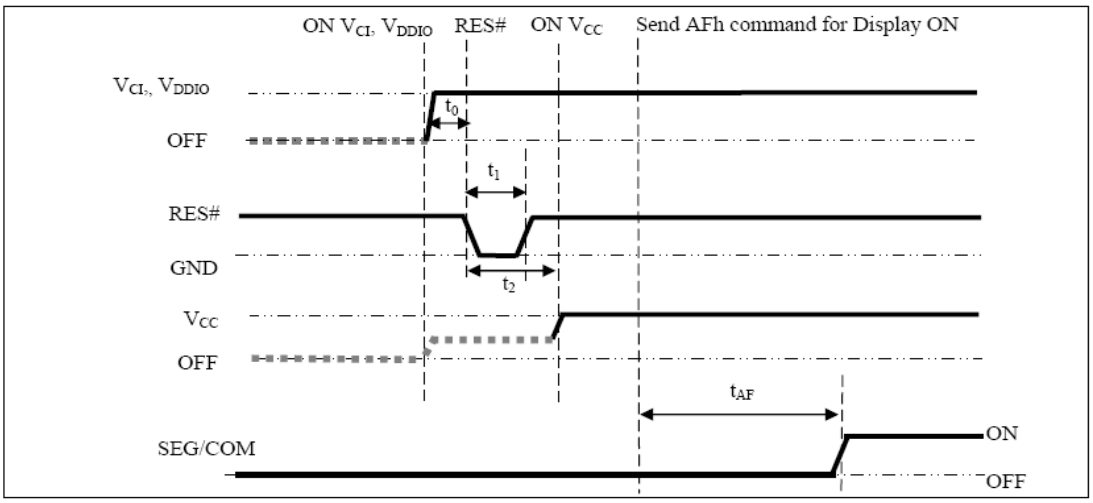


9 Functional Specification and Application Circuit

9.1 Power ON and Power OFF Sequence

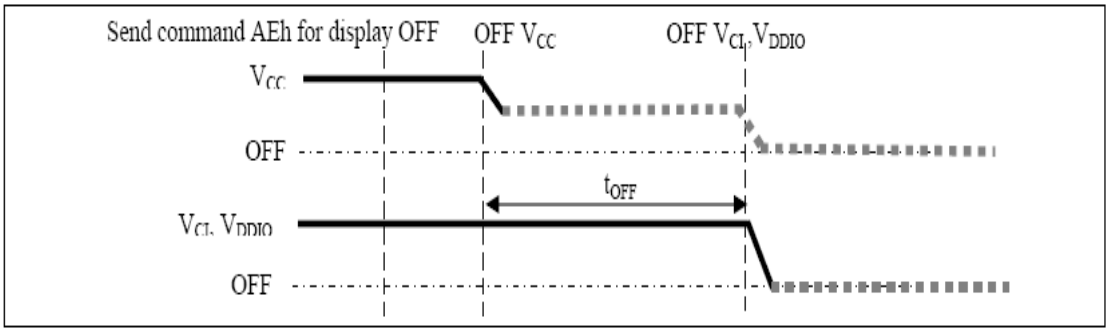
Power ON Sequence:

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 100us (t1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t2). Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(tAF).
5. After VCI become stable, wait for at least 300ms to send command



Power OFF Sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{CI} , V_{DDIO} . (where Minimum t_{OFF}=0ms(3), Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC, VCC becomes lower than VCI whenever VCI,VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in above Figure.

(2)VCC should be kept float (disable) when it is OFF.

(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.

(4) The register values are reset after t1.

(5) Power pins (VDD, VCC) can never be pulled to ground under any circumstance.

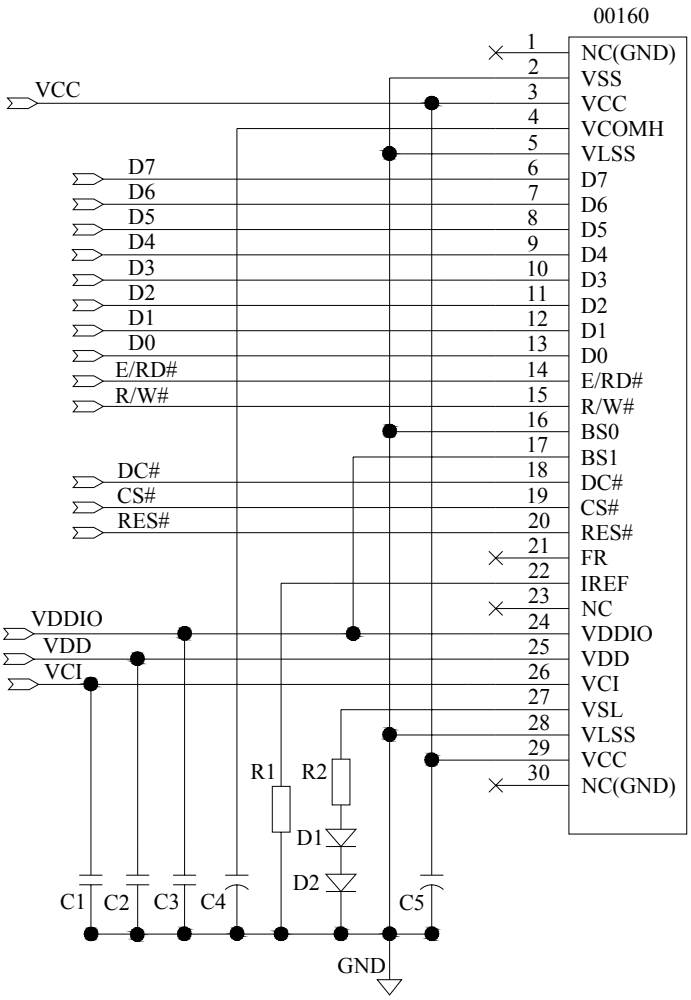
9.2 Application Circuit

The double byte command for 0xAB is used to enable or disable the VDD regulator.

No matter VDD is supplied by external source or internal regulated ; VCI must always be set equivalent to or higher than VDD and VDDIO.

(A) VDD can be supplied externally (with the range of 2.4V to 2.6V,VCI must always be set equivalent to or higher than VDD and VDDIO.) when A[0] is set to 0b.

(1)The configuration for 8080-parallel interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: D[7:0], E/RD#, R/W#, DC#, CS#, RES#

Recommended components

C4,C5: 4.7μF/25V.ROHS (Tantalum Capacitors)

C1,C2,C3: 0.1uF-0603-X7R±10%.ROHS

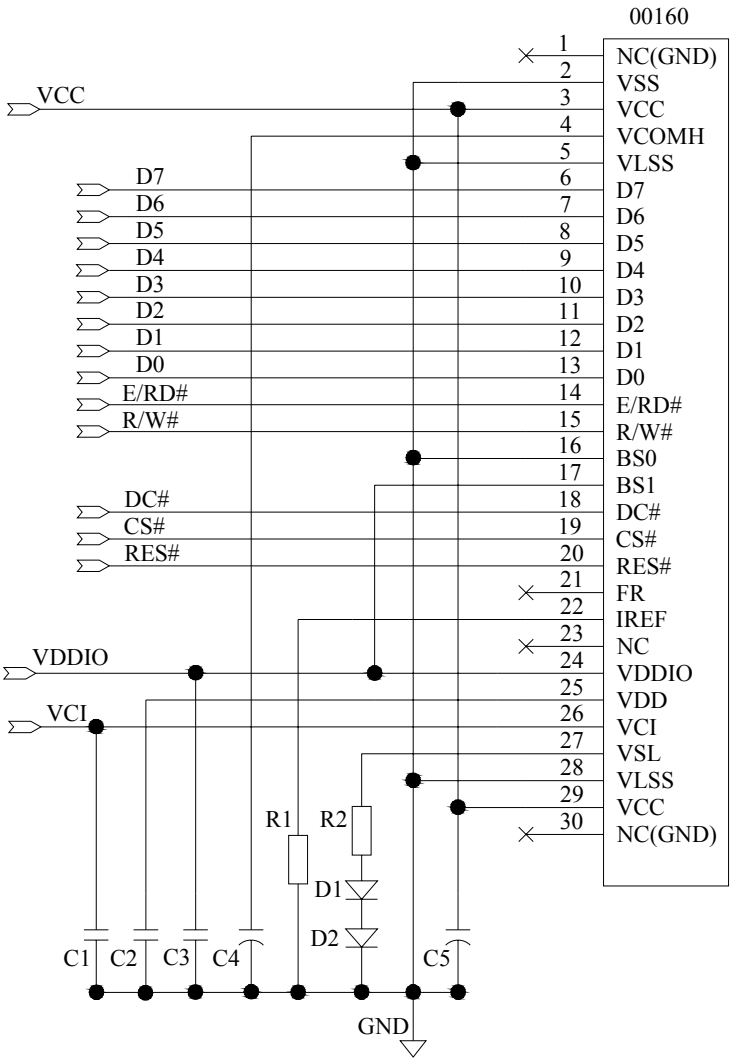
R1: 0603 1/10W +/-5% 680Kohm.ROHS

R2: 0603 1/10W +/-5% 50ohm.ROHS

D1,D2: 1N4148

(B) VDD can be supplied regulated internally from VCI(VCI must be > 2.6V), when A[0] is set to 1b.

(1) The configuration for 8080-parallel interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: D[7:0], E/RD#, R/W#, DC#, CS#, RES#

Recommended components

C4,C5: 4.7μF/25V.ROHS (Tantalum Capacitors)

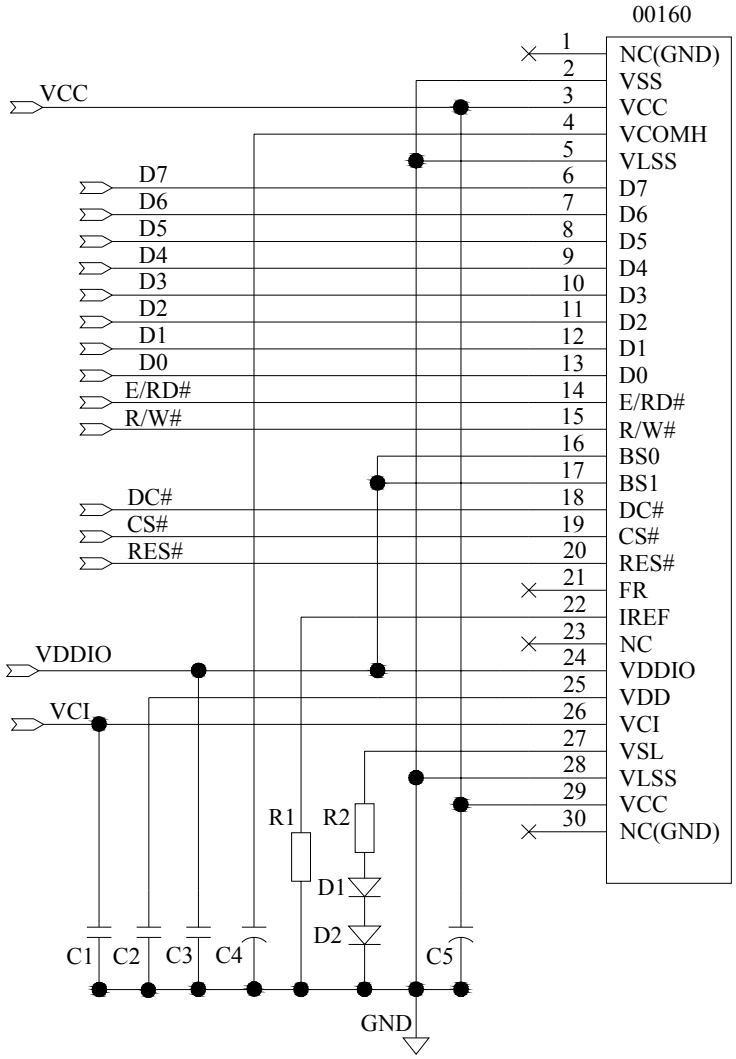
C1,C2,C3: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 680Kohm.ROHS

R2: 0603 1/10W +/-5% 50ohm.ROHS

D1,D2: 1N4148

(2) The configuration for 6800-parallel interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: D[7:0], E/RD#, R/W#, DC#, CS#, RES#

Recommended components

C4,C5: 4.7μF/25V.ROHS (Tantalum Capacitors)

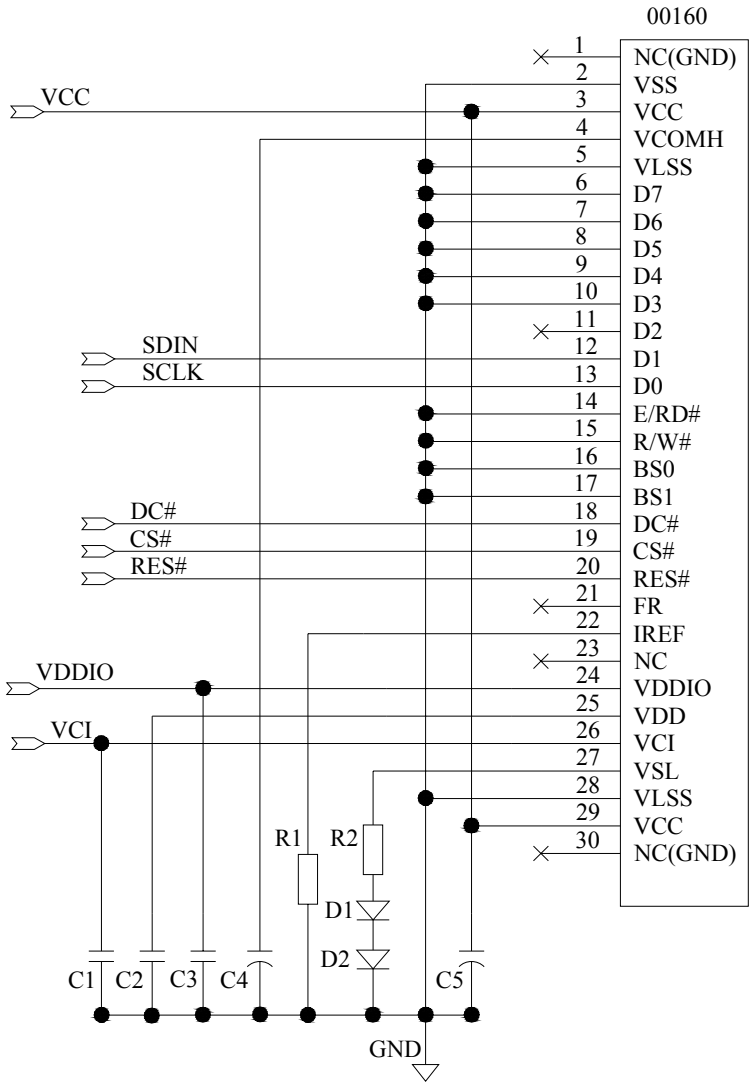
C1,C2,C3: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 680Kohm.ROHS

R2: 0603 1/10W +/-5% 50ohm.ROHS

D1,D2: 1N4148

(3) The configuration for 4-wire SPI interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: SCLK,SDIN, DC#, CS#, RES#

Recommended components

C4,C5: 4.7μF/25V.ROHS (Tantalum Capacitors)

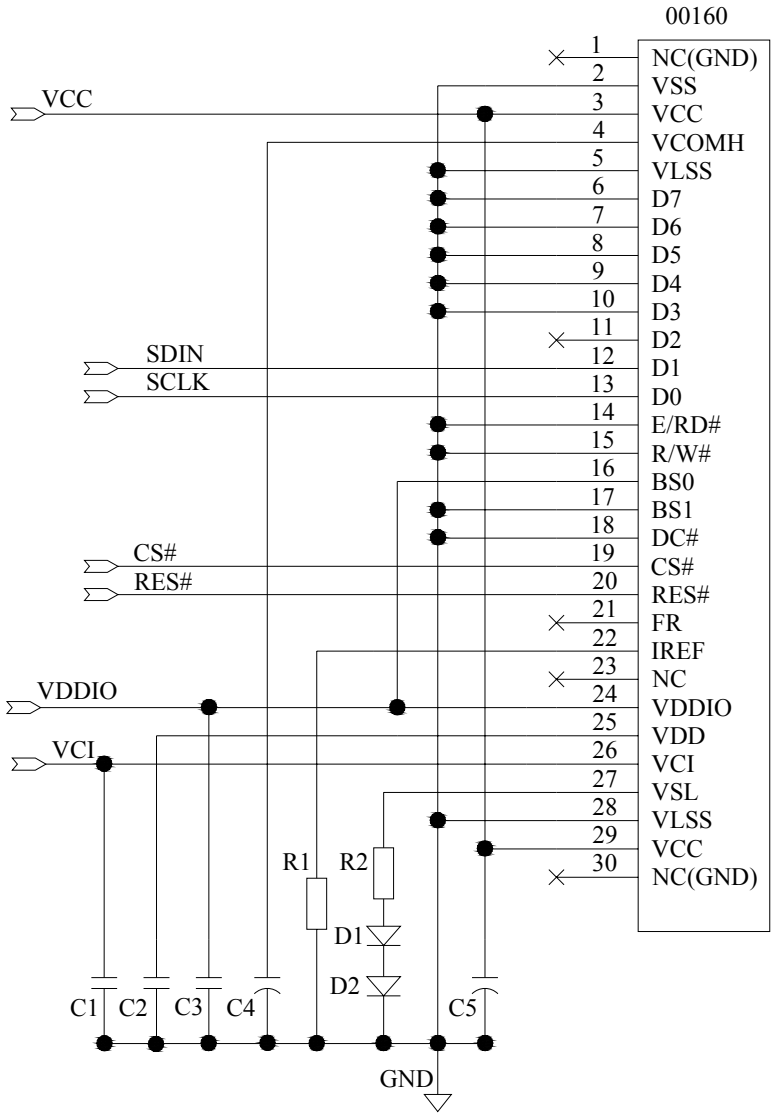
C1,C2,C3: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 680Kohm.ROHS

R2: 0603 1/10W +/-5% 50ohm.ROHS

D1,D2: 1N4148

(4) The configuration for 3-wire SPI interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: SCLK,SDIN, CS#, RES#

Recommended components

C4,C5: 4.7μF/25V.ROHS (Tantalum Capacitors)

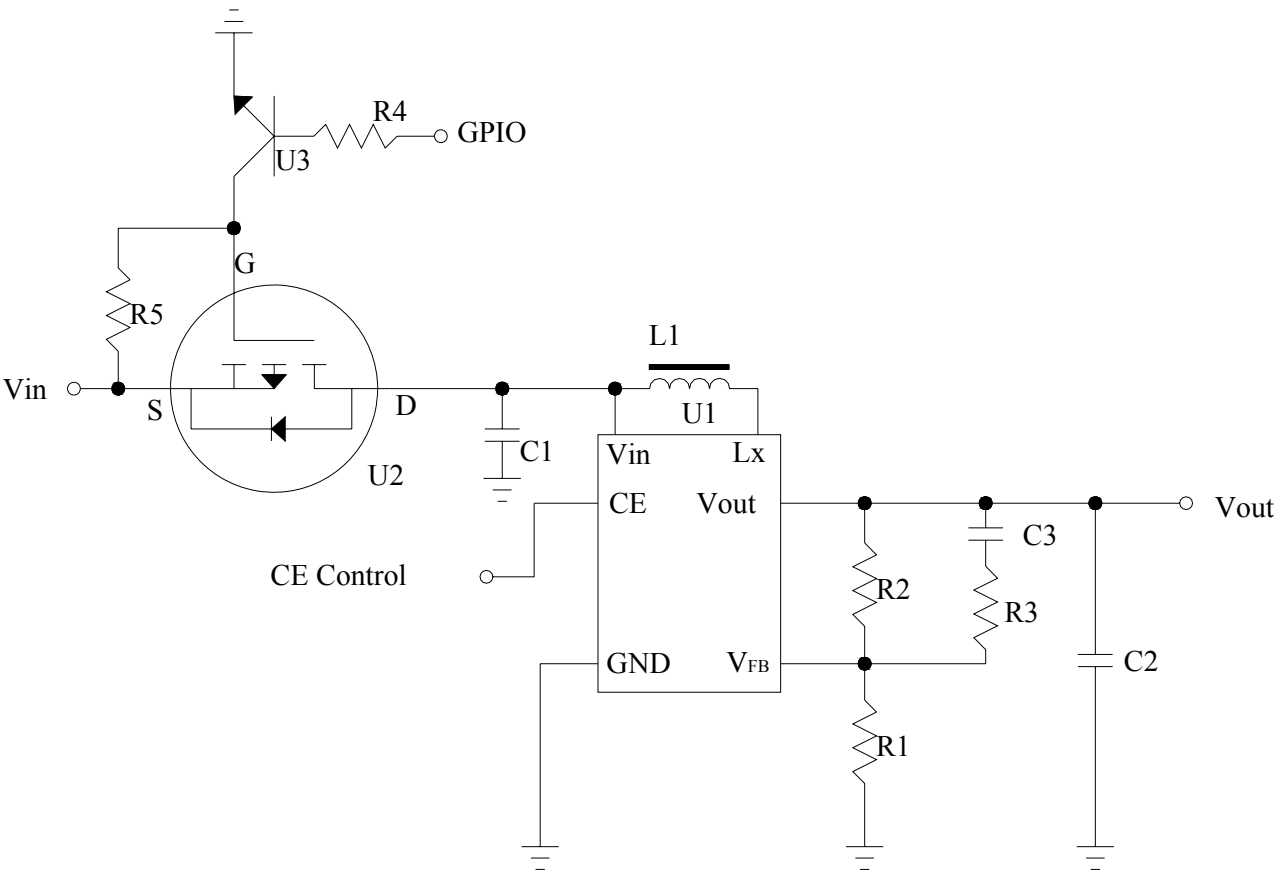
C1,C2,C3: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 680Kohm.ROHS

R2: 0603 1/10W +/-5% 50ohm.ROHS

D1,D2: 1N4148

9.3 External DC-DC application circuit



Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-5% 10Kohm.ROHS
The R2	: 0603 1/10W +/-1% 110Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338P
The U3	: 8050

9.4 Display Control Instruction

Refer to SSD1322 IC Specification.

9.5 Recommended Software Initialization

```
void init_program()
{
    write_c(0xfd); // Set Command Lock
    write_d(0x12);
    write_c(0xae); //Set Sleep mode OFF
    write_c(0x15); //Set Column Address
    write_d(0x1c);
    write_d(0x5b);
    write_c(0x75); //Set Row Address
    write_d(0x00);
    write_d(0x3f);
    write_c(0xa0); //Set Re-map and Dual COM Line mode
    write_d(0x14);
    write_d(0x11);
    write_c(0xa1); //Set Display Start Line
    write_d(0x00);
    write_c(0xa2); //Set Display Offset
    write_d(0x00);
    write_c(0xab); //Function Selection
    write_d(0x00);
    write_c(0xb1); //Set Phase Length
    write_d(0xe2);
    write_c(0xb3); //Set Front Clock Divider / Oscillator
    write_d(0x91);
    write_c(0xb4); //Display Enhancement A
    write_d(0xa0);
    write_d(0xfd);
    write_c(0xb5); //Set GPIO
    write_d(0x00);
    write_c(0xb6); //Set Second Precharge Period
    write_d(0x08);
    write_c(0xb9); //Select Default Linear Gray Scale table
    write_c(0xbb); //Set Pre-charge voltage 0x1F
    write_d(0x1f);
    write_c(0xbe); //Set VCOMH
```

```
        write_d(0x07);
        write_c(0xc1); //Set Contrast
        write_d(0x9f);
        write_c(0xc7); //Master Contrast Current Control
        write_d(0x0f);
        write_c(0xca); //Set MUX Ratio
        write_d(0x3f);
        write_c(0xd1); //Display Enhancement B
        write_d(0x82);
        write_d(0x20);
        write_c(0xa6); //Set Display normal Mode
        write_c(0xaf); //Set Display ON
}
```

10 Package Specification

Controlled Seal

Packing Process(1)~(9)

(1) TRAY Type:00160-MT1-B

(2)

(3) order①、②、①、② fix trays with tape
240 pcs of 1 small carton
1 tray contain 12 pcs
20 contained trays, 1 empty tray

(4) package with plastic bags add five desiccants create a power vacuum

(5)

(6)

(7)

small carton package
L425*W330*L175 mm

(8)

2 small cartons in 1 big carton

(9) 40 contained trays, 2 empty trays,
Package quantity products:
480 pcs of 1 big carton

Package finished
L450*W350*L360 mm

NOTE:1、The inner carton and master carton must be sealed with adhesive tape.

2、Fill up the gap with tray.

3、If the customer has special needs with the RoHS making, the inner carton and master carton need adhesive new RoHS marking at ◎.

11 Reliability

11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	80℃,240hrs	4
2	Low Temperature (Non-operation)	-40℃,240hrs	4
3	High Temperature (Operation)	70℃,240hrs	4
4	Low Temperature (Operation)	-40℃,240hrs	4
5	High Temperature / High Humidity (Operation)	60℃,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40℃~80℃(-40℃/30min;transit/3min;80℃/30min;transit/3min) 1cycle: 66min,30cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
2. The degradation of polarizer is ignored for item 5.
3. The tolerance of temperature is ±3℃, and the tolerance of relative humidity is ±5%.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance:≥50% of initial value.
4. Current consumption: within ± 50% of initial value.

11.2 Lifetime

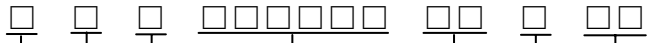
End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	10000	-	hrs	90 cd/m^2, 50% alternating checkerboard, 22±3°C, 55±15% RH

11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22±3°C; 55±15% RH.

12 Illustration of OLED Product Name



Flow No. :

01~99

Display Color :

R—red

G—green

B—blue

Y—yellow

W—white

A—area color

F—full color

Panel Flow No. :

A0~A9, B0~B9…Z0~Z9

Display Format :

Graphic—columns and rows

Character—characters and line number

Segment—segment number

Icon—pixel number

Product Type :

P—panel

M—module

Display Type :

G—graphic

C—character

S—segment

I—Icon

M—mixed

Company :

V—Visionox

13 Outgoing Quality Control Specifications

13.1 Sampling Method

(1) GB/T 2828.1-2003/ISO2859-1：1999, inspection level Ⅱ, normal inspection, single sample inspection

(2) AQL: Major 0.65; Minor 1.0

13.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows.

Temperature: 22±3°C

Humidity: 55±15%R.H

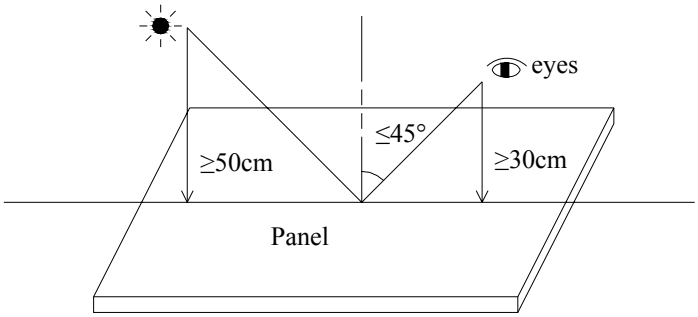
Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥50cm

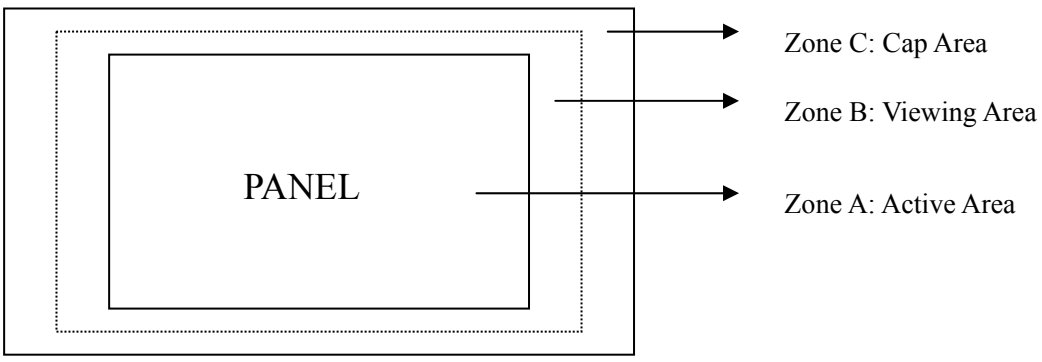
Distance between the Panel & Eyes: ≥30cm

Viewing angle from the vertical in each direction: ≤45°

(See the sketch below)

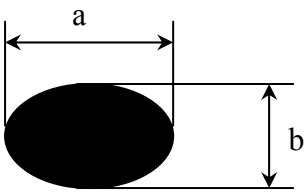


13.3 Quality Assurance Zones

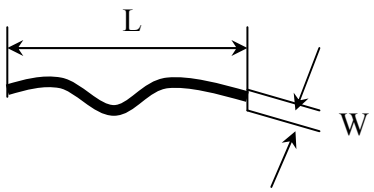


13.4 Inspection Standard

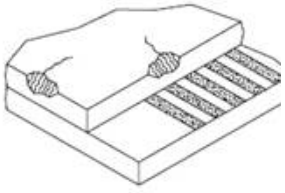
Definition of Φ&L&W (Unit: mm)

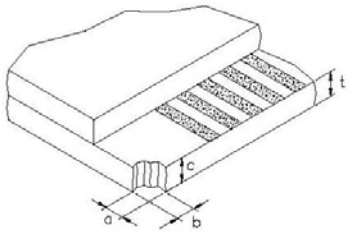
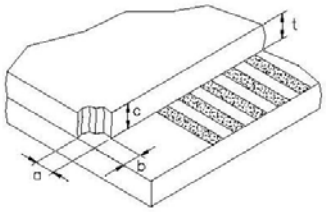
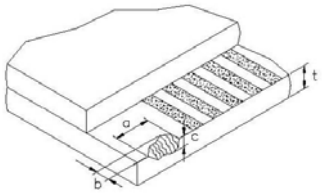
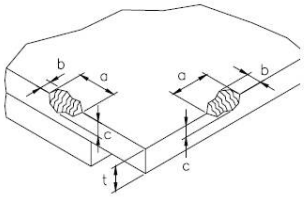
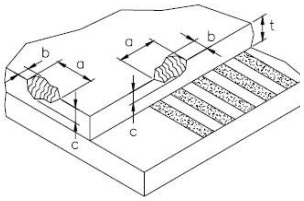


Φ=(a+b)/2



Ⅰ. Appearance Defects

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th><th>CLASSIFICATION</th></tr>
<tr><td>1</td><td>Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.15</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15＜Φ≤0.30</td><td>3</td></tr>
<tr><td>Φ＞0.30</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>Scratch/line on the glass/Polarizer</td><td>
<table>
<tr><td rowspan="2">Width (mm)</td><td rowspan="2">Length (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>W≤0.03</td><td>---</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03＜W≤0.08</td><td>L≤5.0</td><td>3</td></tr>
<tr><td>W＞0.08</td><td>---</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ>0.5</td><td>0</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2＜Φ≤0.5</td><td>3</td></tr>
<tr><td>Φ≤0.2</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>4</td><td>Any Dirt & Scratch on Polarizer’s Protective Film</td><td>Ignore for not affect the polarizer.</td><td>Acceptable</td></tr>
<tr><td>5</td><td>Glass Crack</td><td>  Propagation crack is not acceptable.</td><td>Major</td></tr>
</table>

6	Corner Chip	 t= Glass thickness Accept a≤2.0mm or b≤2.0mm, c≤t	Minor
7	Corner Chip on Cap Glass	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
8	Chip on Contact Pad	 t= Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)	Minor
9	Chip on Face of Display	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
10	Chip on Cap Glass	 t= Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t	Minor
11	Stain on Surface	Stain removable by soft cloth or air blow is acceptable.	Minor
12	TCP/FPC Damage	(1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.	Minor
13	Dimension Unconformity	Checking by mechanical drawing.	Major

Ⅱ. Displaying Defects

<table>
<tr><th>NO.</th><th>Items</th><th>Criteria</th><th>Classification</th></tr>
<tr><td>1</td><td>Black/White spot
Dirty spot
Foreign matter</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Pieces Permitted</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.10</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.10＜Φ≤0.20</td><td>3</td></tr>
<tr><td>Φ＞0.20</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>No Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>3</td><td>Irregular Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>4</td><td>Missing Line
(row or column)</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>5</td><td>Short</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>6</td><td>Flicker</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>7</td><td>Abnormal Color</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>8</td><td>Luminance NG</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>9</td><td>Over Current</td><td>Refer to the SPEC.</td><td>Major</td></tr>
</table>

14 Precautions for operation and Storage

14.1 Precautions for Operation

(1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).

(2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.

(3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.

(4) Do not attempt to disassemble or process the OLED module.

(5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.

(6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

(7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.

(8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

14.2 Soldering

(1) Soldering should be performed only on the I/O terminals.

(2) Use soldering irons with proper grounding and no leakage.

(3) Iron: no higher than 300℃ and 3~4 sec during soldering.

14.3 Precautions for Storage

(1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.

(2) Keep the environment temperature between 10℃ and 35℃ and the relative humidity less than 60%. Avoid high temperature and high humidity.

(3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.

(4) Do not leave any article on the OLED module surface for an extended period of time.

14.4 Warranty period

Visionox Display Co., Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition.