

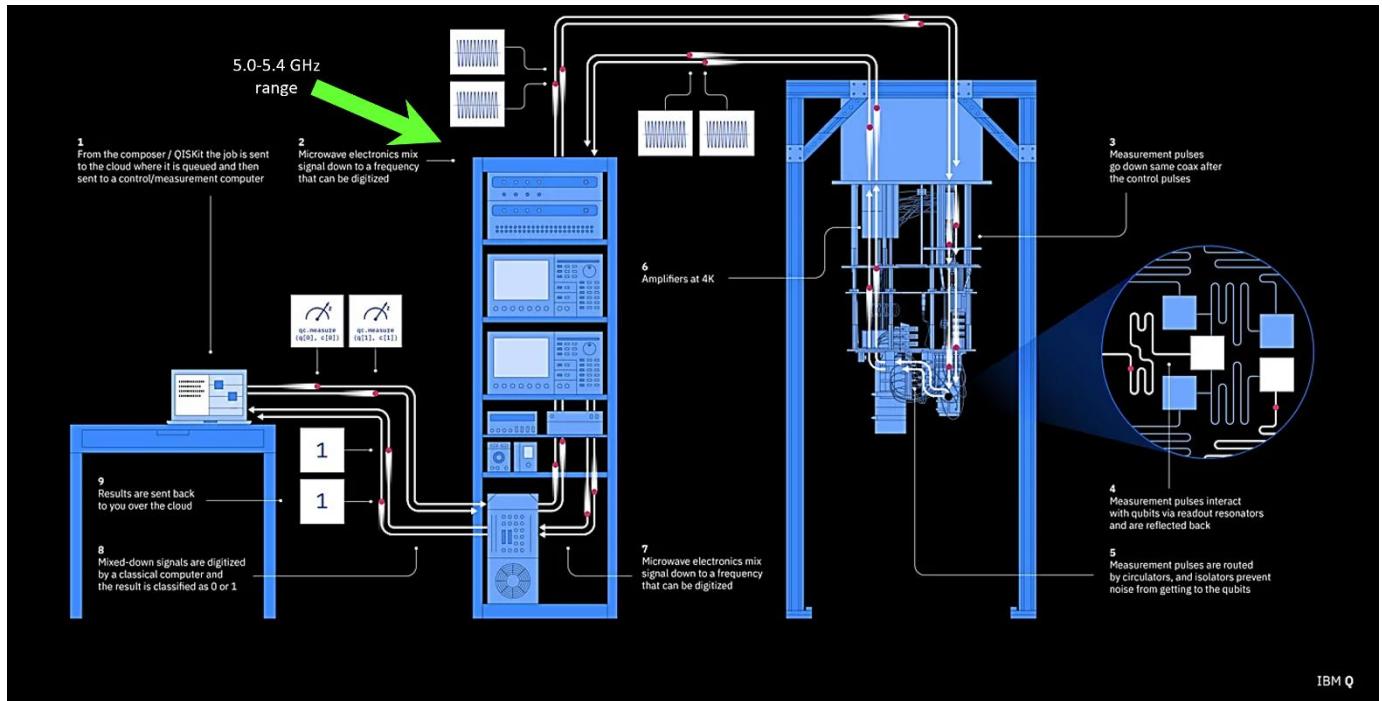
Nanotechnology Used for Quantum Chips

Onri Jay Benally

February 2024

Table of Contents

- I. Background & Motivation.
- II. Fabrication Tools vs. 3D Printing.
- III. The Lithography Design Process (Including 3D Modeling & Simulation).
- IV. Masked vs. Maskless Lithography (with Brief Overview of Deposition).
- V. Application Methods in Lithography Used for Quantum Devices.
- VI. Brief Overview of Packaging.
- VII. Conclusion.
- VIII. Examples of Hardware (Supplementary Images).



Layout of an IBM Quantum System 1 (IBM Research).

A quantum computing system can be described by the *quantum stack*, containing levels of abstraction. The software layer exists on the upper level, while the hardware layer is on the lower level. At the very bottom of this hardware level is the quantum chip, which comprises of a quantum processing unit (QPU). One may notice, in nearly every quantum computing platform, the processor comes in some form of a chip. It contains components that can exploit quantum effects depending on the material's physical properties. The overall control and conversion systems vary in size, however. Some can fit inside a desktop machine, while others take up the space of an entire building room, like early vacuum tube-based computers.

The DiVincenzo criteria is a guide that can be used to realize gate-based quantum computation, of which effects like quantum interference, entanglement, and superposition are highly important. Physical quantum bits (qubits) are primary components for making quantum logic gates, along with their controllers, converters, couplers, readout connectors, etc. To build these devices requires materials that are shapeable and can be patterned into useful objects, typically, a few nanometers thick. These are what we call nanoscale thin films. Many materials used in fabricating thin film devices for quantum are compatible with existing semiconductor fabrication tools (i.e., lithography, thin film deposition, and dry etching equipment).

DiVincenzo Criteria:

1. Scalable architecture containing well-defined qubits.
2. Distinct and reliable qubit state preparation.
3. Decoherence times much longer than gate operation times.
4. Universal set of quantum gates that perform accurate operations on the qubits.
5. Well defined readout capability for each individual qubit.

Physical qubits are a two-level system and can be made of *solid-state* or *non-solid-state* devices. This means that the single atoms or clusters of atoms or molecules being used to make a useful qubit can exist in either a solid form of matter or a non-solid (photons, in this case). Devices based on superconducting junctions, quantum dots, nitrogen vacancies, and topological systems are of the *solid-state* type. Here, *solid-state* quantum devices will be highlighted. (In the future, we can expect more quantum platforms made of different solid-state materials that are also compatible with the latest manufacturing techniques, so keep this in mind).

In recent decades, nanofabrication techniques have made controllable quantum devices a reality, although quantum devices are not necessarily a sub-field of nanotechnology. It is widely acknowledged that device sizes from 1 to 100 nanometers (10 to 1,000 Ångstroms) are of the nanoscale. In this range, it is widely known that quantum effects are more likely to occur and are more observable in measurement. (Measurement

is usually performed physically or converted into an electronic signal that can be easily recorded for analysis to confirm quantum behavior). As a result, many fabricated quantum devices are made of nanometer structures, typically in the vertical direction. One can make a quantum device that uses <100 nanometers of individual layer thickness in the vertical direction while having micrometer dimensions in the lateral direction or one with <100 nanometer dimensions for both vertical and lateral directions.

For nanoscale features, optical (light) microscopes have difficulty in imaging, physically limited by the wavelength of light. Thus, an electron microscope or other specialized imaging system which uses wavelengths shorter than light are needed to properly view nanoscale objects while engineering a device.

The word “lithography” comes from the German word “lithographie,” a combination of the ancient Greek words *lithos*, meaning “stone,” and *gráphein*, meaning “to write.” In the context of nanotechnology manufacturing, lithography is referred to as the development of so-called one- and two-dimensional structures. Here, at least one of its dimensions is in the nanometer range. Lithography allows one to copy patterns from computer generated designs onto an underlying substrate with a compatible adhesion layer. (A substrate is a type of supporting foundation, usually a wafer, while an adhesion layer promotes bonding between the substrate and film of interest). There are two sub-categories of lithography: *masked* and *maskless*. One may also hear the term *direct-write*, which refers to maskless exposure techniques. The *masked* exposure technique is basically

like using a stencil, which allows one to draw designs repeatedly onto a surface by guiding a writing source through cut-out patterns.

General lithography is further divided into photolithography, electron-beam lithography, X-ray and extreme ultraviolet lithography, focused ion beam lithography and neutral atom beam lithography, soft lithography, colloidal lithography, nanopattern/imprinting lithography, scanning (thermal) probe lithography, atomic force microscope lithography, etc. Each method involves energy exposure to a specific area with either the help of beam control systems or a patterned mask.

The two approaches for general manufacturing are called *top-down*, which involves cutting away pieces of a bulk material, and *bottom-up*, which involves growing or assembling atoms and molecules into larger structures. These two methods are applied in nanofabrication. Since thin film etching is a *top-down* process, while thin film growth and nanomolding is a *bottom-up* process, lithography is considered to be a hybrid method since it can use either or both processes. Nanomanipulation and nanoimprinting are examples of mostly *bottom-up* fabrication techniques. Dry (physical) etching and wet (chemical) etching methods correlate to anisotropic and isotropic profiles, respectively. (A profile or side profile is referred to as a cross-sectional view).

Vacuum deposition chambers, their support systems, and interfaces can be seen in fabrication laboratories virtually everywhere. The two main types of deposition chambers are physical vapor deposition and chemical vapor deposition. These systems support the

growth of material multilayers on sample substrates, such as SiO₂ or MgO wafers. Common deposition techniques include sputtering, molecular beam epitaxy, atomic layer deposition, electroplating, and electron-beam evaporation, just to name a few. Each has its own advantages and disadvantages in terms of cost, complexity, reliability, scalability, application, and deposition rates. One may also hear the term *stack engineering*, which refers to the research and development on the improvement of thin film performance. Additionally, lithography, deposition, and etching of thin films can be predicted or simulated with physics-informed modeling using premade paid software or a scientific programming language such as Python. (Examples can be found on the GitHub platform). The computed results can then be 3D animated and analyzed to help inform parameters used on real nanofabrication equipment, with the added benefit of cost-savings.

Improving nanotechnology manufacturing methods enables innovative approaches for solving quantum hardware problems every day. To develop quantum devices, it usually begins with an idea on paper, where a device circuit or cross-sectional diagram of one eventually will become a real chip. One may choose to hand draw the ideas. Then, once the overall device function is principally understood, it can be translated to a software design application, such as *Autodesk AutoCAD*. Geometries can be modified and drawn to-scale on the software so that layers of the chip can overlap, interface, or connect with each other as intended. In more complicated designs, the steps can be programmed and automated using layout processing software.

From here, the design can easily be converted into a machine code by exporting specific file formats, with coordinates that a lithography machine can understand. The converted design file creates a virtually marked pathway to guide or control the beam or write head in a lithography machine. However, before it is uploaded for lithography, it should pass inspection for quality assurance and troubleshooting. Afterwards, the final machine code for patterning can be uploaded. From here, a prepared sample containing necessary (thin film) material layers for devices can be loaded for proper lithography alignment and exposure for polymerization.

When the initial lithography step is completed, the sample will be ready for etching, followed by deposition and planarization of required dielectrics, metals, or non-metal layers until the devices are finished and ready for testing. Sometimes, an extra step to add a device to a larger chip architecture or packaging is performed, including wire bonding. In the many pictures of quantum devices and processors you may find online or in books, the exposed wire bonds and leads can be seen connecting the chip to its packaging. It is the typical appearance of a finished test sample. For industrial-scale quantum device samples that are being mass manufactured, wire bonded components are sealed within the packaging, similar to classical semiconductor chips.

Notice that the general process described above is very similar to the scenario for 3D printing or computer numerical control (CNC) machining. (It involves design files that are converted into G-codes, which guide the printer or milling heads to their locations on

a printing or milling stage, using X-Y-Z coordinates. Coordinates are just the numerical values that are mapped out on a surface, layer-by-layer).

Standard Process Flow for Fabricating Solid-State Quantum Chips

Idea → Hand Drawing (Top-Down & Cross-Section) → Design File (Blueprint) → Design Inspection → Prepare Sample Layers Import Design into Lithography Machine Interface → Load a Substrate Sample (Wafer or Wafer Piece) → Perform Lithography Alignment (X-Y Reference Points) → Expose Substrate Sample → Develop Substrate → Post Processing, Wire Bonding & Packaging → Device Testing.

(Note: an inspection process is typically implemented at the end of each step).

If one wanted to visualize the engineering of atoms into nanostructures that can support quantum information systems, below are some ideas for intuition. The entire fabrication process is like preparing a multi-layered bakery item (e.g., cake), which gets sliced up into pieces and sculpted into arbitrary 3D shapes. (In the supplementary images, you can see an example of how a cake is formed into unique shapes by this description). Another analogy for the process of nanofabrication is the stacking of LEGO bricks, which too can be separated into groups of unique shapes. As a metaphor, each individual brick is the representation of an atom, some of which are slightly larger than others, yet still interlinkable overall.

By examining a close-up of atoms through an imaging system that supports atomic resolution modes, one can observe arrangements of dots. These dots displayed on such a microscope (e.g., transmission electron microscope or scanning tunneling microscope) are more like representations of atoms, based on the interaction of electrons around each atom

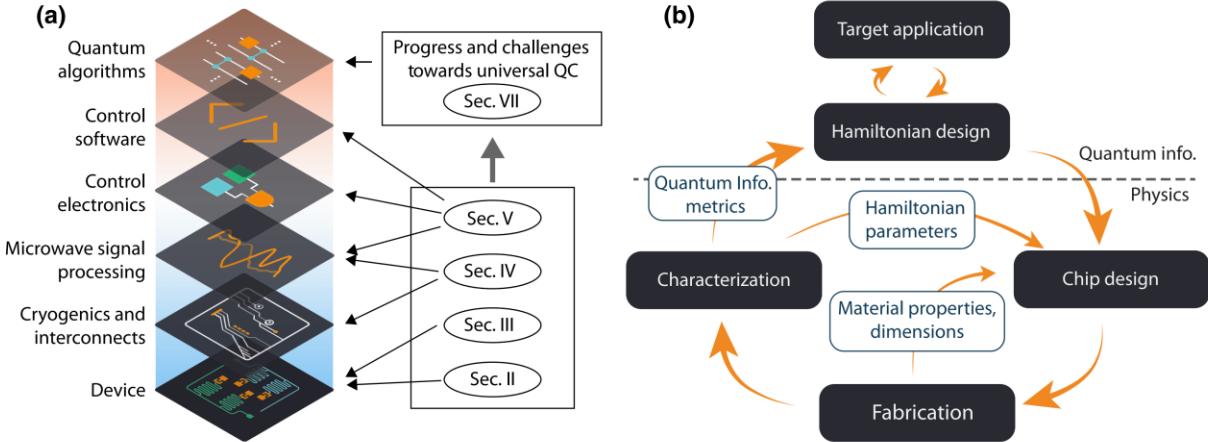
with the beam or probe being used to scan a sample. Although you cannot distinguish between individual electrons or components of the nuclei in each atom being scanned in the microscope, it is possible to measure things like interatomic spacing and crystallinity. In other words, one can choose to inspect nanostructures of fabricated samples using atomic resolution imaging techniques to check on how organized or unorganized its atoms are.

It is useful to combine electron imaging with other surface analysis methods to double-check on how well atomic layers will adhere or interface with each other. Diffusion barriers, tunnel barriers, and blockades are also closely inspected using the above-mentioned techniques in solid-state nanostructures. These layers typically exist at device interfaces and serve the purpose of filtering out states or impurities that may move from region to region based on applied heat, voltage, current, field, etc. Therefore, it is worth performing a cross-sectional inspection of the multilayers before patterning and optionally after a prototype chip has been patterned.

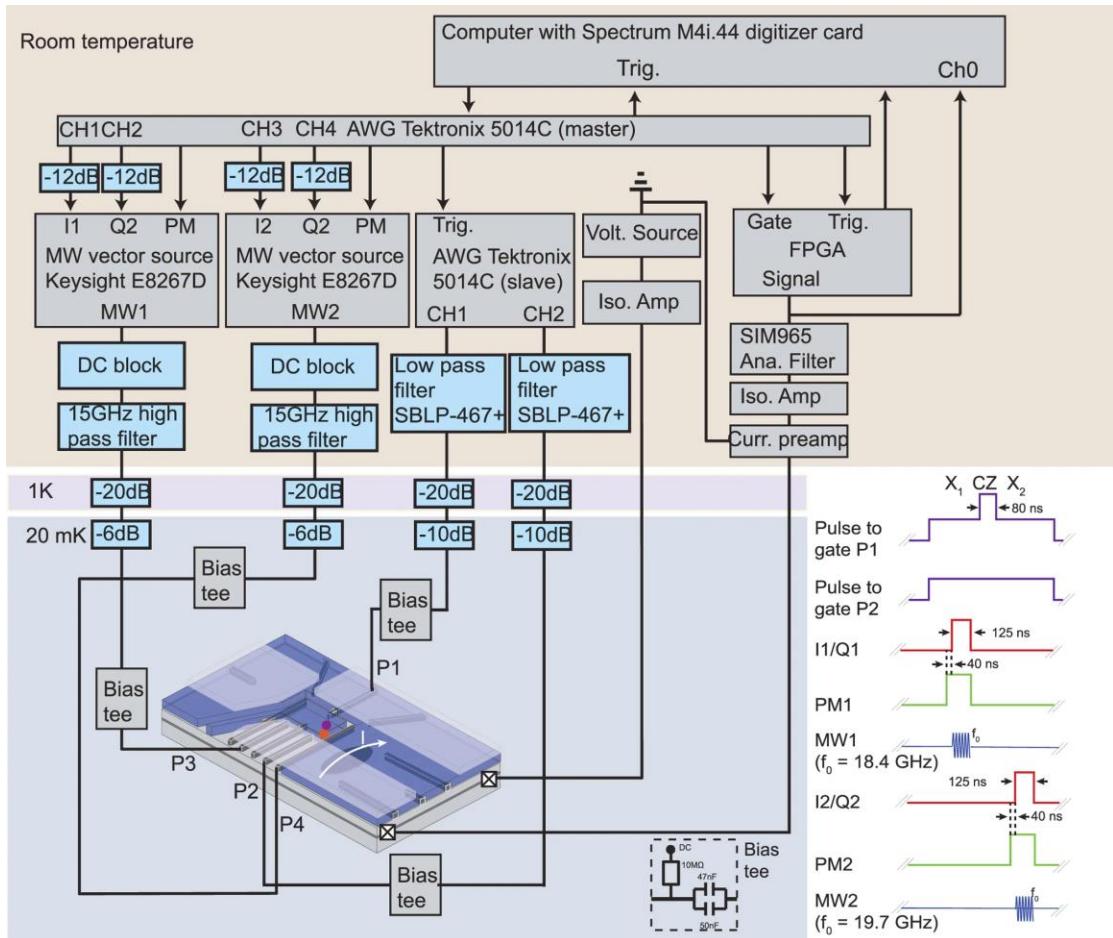
In conclusion, nanotechnology is a highly interdisciplinary STEM field that is applicable to quantum technology yet does not contain quantum as a specific sub-category. On the other hand, quantum technology does have a sub-category in hardware that covers nanotechnology. This is where quantum chips and devices are discussed. To build the chip hardware at the bottom of the *quantum stack* requires an understanding of manufacturing at the atomic and nanoscale. Precision control and fine tuning of systems

are key ideas of the intersection between both technologies. It can be leveraged to meet the needs of tomorrow and the future.

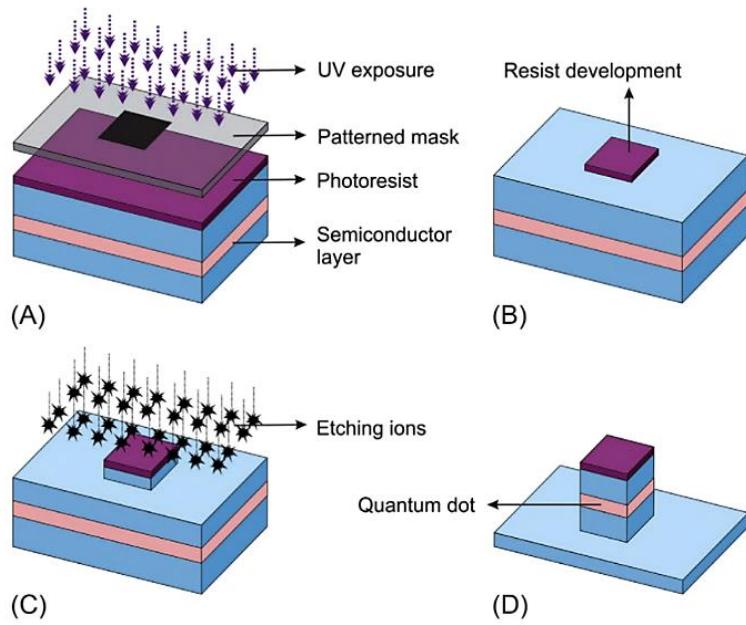
Supplementary Images:



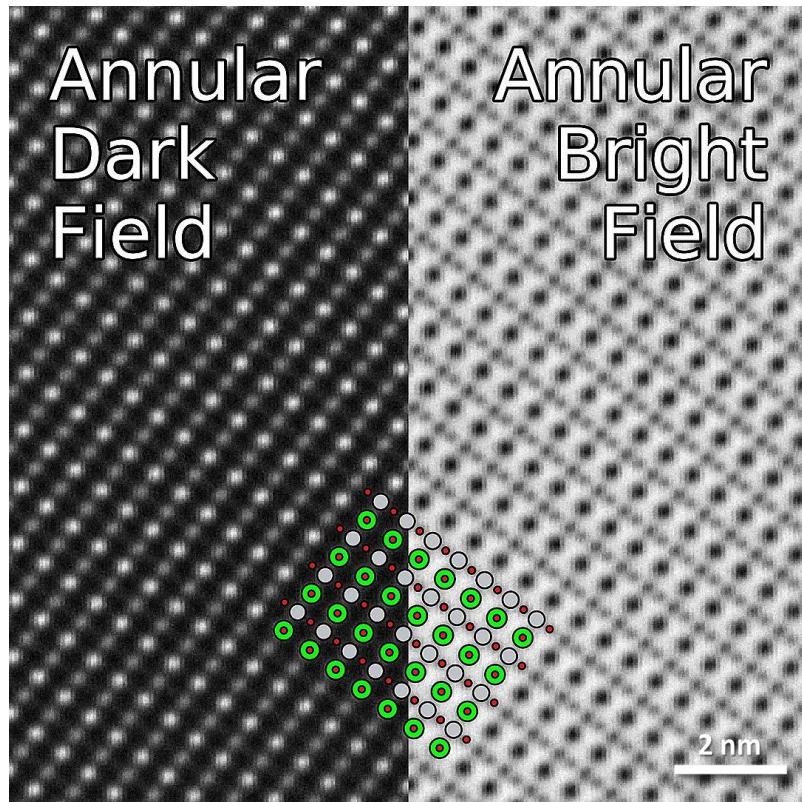
Overview of the Full Quantum Stack vs. the Engineering Cycle of Circuit Quantum Electrodynamics (cQED) Device (Gao et al., *PRX Quantum*, 2021).



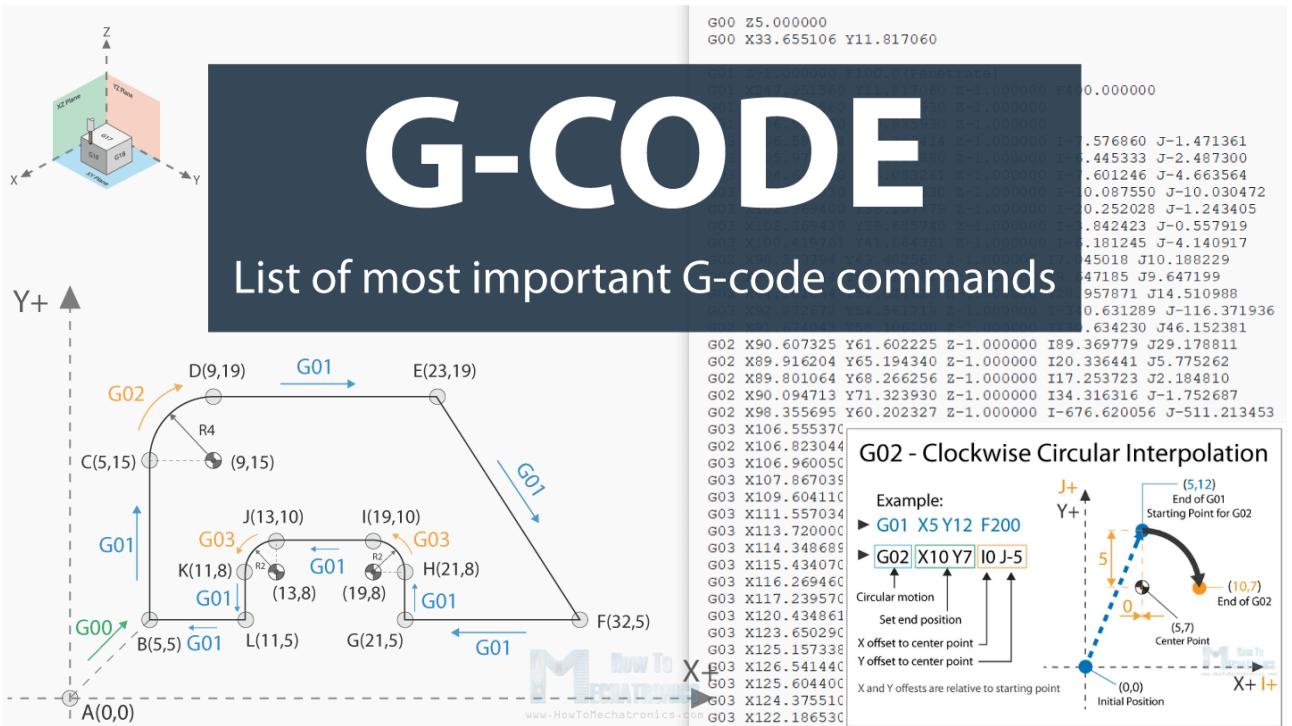
Detailed Schematic of the Measurement Configuration for a Quantum Processor Containing Two Single-Electron Spin Qubits from Quantum Dots (Watson et al., *Nature*, 2018).



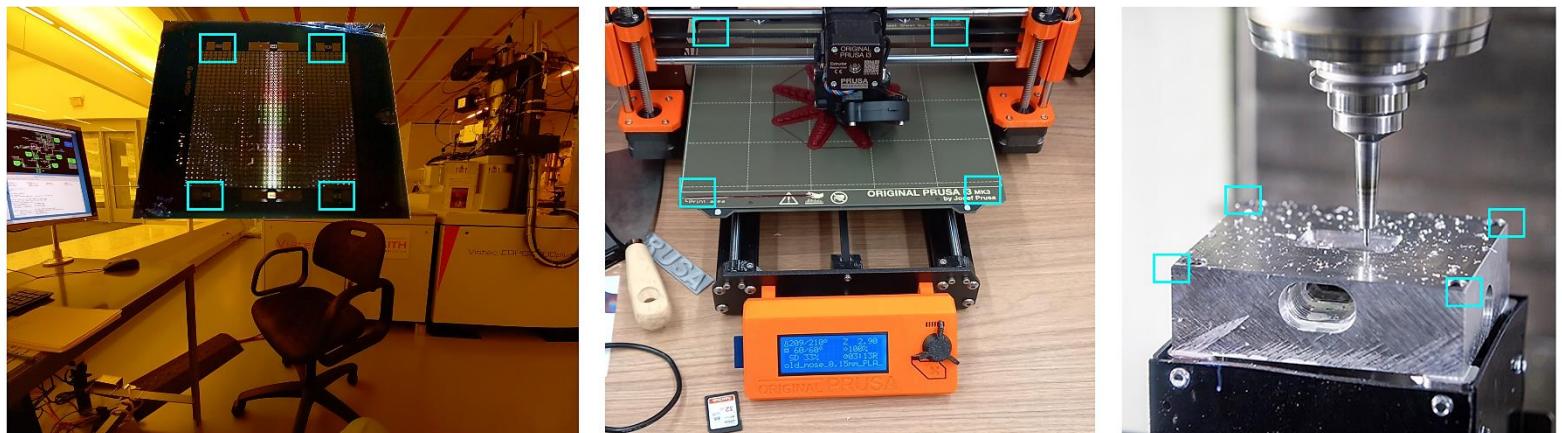
Stencil Cut-Out [Left] vs. Lithography Exposure Mask [Right]
(Onri Jay Benally) & (Kumar et al., *Synthesis of Inorganic Nanomaterials*, 2018).



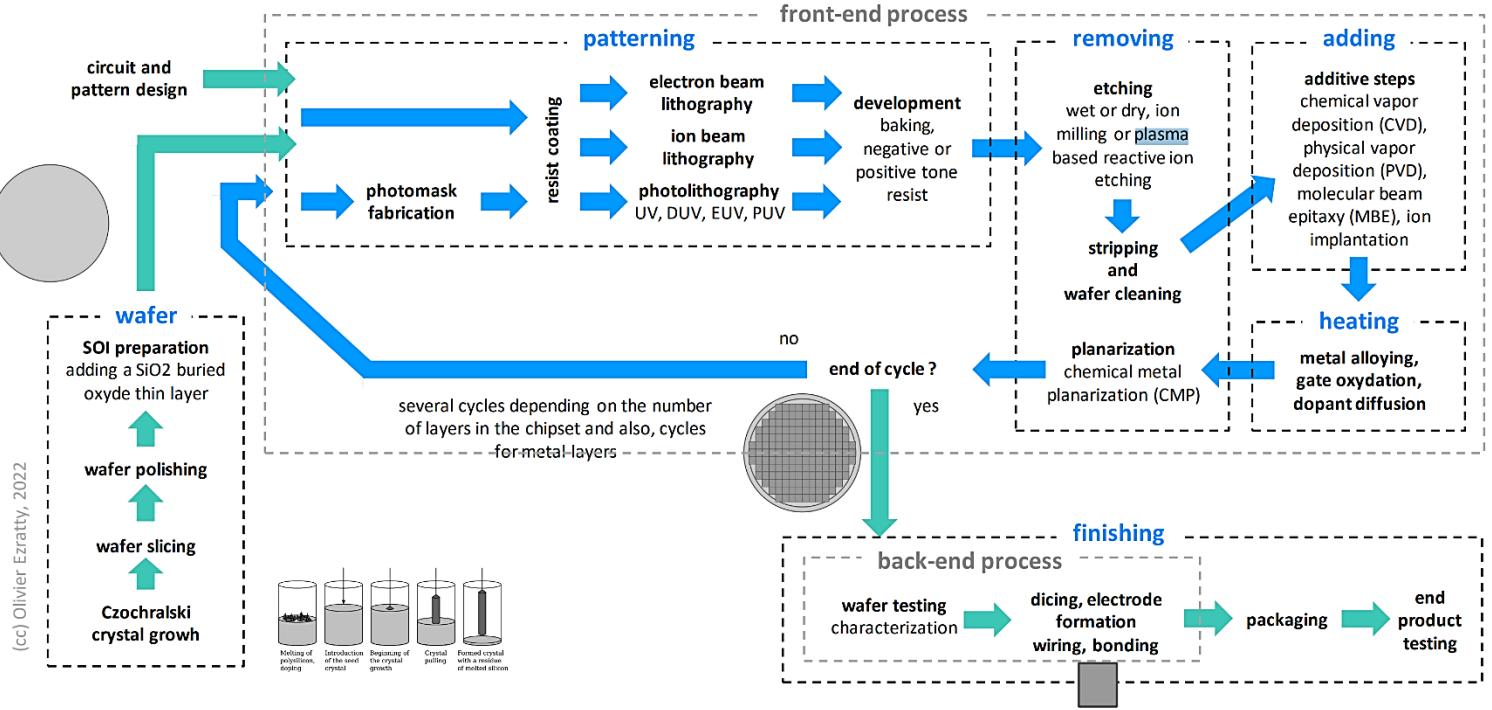
Dark Field & Light Field Images Taken Using a Scanning Transmission Electron Microscope (STEM). Shown is Crystalline Structure of Atoms From a SrTiO₃ Thin Film Sample. The Colored Dots Represent Positions of Atoms. Green: Strontium, Red: Oxygen, & Grey: Ti. (Wikimedia Commons).



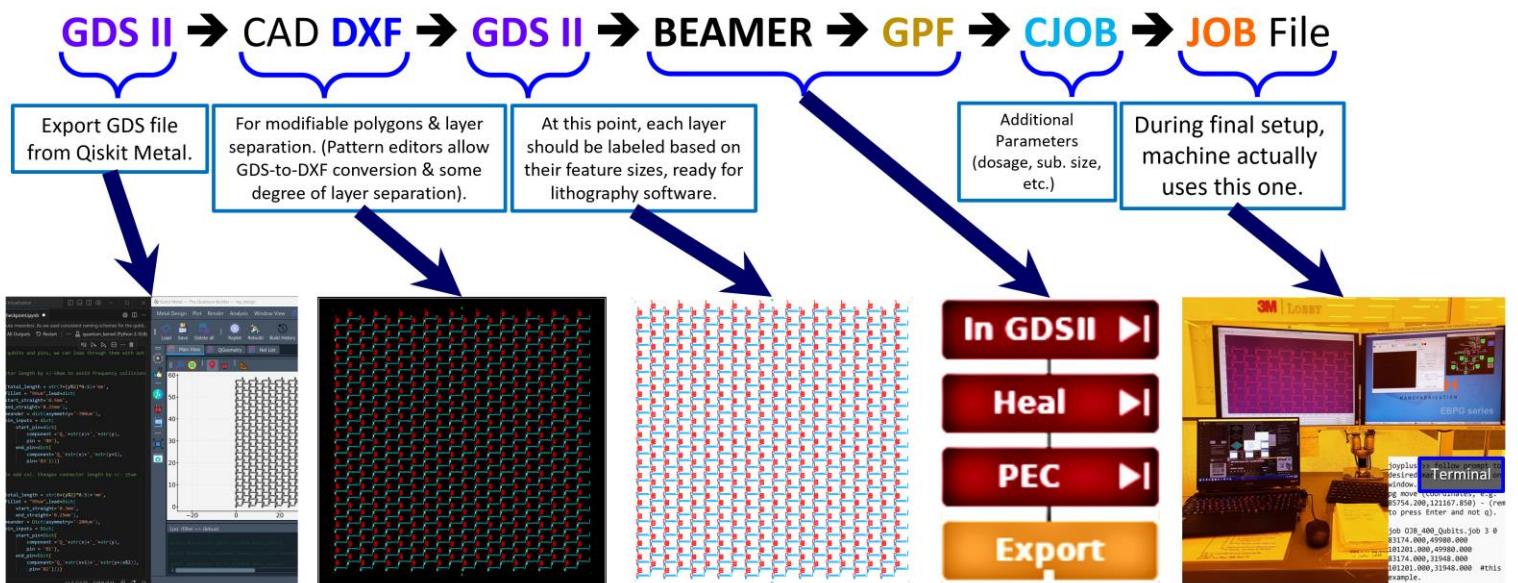
Example of G-Code Used in Both Top-Down and Bottom-Up Manufacturing. Application Includes But is Not Limited to LASER Cutting, CNC Machining, and 3D Printing (howtomechatronics.com).



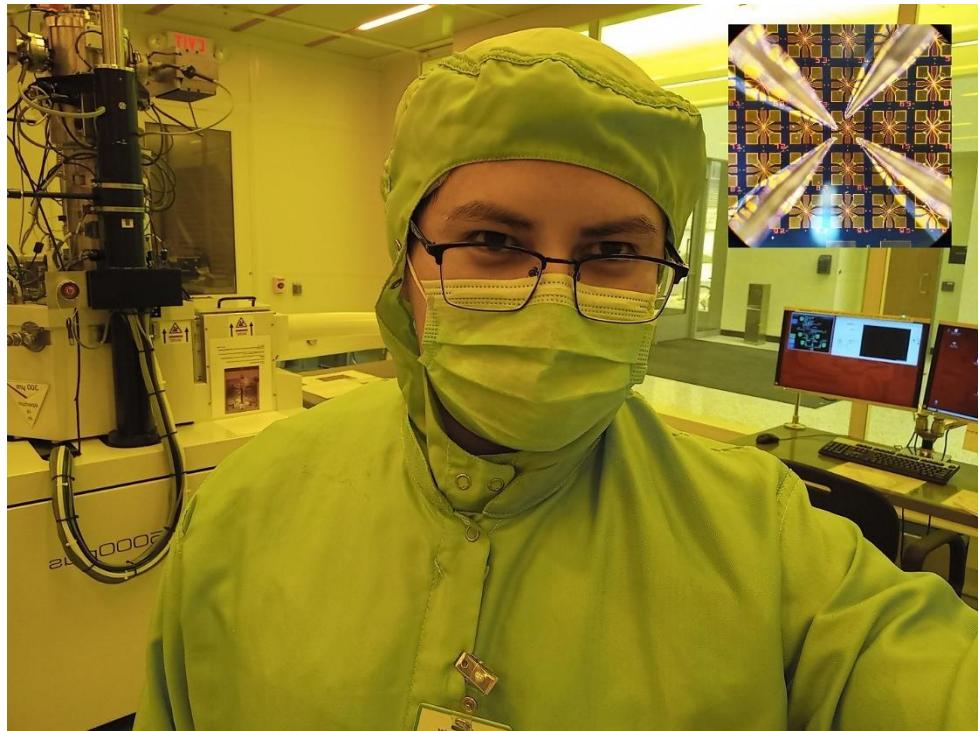
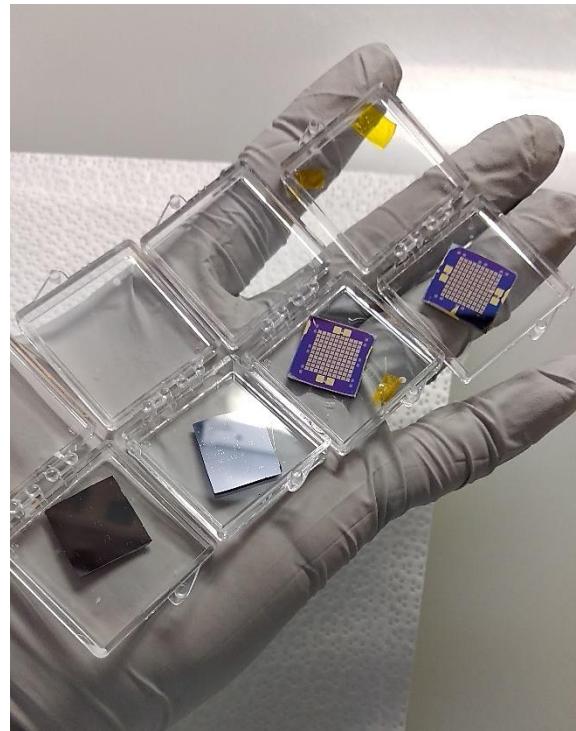
Reference Points Highlighted in Light Blue. Electron-Beam Lithography System [Left], Fused Deposition Modeling 3D Printer [Center], Computer Numerical Control Milling Machine [Right] (Onri Jay Benally) & (Protolabs).



Layout of a General Chipset Manufacturing Process
(Ezratty, *Understanding Quantum Technologies*, 2022).



Example of a Design Process Flow in Preparation for Electron-Beam Lithography Exposure (Onri Jay Benally).



Collection of Unpatterned & Patterned Spintronic Chips [Left]. Self-Portrait Containing a Raith EBPG 5000+ Maskless Electron-Beam Lithography System in the Background [Right] (Onri Jay Benally).

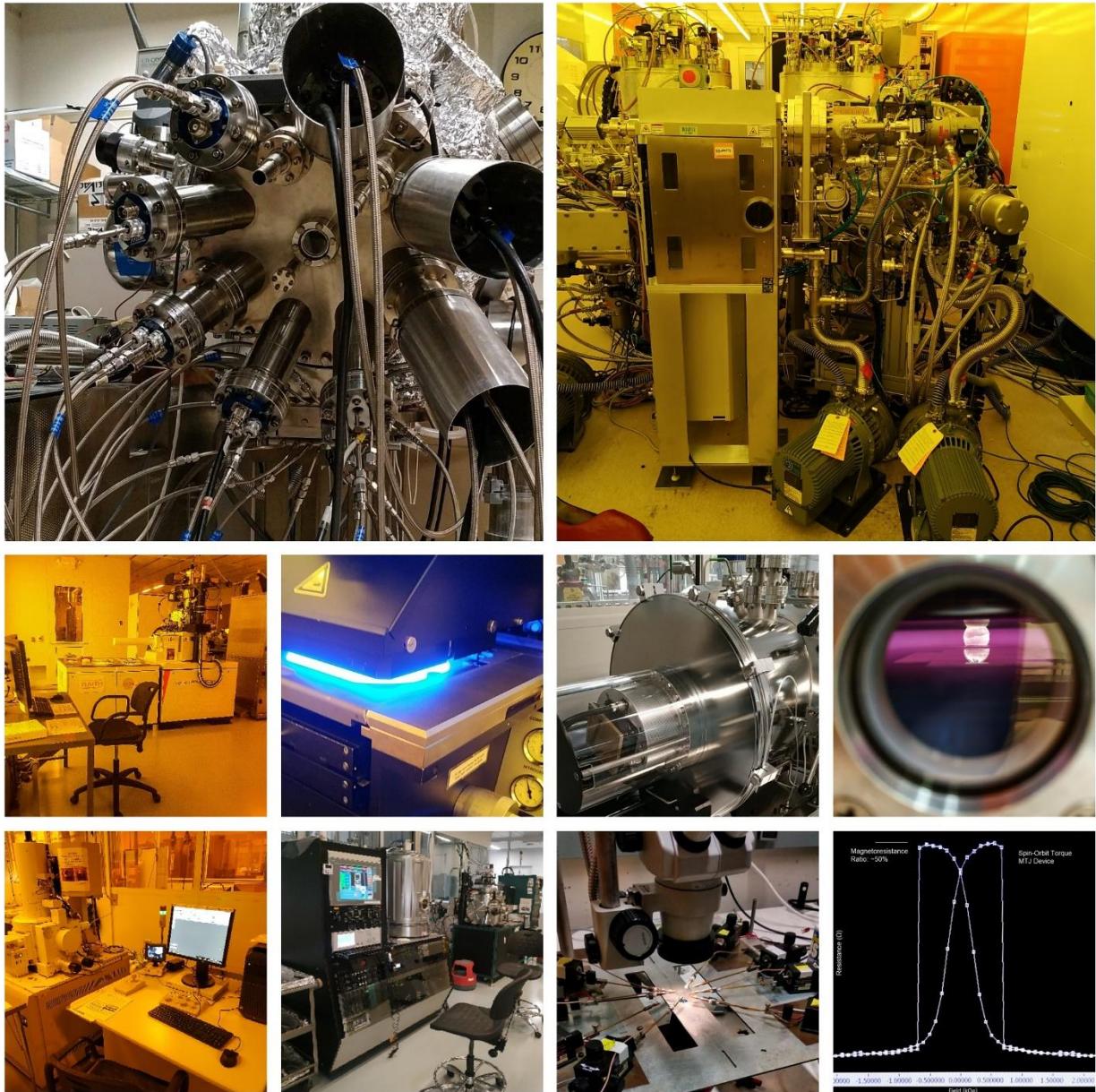
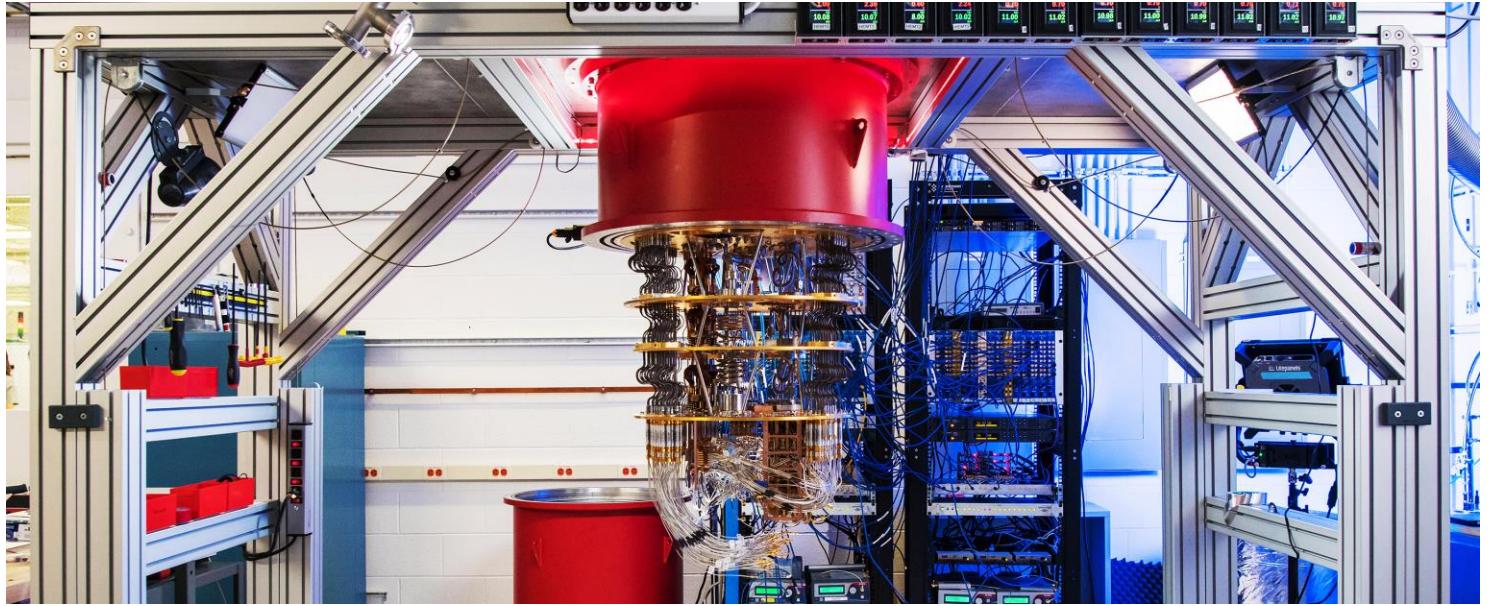
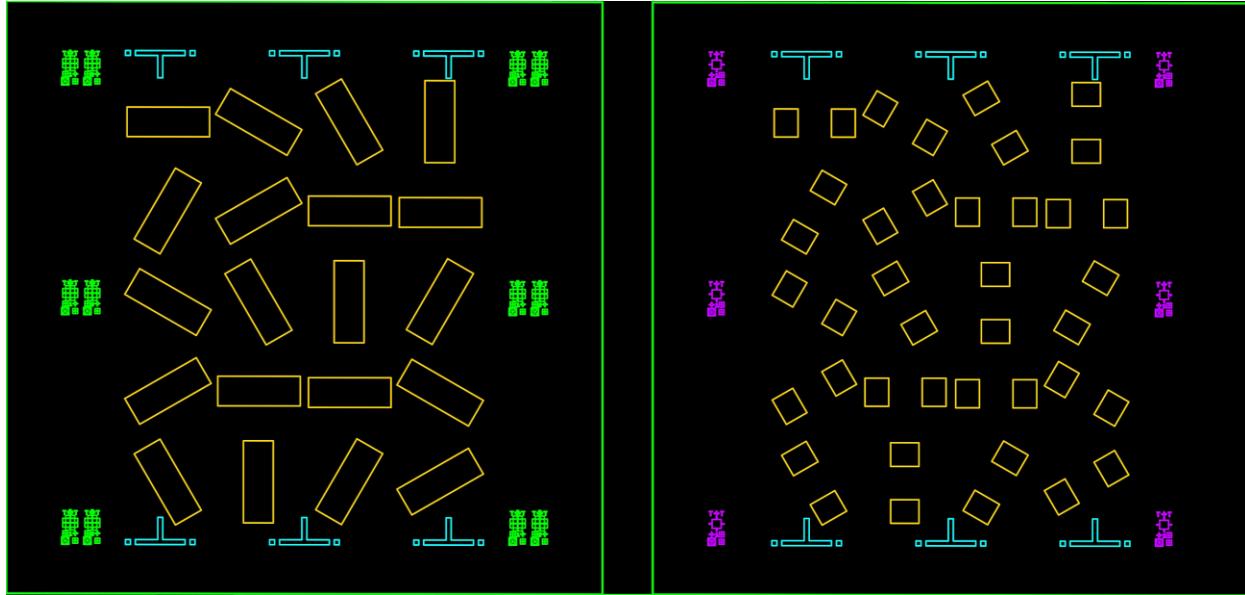


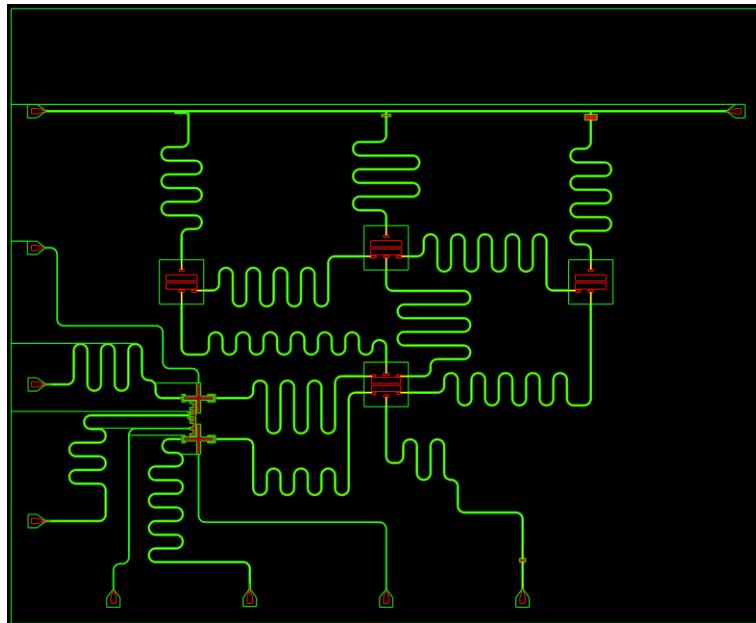
Image Collection of Deposition, Etching, Lithography, and Testing Equipment From the (Nano Magnetism & Quantum Spintronics Lab) & (Minnesota Nano Center), Located at the University of Minnesota-Twin Cities, USA (Onri Jay Benally).



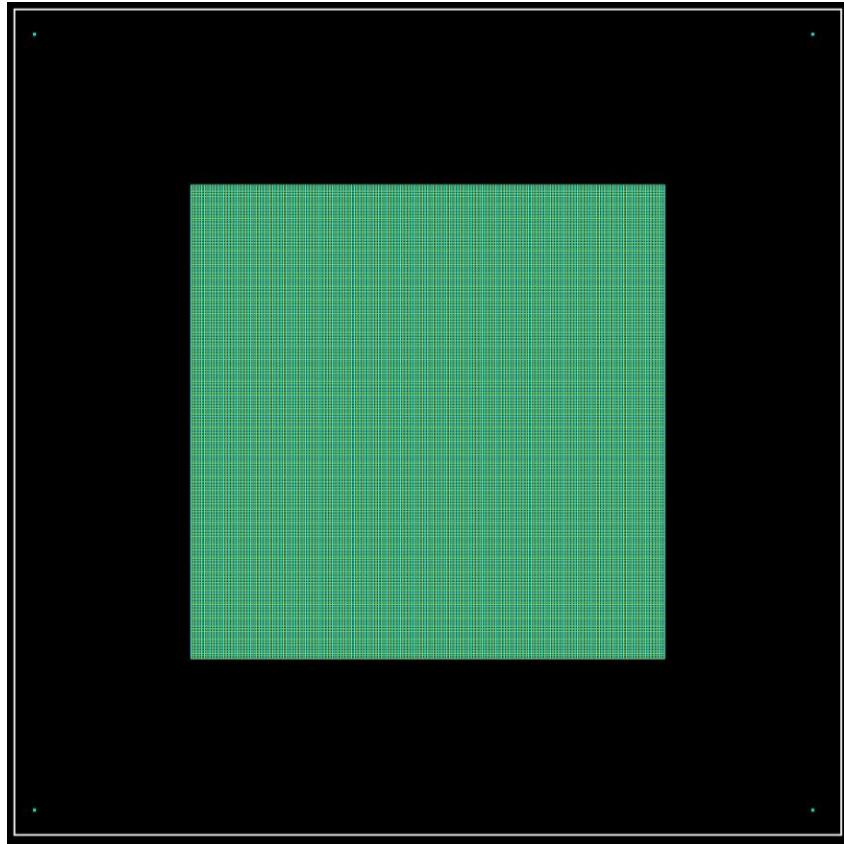
Wide Shot of the Cryogenic Lab within the Quantum Device Lab
(Google Quantum AI).



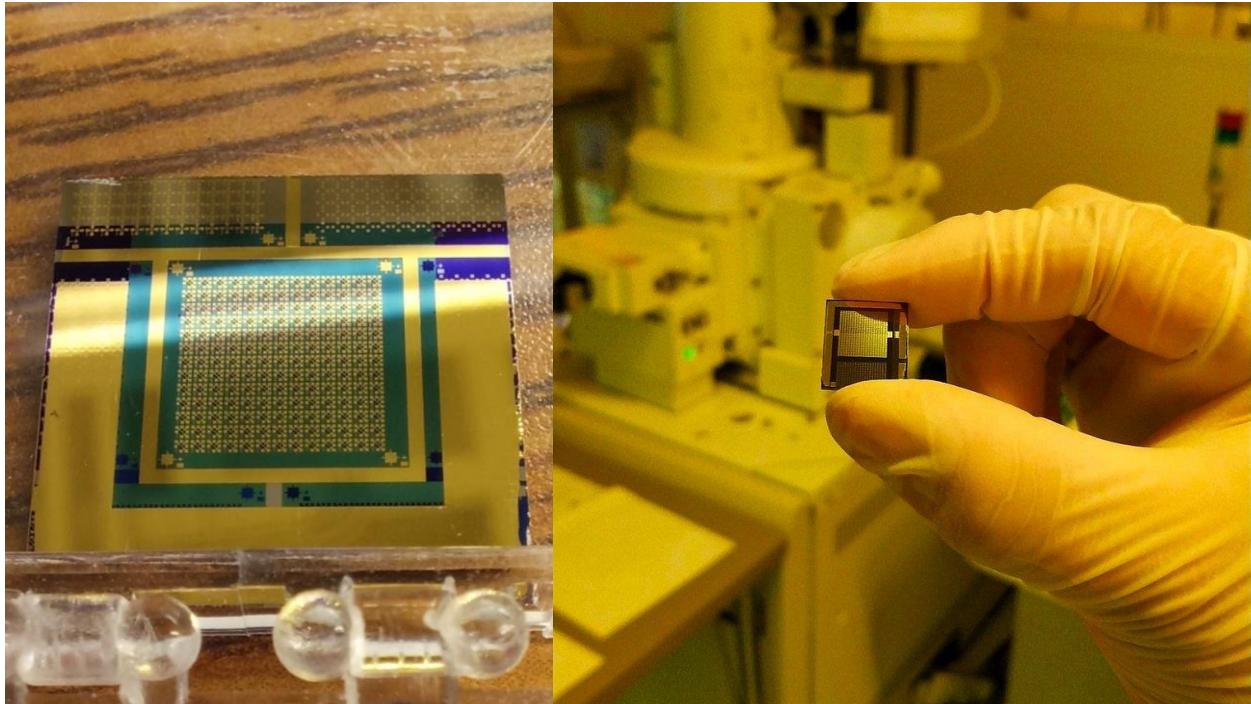
Randomized Micropattern Example of a 2-Step Lithography Mask Drawing Performed in AutoCAD, Containing Rough & Fine Alignment Markers (Onri Jay Benally).



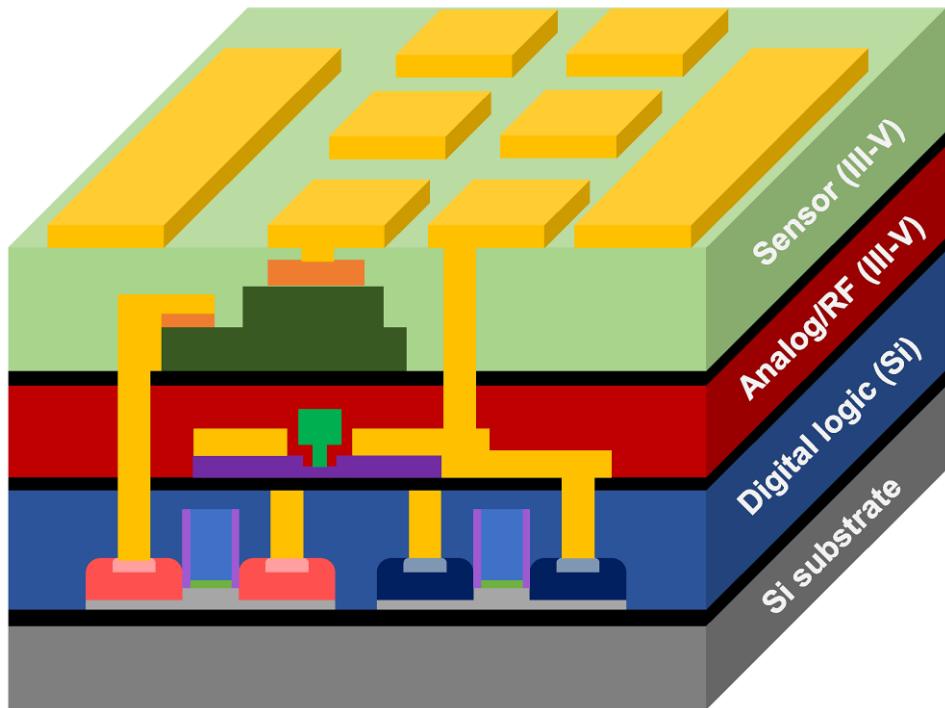
Example of a Multi-Step Lithography Pattern Layout of 6 Superconducting Qubits Converted from an Automated GDS Design File in Qiskit Metal to an AutoCAD Drawing for Inspection (Onri Jay Benally).



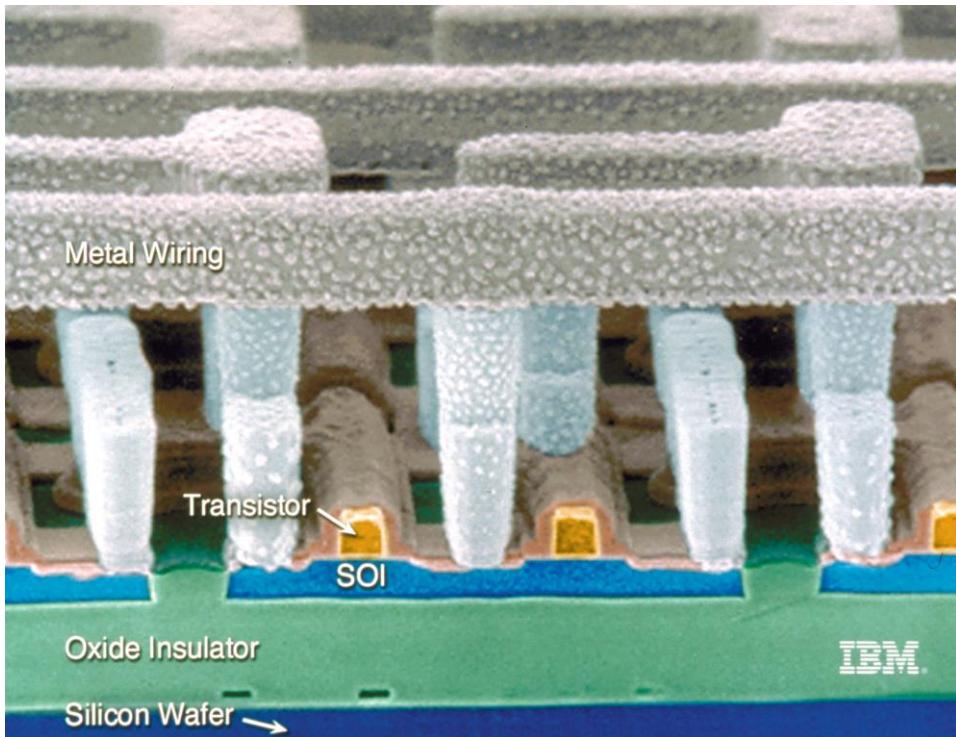
Example of a Generic Crossbar Array Layout Shown as an AutoCAD Drawing with Tiny Square Alignment Markers Near the Corners of the Chip (Onri Jay Benally).



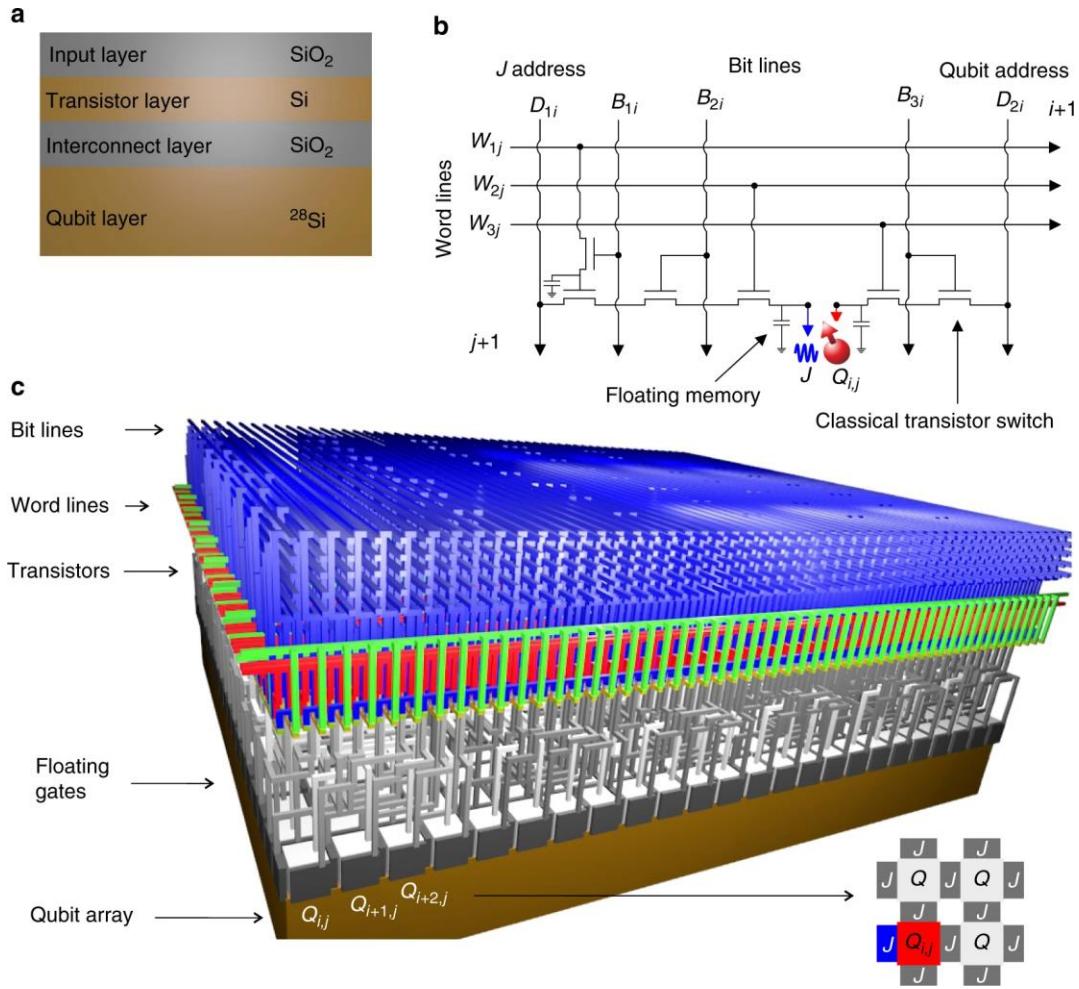
Two Fully Fabricated Samples That Employ Spin Dependent Quantum Tunneling For Efficient Classical Memory in Spintronic Devices Called Spin-Orbit Torque Magnetic Tunnel Junctions (SOT-MTJs). Applications Include but are Not Limited to Magnetic Random Access Memory, Spin Logic Arrays, & Spin-Based Oscillators
(Onri Jay Benally).



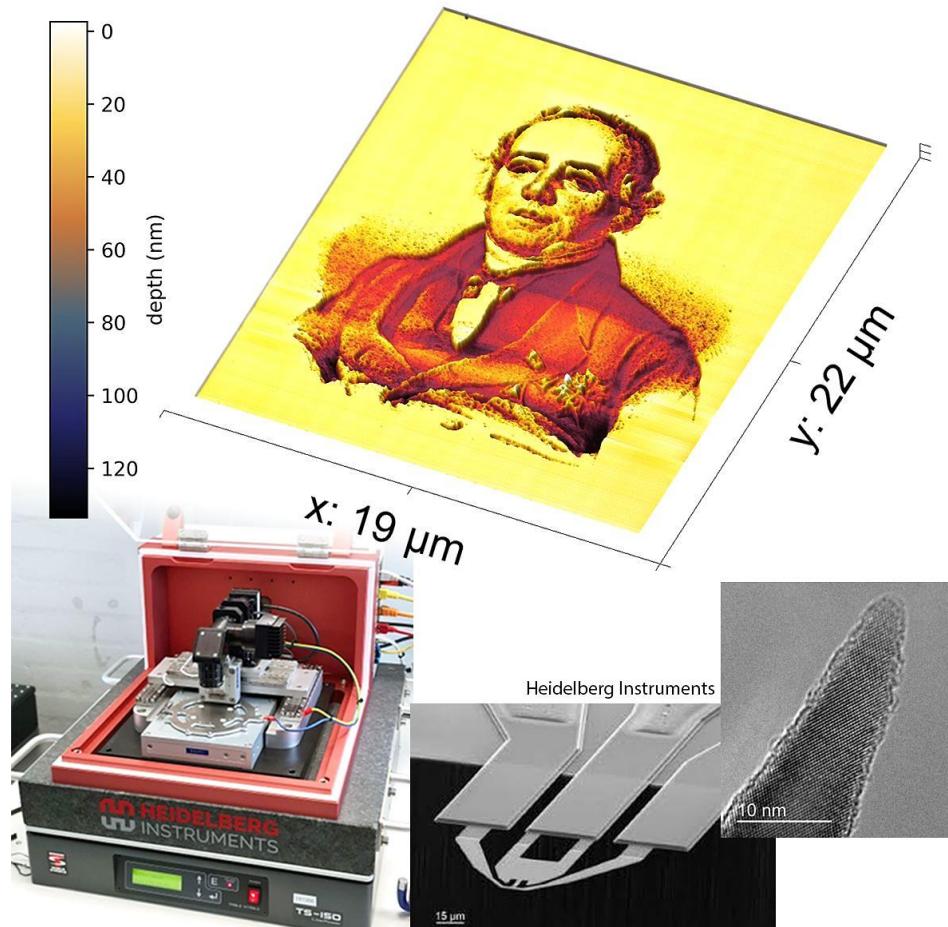
3D Model Cross-Section Of An Integrated Device Containing Many Layers Of Deposited, Lithographed, Etched, & Polished Metal (Conductors), Oxides, Nitrides, & Semiconductors (Wikimedia Commons - KAIST).



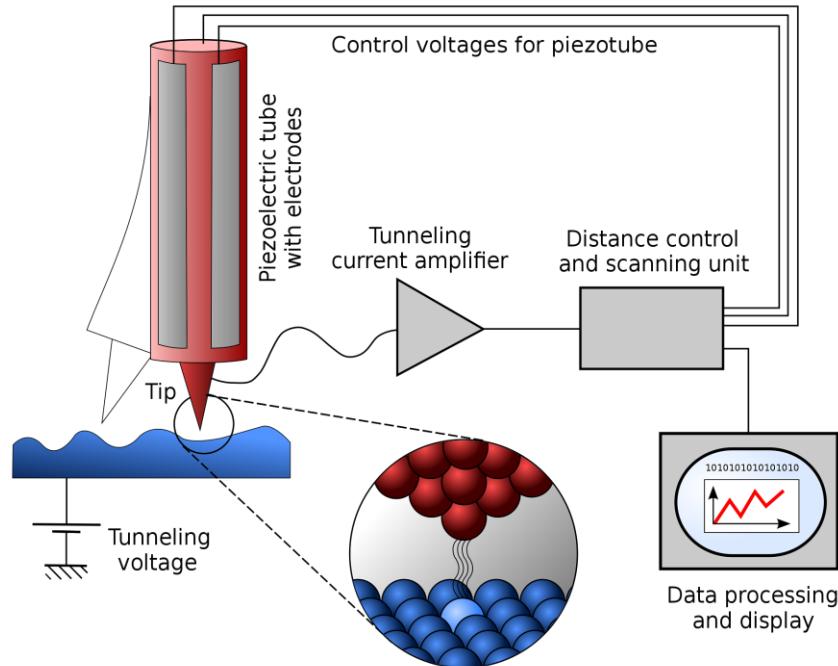
A Multi-Layered Application Specific Integrated Circuit on Silicon (IBM Research).



3D Model of a Quantum Integrated Circuit (Veldhorst et al., *Nat Commun*, 2017).



A Portrait of Hans Christian Ørsted That Was Nanopatterned and Subsequently Scanned with an Atomic Force Microscope Probe on the Same Machine, a Heidelberg NanoFrazor® Scanning Thermal Probe Lithography System (Technical University of Denmark-Physics & Heidelberg Instruments).

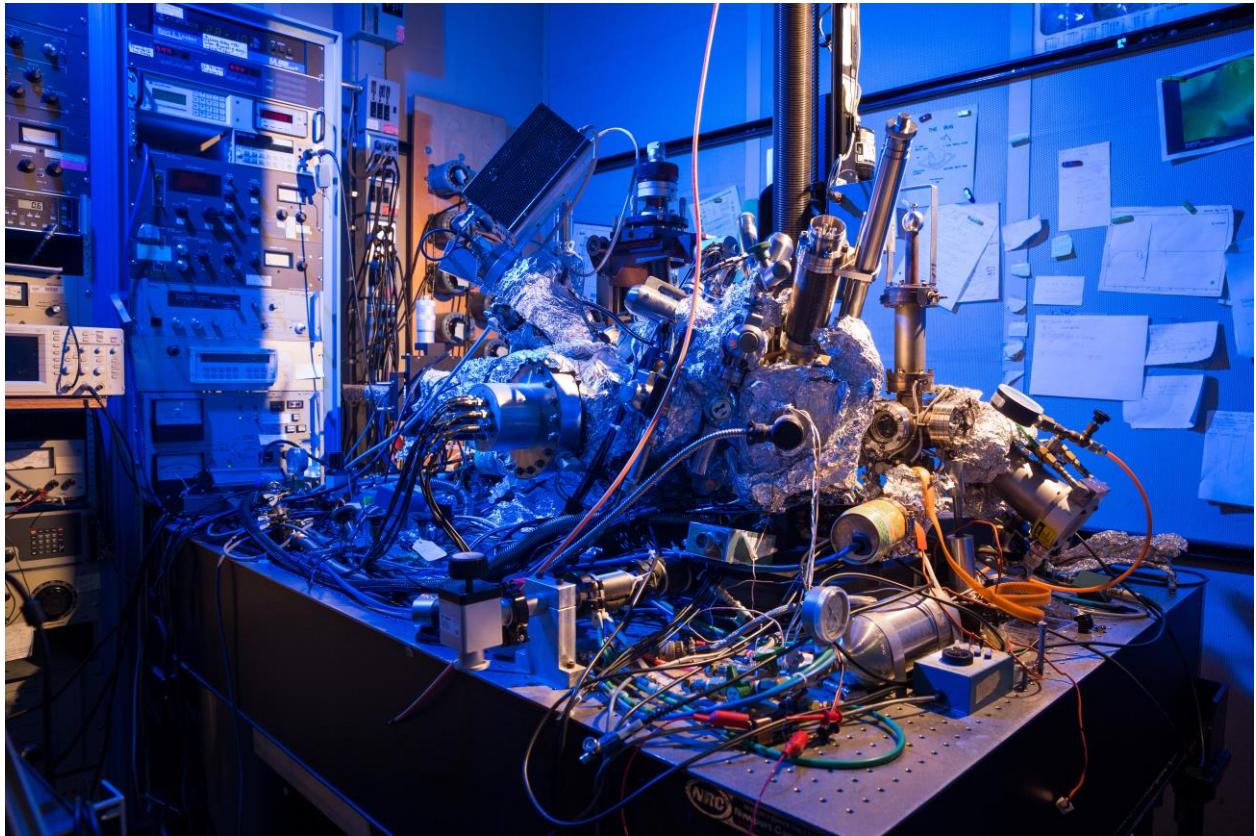


Schematic of a Scanning Tunneling Microscope Used to Image the Topology of a Material or Device Surface at the Atomic Level.

(Michael Schmid and Grzegorz Pietrzak, CC BY-SA 2.0 at, <https://commons.wikimedia.org/w/index.php?curid=89194170>)



A Desktop Scanning Tunneling Microscope (STM) Capable of Atomic-Level Resolution.
(Nanosurf)



Setup of a Scanning Tunneling Microscope, Used to Capture Images of Single Atoms or Manipulate Their Position on a Substrate (IBM Research).

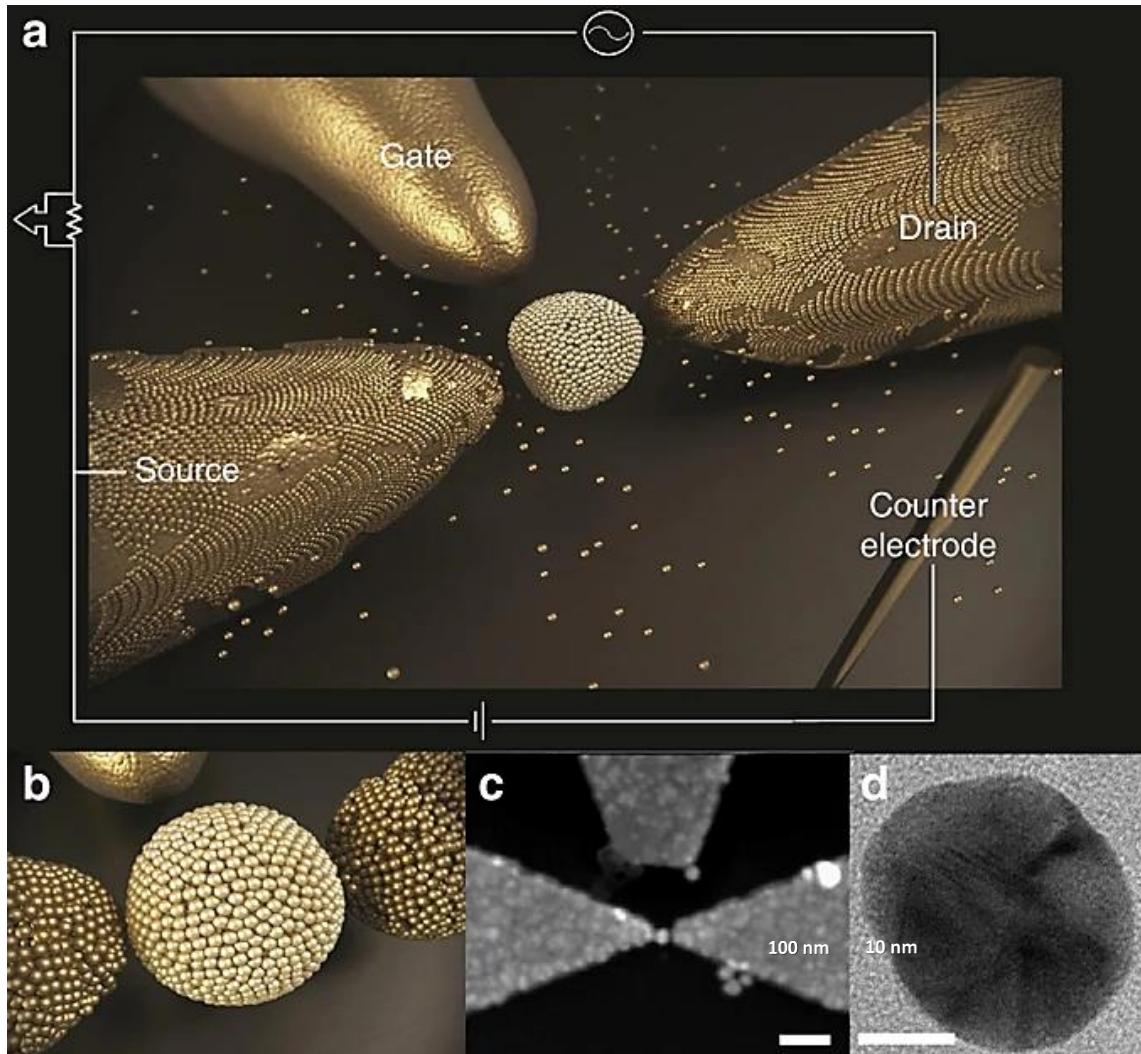
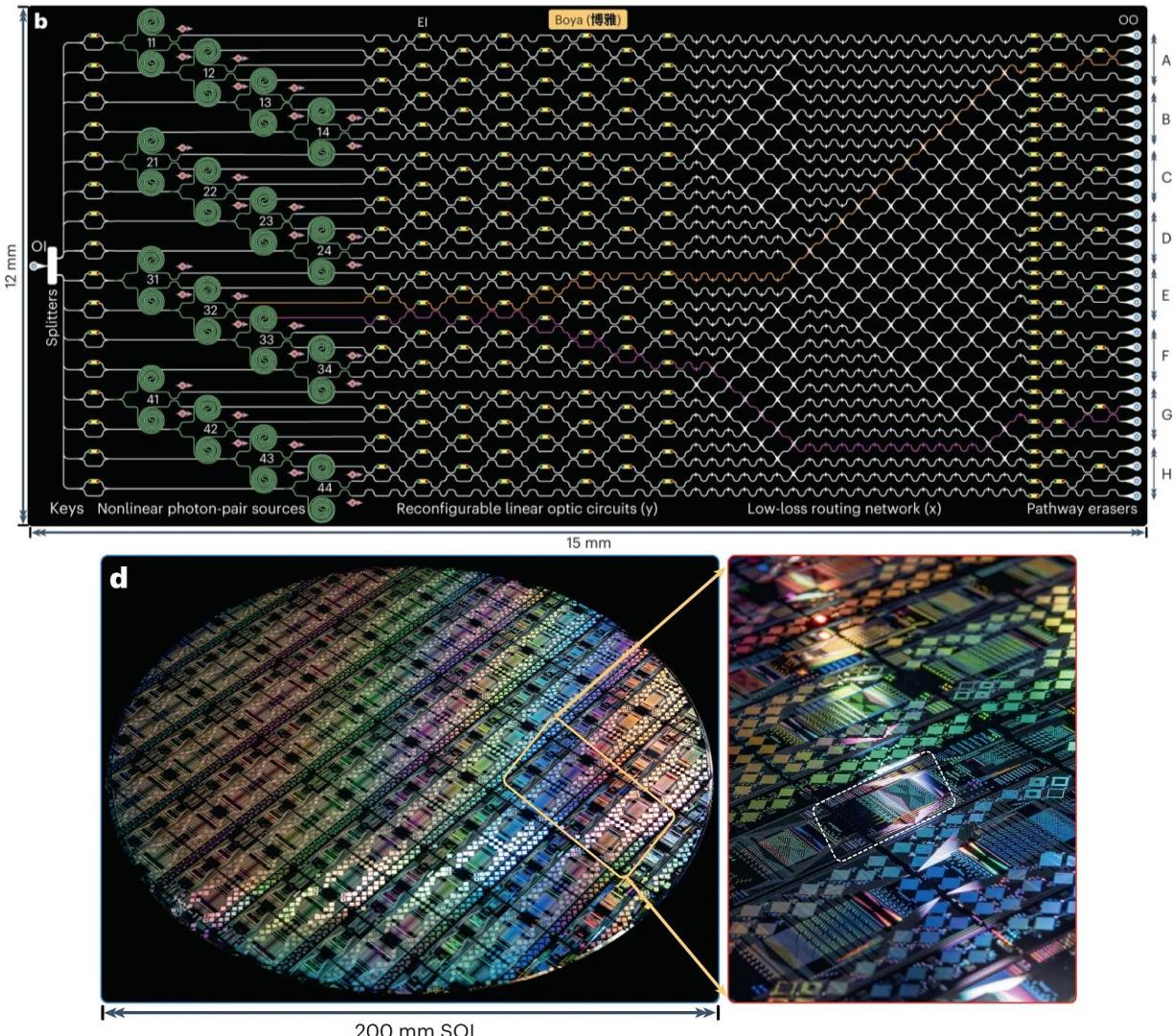
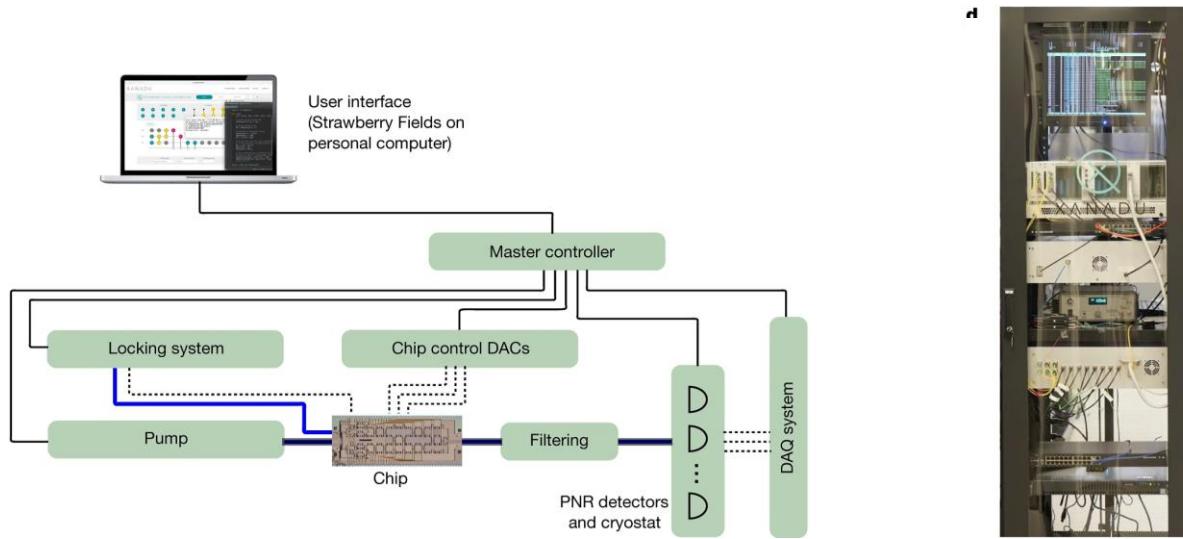


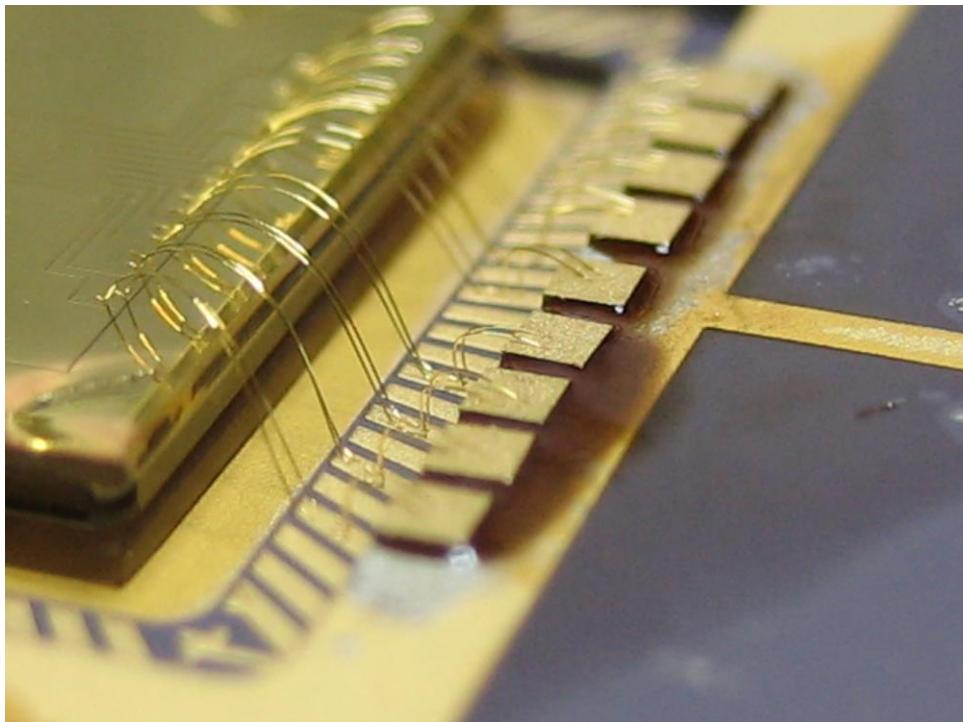
Illustration and Images of a Nanoparticle-based Single-Electron Transistor (SET), with an Arrangement of Source, Drain, and Gate Electrodes. The Last Two Images on the Bottom Show Both Scanning & Transmission Electron Micrographs of the Device
(Bitton et al., *Nat. Commun.*, 2017).



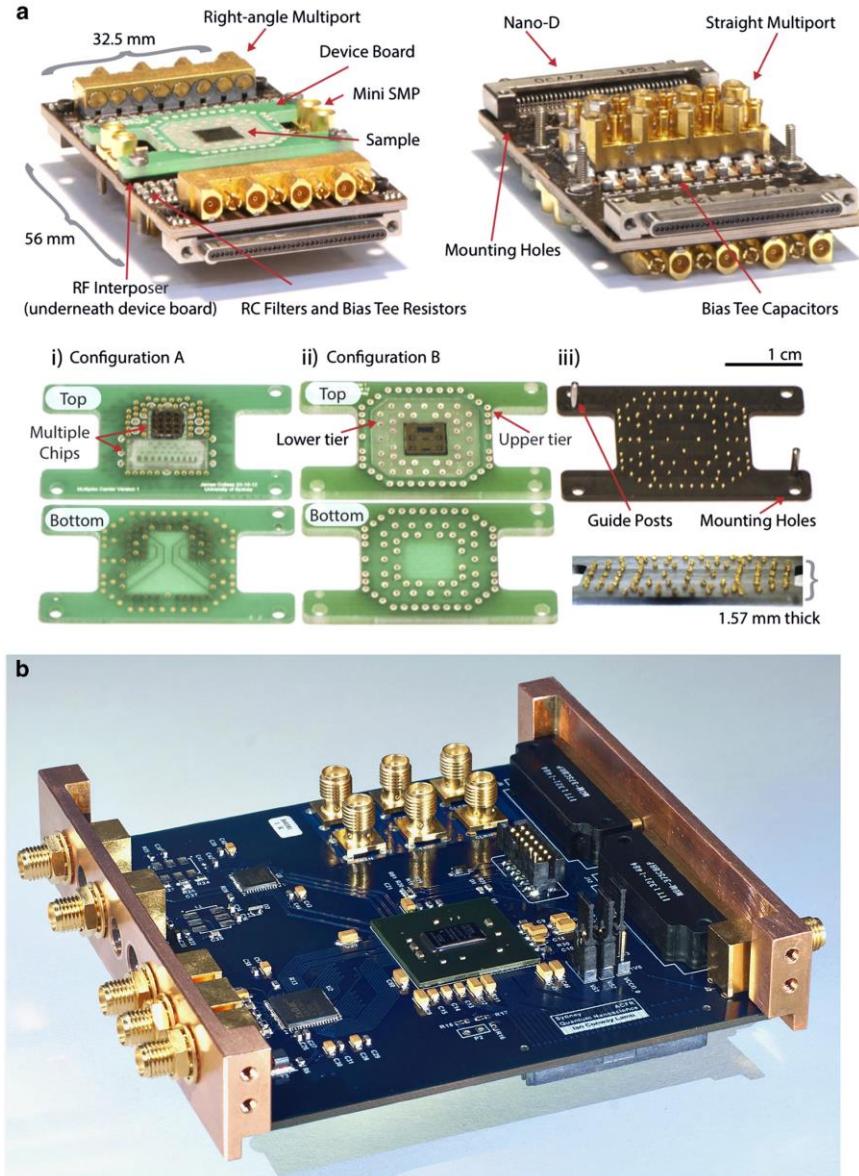
Chip Layout & Wafer Fabricated by Complementary Metal Oxide Semiconductor (CMOS) Processes for Quantum Photonic Circuits (Bao et al., *Nature Photonics*, 2023).



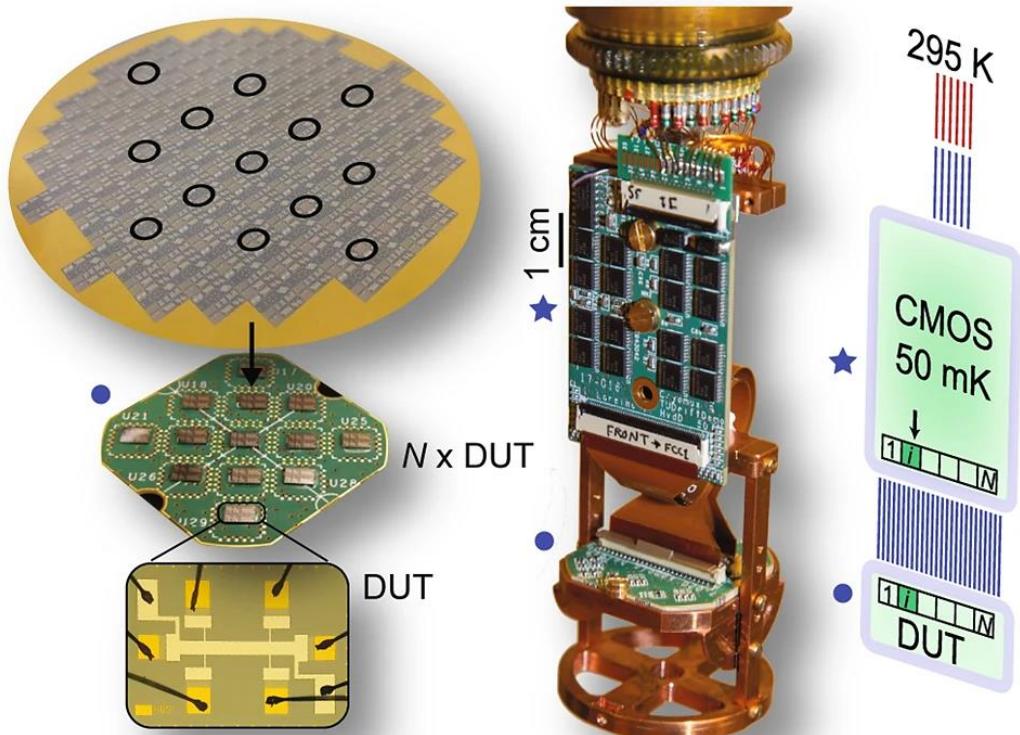
Example of a Measurement Configuration for a Quantum Photonics Chip
(Arrazola et al., *Nature*, 2021).



A Close-Up of Gold Wire Bonds on an Oxford Surface Ion Trap Chip,
(Jeff Sherman, 2009).



A Modular Cryogenic Circuit Board Containing Digital-To-Analog Converters & Analog-To-Digital Converters, for Interfacing Solid-State Qubits With Commercially Available Field-Programmable Gate Arrays (FPGAs). Its Purpose is Qubit Readout & Control (Reilly, *npj Quantum Inf*, 2015).



Example of a Compact Sub-Kelvin Measurement Configuration Using Commercially Available Complementary Metal Oxide (CMOS) Multiplexer.
(Wuetz et al., *npj Quantum Inf*, 2020).