# FILE OROLIA
# ART_CARD

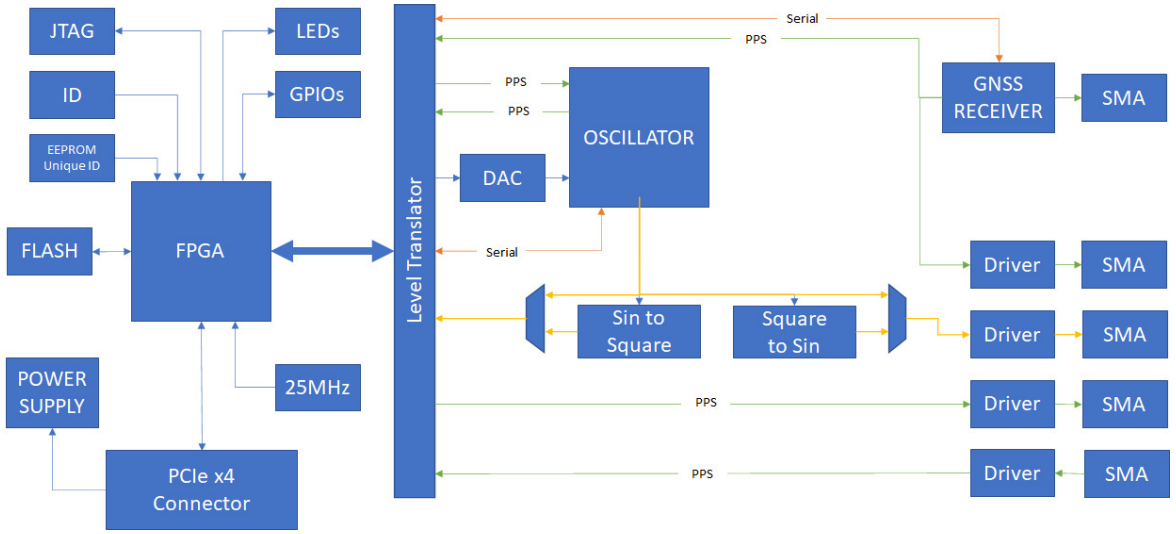
Réf PCB : **ART_CARD Rev 2**

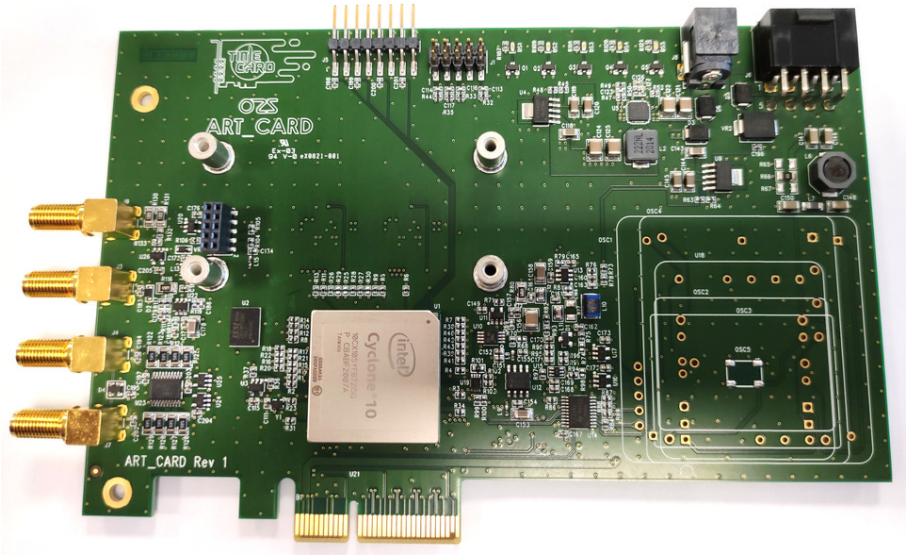
| | | |
|---|---|---|
| ⇨ | 7 | SHEETS OF ELECTRICAL SCHEMATICS |
| ⇨ | 1 | ASSEMBLY DRAWING TOP |
| ⇨ | 1 | ASSEMBLY DRAWING BOTTOM |
| ⇨ | 1 | SILKSCREEN TOP |
| ⇨ | 1 | SOLDER MASK TOP |
| ⇨ | 1 | COPPER LAYER TOP |
| ⇨ | 1 | COPPER LAYER INNER 1 |
| ⇨ | 1 | COPPER LAYER INNER 2 |
| ⇨ | 1 | COPPER LAYER INNER 3 |
| ⇨ | 1 | COPPER LAYER INNER 4 |
| ⇨ | 1 | COPPER LAYER BOTTOM |
| ⇨ | 1 | SOLDER MASK BOTOM |
| ⇨ | 1 | SILKSCREEN BOTTOM |
| ⇨ | 1 | DRILL DRAWING |
| ⇨ | 1 | STACK-UP |
| ⇨ | 1 | CIRCUIT BOARD SPECIFICATION |

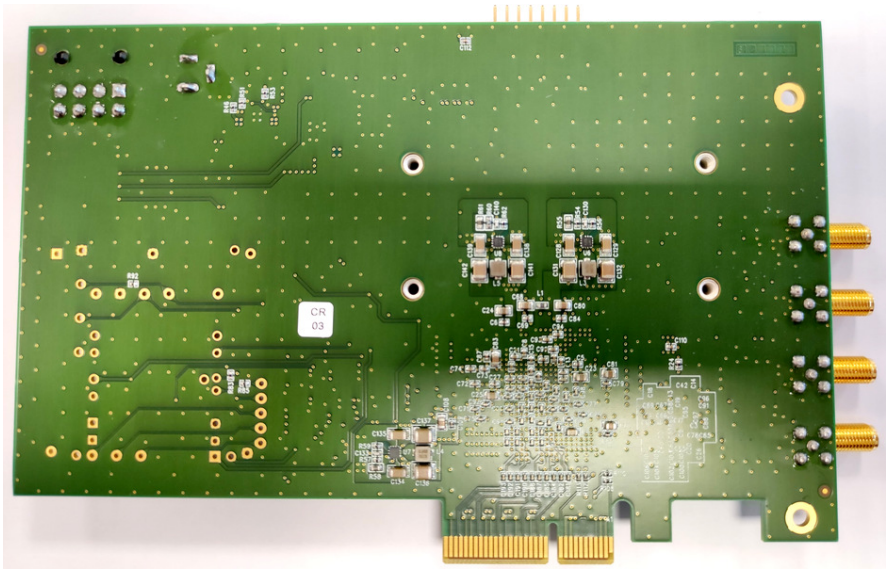
Artémis CAO ELECTRONIQUE

Angers Technopole
49070 BEAUCOUZÉ
Tél. : +33(0)2-41-48-41-40
contact@artemis-cad.com

1 bis Avenue du Bois l'Abbé
FRANCE
Fax : +33(0)2-41-48-41-44
www.artemis-cad.com



<Variant Name>

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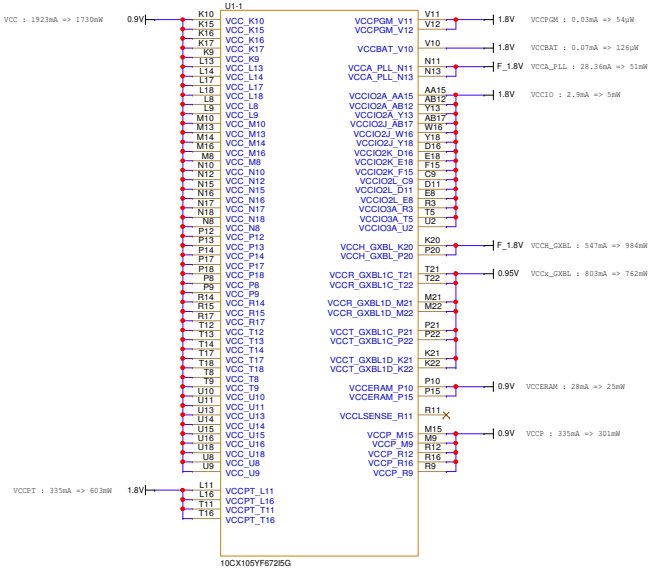
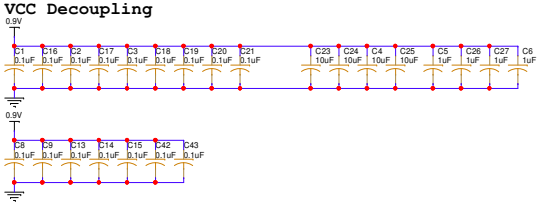
| | | |
|---|---|---|
| Title: OVERVIEW | | |
| Size: A2 | Document Number: ART_CARD | Rev: 2 |
| Date: Tuesday, April 13, 2021 | | |
| FILE NAME: ART_CARD | Sheet: 1 of 7 | |

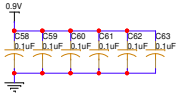
# FPGA POWER SUPPLY



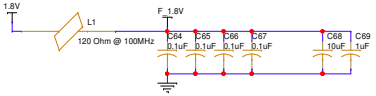

## VCC Decoupling



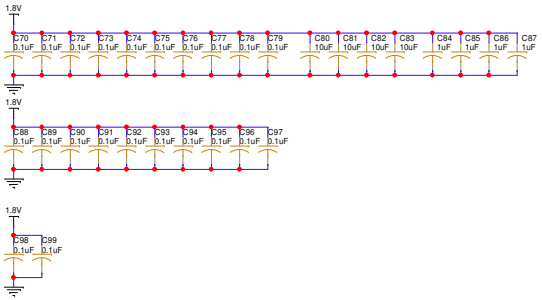

## VCCP and VCCERAM Decoupling



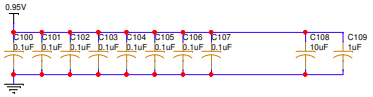

## VCCA_PLL and VCCH_GXBL Decoupling

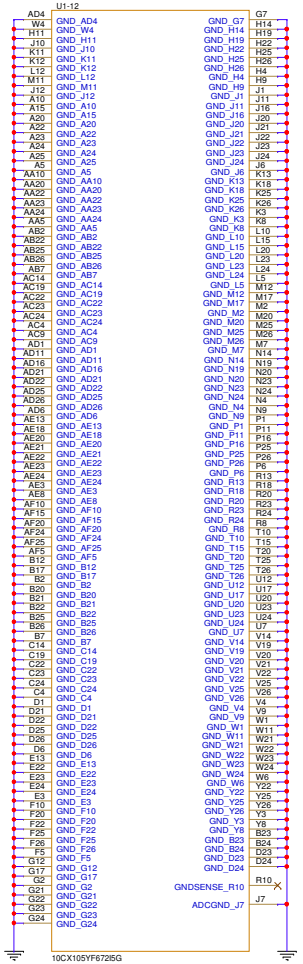



## VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling




## VCCR/VCCT Decoupling





<Variant Name>

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Title: FPGA POWER

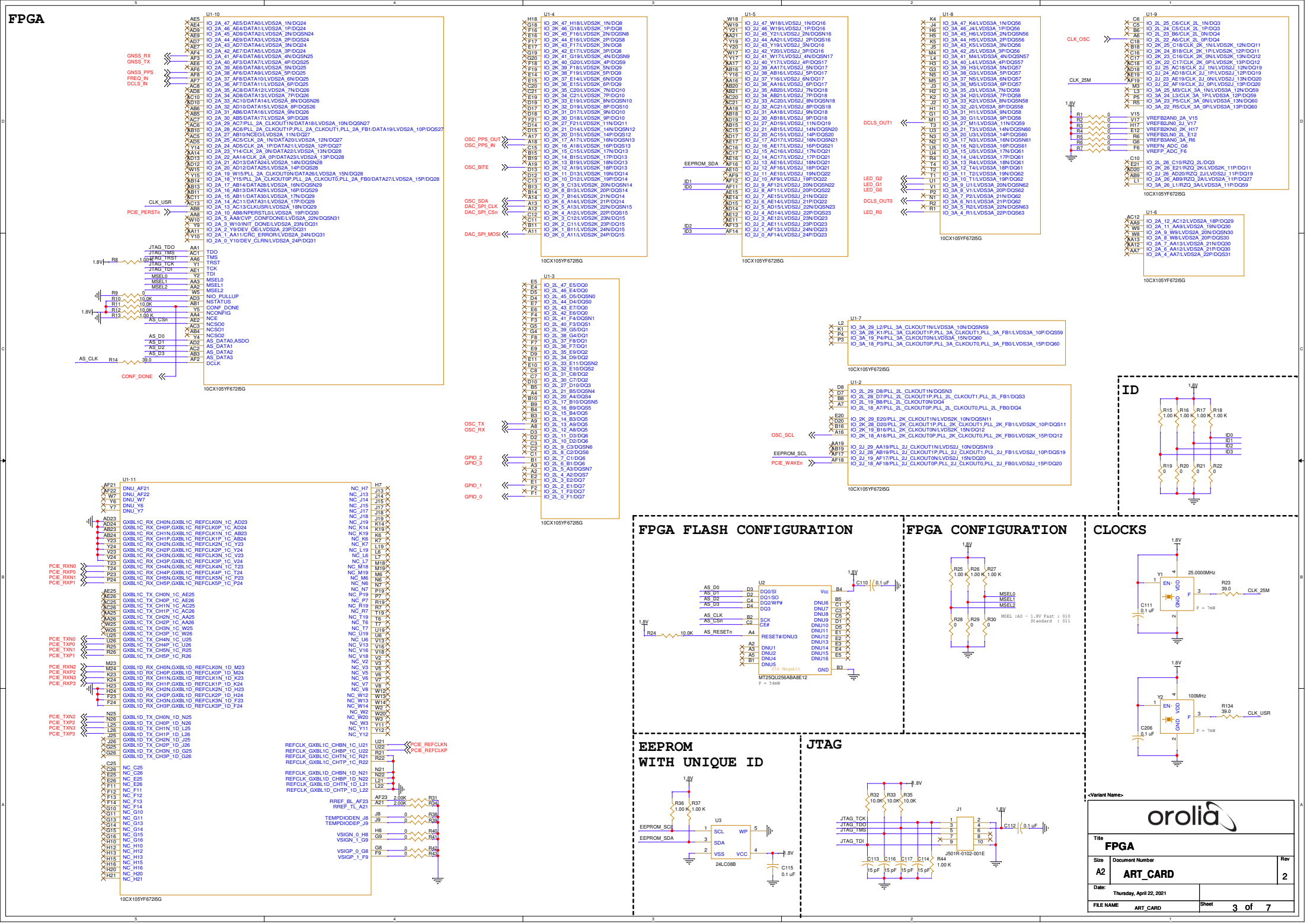
| Size | Document Number | Rev |
|---|---|---|
| A2 | ART_CARD | 2 |

Date: Tuesday, April 13, 2021

FILE NAME: ART_CARD

Sheet: 2 of 7

# FPGA




## ID



## FPGA FLASH CONFIGURATION




## FPGA CONFIGURATION




## CLOCKS




## EEPROM WITH UNIQUE ID




## JTAG




<Variant Name>

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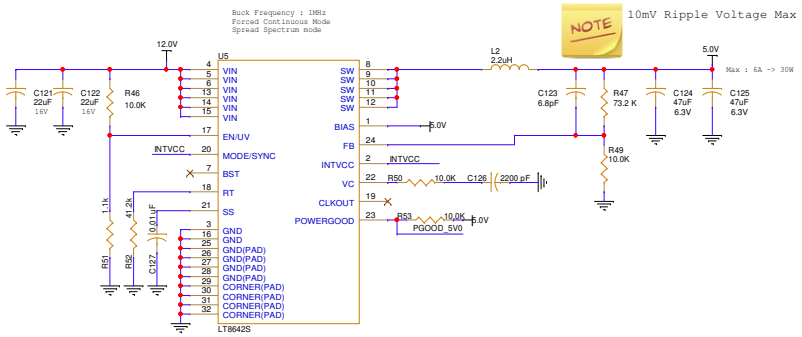
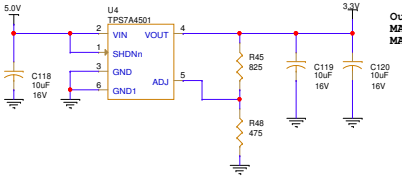
| | |
|---|---|
| Title | FPGA |
| Size | A2 |
| Document Number | ART_CARD |
| Rev | 2 |
| Date: | Thursday, April 22, 2021 |
| Sheet | 3 of 7 |
| FILE NAME | ART_CARD |

```
POWER NEED  : FPGA : OCXO : Comp : TOTAL
on 12V      :      : 7500 :      : 7500 mW
On 11V_ANA  :      :      :   80 :   80 mW
On 5.0V     :      :      :  350 :  350 mW
On 3.3V     :      :      :  243 :  243 mW
On 1.8V     : 1643 :      :   61 : 1704 mW
On 0.95V    :  762 :      :      :  762 mW
On 0.9V     : 2056 :      :      : 2056 mW
                                  -> 12695 mW
```

## 12V to 5V Switch Converter

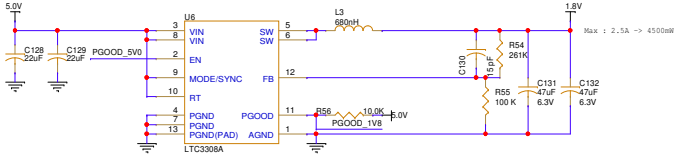



## 5V to 3.3V LDO Converter

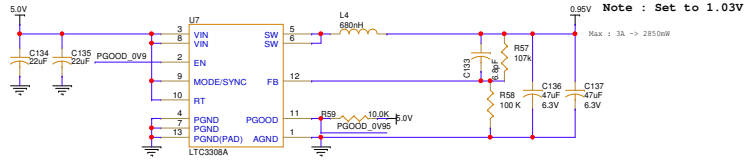



**Output : 3.3V**
**MAX : 0.46A / 1.53W @ Tamb = 85°C**
**MAX : 0.73A / 2.42W @ Tamb = 60°C**

## 5V to 1.8V Switch Converter

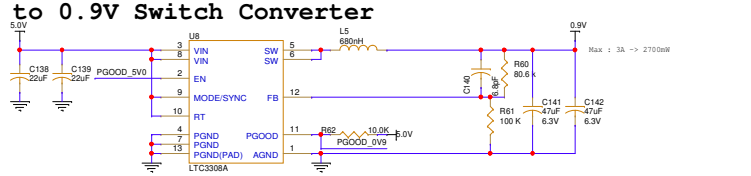



## 5V to 0.95V Switch Converter

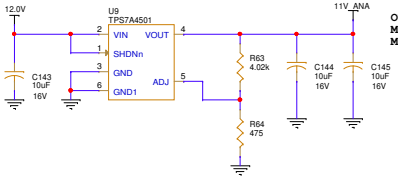



**Note : Set to 1.03V**

## 5V to 0.9V Switch Converter




## ANALOG POWER SUPPLY




**OUTPUT : 11V**
**MAX : 0.79A / 8.69W @ Tamb = 85°C**
**MAX : 1.25A / 13.75W @ Tamb = 60°C**

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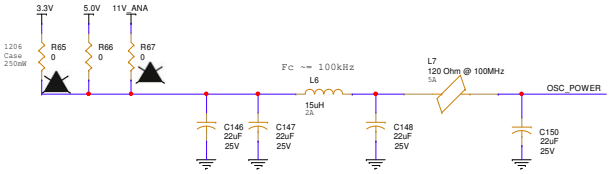
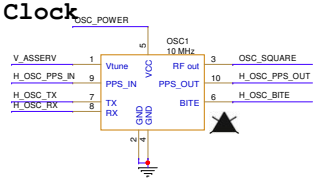
|---|---|---|
| Title: POWER SUPPLY | | |
| Size: A2 | Document Number: ART_CARD | Rev: 2 |
| Date: Tuesday, April 13, 2021 | | |
| FILE NAME: ART_CARD | Sheet: 4 of 7 | |

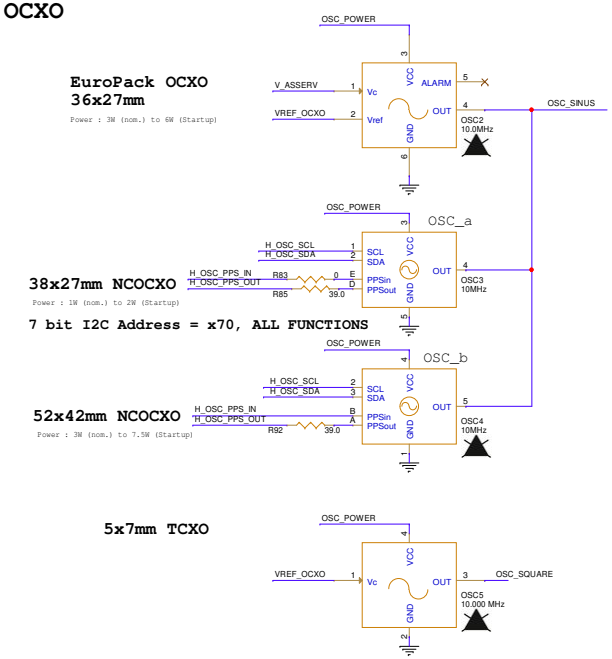
## OSCILLATOR POWER SUPPLY



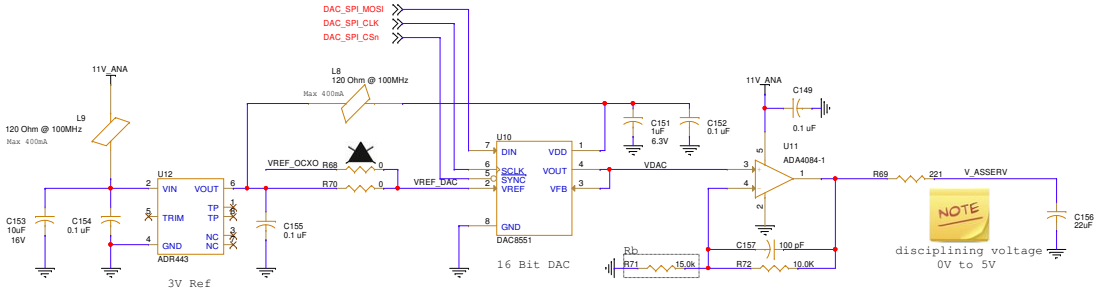

## MiniRubidium
## Miniature Atomic Clock



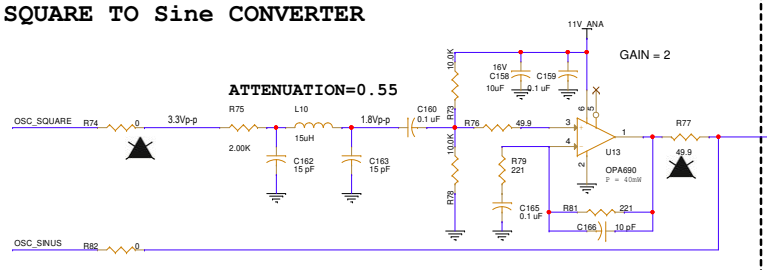

## OCXO



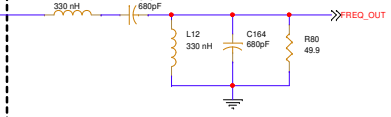

## OSCILLATOR CONTROL VOLTAGE



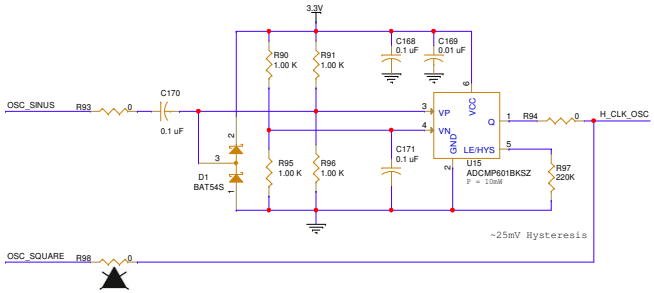

## SQUARE TO Sine CONVERTER



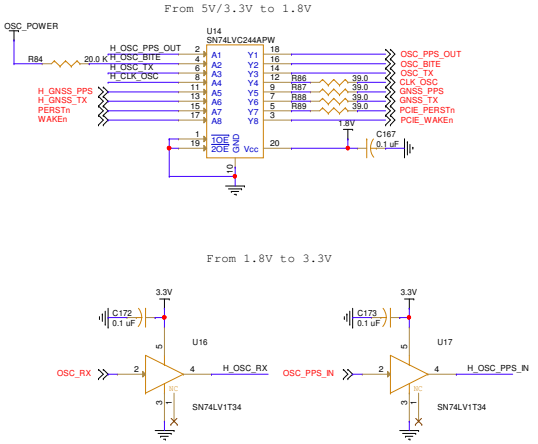

## HARMONIC FILTER



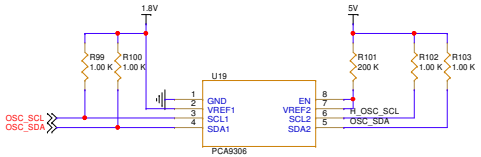

## SINUS TO SQUARE CONVERTER



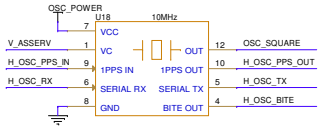

## LOGIC VOLTAGE-LEVEL TRANSLATOR




## I2C VOLTAGE-LEVEL TRANSLATOR




## Chip Scale Atomic Clock

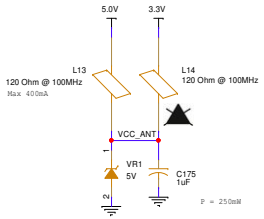



<variant_name>

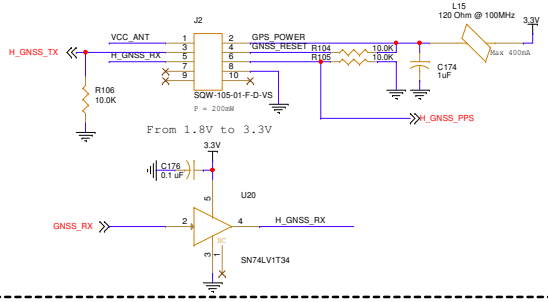
orolia

| | | |
|---|---|---|
| Title: TIMING | | |
| Size: A2 | Document Number: ART_CARD | Rev: 2 |
| Date: Tuesday, April 13, 2021 | | |
| FILE NAME: ART_CARD | Sheet: 5 of 7 | |

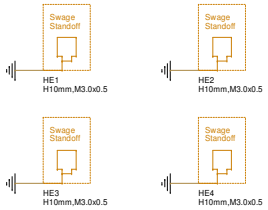
## ANTENNA POWER SUPPLY




## GNSS RECEIVER




## GNSS STANDOFF




<Variant Name>

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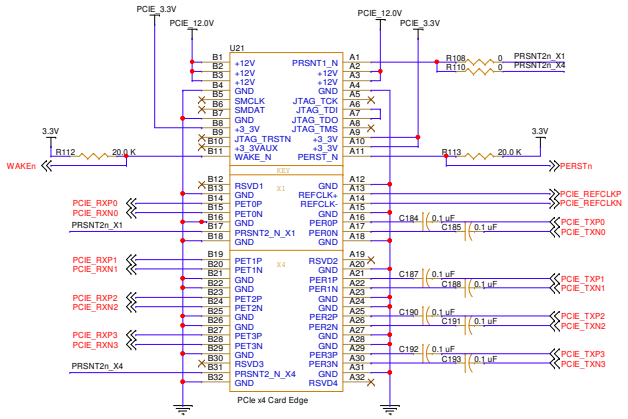
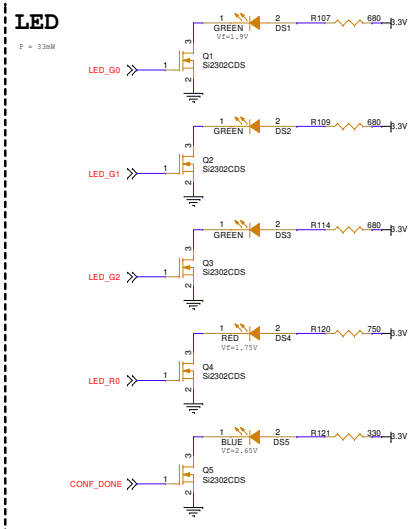
| | | |
|---|---|---|
| Title: GNSS | | |
| Size: A2 | Document Number: ART_CARD | Rev: 2 |
| Date: Tuesday, April 13, 2021 | | |
| FILE NAME: ART_CARD | Sheet: 6 of 7 | |

## PCIe CONNECTOR

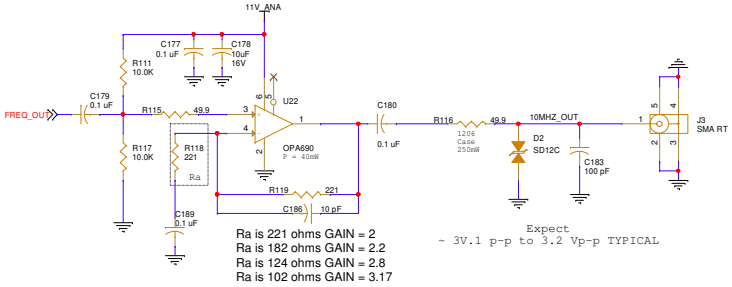



## LED

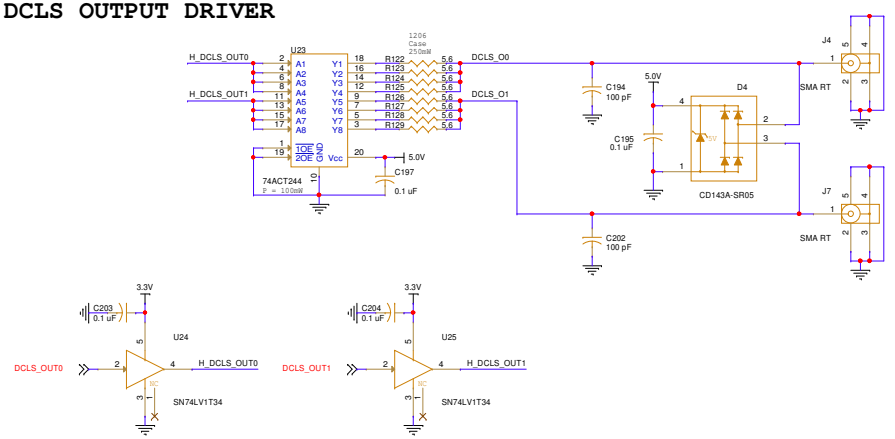



## FREQ OUTPUT DRIVER

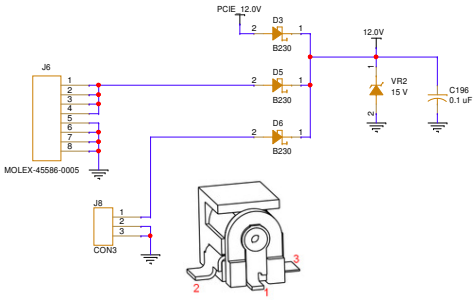
### 10MHZ OSC Buffer Driver



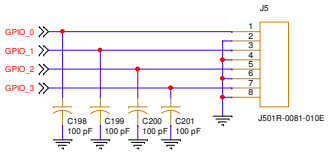

## DCLS OUTPUT DRIVER




## POWER CONNECTOR



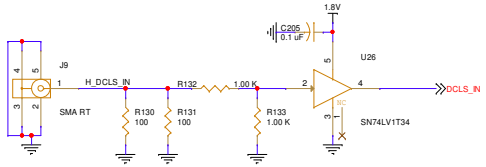

## GPIO



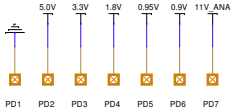

## BRACKET HOLES / MOUNT HOLES


## DCLS INPUT DRIVER

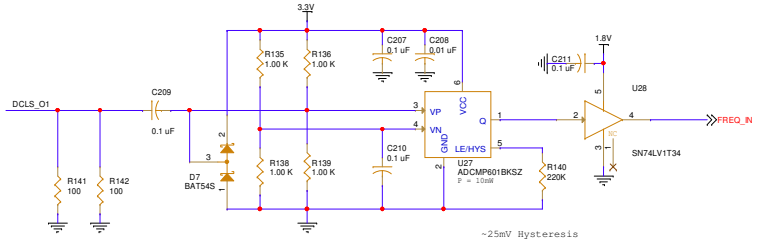
From 5V input to 1.8V




## TEST POINT




## OPTIONNAL FREQUENCY INPUT




<Variant Name>

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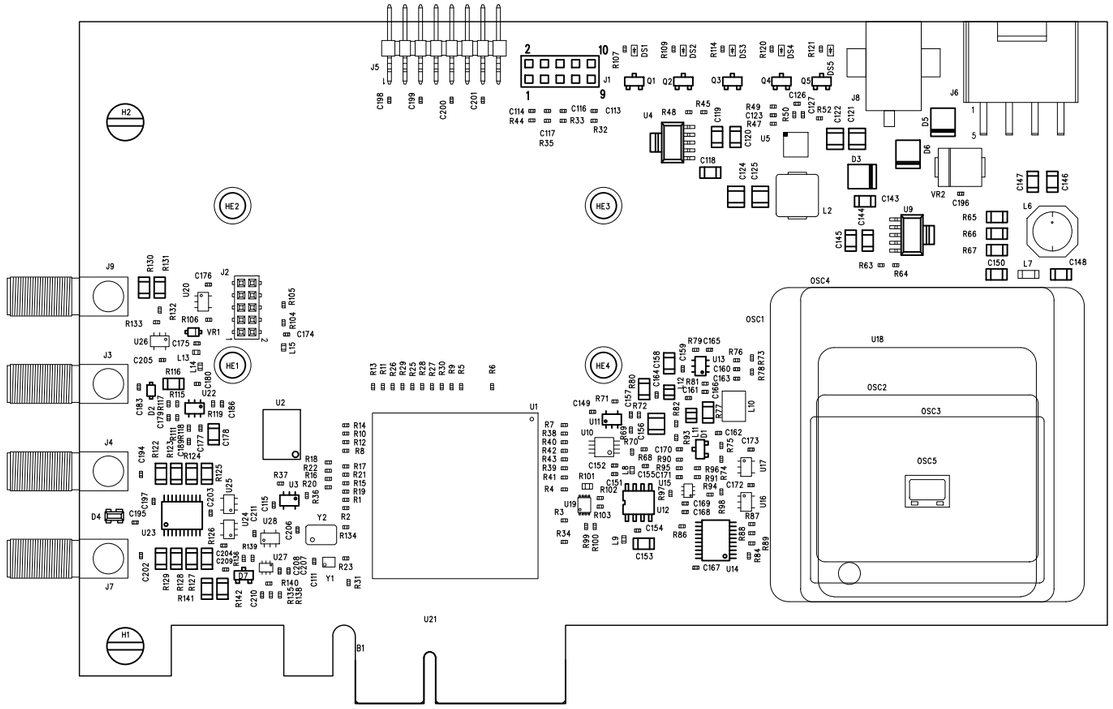
| | | |
|---|---|---|
| Title: CONNECTORS | | |
| Size: A2 | Document Number: ART_CARD | Rev: 2 |
| Date: Tuesday, April 13, 2021 | | |
| FILE NAME: ART_CARD | Sheet: 7 of 7 | |

| Rev | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| 1 | | | |




| | | | |
|---|---|---|---|
| UNLESS OTHERWISE SPECIFIED: | | NAME | DATE |
| | DRAWN | H ECHELARD | 03/02/2021 |
| MATERIAL: PCB | | | |
| FINISH | | | |



CHANGE RESTRICTED
NO MANUAL CHANGES

THIRD ANGLE PROJECTION

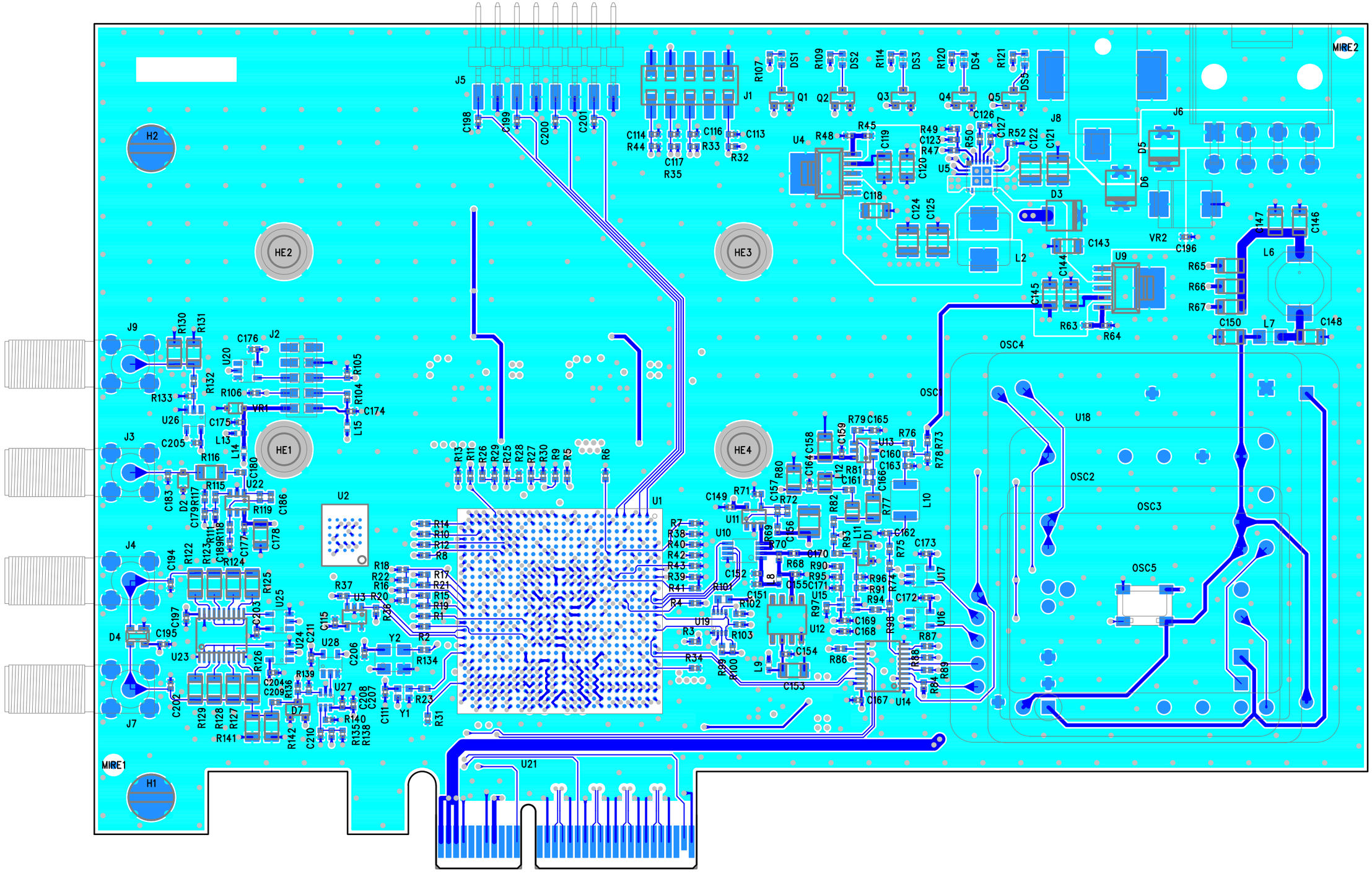
OROLIA FRANCE

PART NUMBER: ART_CARD_PCB

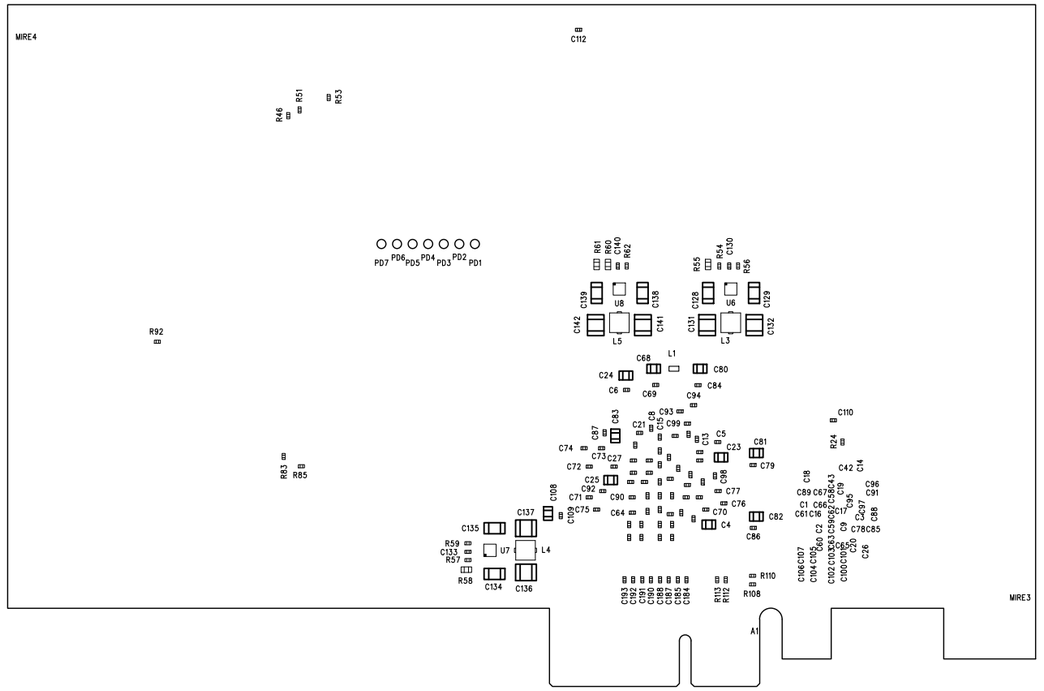
TITLE: ART_CARD

| SIZE | DWG. NO. | REV |
|---|---|---|
| A3 | ART_CARD_PCB | 2 |

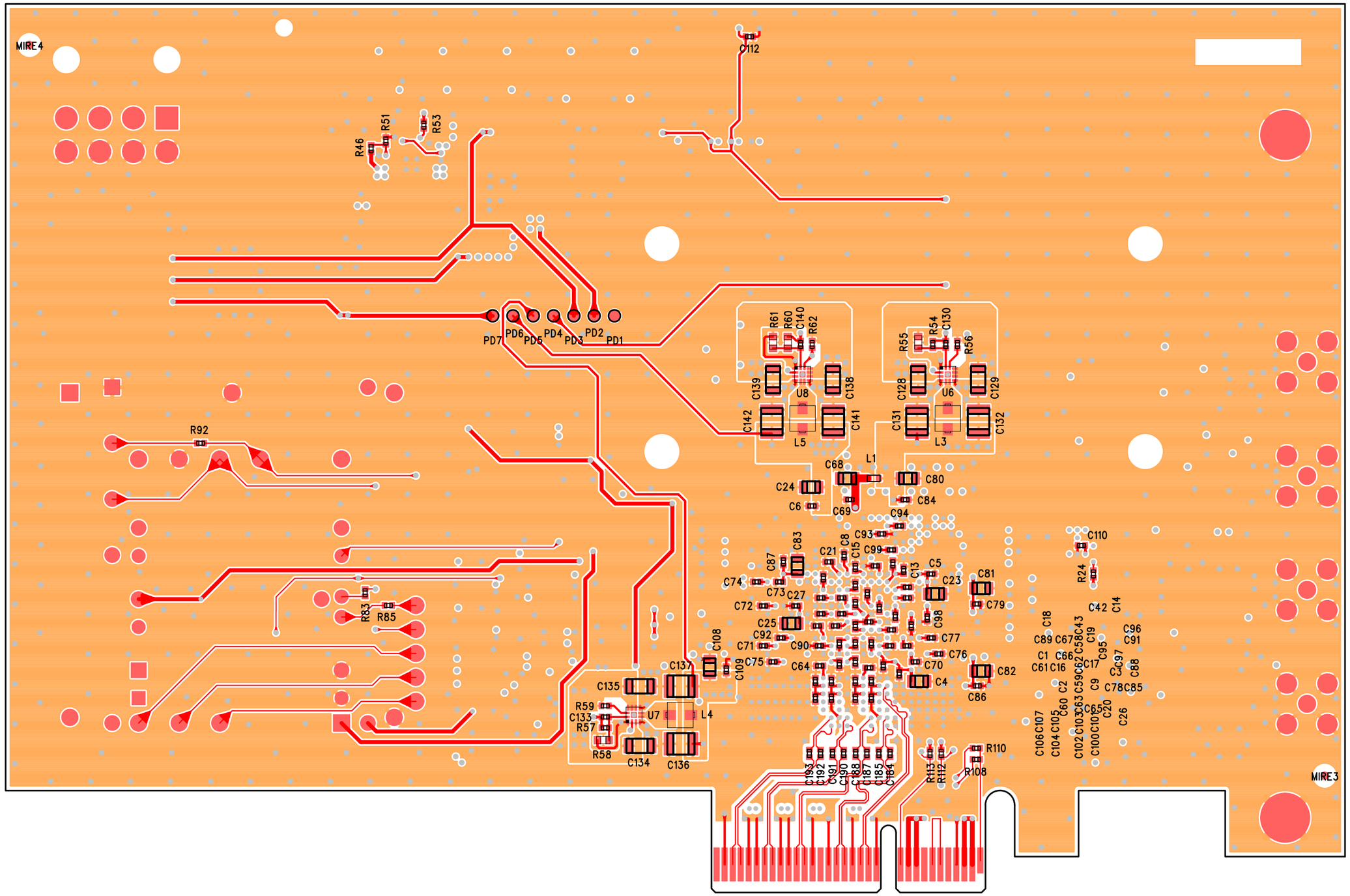
SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1

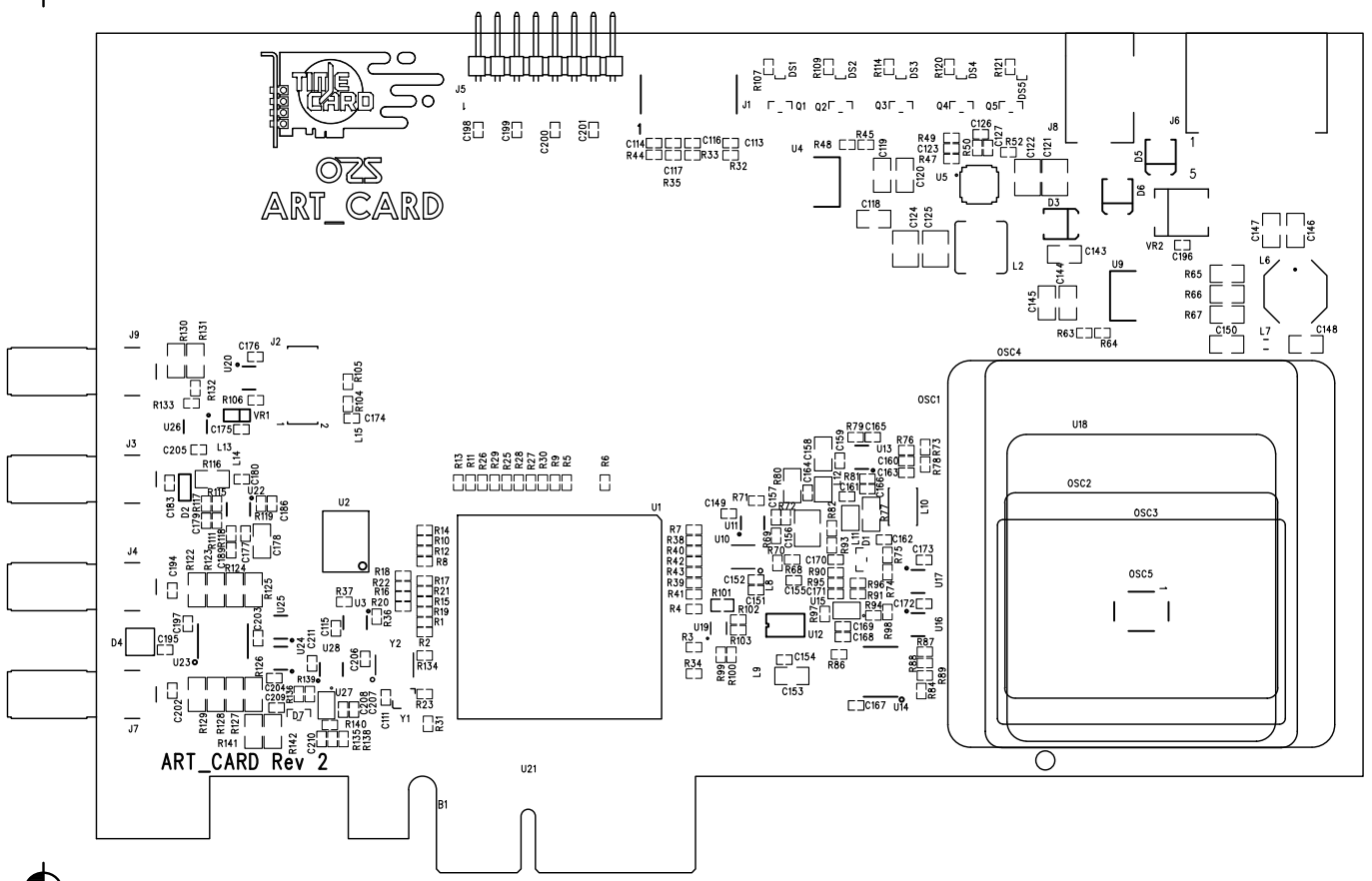

MIRE2
H2
HE2
HE3
HE1
HE4
MIRE1
H1
J5
J1
J9
J2
J3
J4
J7
J8
J6
U1
U2
U3
U4
U5
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
VR1
VR2
Y1
Y2
L2
L6
L7
L9
L10
L11
L12
L13
L14
L15
D1
D2
D3
D4
D5
D6
D7
DS1
DS2
DS3
DS4
DS5
Q1
Q2
Q3
Q4
Q5
OSC1
OSC2
OSC3
OSC4
OSC5

| Rev | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| 1 | | | |

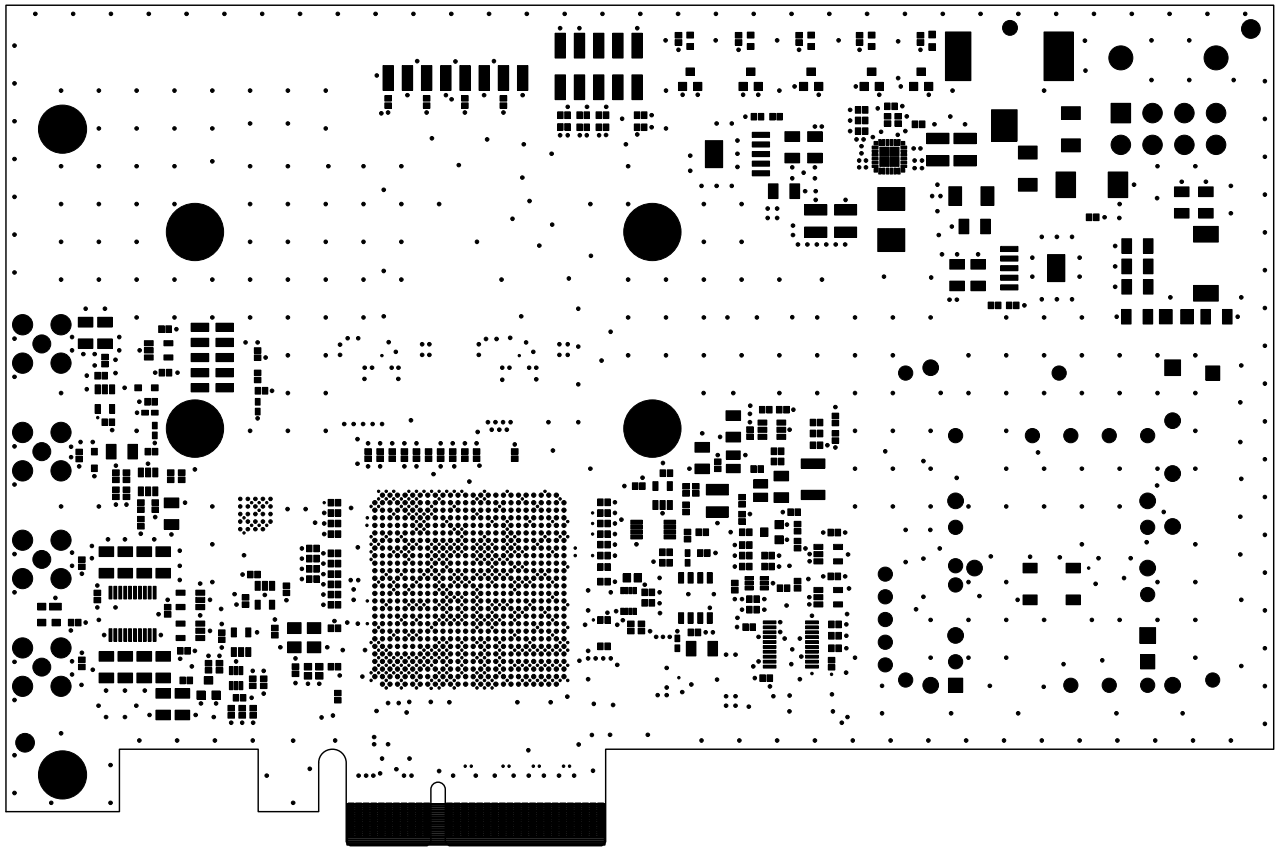



| UNLESS OTHERWISE SPECIFIED: | | NAME | DATE | OROLIA FRANCE |
|---|---|---|---|---|
| | DRAWN | H ECHELARD | 03/02/2021 | PART NUMBER: ART_CARD_PCB |
| | THE INFORMATION CONTAINED IN THIS DOCUMENT IS THE SOLE PROPERTY OF OROLIA. ANY REPRODUCTION, DISCLOSURE OR MANUFATURE OF THIS INFORMATION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF OROLIA GROUP IS PROHIBITED. | | | TITLE: ART_CARD |
| MATERIAL: PCB | CHANGE RESTRICTED NO MANUAL CHANGES | | | SIZE: A3 / DWG. NO.: ART_CARD_PCB / REV: 2 |
| FINISH | THIRD ANGLE PROJECTION | | | SCALE: 1:1 / DO NOT SCALE / SHEET 1 OF 1 |

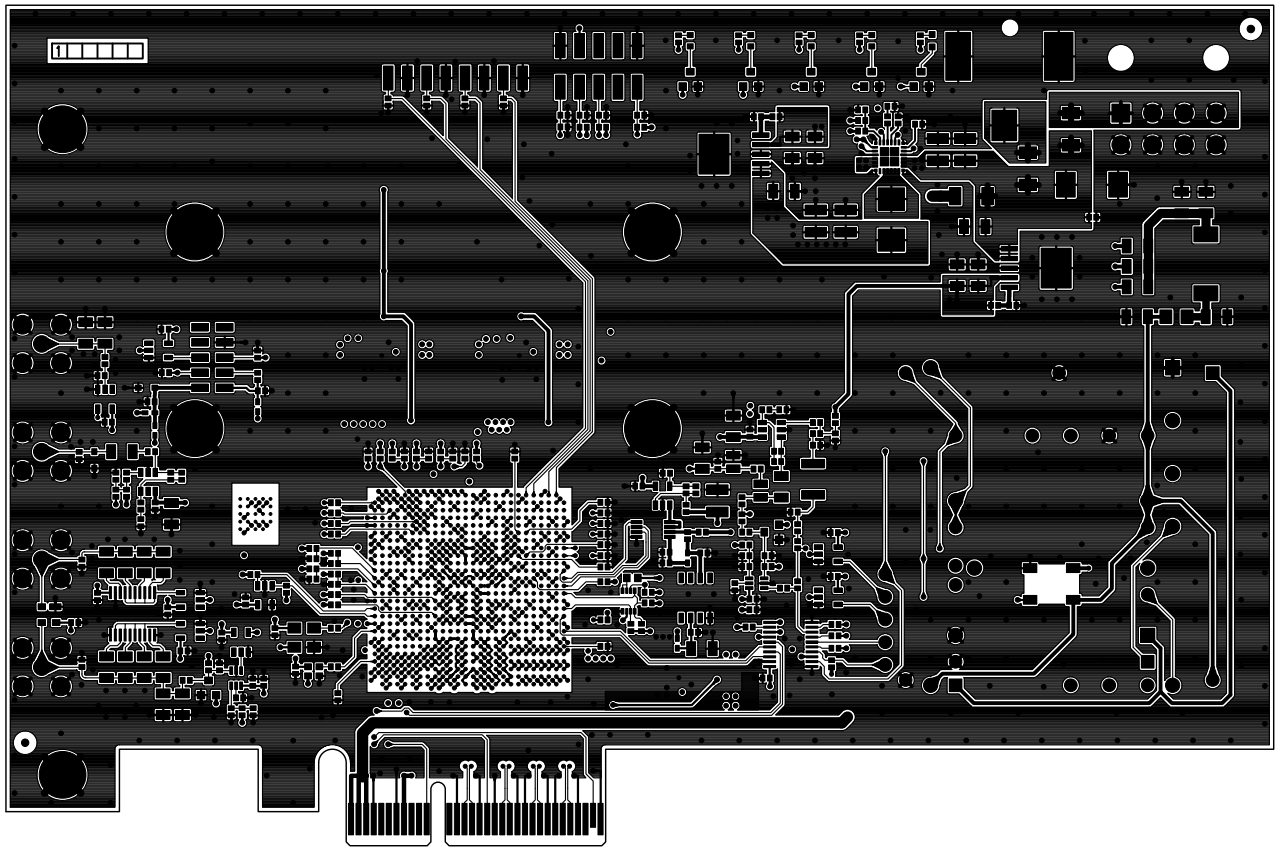

MIRE4
C112
R46
R51
R53
PD7
PD6
PD5
PD4
PD3
PD2
PD1
R61
R60
C140
R62
C139
U8
C138
C142
C141
L5
R55
R54
C130
R56
C128
U6
C129
C131
C132
L3
R92
C68
L1
C80
C24
C84
C6
C69
C94
C93
C99
C21
C15
C8
C83
C87
C74
C73
C27
C72
C25
C92
C71
C90
C75
C64
C108
C109
C137
C135
R59
C133
R57
U7
L4
R58
C134
C136
R83
R85
C5
C13
C23
C81
C79
C98
C77
C76
C70
C4
C82
C86
C110
R24
C42
C14
C18
C89
C67
C58
C43
C19
C96
C91
C1
C66
C61
C16
C62
C17
C95
C97
C88
C59
C9
C78
C85
C2
C60
C63
C65
C20
C26
C107
C106
C105
C104
C103
C102
C101
C100
R110
R108
R113
R112
C193
C192
C191
C190
C188
C187
C185
C184
MIRE3



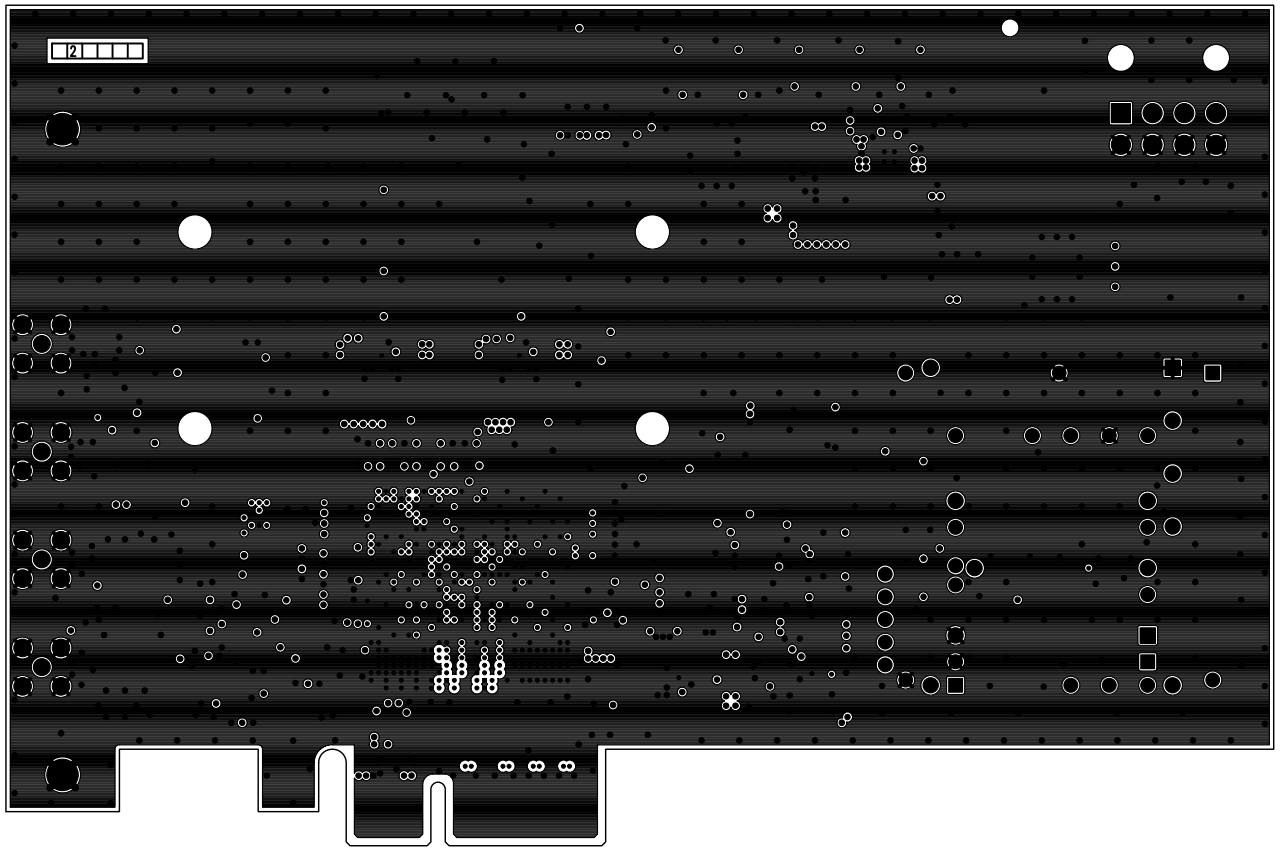

| SILKSCREEN TOP | ARTEMIS |
|---|---|
| FILE: ART_CARD REV 2 | 26/04/21 |



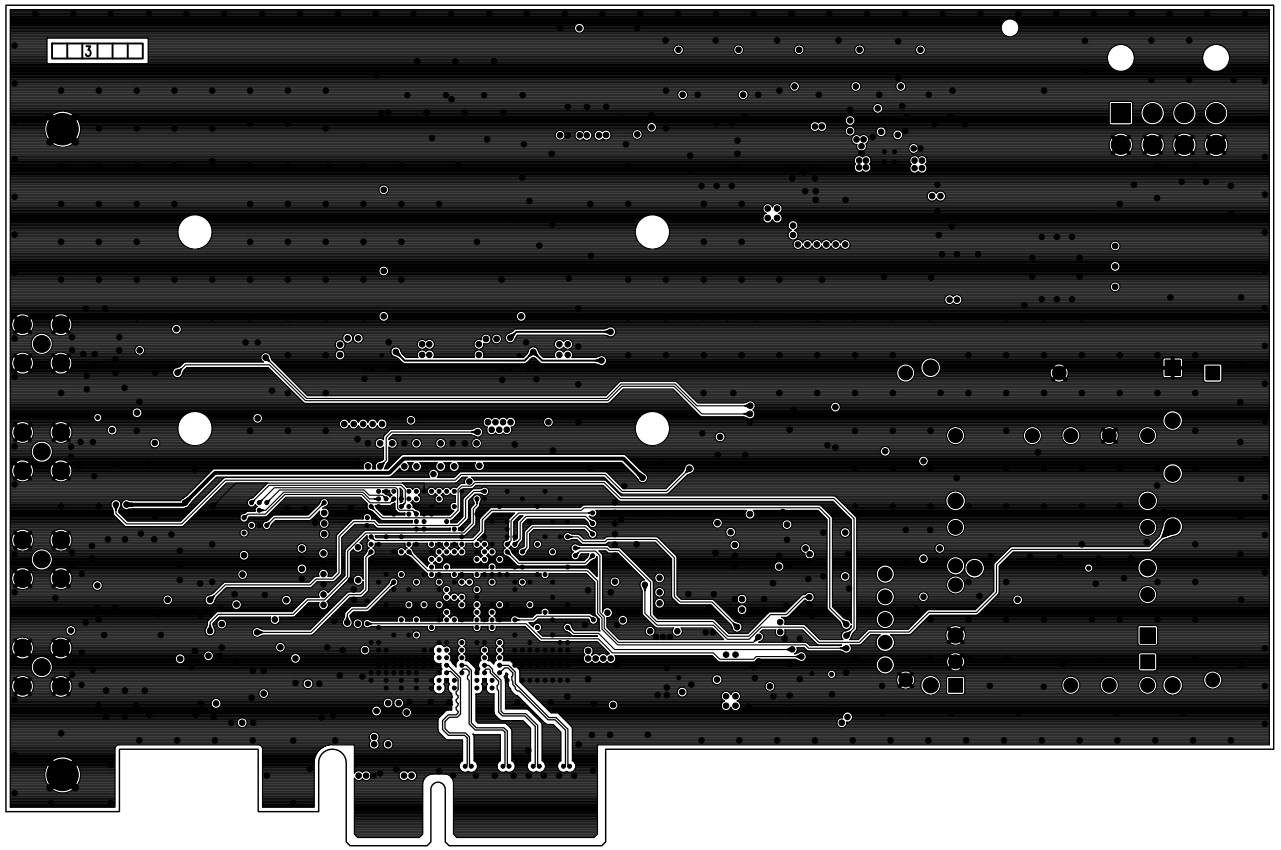
| SOLDER MASK TOP | ARTEMIS |
| --- | --- |
| FILE: ART_CARD REV 2 | 26/04/21 |



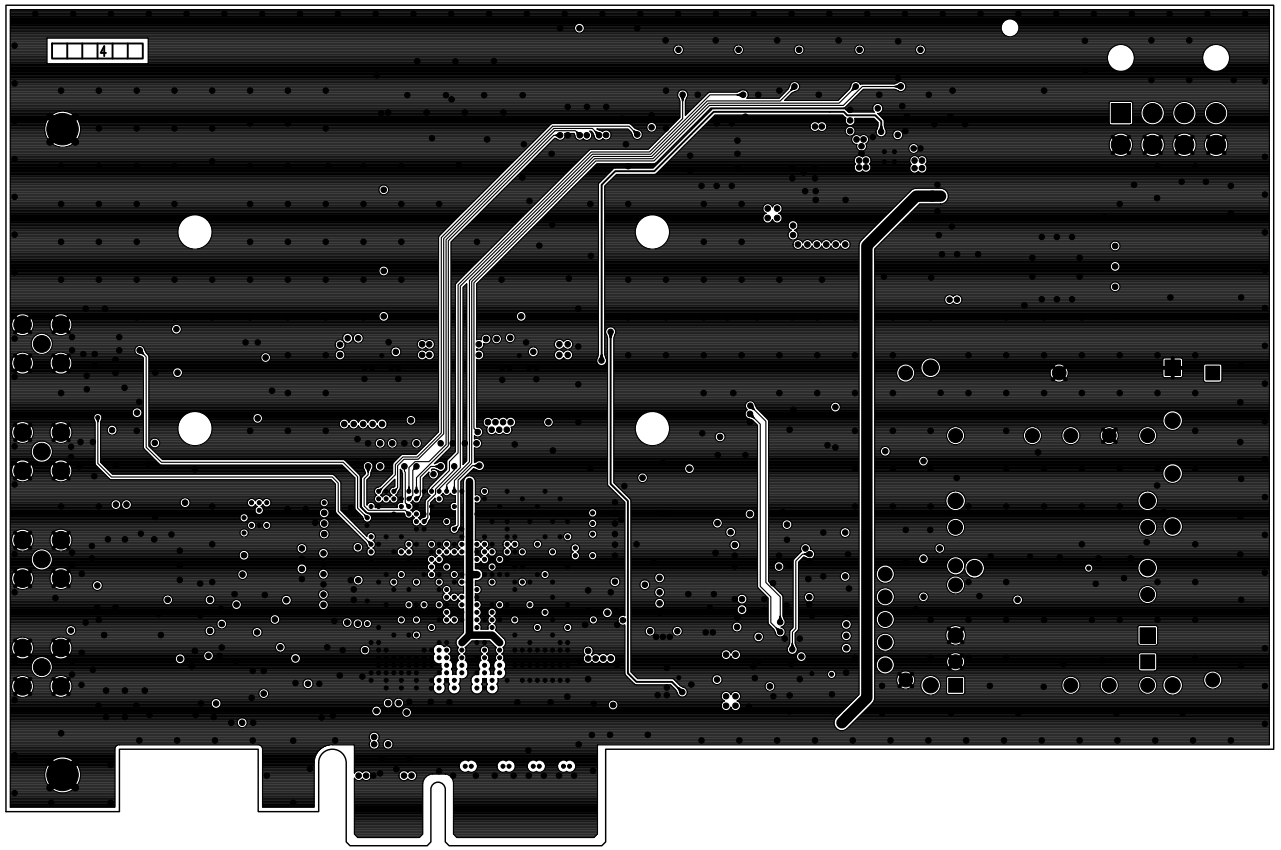
| TOP LAYER | ARTEMIS |
|---|---|
| FILE: ART_CARD REV 2 | 26/04/21 |



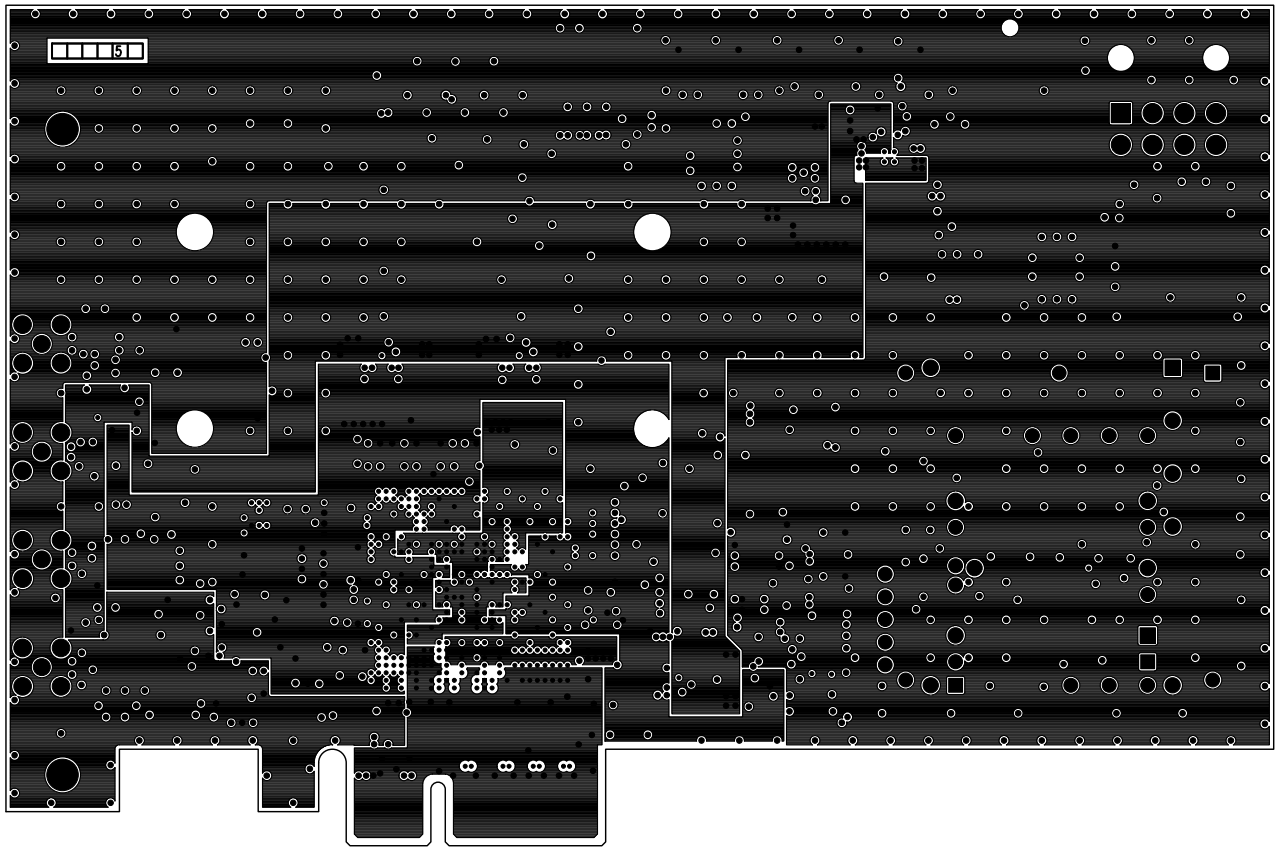

| | |
|---|---|
| INTERNAL 1 LAYER | ARTEMIS |
| FILE: ART_CARD REV 2 | 26/04/21 |



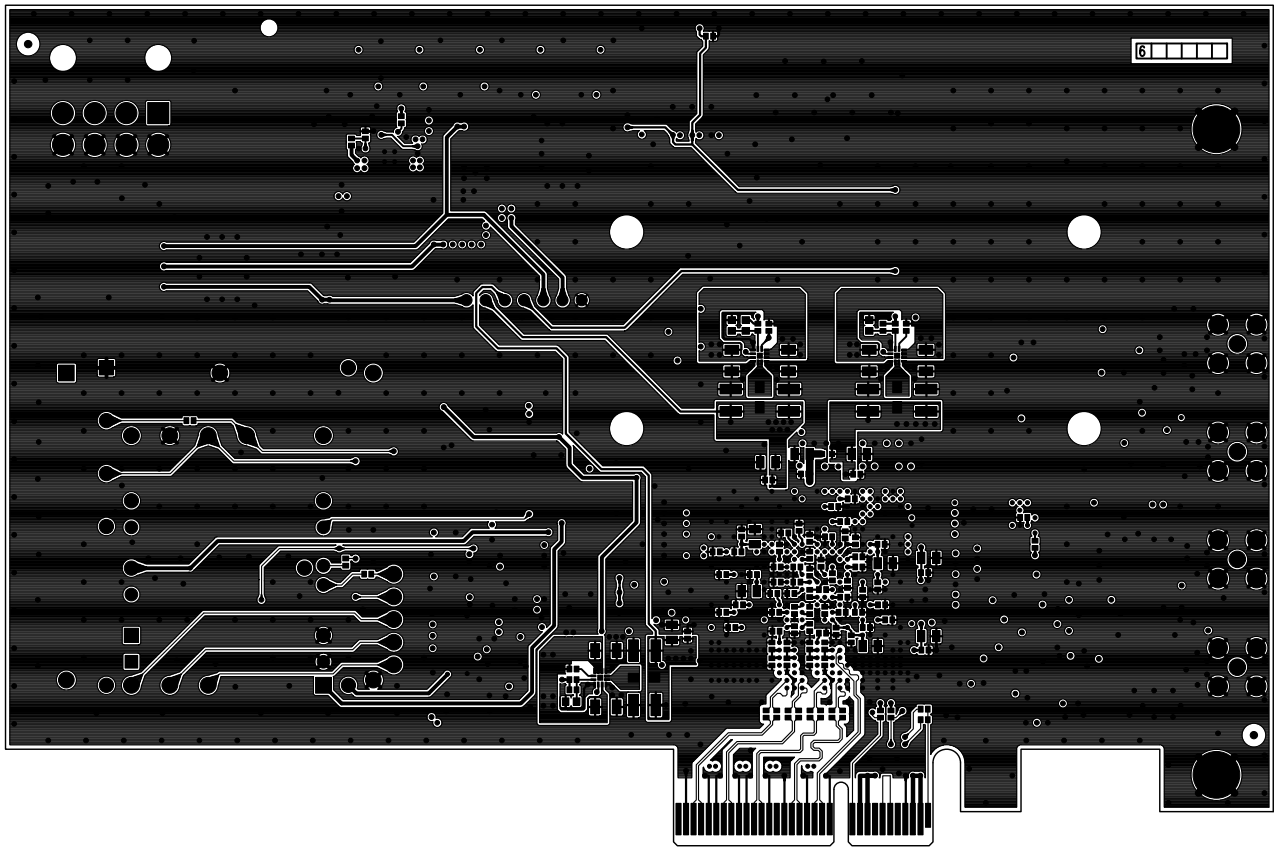

| | |
|---|---|
| INTERNAL 2 LAYER | ARTEMIS |
| FILE: ART_CARD REV 2 | 26/04/21 |



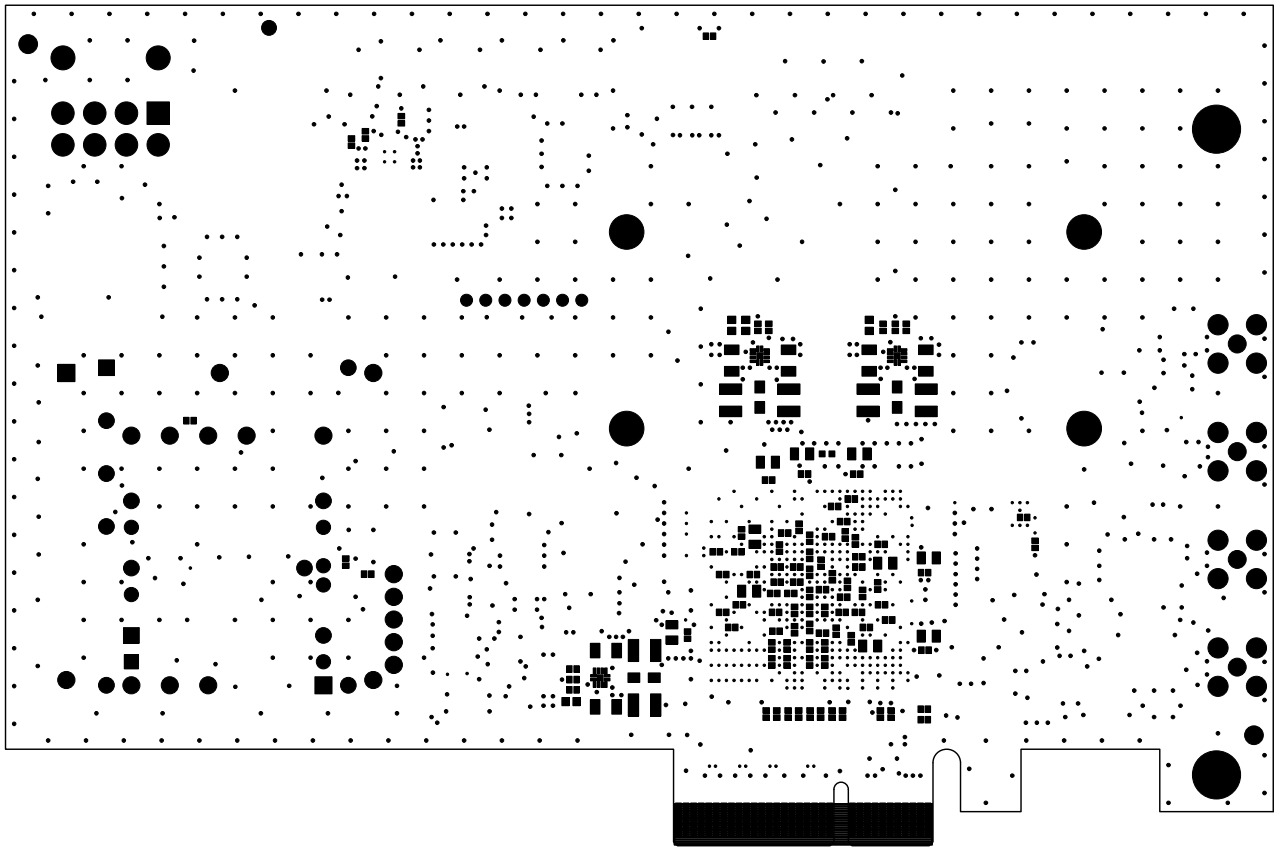

| INTERNAL 3 LAYER | ARTEMIS |
|---|---|
| FILE: ART_CARD REV 2 | 26/04/21 |



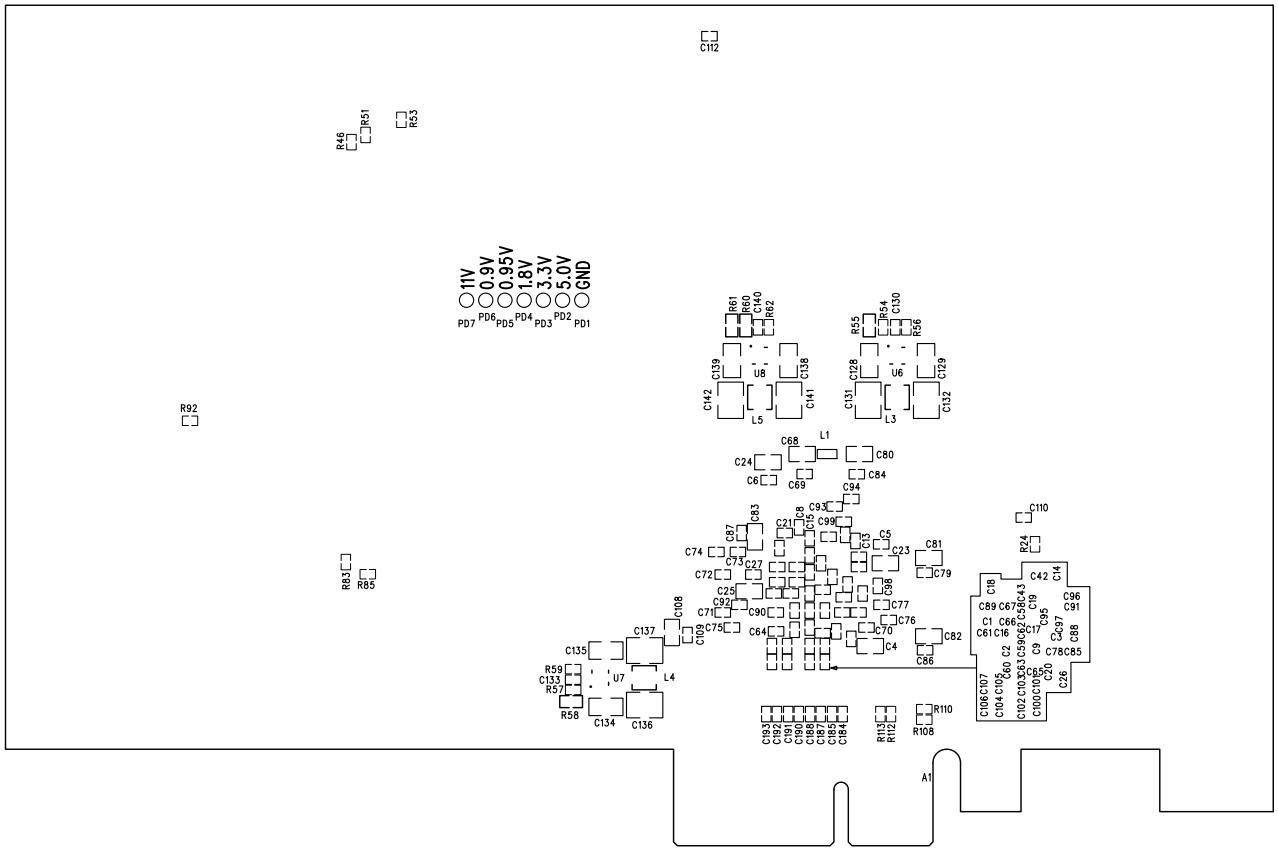

| | |
|---|---|
| FILM: COUCHE INTERNE 4 | ARTEMIS |
| FILE: ART_CARD REV 2 | 26/04/21 |



| BOTTOM LAYER | ARTEMIS |
| --- | --- |
| FILE: ART_CARD REV 2 | 26/04/21 |



| SOLDER MASK BOTTOM | ARTEMIS |
| --- | --- |
| FILE: ART_CARD REV 2 | 26/04/21 |




| SILKSCREEN BOTTOM | ARTEMIS |
|---|---|
| FILE: ART_CARD REV 2 | 26/04/21 |

| Rev | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| 1 | | | |

NOTES:

1. FABRICATE BOARD PER:
Latest revision of IPC-A-600 Class 2. Electrical integrity testing required, per section 5.2 of IPC-A-600.

2. MATERIAL : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
Rigid laminate and prepeg shall be per IPC-4101/99/101/126. As described in the StackUp.
Laminate must meet latest RoHS directive subject to Orolia Engineering Approval.

3. FINISH : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
ENIG (Electroless Nickel, Immersion Gold) per IPC-4552

4. SOLDER MASK : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
LPI per IPC-SM-840 (current rev) COLOR : GREEN
Soldermask provided as 1 to 1 and shall be oversized at the fabricator as required in order to insure that soldermask does not encroach upon thru hole and SMT pads.
0.008 DIA Vias shall be plugged/tented from top and bottom side per artwork supplied unless mask is removed by artwork. These vias are required to be filled and copper capped. It is acceptable to use and epoxy fill after initial plating, followed by a copper cap process to cap the via fill.
Continuous copper plate is required.

5. SILKCREEN : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
White (All silkscreen to be removed from any exposed plated areas)

6. DIMENSIONING AND TOLERANCING PER ANSI-Y-14.5 (LATEST REV).

7. 94V-0 Min is required and shall be marked on top or bottom side silkscreen or copper

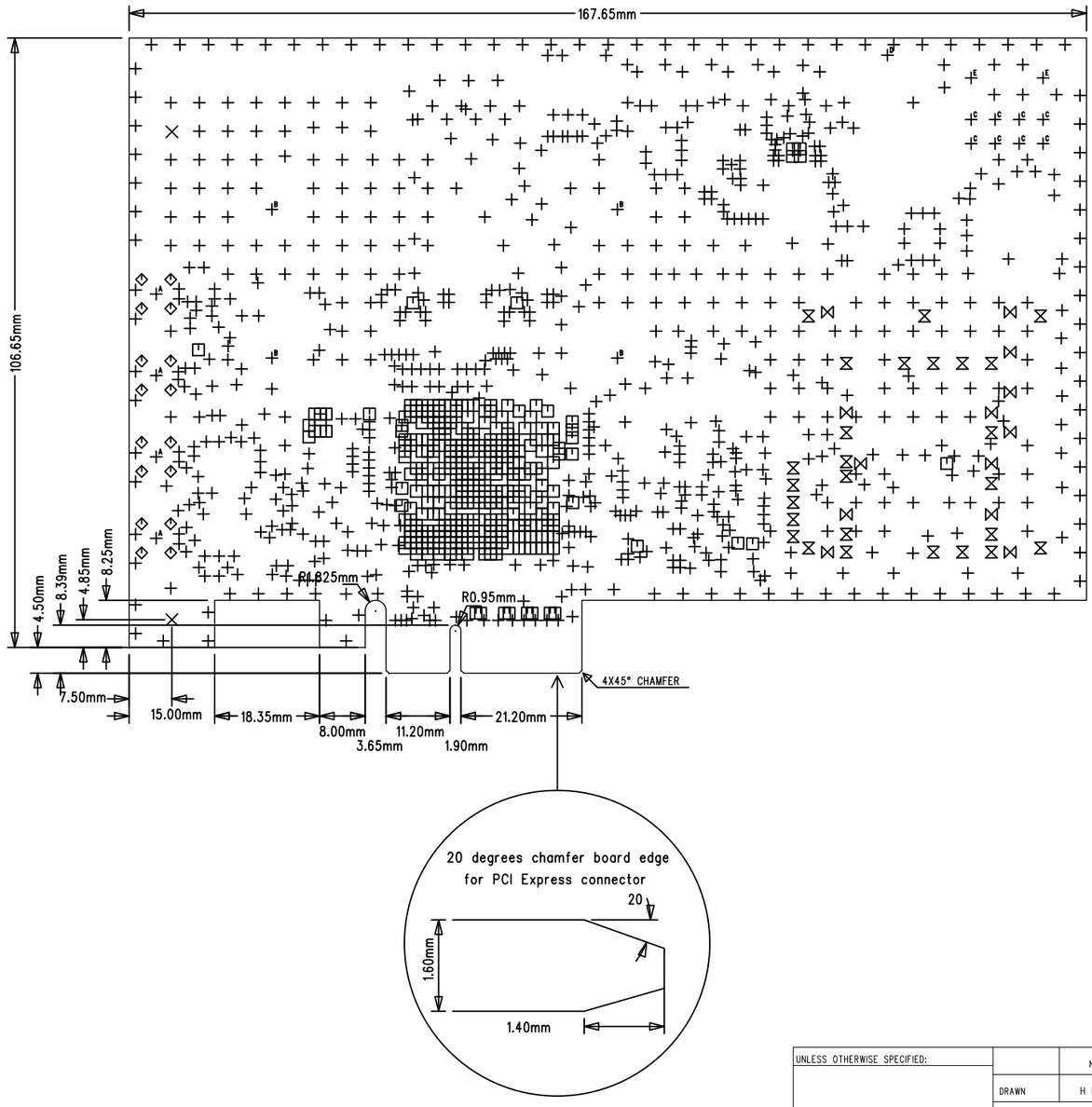
8. All copper on any layer shall be trimmed back 0.015 from the board edge as required.

9. All internal unused pads shall be removed

10. Teardrops shall be added where possible

11. All holes sizes shown are expected finished hole sizes after processing.

12. This board shall be supplied in array format that shall be determined/approved by the purshaser of the bare board




| SIZE | QTY | SYM | PLATED | TOL |
|---|---|---|---|---|
| 0.25 | 333 | □ | YES | +/-0.1 |
| 0.4 | 886 | + | YES | +/-0.1 |
| 1.1 | 26 | ⊠ | YES | +/-0.1 |
| 1.3 | 13 | ⋈ | YES | +/-0.1 |
| 1.6 | 4 | +A | YES | +/-0.1 |
| 1.7 | 16 | ◇ | YES | +/-0.1 |
| 1.8 | 8 | +C | YES | +/-0.1 |
| 3.5 | 2 | × | YES | +/-0.1 |
| 1.8 | 1 | +D | NO | +/-0.1 |
| 3 | 2 | +E | NO | +/-0.1 |
| 4.4 | 4 | +B | NO | +/-0.1 |

UNLESS OTHERWISE SPECIFIED:

MATERIAL
PCB

FINISH

| | NAME | DATE |
|---|---|---|
| DRAWN | H ECHELARD | 03/02/2021 |



CHANGE RESTRICTED
NO MANUAL CHANGES

THIRD ANGLE PROJECTION

OROLIA FRANCE

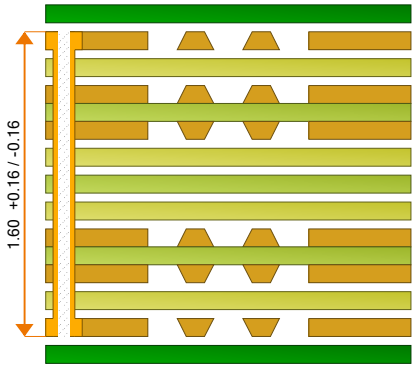
PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

SIZE A3 | DWG. NO. ART_CARD_PCB | REV 2

SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1

| Layer | Stack up | Supplier | Description | Supplier Description | Type | Base Thickness | Finish Thickness | Mask Thickness | εr | Loss Tangent | Resin Content | Impedance ID |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Solder resist | LPI | Solder resist | | | 0.020 | 4.100 | 0.0000 | | |
| 1 | | | Foil | 17um Copper Foil | Foil | 0.018 | 0.040 | | | | | 1, 2 |
| | | VENTEC | VT47-2113 | VT-47 | PREPREG | 0.106 | 0.095 | | 4.060 | 0.0000 | 57.000 | |
| 2 | | | | | | 0.017 | 0.017 | | | | | |
| | | VENTEC | VT-47 | 0.127mm | Core | 0.127 | 0.127 | | 4.350 | 0.0000 | 0.000 | |
| 3 | | | | | | 0.017 | 0.017 | | | | | 3, 4 |
| | | VENTEC | VT47-2116 | VT-47 | PREPREG | 0.132 | 0.121 | | 4.150 | 0.0000 | 54.000 | |
| | | VENTEC | VT-47 | 0.711mm | Core | 0.711 | 0.711 | | 4.400 | 0.0000 | 0.000 | |
| | | VENTEC | VT47-2116 | VT-47 | PREPREG | 0.132 | 0.121 | | 4.150 | 0.0000 | 54.000 | |
| 4 | | | | | | 0.017 | 0.017 | | | | | 5, 6 |
| | | VENTEC | VT-47 | 0.127mm | Core | 0.127 | 0.127 | | 4.350 | 0.0000 | 0.000 | |
| 5 | | | | | | 0.017 | 0.017 | | | | | |
| | | VENTEC | VT47-2113 | VT-47 | PREPREG | 0.106 | 0.095 | | 4.060 | 0.0000 | 57.000 | |
| 6 | | | Foil | 17um Copper Foil | Foil | 0.018 | 0.040 | | | | | 7, 8 |
| | | | Solder resist | LPI | Solder resist | | | 0.020 | 4.100 | 0.0000 | | |




Copper Thickness = 0.148 | Dielectric Thickness = 1.399 | Solder Mask Thickness = 0.040 | Stack Up Thickness = 1.546 | Stack Up Thickness with Soldermask = 1.586

| Impedance ID | Structure Image | Structure Name | Impedance Signal Layer | Ref. Plane 2 in Layer | Ref. Plane 1 in Layer | Lower Trace Width (W1) | Trace Separation (S1) | Ground Strip Separation (D1) | Broadside 2nd Layer | Calculated Impedance | Target Impedance | Tol (+/- %) | Coating Between Traces (C3) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | Coated Microstrip 1B | 1 | 0 | 2 | 0.150 | 0.000 | 0.000 | 0 | 50.090 | 50.000 | 10.000 | 0.000 |
| 2 | | Edge Coupled Coated Microstrip 1B | 1 | 0 | 2 | 0.150 | 0.150 | 0.000 | 0 | 87.470 | 85.000 | 10.000 | 0.020 |
| 3 | | Offset Stripline 1B1A | 3 | 5 | 2 | 0.160 | 0.000 | 0.000 | 0 | 50.950 | 50.000 | 10.000 | 0.000 |
| 4 | | Edge Coupled Offset Stripline 1B1A | 3 | 5 | 2 | 0.160 | 0.150 | 0.000 | 0 | 85.010 | 85.000 | 10.000 | 0.000 |
| 5 | | Offset Stripline 1B1A | 4 | 5 | 2 | 0.160 | 0.000 | 0.000 | 0 | 50.950 | 50.000 | 10.000 | 0.000 |
| 6 | | Edge Coupled Offset Stripline 1B1A | 4 | 5 | 2 | 0.160 | 0.150 | 0.000 | 0 | 85.010 | 85.000 | 10.000 | 0.000 |
| 7 | | Coated Microstrip 1B | 6 | 0 | 5 | 0.150 | 0.000 | 0.000 | 0 | 50.090 | 50.000 | 10.000 | 0.000 |

| StackName: Ouestronic_PCI Express_246183-Q_6L_VT47 | Version: | Revision: | Modification: | Date of Revision: | Editor | Page 1/2 |
|---|---|---|---|---|---|---|
| Date: 28/01/2021 | Associated Documents: | | | | | |
| Author: Mostefa Abdali | | | | | | |
| Department: IDS | | | | | | |
| Site: Tewkesbury | | | | | | |

| Impedance ID | Structure Image | Structure Name | Impedance Signal Layer | Ref. Plane 2 in Layer | Ref. Plane 1 in Layer | Lower Trace Width (W1) | Trace Separation (S1) | Ground Strip Separation (D1) | Broadside 2nd Layer | Calculated Impedance | Target Impedance | Tol (+/- %) | Coating Between Traces (C3) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 |  | Edge Coupled Coated Microstrip 1B | 6 | 0 | 5 | 0.150 | 0.150 | 0.000 | 0 | 87.470 | 85.000 | 10.000 | 0.020 |

| Column Position | Drill Image | 1st Layer | 2nd Layer | Drill Type | Minimum Size | Fill Type | Data Filenames | Minimum Pad Size |
|---|---|---|---|---|---|---|---|---|
| 1 |  | 1 | 6 | Mechanical PTH | 0.250 | None | | 0.500 |

Notes

| StackName: Ouestronic_PCI Express_246183-Q_6L_VT47 | Version: | Revision: | Modification: | Date of Revision: | Editor | Page 2/2 | |
|---|---|---|---|---|---|---|---|
| Date: 28/01/2021 | Associated Documents: | | | | | | |
| Author: Mostefa Abdali | | | | | | | |
| Department: IDS | | | | | | | |
| Site: Tewkesbury | | | | | | | |

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p.benoit@artemis-cad.com
www.artemis-cad.com

# *TECHNICAL SPECIFICATION*

IPC-A-600

CUSTUMER : OROLIA
MANUFACTURER :

| | | | |
|---|---|---|---|
| **PCB Reference :** | ART_CARD | **Index :** | Rev 2 |

| | | | | | | |
|---|---|---|---|---|---|---|
| ☑ **PCB Unit** | **Unit PCB dimensions :** | 167.65 | X | 106.65 | mm | |
| ☐ **Panel PCB :** 0 | **Panel dimensions :** | 0 | X | 0 | mm | |
| **Material :** FR4 | **Surface :** 1.79 **dm²** | **Track / Gap :** | 0.15 | / | 0.15 | mm |

| | | | | | |
|---|---|---|---|---|---|
| PCB Type : | MC6 | Finish Copper Thikness (µm) : | 12µ | 17,5µ | 35µ | 40µm |
| PCB Thickness (mm) : | 16/10 | External Layer : | ☐ | ☐ | ☐ | ☑ |
| | | Intern Layer : | ☐ | ☑ | ☐ | ☐ |

| | | | | | | |
|---|---|---|---|---|---|---|
| **Technology** | ☑ Plated Trough Hole | **Via type :** | Hole / pads ratio : 0,25/0,55 | | | |
| ☑ Traditional | ☐ Press-fit Hole | ☑ Traditional Via | ☐ Via in pad | | | |
| ☑ SMT | ☐ Autre | ☐ Laser Via | ☐ Stacked | ☐ Staggered | | |
| **Surface Treatement Finished** | | ☐ Blinded Via | Couche départ et d'arrivée | | | |
| ☑ Ni/Au Chemical | ☐ Sn/Pb surfondu | ☐ Buried Via | Couche départ et d'arrivée | | | |
| ☐ Sn/Cu HAL | ☐ Autre | ☐ Filled Via | ☐ Resin | ☐ Copper | | |

| | | | | |
|---|---|---|---|---|
| **Peelable Solder Mask** | ☐ Standard | | ☐ TOP | ☐ BOTTOM |
| **Solder Mask** | ☑ Photo-imageable | Green | ☑ TOP | ☑ BOTTOM |
| **Silkscreen** | ☑ Ink | White | ☑ TOP | ☑ BOTTOM |
| **Electrical Test** | | | ☑ Yes | ☐ No |

| | | |
|---|---|---|
| ☑ **Impedance control :** | ☑ Produced | ☐ Measured |
| 50 ohms on layer 1, 3 and 4 | | |
| ☑ **Differential Pairs :** | ☑ Produced | ☐ Measured |
| 85 ohms on layer 1, 3 and 6 | | |

| | |
|---|---|
| ☑ **Stack-up :** | Ouestronic_PCI Express_246183-Q_6L_VT47.pdf |
| ☐ **Milling** | Milling Diameter : 0 mm |

**Comments :**