FILE OROLIA
ART_CARD

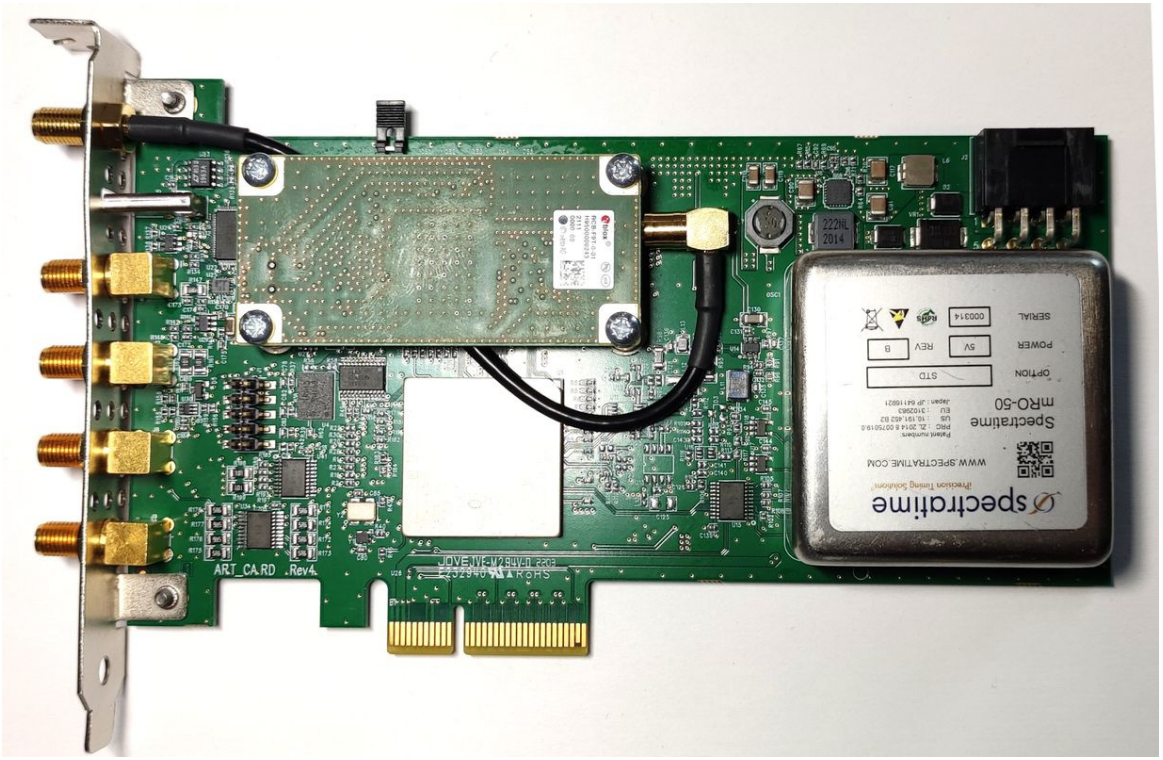
Réf PCB : **ART_CARD Rev 5**

⇨	7	SHEETS OF ELECTRICAL SCHEMATICS
⇨	1	ASSEMBLY DRAWING TOP
⇨	1	ASSEMBLY DRAWING BOTTOM
⇨	1	SILKSCREEN TOP
⇨	1	SOLDER MASK TOP
⇨	1	COPPER LAYER TOP
⇨	1	COPPER LAYER INNER 1
⇨	1	COPPER LAYER INNER 2
⇨	1	COPPER LAYER INNER 3
⇨	1	COPPER LAYER INNER 4
⇨	1	COPPER LAYER INNER 5
⇨	1	COPPER LAYER INNER 6
⇨	1	COPPER LAYER BOTTOM
⇨	1	SOLDER MASK BOTOM
⇨	1	SILKSCREEN BOTTOM
⇨	1	DRILL DRAWING
⇨	1	CIRCUIT BOARD SPECIFICATION

Artémis CAO ELECTRONIQUE

Angers Technopole
49070 BEAUCOUZÉ
Tél. : +33(0)2-41-48-41-40
contact@artemis-cad.com

1 bis Avenue du Bois l'Abbé
FRANCE
Fax : +33(0)2-41-48-41-44
www.artemis-cad.com



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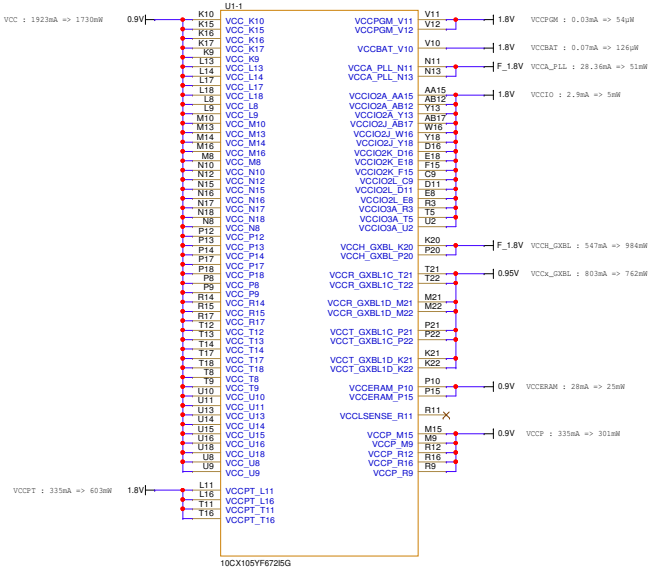
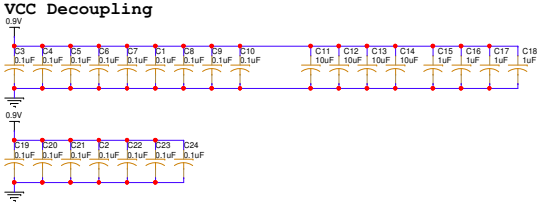
Title: OVERVIEW		
Size: A2	Document Number: ART_CARD	Rev: 5
Date: Thursday, March 03, 2022		
FILE NAME: ART_CARD	Sheet: 1 of 7	

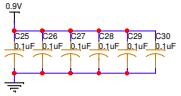
FPGA POWER SUPPLY



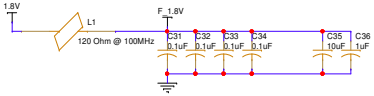
VCC Decoupling



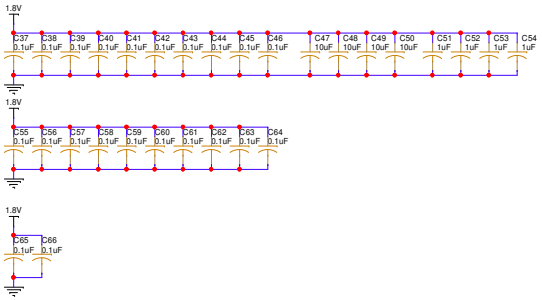
VCCP and VCCERAM Decoupling



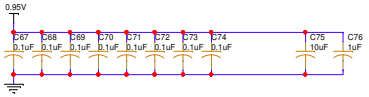
VCCA_PLL and VCCH_GXBL Decoupling

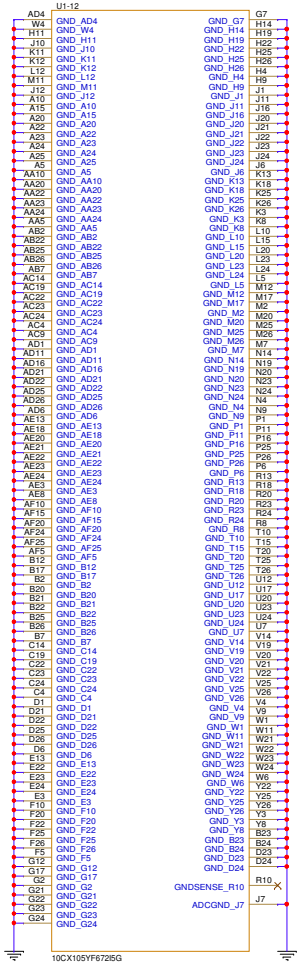


VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling



VCCR/VCCT Decoupling





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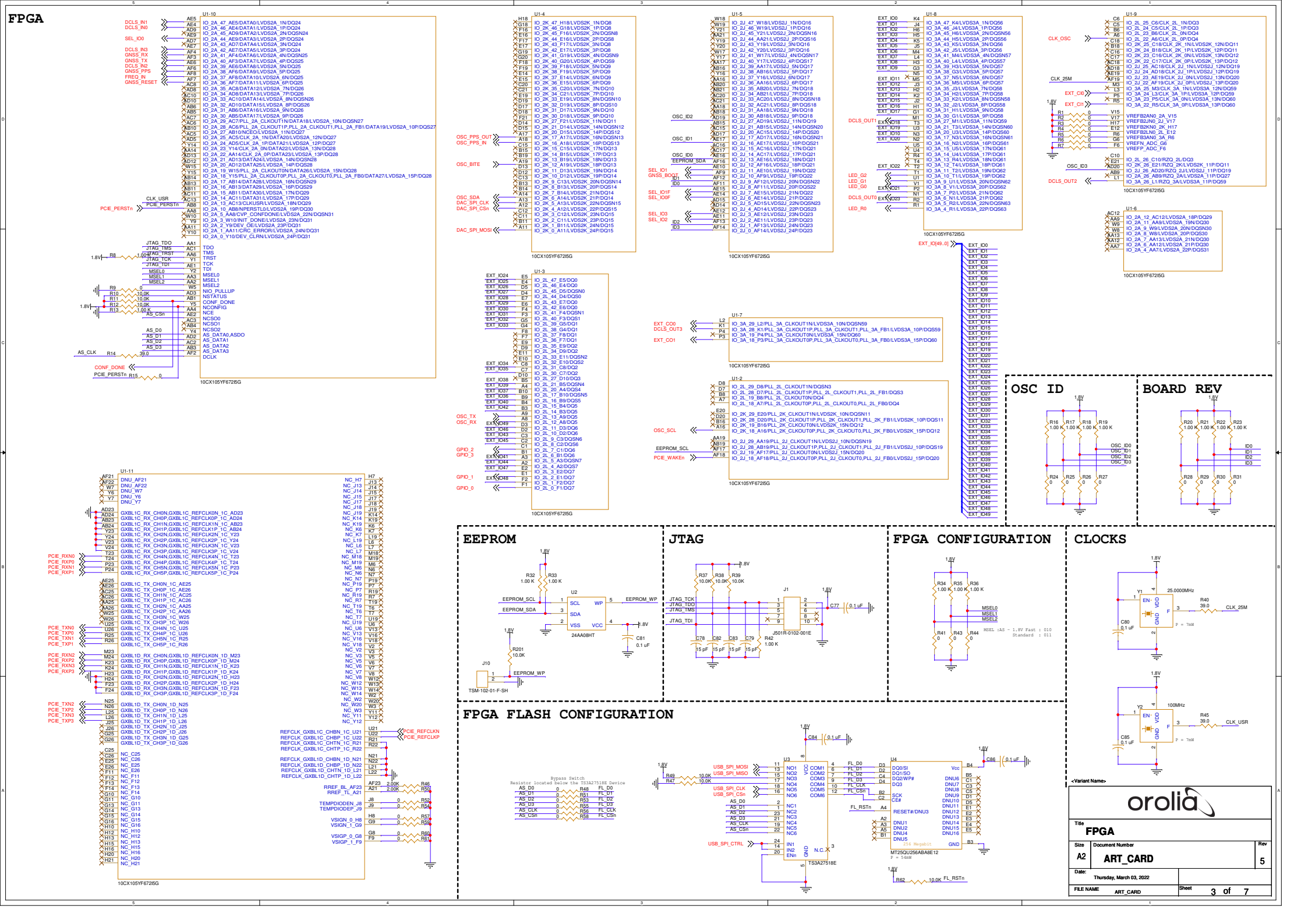
Date: Thursday, March 03, 2022		
FILE NAME: ART_CARD	Sheet: 2 of 7	


FPGA
U1-10
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U1-4
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U1-5
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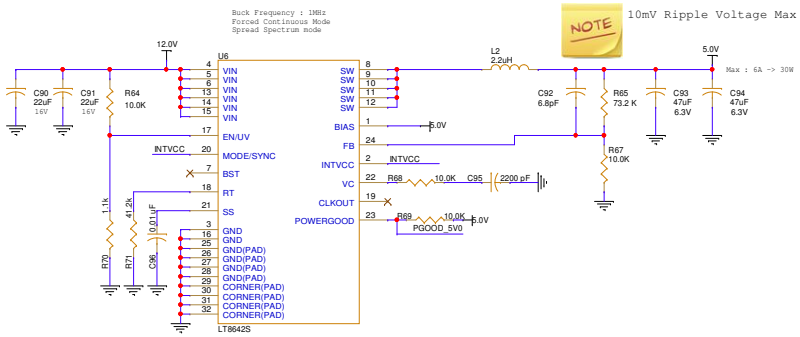
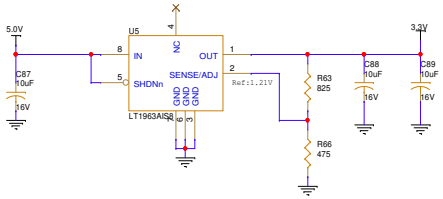
U1-8
10CX105YF672I5G
U1-9
10CX105YF672I5G
U1-6
10CX105YF672I5G
U1-3
10CX105YF672I5G
U1-7
10CX105YF672I5G
U1-2
10CX105YF672I5G
U1-11
10CX105YF672I5G
OSC ID
BOARD REV
EEPROM
JTAG
FPGA CONFIGURATION
CLOCKS
FPGA FLASH CONFIGURATION
orolia
Title
FPGA
Size
A2
Document Number
ART_CARD
Rev
5
Date:
Thursday, March 03, 2022
FILE NAME
ART_CARD
Sheet
3 of 7

```
POWER NEED  : FPGA : OCXO : Comp : TOTAL
on 12V      :      : 7500 :      : 7500 mW
On 11V_ANA  :      :      :   80 :   80 mW
On 5.0V     :      :      :  350 :  350 mW
On 3.3V     :      :      :  243 :  243 mW
On 1.8V     : 1643 :      :   61 : 1704 mW
On 0.95V    :  762 :      :      :  762 mW
On 0.9V     : 2056 :      :      : 2056 mW
                                  -> 12695 mW
```

12V to 5V Switch Converter

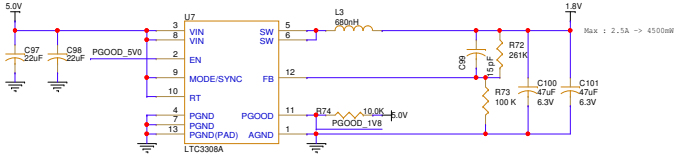


5V to 3.3V LDO Converter

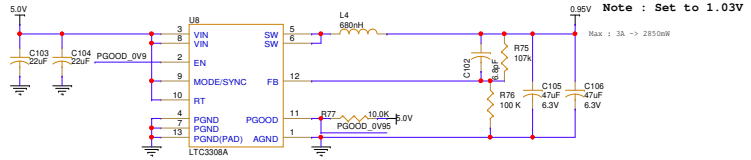


Output : 3.3V
MAX : 0.33A / 1.1W @ Tamb = 85°C
MAX : 0.55A / 1.8W @ Tamb = 60°C

5V to 1.8V Switch Converter

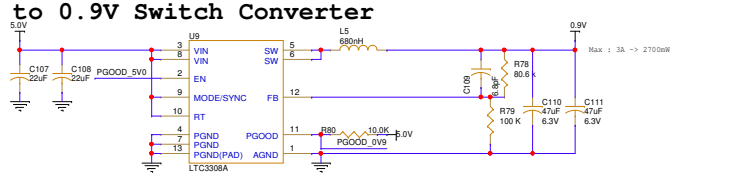


5V to 0.95V Switch Converter

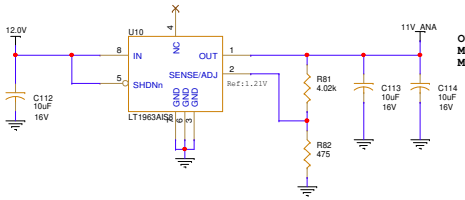


Note : Set to 1.03V

5V to 0.9V Switch Converter

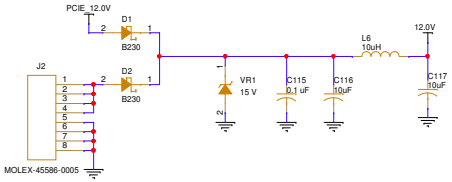


ANALOG POWER SUPPLY



OUTPUT : 11.45V
MAX : 1.03A / 11.86W @ Tamb = 85°C
MAX : 1.5A / 17.17W @ Tamb = 60°C

POWER CONNECTOR



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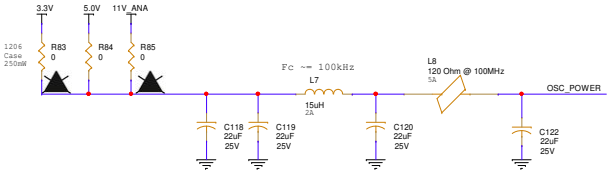
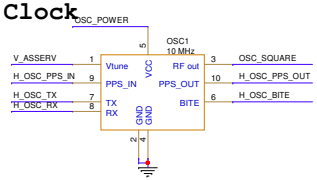
Title: POWER SUPPLY		
Size: A2	Document Number: ART_CARD	Rev: 5
Date: Thursday, March 03, 2022		
FILE NAME: ART_CARD	Sheet: 4 of 7	

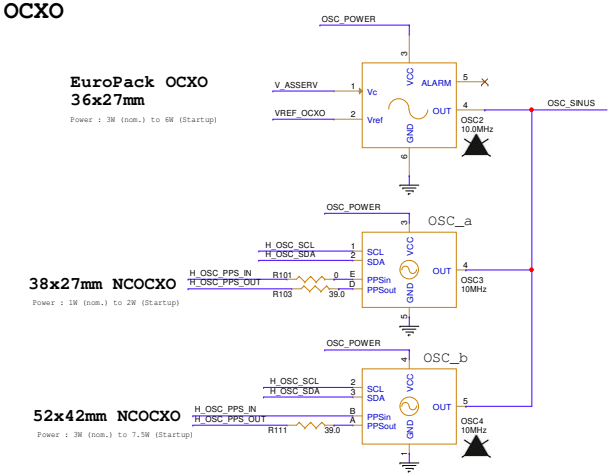
OSCILLATOR POWER SUPPLY



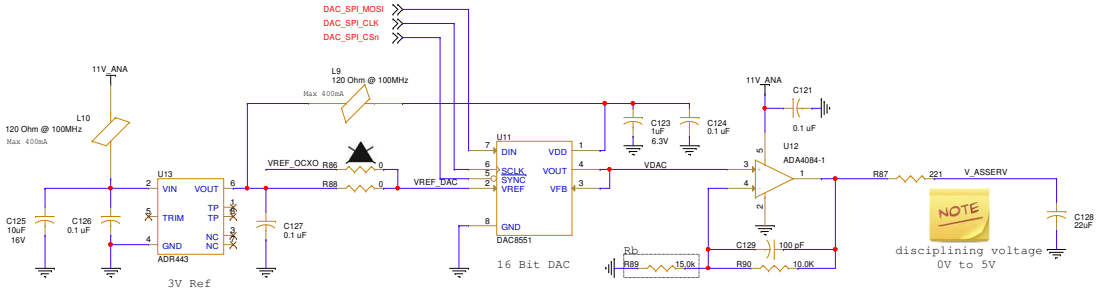
MiniRubidium
Miniature Atomic Clock



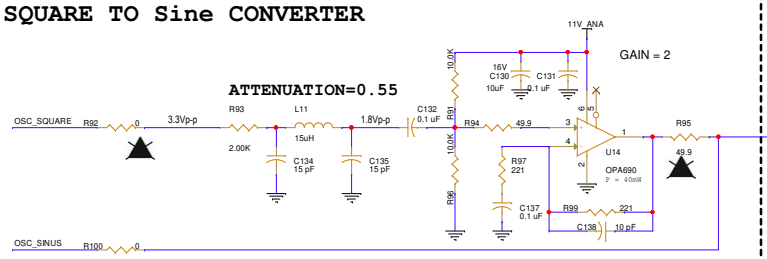
OCXO



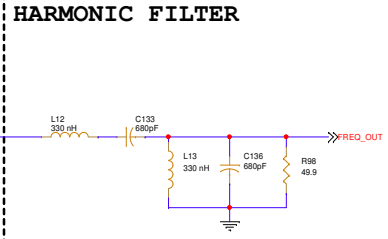
OSCILLATOR CONTROL VOLTAGE



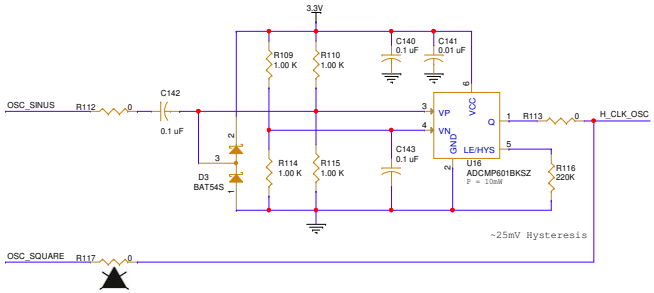
SQUARE TO Sine CONVERTER



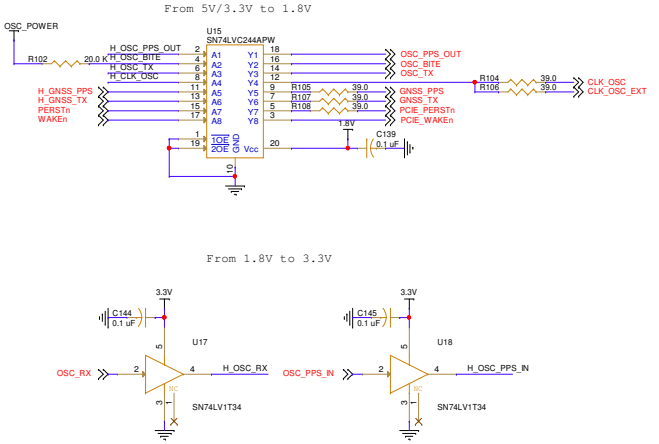
HARMONIC FILTER



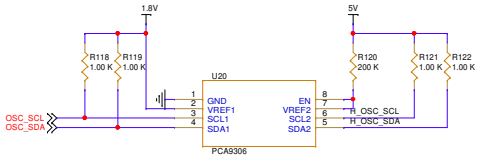
SINUS TO SQUARE CONVERTER



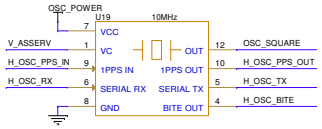
LOGIC VOLTAGE-LEVEL TRANSLATOR



I2C VOLTAGE-LEVEL TRANSLATOR



Chip Scale Atomic Clock



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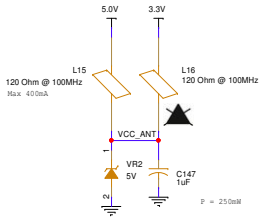
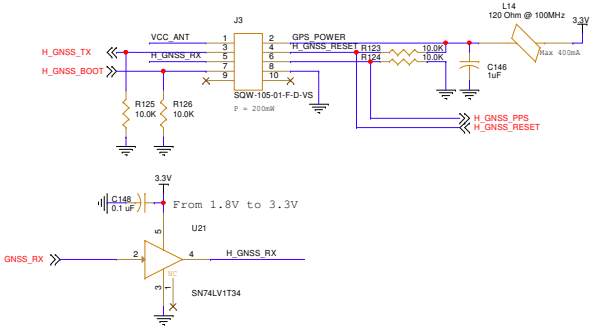
Title: TIMING		
Size: A2	Document Number: ART_CARD	Rev: 5
Date: Thursday, March 03, 2022		
FILE NAME: ART_CARD	Sheet: 5 of 7	

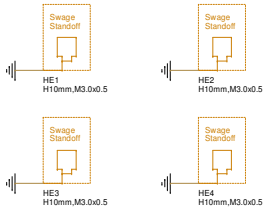
ANTENNA POWER SUPPLY



GNSS RECEIVER

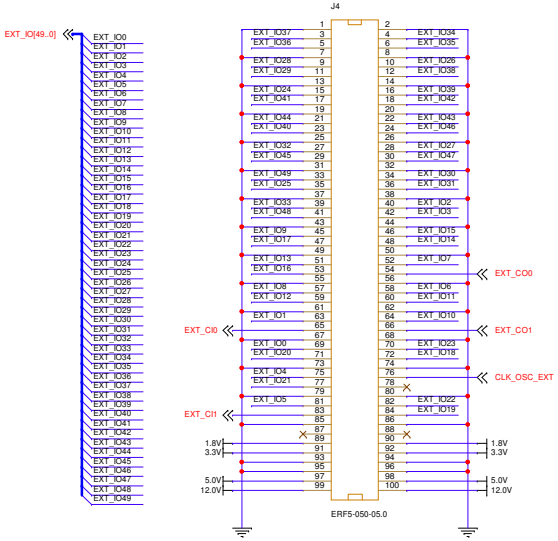


GNSS STANDOFF



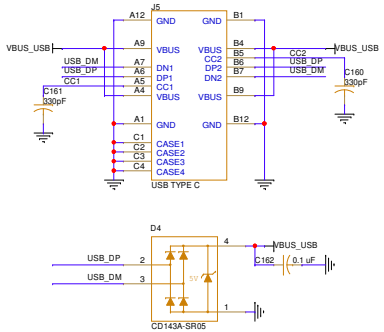
BRACKET HOLES

EXTENSION CONNECTOR

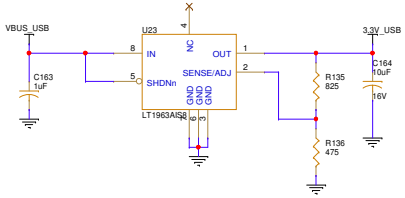


USB-C CONNECTOR

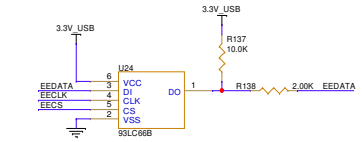
Support USB2.0



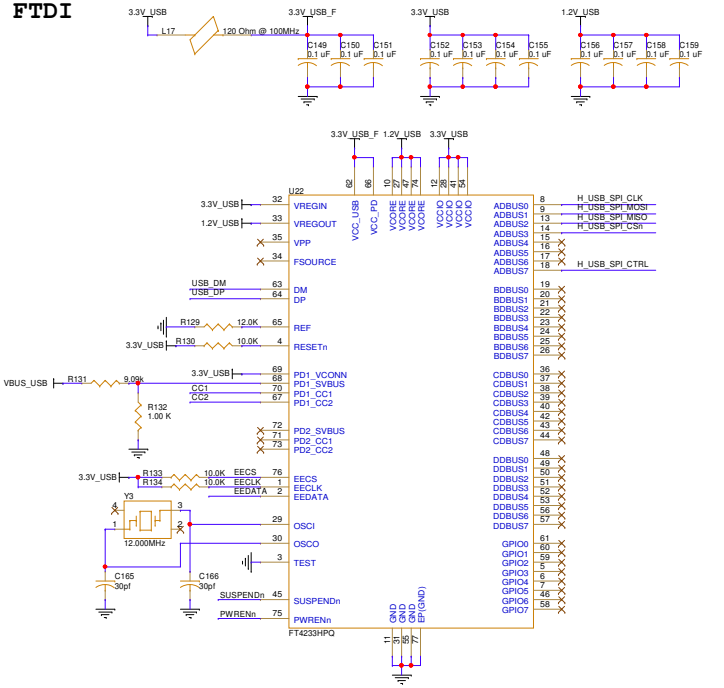
USB SELF-POWERED



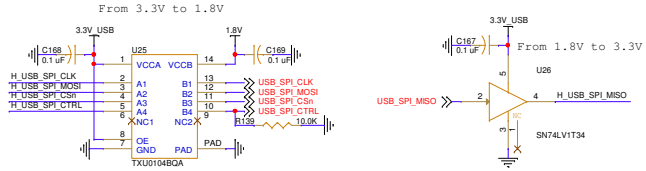
EEPROM FTDI



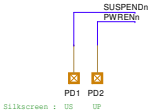
EEPROM FTDI



SPI VOLTAGE-LEVEL TRANSLATOR



TEST POINTS



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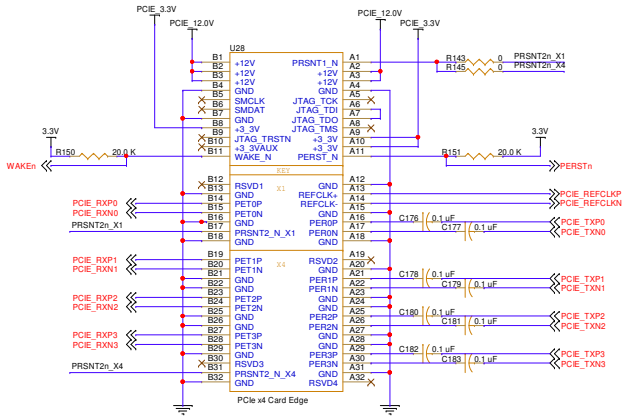
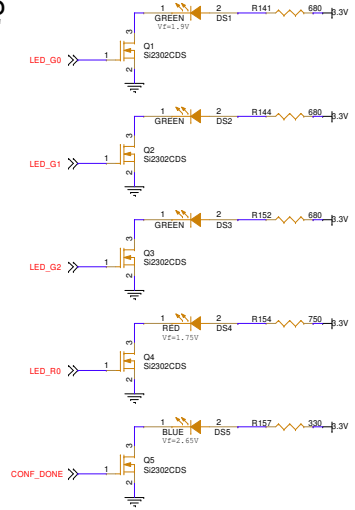
Title	GNSS - EXTENSION
Size	A2
Document Number	ART_CARD
Rev	5
Date:	Thursday, March 03, 2022
FILE NAME	ART_CARD
Sheet	6 of 7

PCIe CONNECTOR



LED



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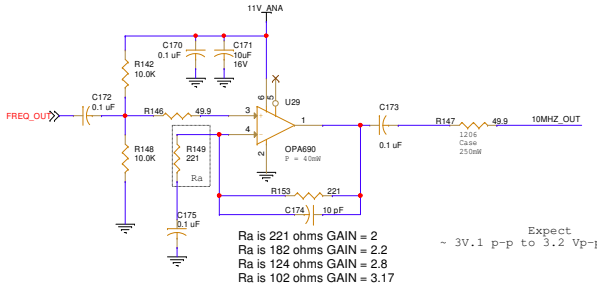

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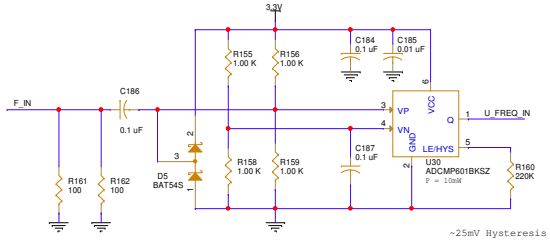
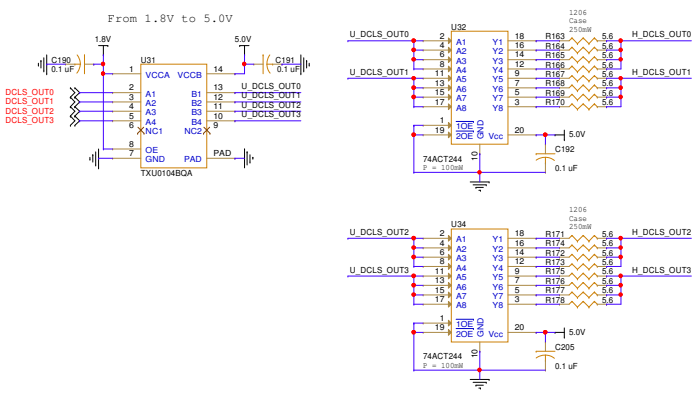
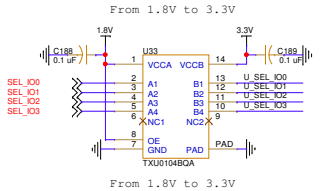
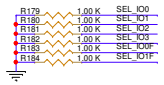


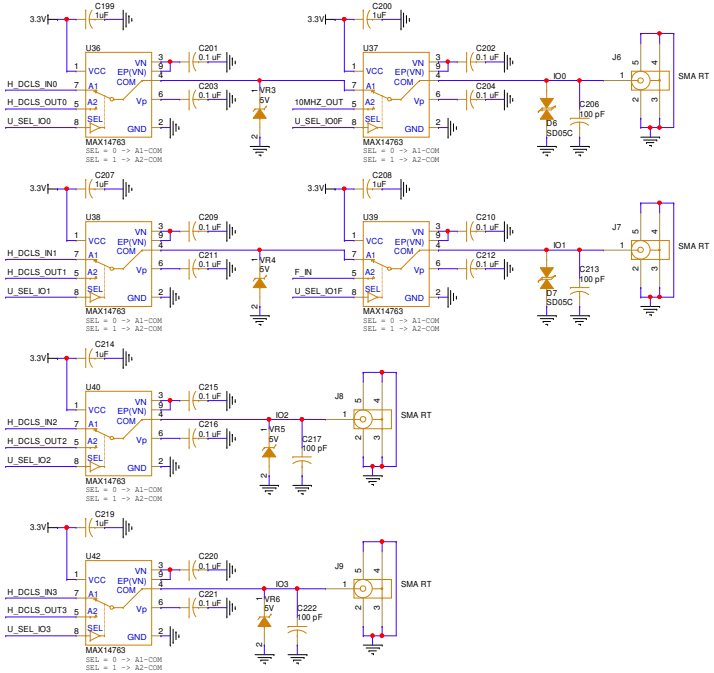
DCLS OUTPUT DRIVER



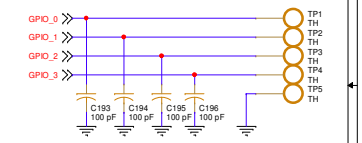




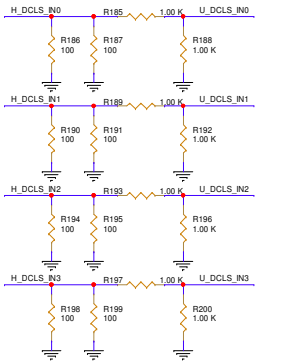
IO CONNECTORS / SWITCH

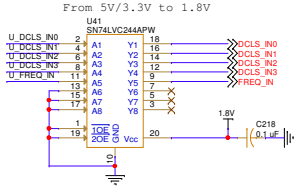


GPIO

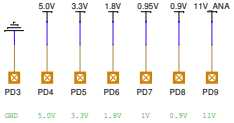


DCLS INPUT DRIVER





TEST POINTS

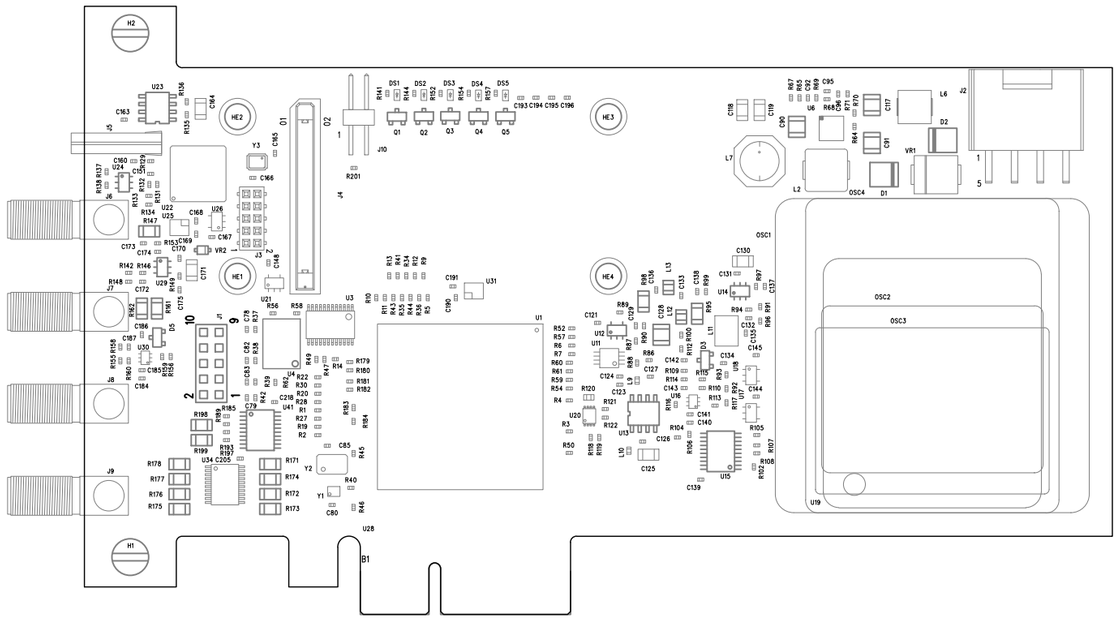


<Variant Name>

orolia

Title	CONNECTORS	
Size	Document Number	Rev
A2	ART_CARD	5
Date:	Thursday, March 03, 2022	
FILE NAME	ART_CARD	Sheet 7 of 7

Rev	DESCRIPTION	DATE	APPROVED
1			



UNLESS OTHERWISE SPECIFIED:		NAME	DATE
	DRAWN	H ECHELARD	03/03/2022
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MATERIAL: PCB	CHANGE RESTRICTED NO MANUAL CHANGES		
FINISH	THIRD ANGLE PROJECTION		

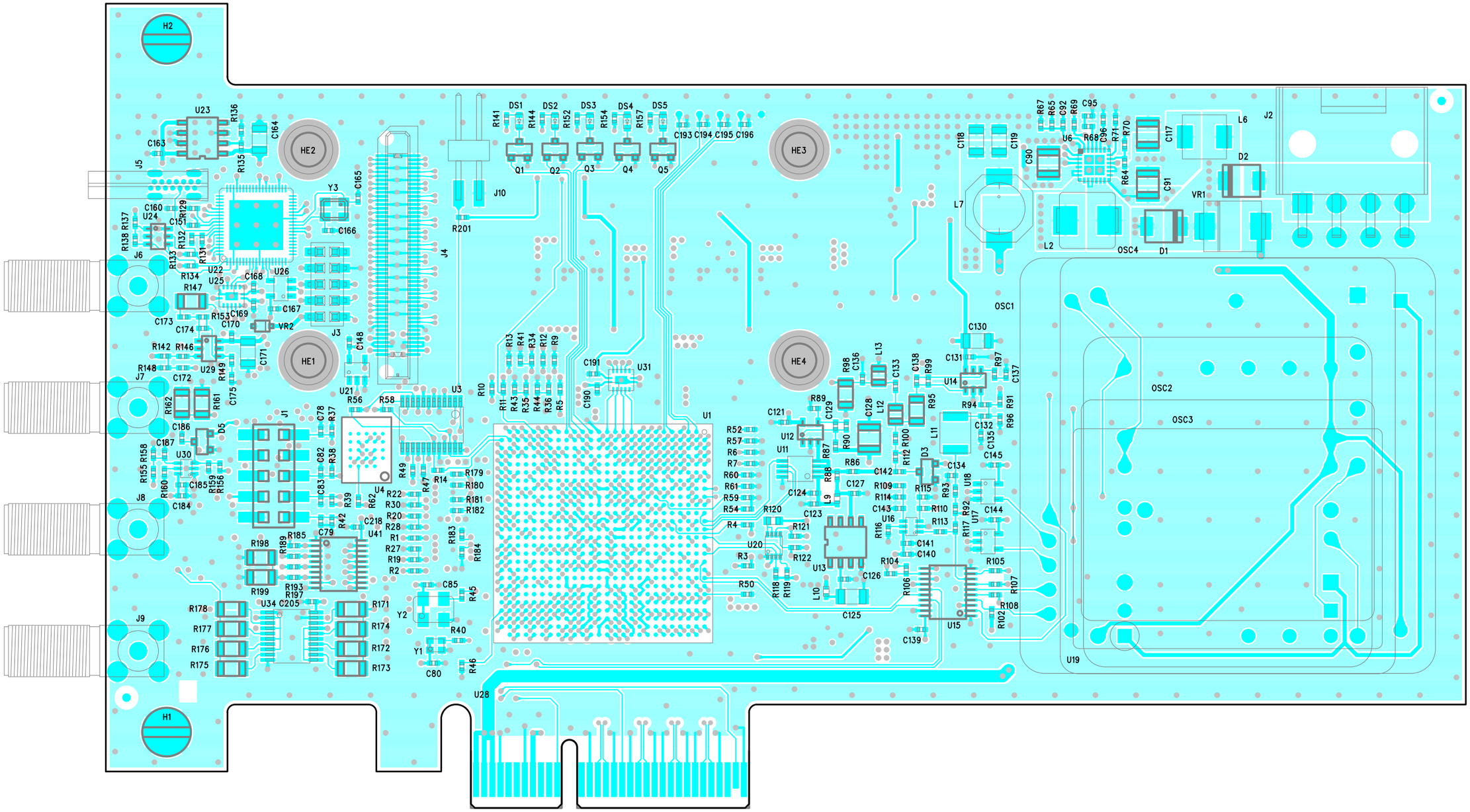
OROLIA FRANCE

PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

SIZE A3 | DWG. NO. ART_CARD_PCB | REV 5

SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1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HE1
HE2
HE3
HE4
J1
J2
J3
J4
J5
J6
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U1
U2
U3
U4
U19
U20
U21
U22
U23
U24
U25
U26
U28
U29
U30
U31
U34
U41
OSC1
OSC2
OSC3
OSC4
VR1
VR2
D1
D2
D3
L2
L6
L7
Y1
Y2
Y3
DS1
DS2
DS3
DS4
DS5
Q1
Q2
Q3
Q4
Q5
R201
C80
C85
C125
C126
C139
C163
C164
C165
C166
C167
C168
C169
C170
C171
C173
C174
C186
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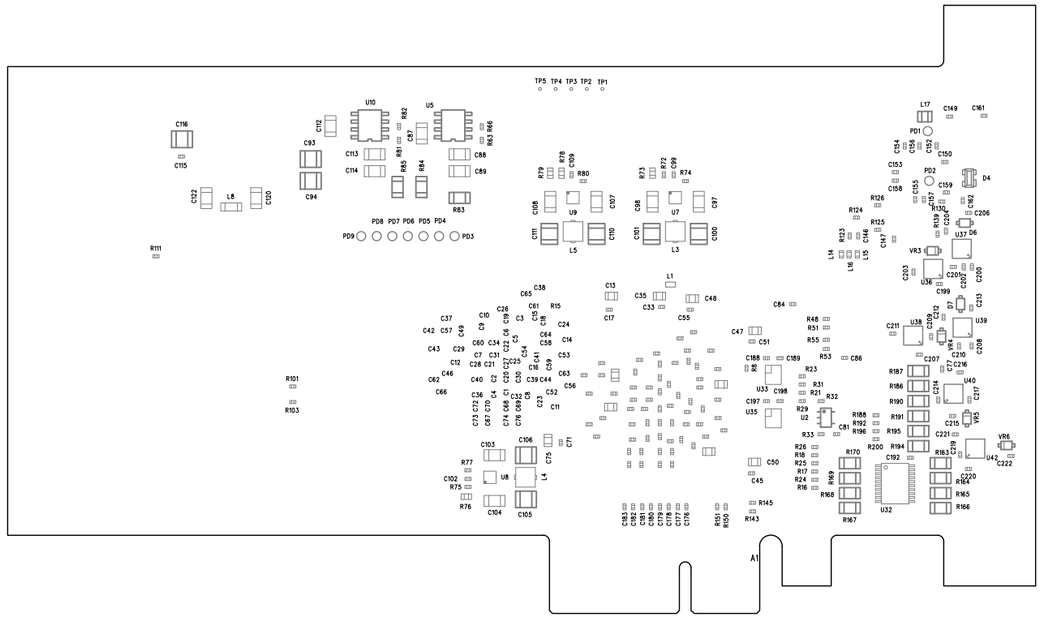
R199

Rev	DESCRIPTION	DATE	APPROVED
1			



UNLESS OTHERWISE SPECIFIED:		NAME	DATE
	DRAWN	H ECHELARD	03/03/2022
MATERIAL: PCB			
FINISH			

CHANGE RESTRICTED
NO MANUAL CHANGES

THIRD ANGLE PROJECTION

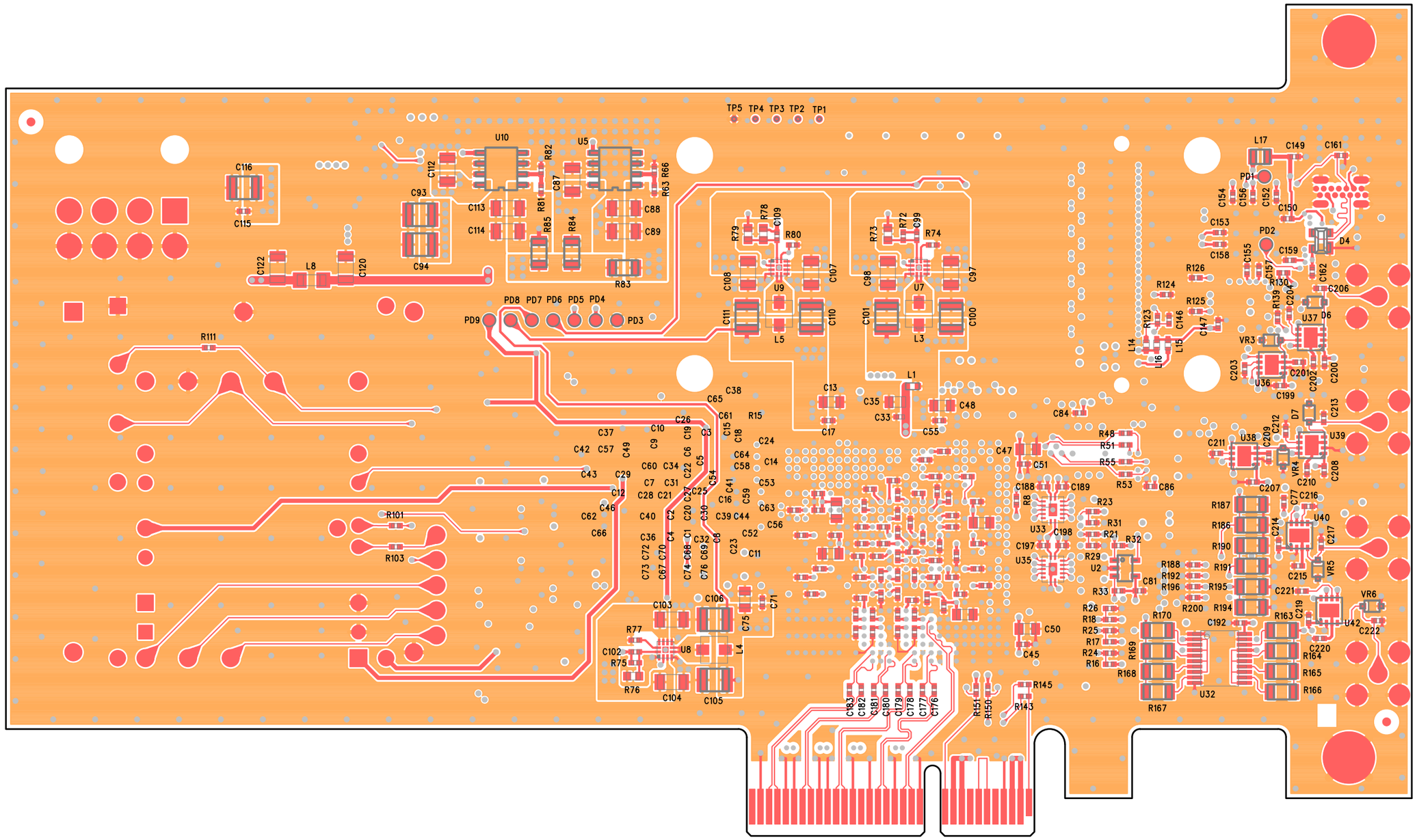
OROLIA FRANCE

PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

SIZE	DWG. NO.	REV
A3	ART_CARD_PCB	5

SCALE: 1:1	DO NOT SCALE	SHEET 1 OF 1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U5
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C115
C112
C93
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R82
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R81
R85
R84
R83
R63 R66
C88
C89
C122
L8
C120
PD9
PD8 PD7 PD6 PD5 PD4
PD3
R111
R101
R103
C38
C65
C61
R15
C26
C10
C19
C3
C15
C18
C24
C37
C42 C57 C49
C9
C64
C58
C14
C60 C34
C22 C6 C5
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C43
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C40
C2
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C56
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C6
C52
C23
C11
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C67 C70
C74 C66 C69
C76
C71
C103
C106
C75
R77
C102
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U8
L4
R76
C104
C105
C108
R79
R78
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C98
R73
R72
C99
R74
U7
C97
C101
C100
L3
L1
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C17
C35
C33
C48
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R48
R51
R55
R53
C86
C188
C189
R8
C197
U33
C198
U35
R23
R31
R21
R32
R29
U2
R33
C81
R26
R18
R25
R17
R24
R16
C50
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R143
R151
R150
C183
C182
C181
C180
C179
C178
C177
C176
R123
R124
R126
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C147
L14
L16
L15
L17
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C161
PD1
C154
C156
C152
C150
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PD2
C158
C155
C159
D4
C162
C157
R130
C204
C206
R139
U37
D6
VR3
C203
C201
C202
C200
U36
C199
D7
C213
C212
C209
U38
U39
C211
VR4
C208
C210
C207
C77
C216
U40
C214
C217
VR5
C215
C221
VR6
C219
U42
C222
C220
R164
R165
R166
R163
C192
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R200
R188
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R167
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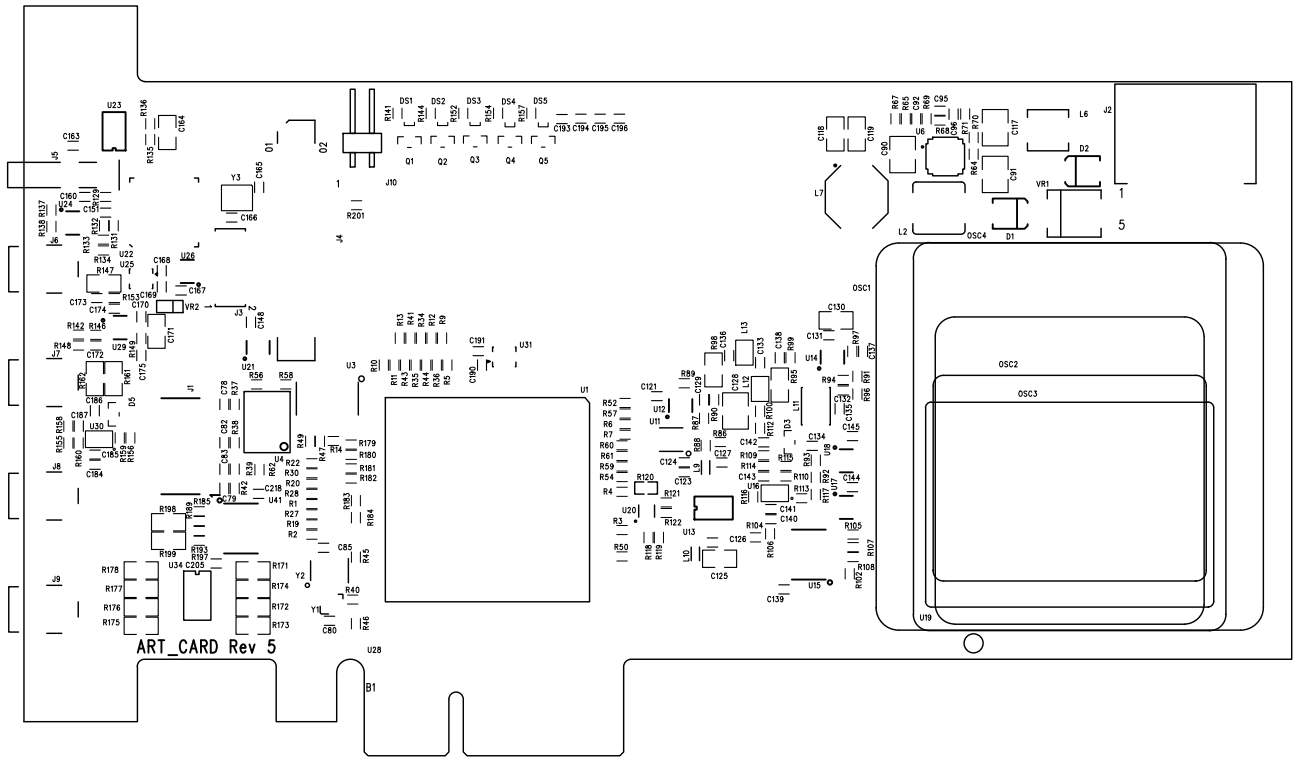

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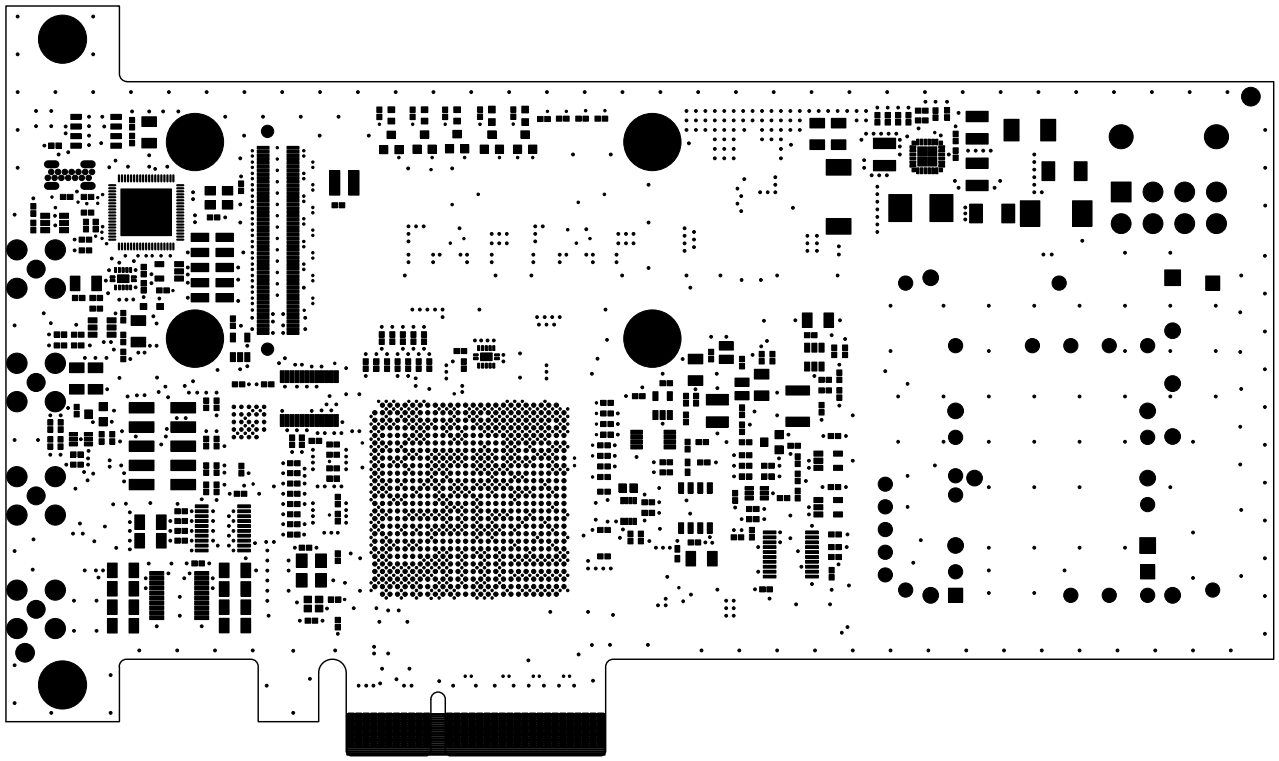
DOSSIER: ART_CARD Rev 5	03/03/22



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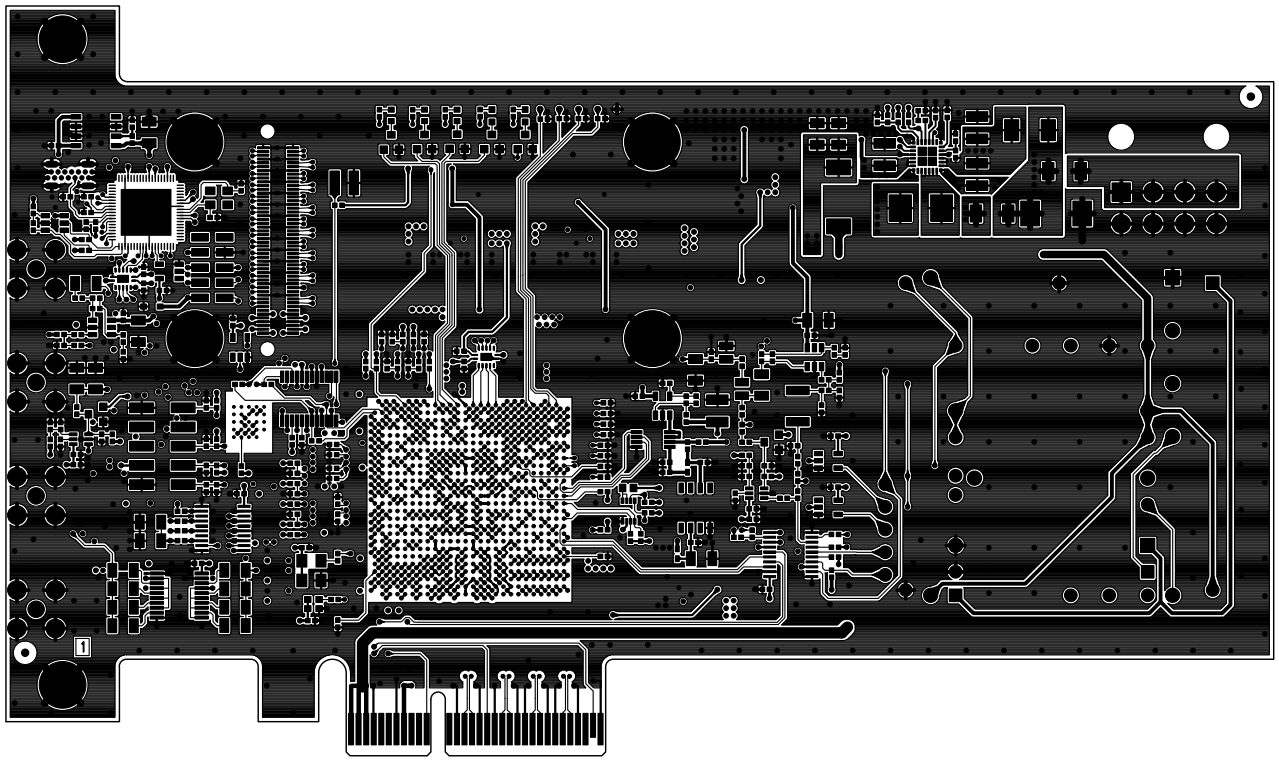
DOSSIER: ART_CARD Rev 5	03/03/22



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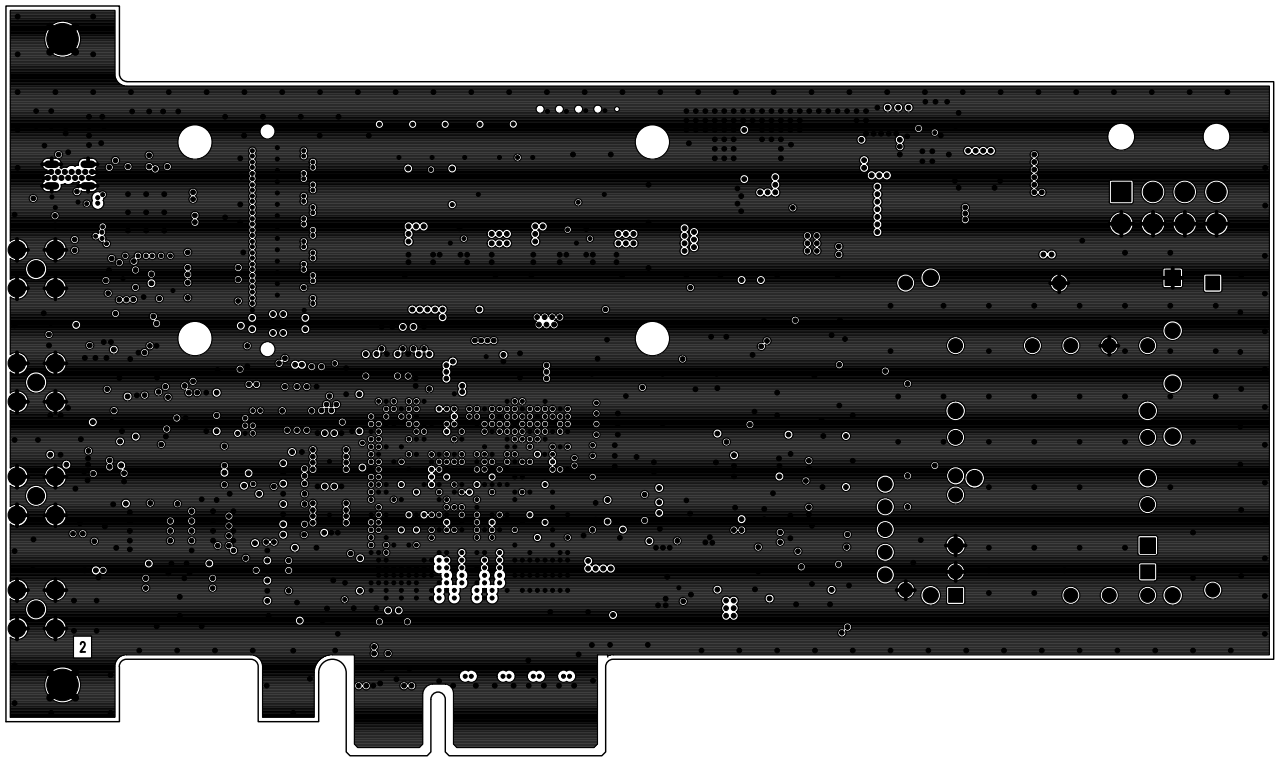
DOSSIER: ART_CARD Rev 5	03/03/22



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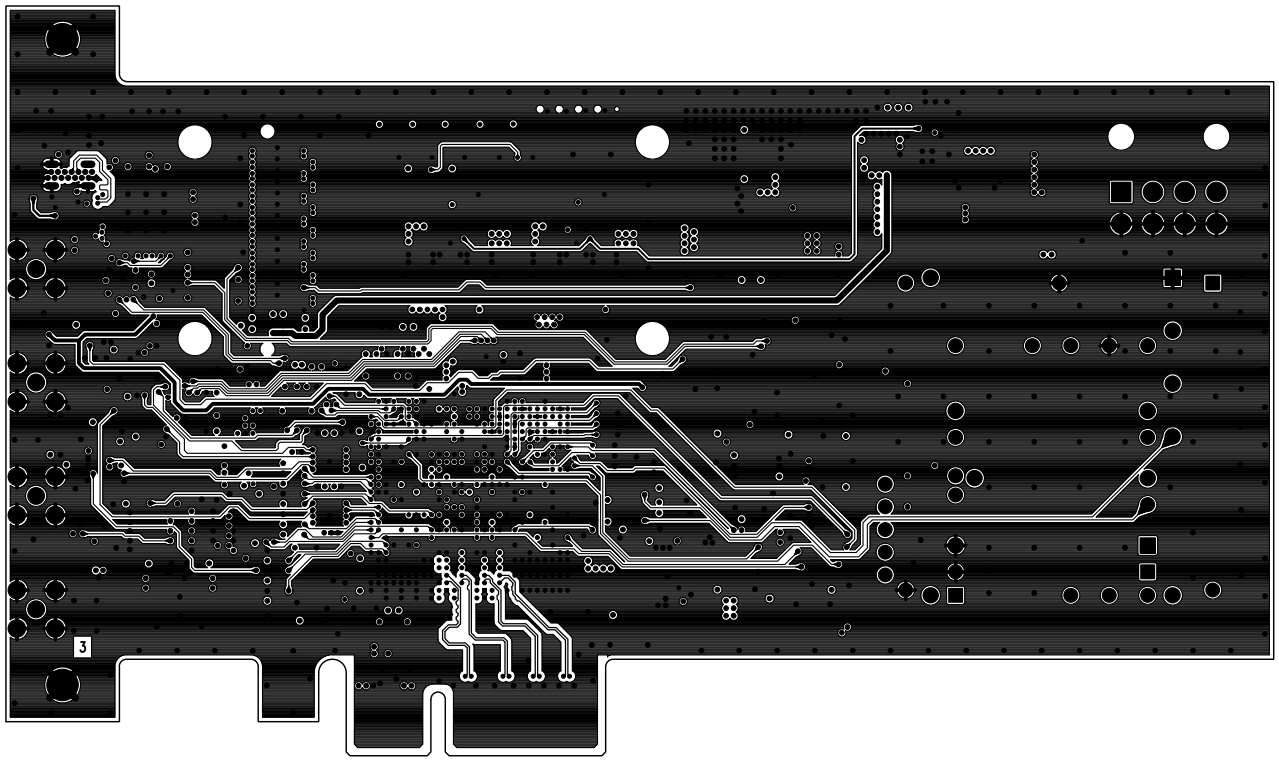

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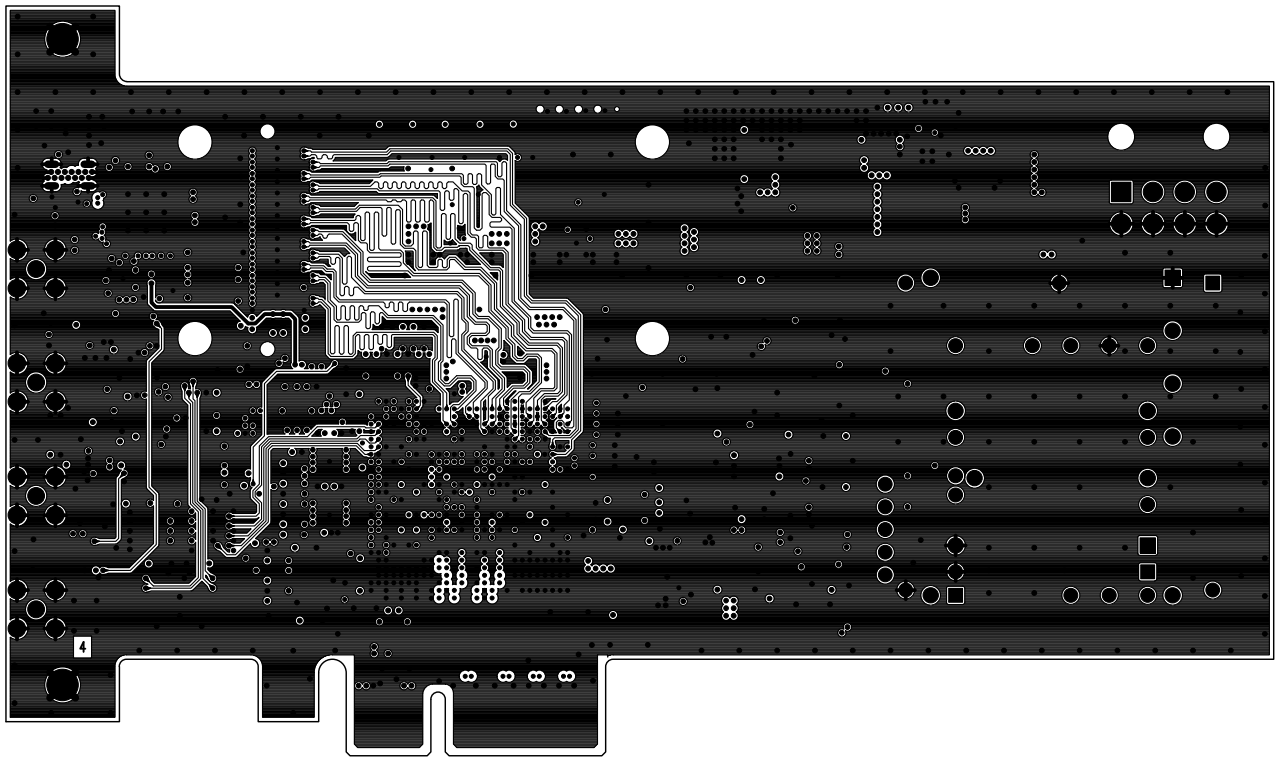

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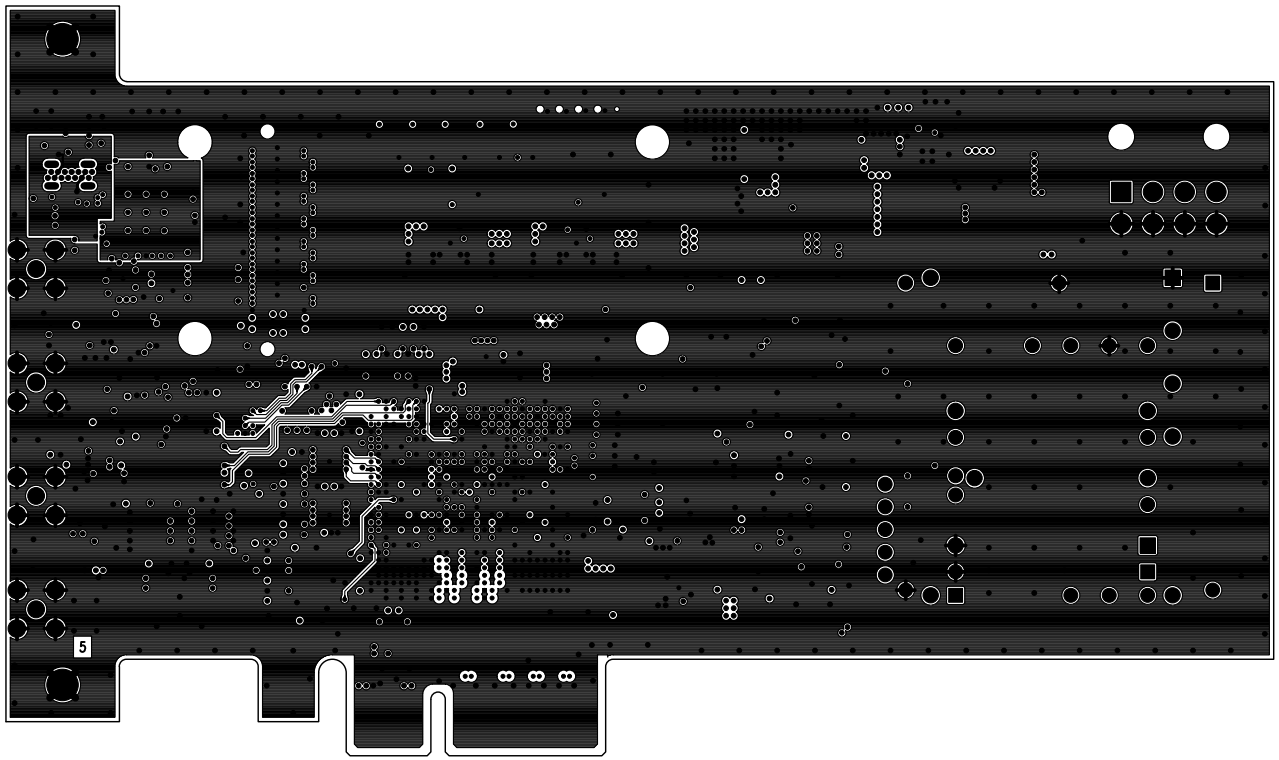

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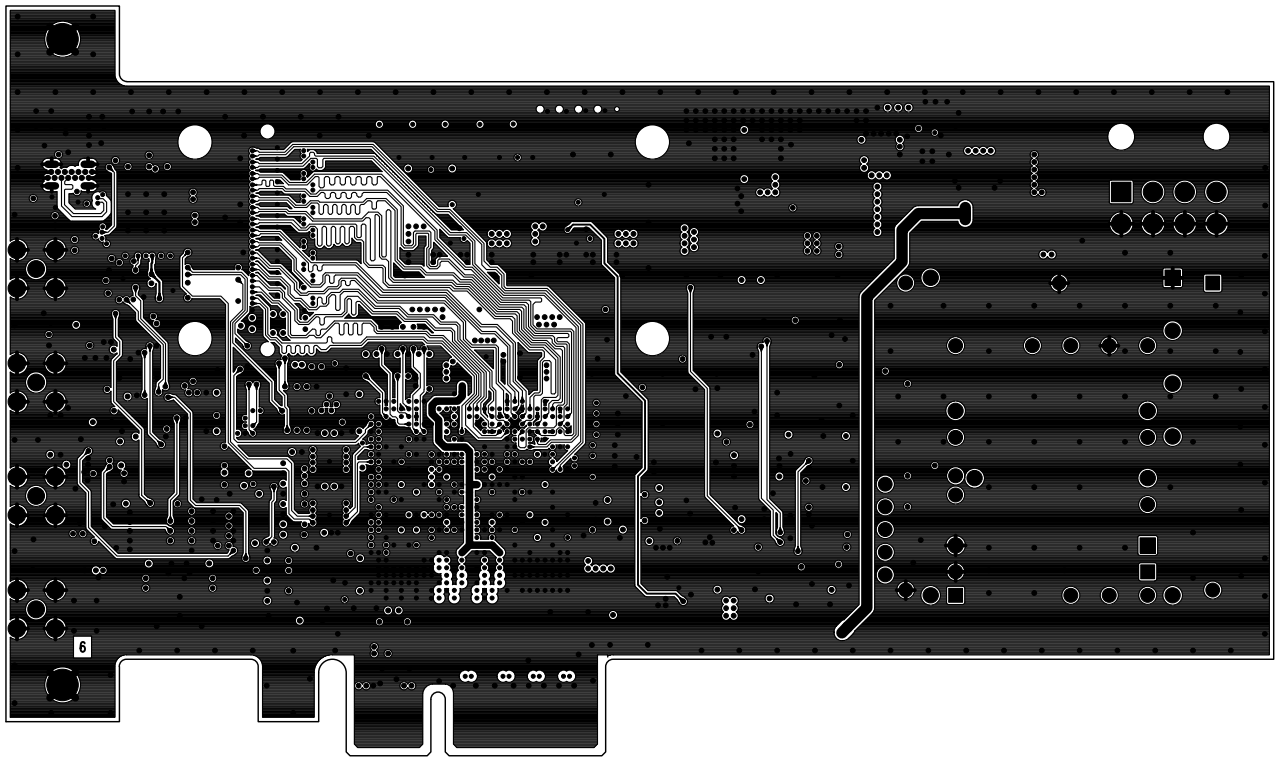

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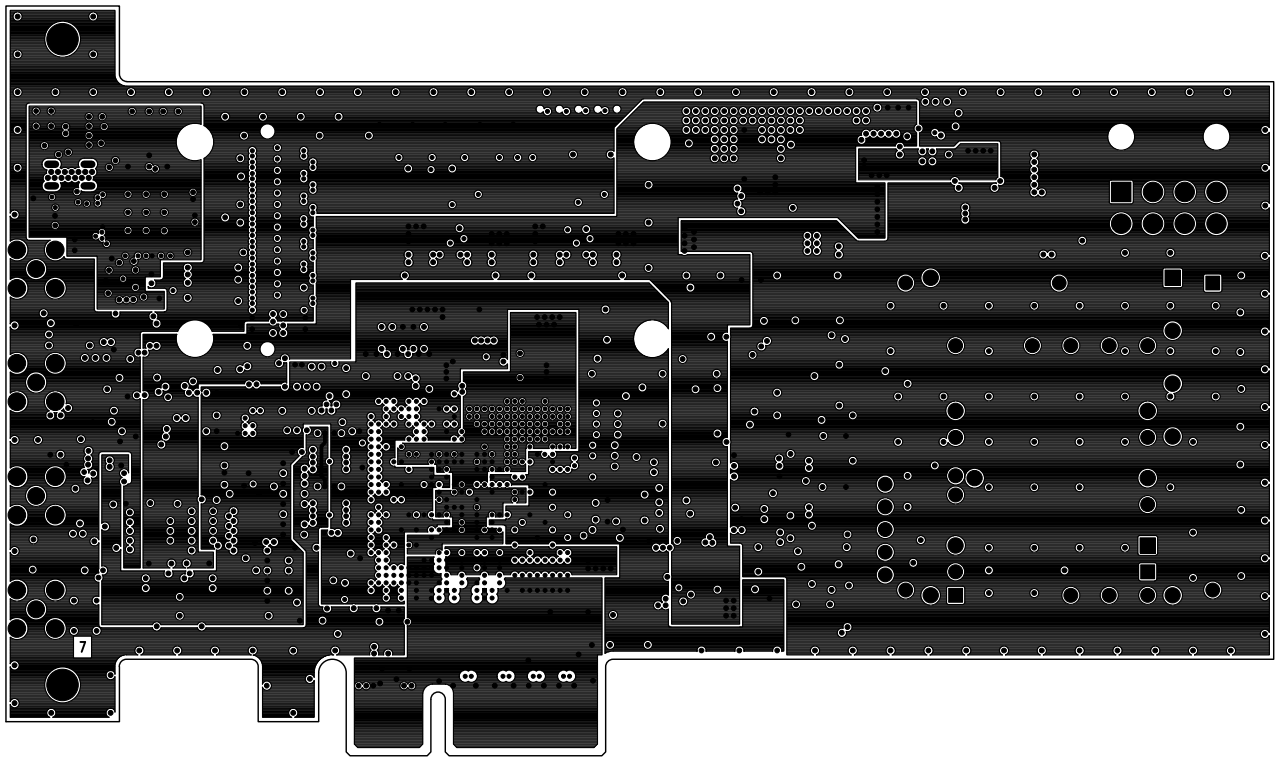
DOSSIER: ART_CARD Rev 5	03/03/22



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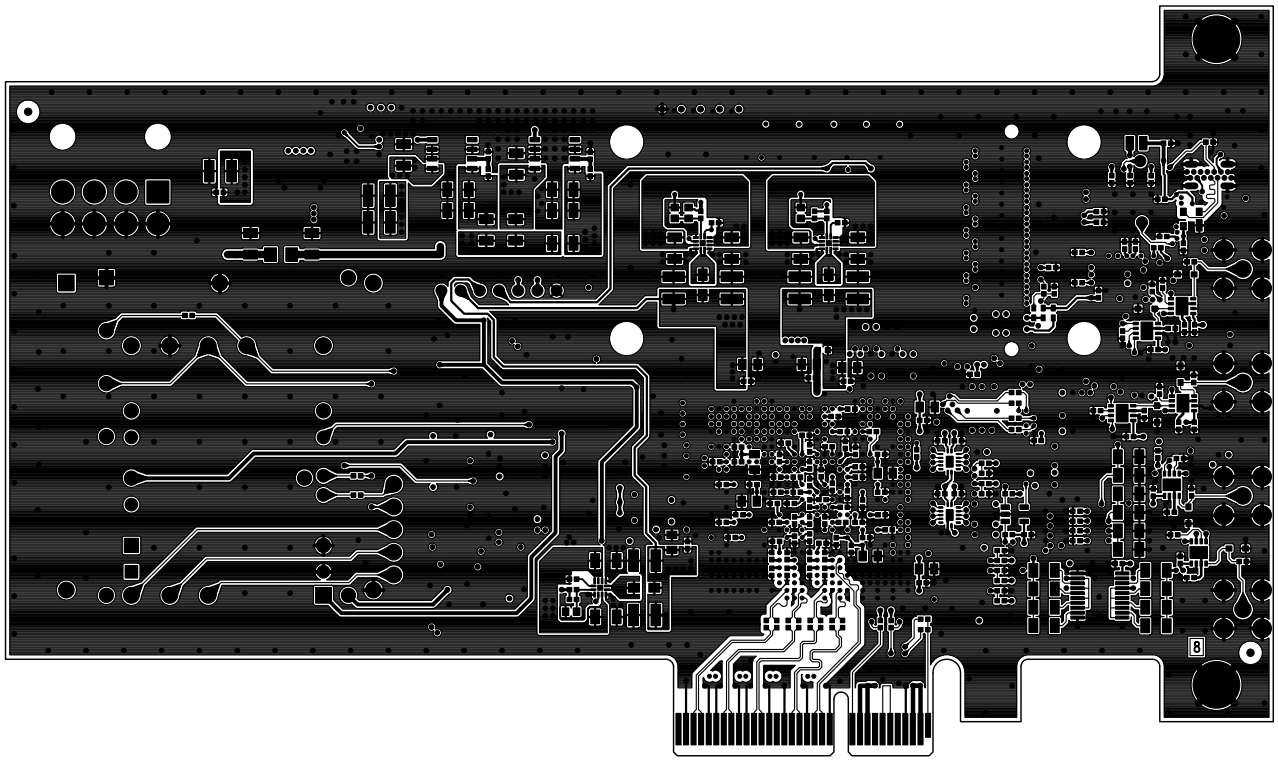

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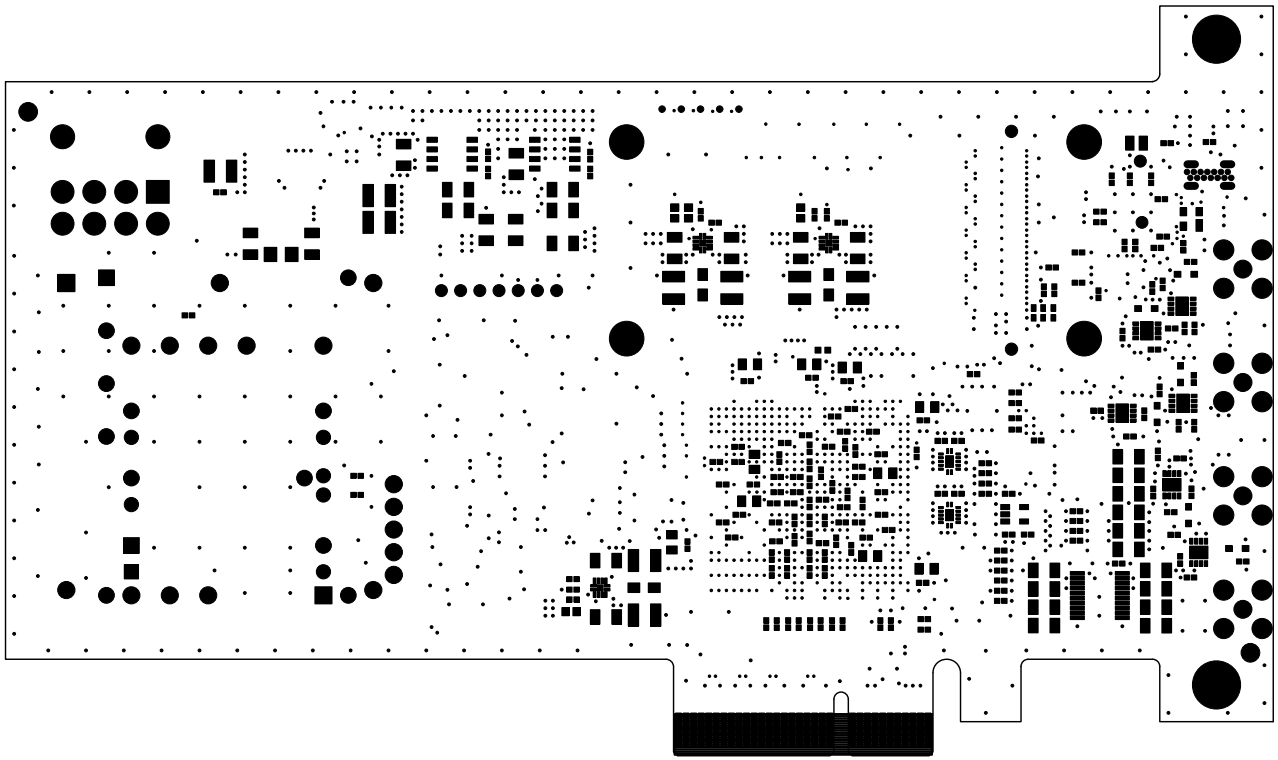
DOSSIER: ART_CARD Rev 5	03/03/22



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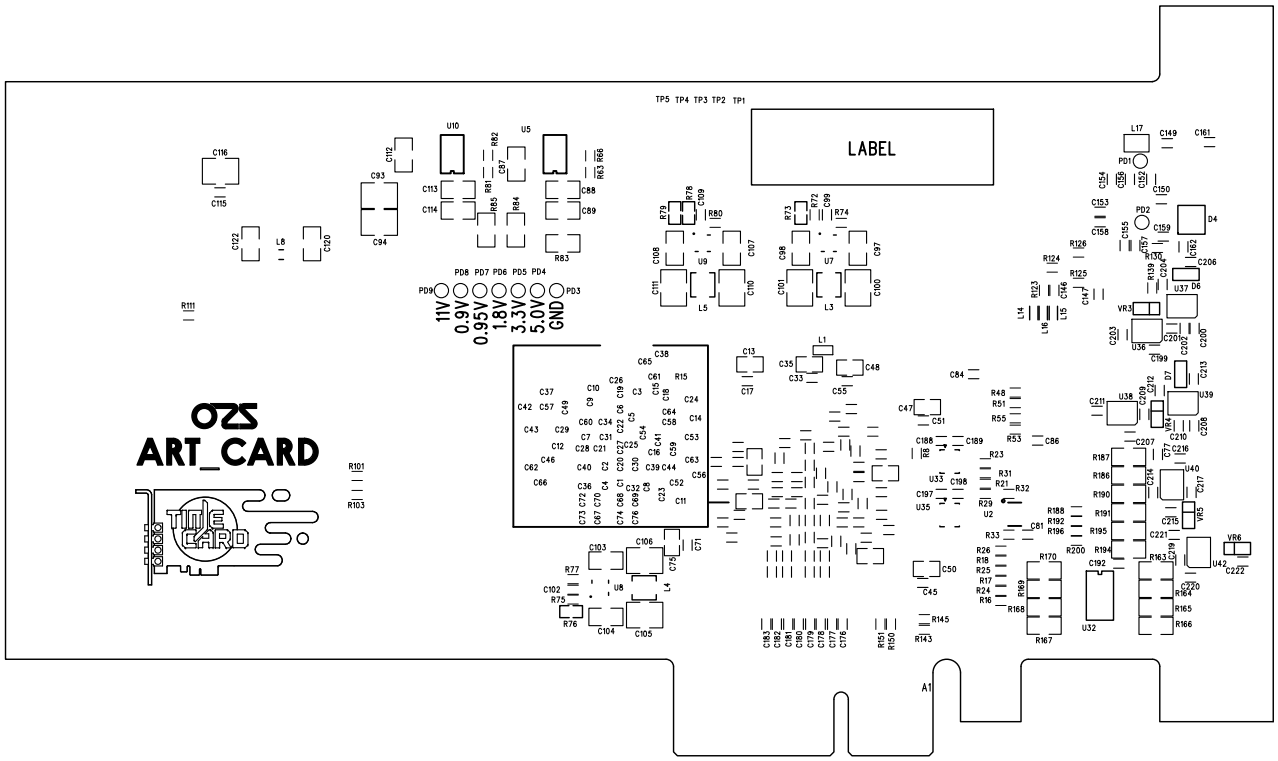
DOSSIER: ART_CARD Rev 5	03/03/22



FILM: SERIGRAPHIE SOUDURE	ARTEMIS
DOSSIER: ART_CARD Rev 5	03/03/22

Rev	DESCRIPTION	DATE	APPROVED
1			

NOTES:

1. FABRICATE BOARD PER:
Latest revision of IPC-A-600 Class 2. Electrical integrity testing required, per section 5.2 of IPC-A-600.

2. MATERIAL : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
Rigid laminate and prepeg shall be per IPC-4101/99/101/126. As described in the StackUp.
Laminate must meet latest RoHS directive subject to Orolia Engineering Approval.

3. FINISH : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
ENIG (Electroless Nickel, Immersion Gold) per IPC-4552

4. SOLDER MASK : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
LPI per IPC-SM-840 (current rev) COLOR : GREEN
Soldermask provided as 1 to 1 and shall be oversized at the fabricator as required in order to insure that soldermask does not encroach upon thru hole and SMT pads.
0.008 DIA Vias shall be plugged/tented from top and bottom side per artwork supplied unless mask is removed by artwork. These vias are required to be filled and copper capped. It is acceptable to use and epoxy fill after initial plating, followed by a copper cap process to cap the via fill.
Continuous copper plate is required.

5. SILKCREEN : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
White (All silkscreen to be removed from any exposed plated areas)

6. DIMENSIONING AND TOLERANCING PER ANSI-Y-14.5 (LATEST REV).

7. 94V-0 Min is required and shall be marked on top or bottom side silkscreen or copper

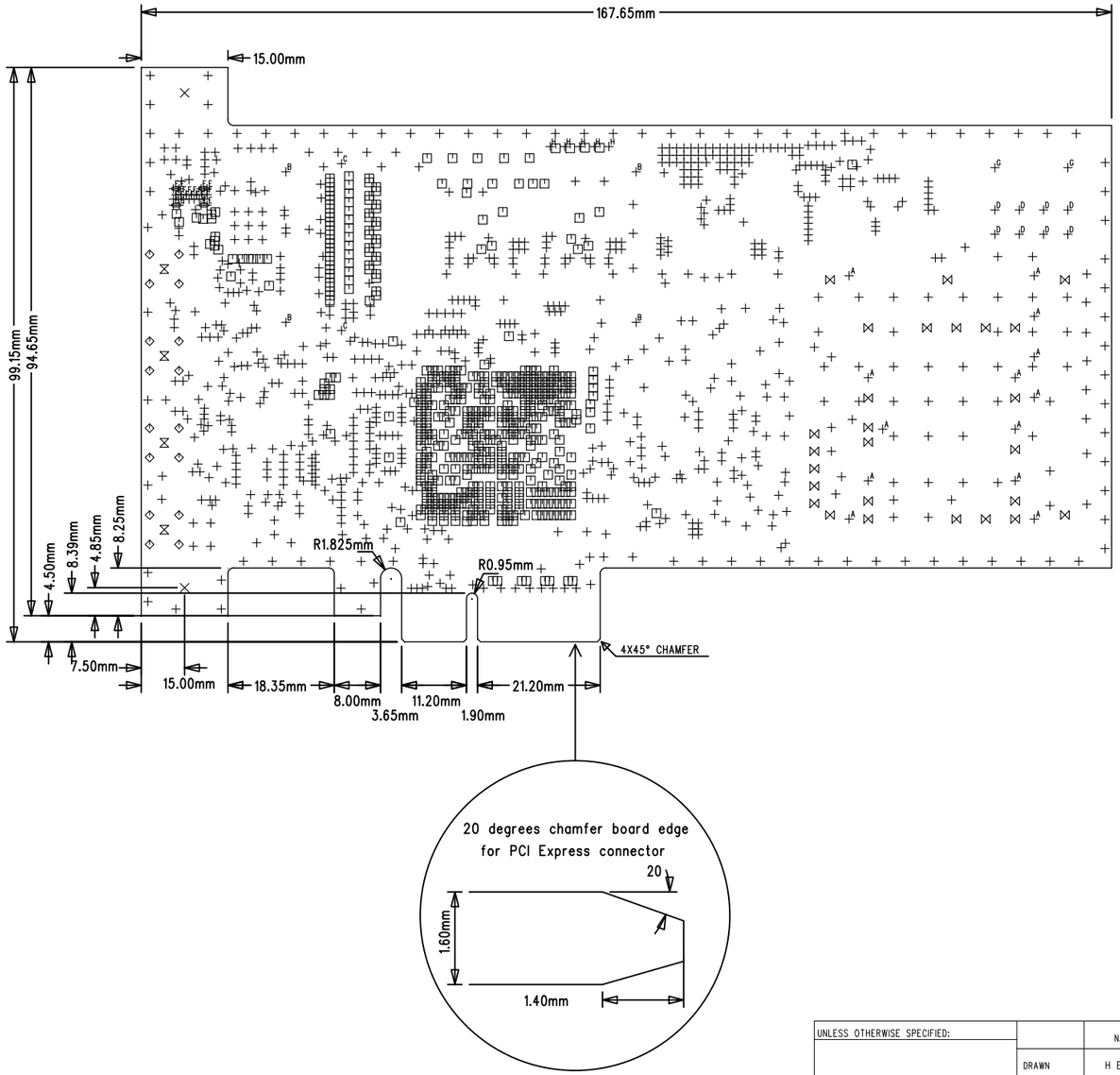
8. All copper on any layer shall be trimmed back 0.015 from the board edge as required.

9. All internal unused pads shall be removed

10. Teardrops shall be added where possible

11. All holes sizes shown are expected finished hole sizes after processing.

12. This board shall be supplied in array format that shall be determined/approved by the purshaser of the bare board



SIZE	QTY	SYM	PLATED	TOL
0.25	518	□	YES	+/-0.05
0.3	915	+	YES	+/-0.05
0.4	14	+F	YES	+/-0.05
0.45	5	+H	YES	+/-0.05
0.6 x 1.6	4	+E	YES	+/-0.05
1.1	26	⋈	YES	+/-0.05
1.3	13	+A	YES	+/-0.05
1.65	4	⧖	YES	+/-0.05
1.8	16	◇	YES	+/-0.05
1.95	8	+D	YES	+/-0.05
3.5	2	×	YES	+/-0.05
1.45	2	+C	NO	+/-0.05
3	2	+G	NO	+/-0.05
4.4	4	+B	NO	+/-0.05

		NAME	DATE	
UNLESS OTHERWISE SPECIFIED:	DRAWN	H ECHELARD	03/03/2022	OROLIA FRANCE
	PART NUMBER: ART_CARD_PCB			
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MATERIAL: PCB	CHANGE RESTRICTED NO MANUAL CHANGES			SIZE A3 / DWG. NO. ART_CARD_PCB / REV 5
FINISH	THIRD ANGLE PROJECTION			SCALE: 1:1 / DO NOT SCALE / SHEET 1 OF 1

Angers Technopole
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49070 BEAUCOUZÉ FRANCE
Phone : +33(0)2-41-48-98-68
p.benoit@artemis-cad.com
www.artemis-cad.com

TECHNICAL SPECIFICATION

IPC-A-600

CUSTUMER : OROLIA
MANUFACTURER :

PCB Reference :	ART_CARD	**Index :**	Rev 5

☑	**PCB Unit**	**Unit PCB dimensions :**	167.65	X	99.15	mm	
☐	**Panel PCB : 0**	**Panel dimensions :**	0	X	0	mm	
Material :	FR4	**Surface :**	1.66	**dm²**	**Track / Gap :**	0.15 / 0.15	mm

PCB Type :	MC8	Finish Copper Thikness (µm) :	12µ	17,5µ	35µ	40µm
PCB Thickness (mm) :	16/10	External Layer :	☐	☐	☐	☑
		Intern Layer :	☐	☑	☐	☐

Technology	☑ Plated Trough Hole	**Via type :**	Hole / pads ratio : 0,25/0,55
☑ Traditional	☐ Press-fit Hole	☑ Traditional Via	☐ Via in pad
☑ SMT	☐ Autre	☐ Laser Via	☐ Stacked ☐ Staggered
Surface Treatement Finished		☐ Blinded Via	Couche départ et d'arrivée
☑ Ni/Au Chemical	☐ Sn/Pb surfondu	☐ Buried Via	Couche départ et d'arrivée
☐ Sn/Cu HAL	☐ Autre	☐ Filled Via	☐ Resin ☐ Copper

Peelable Solder Mask	☐ Standard		☐ TOP	☐ BOTTOM
Solder Mask	☑ Photo-imageable	Green	☑ TOP	☑ BOTTOM
Silkscreen	☑ Ink	White	☑ TOP	☑ BOTTOM
Electrical Test			☑ Yes	☐ No

☑ **Impedance control :** ☑ Produced ☐ Measured
50 ohms

☑ **Differential Pairs :** ☑ Produced ☐ Measured
85 ohms on layer 1, 3 and 8 ; 90 ohms on layer 4, 5 and 8

☑ **Stack-up :** voir avec le fabricant PCB et selon contraintes.

☐ **Milling** Milling Diameter : 0 mm

Comments :

Construire un empilage pour avoir avoir des lignes 50 ohms en 150µm (classe de la carte)
Pour les lignes 85 et 90 ohms, ajuster les largeurs si necessaire en gardant les isolations.