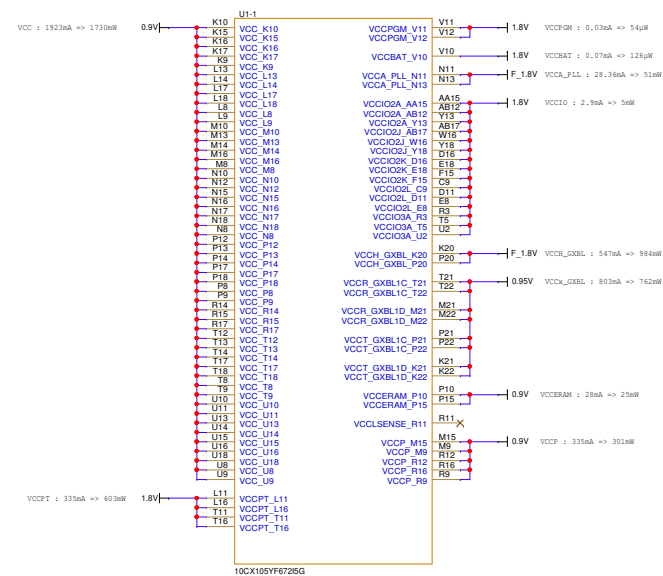
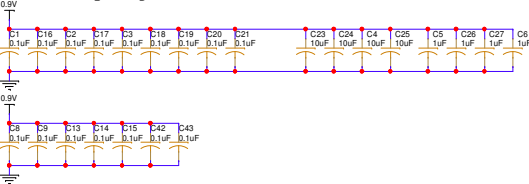


orolia		
Title <b>OVERVIEW</b>		
Size <b>A2</b>	Document Number <b>ART_CARD</b>	Rev <b>2</b>
Date: <b>Tuesday, April 13, 2021</b>		
FILE NAME <b>ART_CARD</b>	Sheet <b>1 of 7</b>	

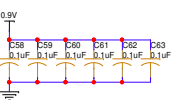
## FPGA POWER SUPPLY



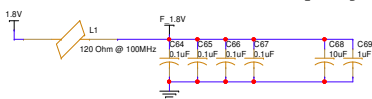
## VCC Decoupling



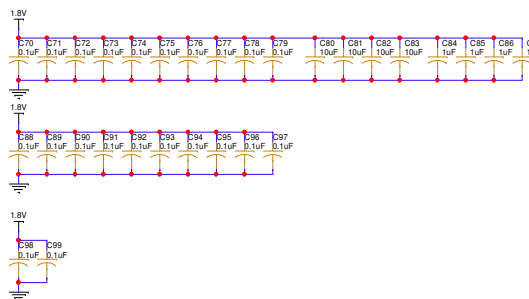
## VCCP and VCCERAM Decoupling



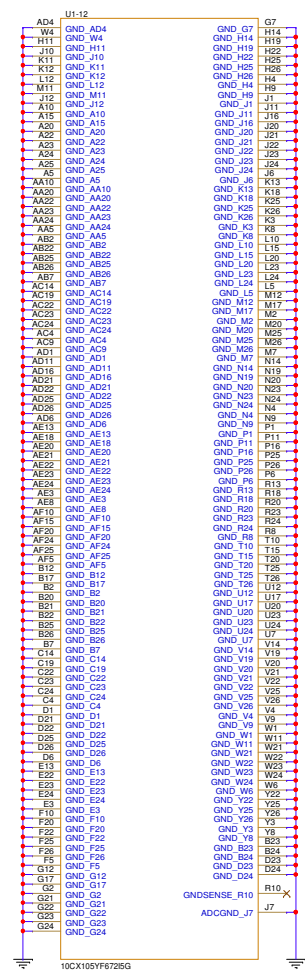
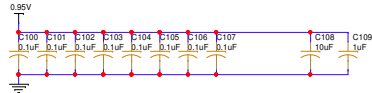
### VCCA\_PLL and VCCH\_GXBL Decoupling



## VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling



## VCCR/VCCT Decoupling



The image displays a complex PCB layout for an FPGA-based system. The layout is organized into several functional blocks:

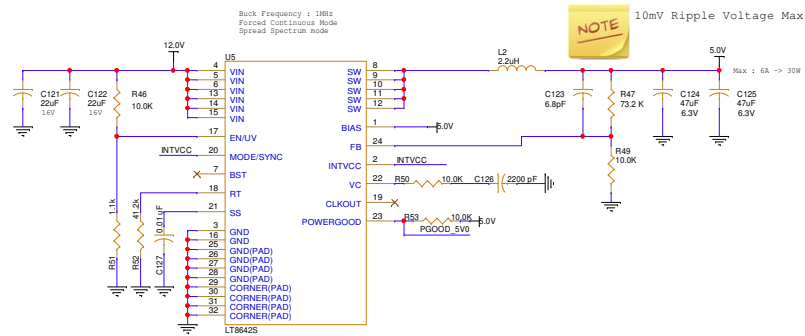
- Top Section:** Contains various signal traces and components, including resistors (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100) and capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100).
- FPGA FLASH CONFIGURATION:** A schematic diagram showing the connection of the FPGA to an EEPROM (U2) for configuration. It includes a 1.8V supply and a 10k resistor (R24).
- FPGA CONFIGURATION:** A schematic diagram showing the connection of the FPGA to an EEPROM (U2) for configuration. It includes a 1.8V supply and a 10k resistor (R24).
- CLOCKS:** A schematic diagram showing the connection of the FPGA to a clock source (U1) for configuration. It includes a 1.8V supply and a 10k resistor (R24).
- EEPROM WITH UNIQUE ID:** A schematic diagram showing the connection of the FPGA to an EEPROM (U2) for configuration. It includes a 1.8V supply and a 10k resistor (R24).
- JTAG:** A schematic diagram showing the connection of the FPGA to a JTAG interface (U1) for configuration. It includes a 1.8V supply and a 10k resistor (R24).

At the bottom right, there is a table with project information:

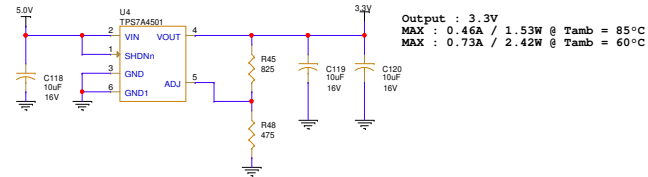
Title		
FPGA	Size	A2
Document Number	ART_CARD	Rev
Date	Thursday, April 15, 2021	2
File Name	ART_CARD	Sheet
		3 of 7

POWER NEED	:	FPGA	:	OCXO	:	Comp	:	TOTAL	
On 12V	:	:	:	7500	:	:	:	7500	mW
On 11V_ANA	:	:	:	:	:	80	:	80	mW
On 5.0V	:	:	:	:	:	350	:	350	mW
On 3.3V	:	:	:	:	:	243	:	243	mW
On 1.8V	:	1643	:	:	:	61	:	1704	mW
On 0.95V	:	762	:	:	:	:	:	762	mW
On 0.9V	:	2056	:	:	:	:	:	2056	mW
								-> 12695	mW

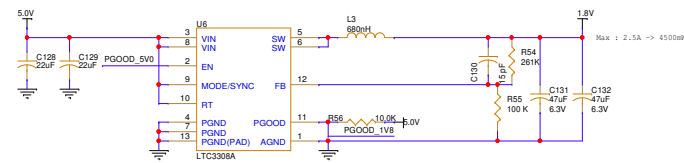
## 12V to 5V Switch Converter



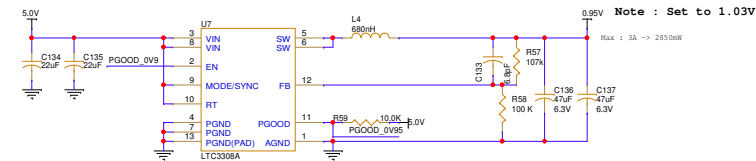
## 5V to 3.3V LDO Converter



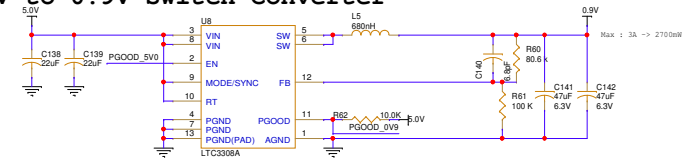
## 5V to 1.8V Switch Converter



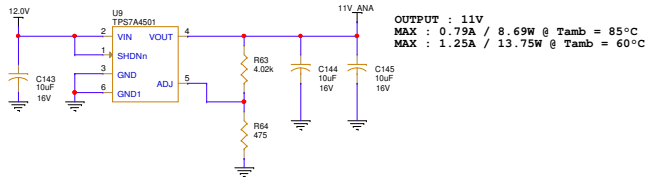
## 5V to 0.95V Switch Converter

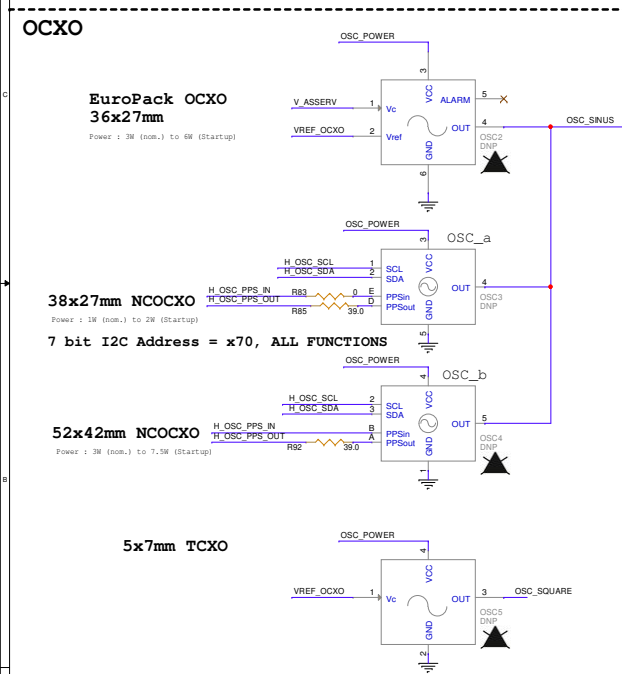


## 5V to 0.9V Switch Converter



## ANALOG POWER SUPPLY



[illegible][illegible]

**ATTENUATION=0.55**

**GAIN = 2**

OSC\_SQUARE R74 CNP 3.3Vp-p

R75 L10 1.8Vp-p

2.00K 15uH

C162 15 pF C163 15 pF

C160 0.1 uF

100K 100K

16V C158 10uF C159 0.1 uF

U13 OPA690  $f = 400kHz$

R79 221 100K

C165 0.1 uF

R81 221 C166 10 pF

OSC\_SINUS R82 0

The circuit diagram illustrates a square wave generator using an ADCMP601BKSZ comparator. The input signal, labeled OSC\_SINUS, is connected to a network of resistors (R90, R91, R95, R96) and capacitors (C170, C169, C168). A battery (BAT54S) is connected to the input. The comparator (U15) is configured with feedback resistors (R97, R98) and a hysteresis resistor (R94). The output (H\_CLK\_OUT) is shown as a square wave. The circuit is powered by a 3.3V supply.

Pin connection diagram for the UT18 DNP component:

- Pin 7: OSC\_POWER (connected to ground)
- Pin 1: V\_ASSERV
- Pin 2: H\_OSC\_PPS\_IN
- Pin 6: H\_OSC\_RX
- Pin 8: (connected to ground)
- Pin 4: GND
- Pin 5: SERIAL\_RX
- Pin 6: SERIAL\_TX
- Pin 7: BITE\_OUT
- Pin 12: OSC\_SQUARE
- Pin 10: H\_OSC\_PPS\_OUT
- Pin 11: H\_OSC\_TX
- Pin 9: H\_OSC\_BITE

The diagram shows a parallel LC resonant circuit. It begins with an inductor L11 (330 nH) in series with a capacitor C161 (680 pF). This is followed by a parallel combination of an inductor L12 (330 nH), a capacitor C164 (680 pF), and a resistor R80 (49.9 ohms). The output is labeled FREQ\_OUT.

The schematic diagram illustrates the power and clock management for the SN74LV1T34. The top section shows the power supply and clock input for the SN74LV1T34A (U14). The bottom section shows the clock output and power supply for the SN74LV1T34 (U16 and U17).

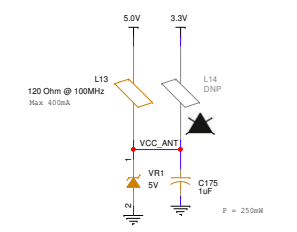
**Top Section: Power and Clock Input for U14**

- Power Supply:** The power supply is connected to the VCC pin (pin 1) of U14. The power supply is labeled "OSC\_POWER" and is connected to a 20.0 kΩ resistor (R84) and a 1.8V regulator (U18). The power supply is also connected to the GND pin (pin 20) of U14.
- Clock Input:** The clock input is connected to the Y1 pin (pin 18) of U14. The clock input is labeled "OSC\_PPS\_OUT" and is connected to a 20.0 kΩ resistor (R84) and a 1.8V regulator (U18). The clock input is also connected to the GND pin (pin 20) of U14.
- Other Pins:** The other pins of U14 are connected to the power supply and ground. The pins are labeled: A1, A2, A3, A4, A5, A6, A7, A8, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y24, Y25, Y26, Y27, Y28, Y29, Y30, Y31, Y32, Y33, Y34, Y35, Y36, Y37, Y38, Y39, Y40, Y41, Y42, Y43, Y44, Y45, Y46, Y47, Y48, Y49, Y50, Y51, Y52, Y53, Y54, Y55, Y56, Y57, Y58, Y59, Y60, Y61, Y62, Y63, Y64, Y65, Y66, Y67, Y68, Y69, Y70, Y71, Y72, Y73, Y74, Y75, Y76, Y77, Y78, Y79, Y80, Y81, Y82, Y83, Y84, Y85, Y86, Y87, Y88, Y89, Y90, Y91, Y92, Y93, Y94, Y95, Y96, Y97, Y98, Y99, Y100.

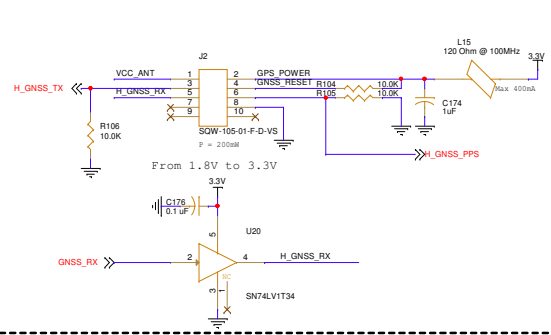
**Bottom Section: Clock Output and Power Supply for U16 and U17**

- Clock Output:** The clock output is connected to the Y1 pin (pin 18) of U16 and U17. The clock output is labeled "OSC\_PPS\_IN" and is connected to a 20.0 kΩ resistor (R84) and a 1.8V regulator (U18). The clock output is also connected to the GND pin (pin 20) of U16 and U17.
- Power Supply:** The power supply is connected to the VCC pin (pin 1) of U16 and U17. The power supply is labeled "OSC\_POWER" and is connected to a 20.0 kΩ resistor (R84) and a 1.8V regulator (U18). The power supply is also connected to the GND pin (pin 20) of U16 and U17.
- Other Pins:** The other pins of U16 and U17 are connected to the power supply and ground. The pins are labeled: A1, A2, A3, A4, A5, A6, A7, A8, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y24, Y25, Y26, Y27, Y28, Y29, Y30, Y31, Y32, Y33, Y34, Y35, Y36, Y37, Y38, Y39, Y40, Y41, Y42, Y43, Y44, Y45, Y46, Y47, Y48, Y49, Y50, Y51, Y52, Y53, Y54, Y55, Y56, Y57, Y58, Y59, Y60, Y61, Y62, Y63, Y64, Y65, Y66, Y67, Y68, Y69, Y70, Y71, Y72, Y73, Y74, Y75, Y76, Y77, Y78, Y79, Y80, Y81, Y82, Y83, Y84, Y85, Y86, Y87, Y88, Y89, Y90, Y91, Y92, Y93, Y94, Y95, Y96, Y97, Y98, Y99, Y100.

ANTENNA POWER SUPPLY



GNSS RECEIVER



GNSS STANDOFF

