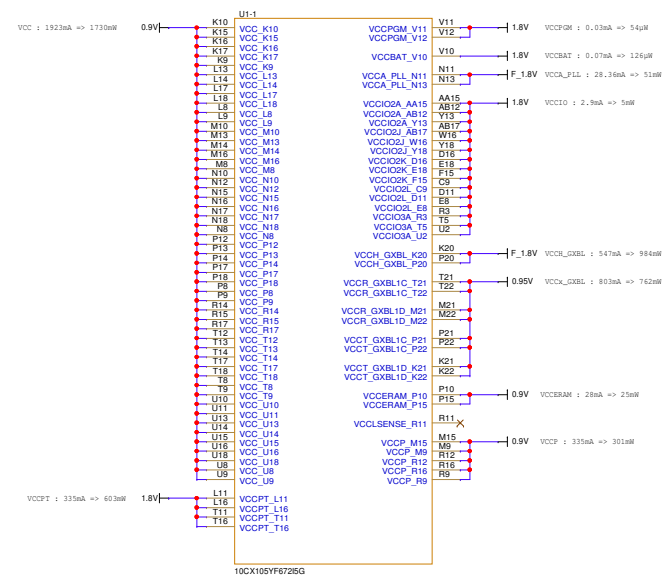
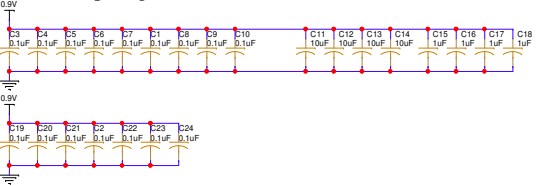


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Title			
OVERVIEW			
Size	Document Number		Rev
A2	ART_CARD		5
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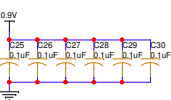
FPGA POWER SUPPLY



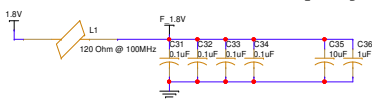
VCC Decoupling



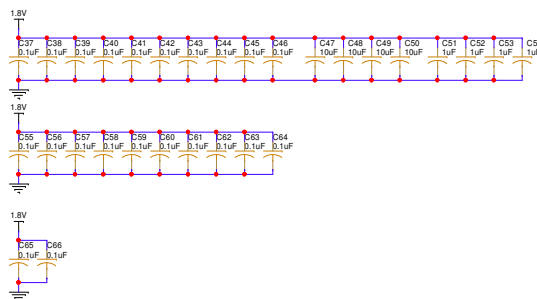
VCCP and VCCERAM Decoupling



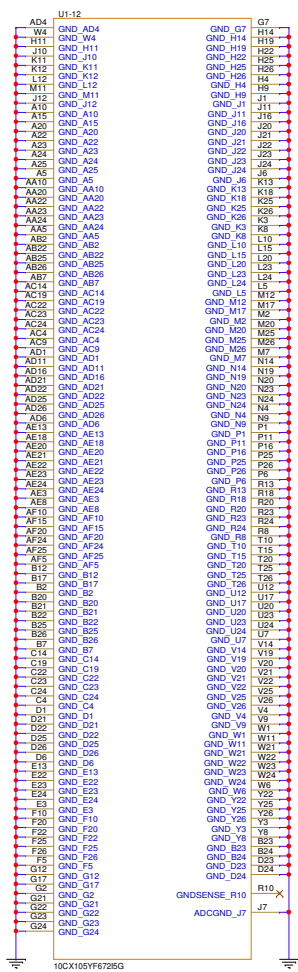
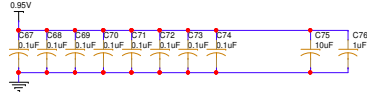
VCCA_PLL and VCCH_GXBL Decoupling



VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling



VCCR/VCCT Decoupling



Title			FPGA POWER		
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The diagram illustrates the hardware configuration of an FPGA-based system. It includes a large block of logic equations for the FPGA, a JTAG interface, a 24AA08HT EEPROM, a TSM102-01-F-SH flash, and various clock and power management components. The board is populated with a 10C105YF6725G FPGA, a 24AA08HT EEPROM, a TSM102-01-F-SH flash, and various passive components like resistors and capacitors. The diagram also shows the connection of the FPGA to a USB and a JTAG interface.

FPGA

DCLS_N1
DCLS_N0
SEL_I00
DCLS_N3
GNSS_RX
GNSS_TX
DCLS_N2
GNSS_PPS
FREQ_N
GNSS_RESET

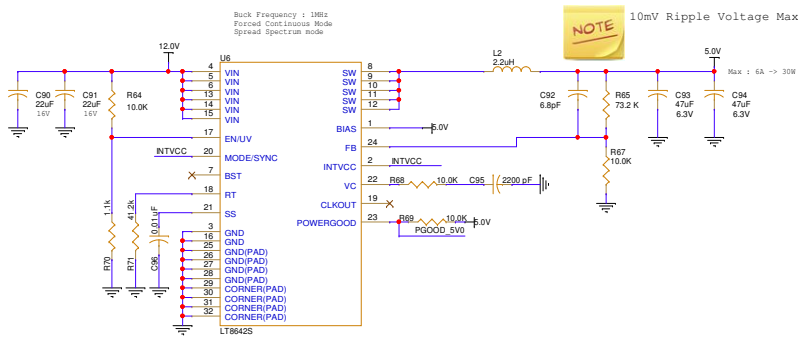
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IO_2A_45_AE50DATA1_VLDSS2A_1P0DQ24
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IO_2A_44_AE50DATA1_VLDSS2A_3P0DQ24
IO_2A_43_AE50DATA1_VLDSS2A_4N0DQ24
IO_2A_42_AE50DATA1_VLDSS2A_5P0DQ24
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IO_2A_37_AE50DATA1_VLDSS2A_10N0DQ24
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IO_2A_35_AE50DATA1_VLDSS2A_12N0DQ24
IO_2A_34_AE50DATA1_VLDSS2A_13P0DQ24
IO_2A_33_AE50DATA1_VLDSS2A_14N0DQ24
IO_2A_32_AE50DATA1_VLDSS2A_15P0DQ24
IO_2A_31_AE50DATA1_VLDSS2A_16N0DQ24
IO_2A_30_AE50DATA1_VLDSS2A_17P0DQ24
IO_2A_29_AE50DATA1_VLDSS2A_18N0DQ24
IO_2A_28_AE50DATA1_VLDSS2A_19P0DQ24
IO_2A_27_AE50DATA1_VLDSS2A_20N0DQ24
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IO_2A_17_AE50DATA1_VLDSS2A_30N0DQ24
IO_2A_16_AE50DATA1_VLDSS2A_31P0DQ24
IO_2A_15_AE50DATA1_VLDSS2A_32N0DQ24
IO_2A_14_AE50DATA1_VLDSS2A_33P0DQ24
IO_2A_13_AE50DATA1_VLDSS2A_34N0DQ24
IO_2A_12_AE50DATA1_VLDSS2A_35P0DQ24
IO_2A_11_AE50DATA1_VLDSS2A_36N0DQ24
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IO_2A_03_AE50DATA1_VLDSS2A_44N0DQ24
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IO_2K_27_H18VLDS2K_20N0DQ8
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IO_2K_08_H18VLDS2K_39P0DQ8
IO_2K_07_H18VLDS2K_40N0DQ8
IO_2K_06_H18VLDS2K_41P0DQ8
IO_2K_05_H18VLDS2K_42N0DQ8
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IO_2K_03_H18VLDS2K_44N0DQ8
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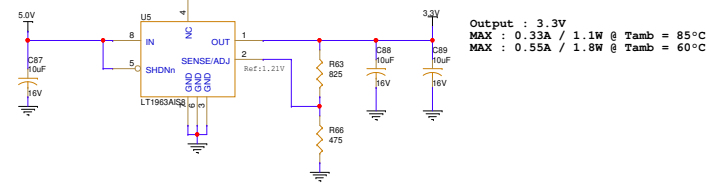
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IO_2J_32_W18VLDS2J_15P0DQ16
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IO_2J_30_W18VLDS2J_17P0DQ16
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IO_2J_07_W18VLDS2J_40N0DQ16
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IO_2J_05_W18VLDS2J_42N0DQ16
IO_2J_04_W18VLDS2J_43P0DQ16
IO_2J_03_W18VLDS2J_44N0DQ16
IO_2J_02_W18VLDS2J_45P0DQ16
IO_2J_01_W18VLDS2J_46N0

POWER NEED : FPGA : OCKO : Comp : TOTAL
on 12V : : : 7500 : : 7500 mW
on 11V_ANA : : : : 80 : 80 mW
on 5.0V : : : : 350 : 350 mW
on 3.3V : : : : 243 : 243 mW
on 1.8V : : : : 61 : 1704 mW
on 0.95V : : : : 762 : 762 mW
on 0.9V : : : : 2056 : 2056 mW
-> 12695 mW

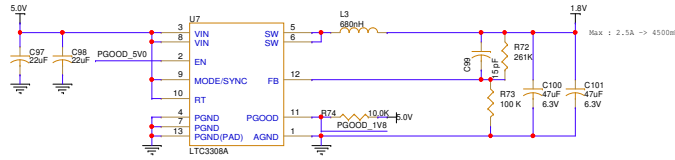
12V to 5V Switch Converter



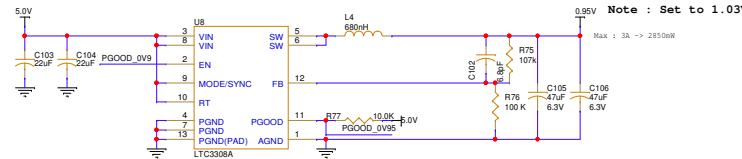
5V to 3.3V LDO Converter



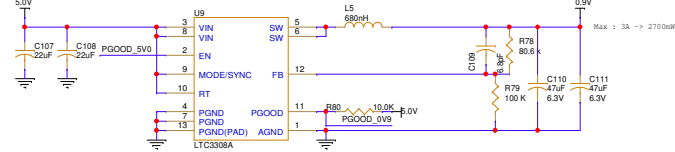
5V to 1.8V Switch Converter



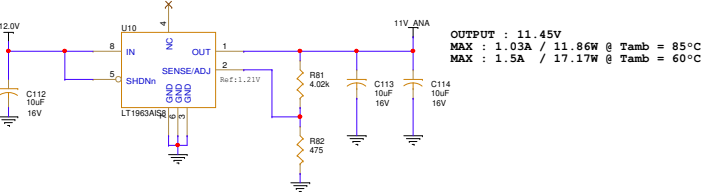
5V to 0.95V Switch Converter



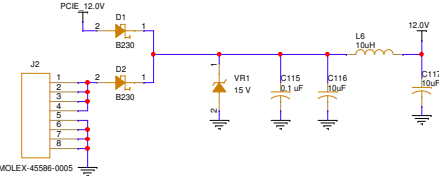
5V to 0.9V Switch Converter



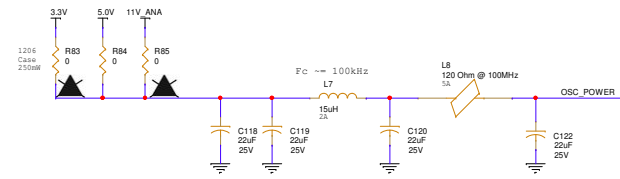
ANALOG POWER SUPPLY



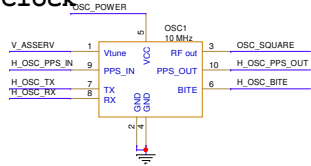
POWER CONNECTOR



OSCILLATOR POWER SUPPLY

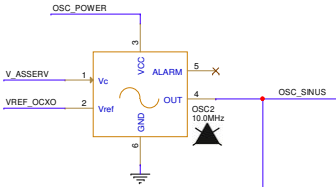


MiniRubidium
Miniature Atomic Clock

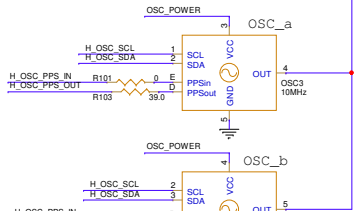


OCXO

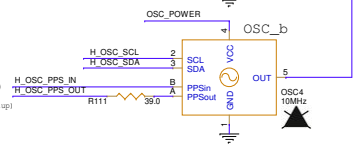
EuroPack OCXO
36x27mm
Power : 3W (nom.) to 6W (Startup)



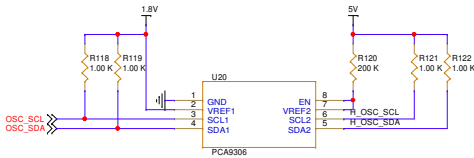
38x27mm NCOCXO
Power : 1W (nom.) to 2W (Startup)



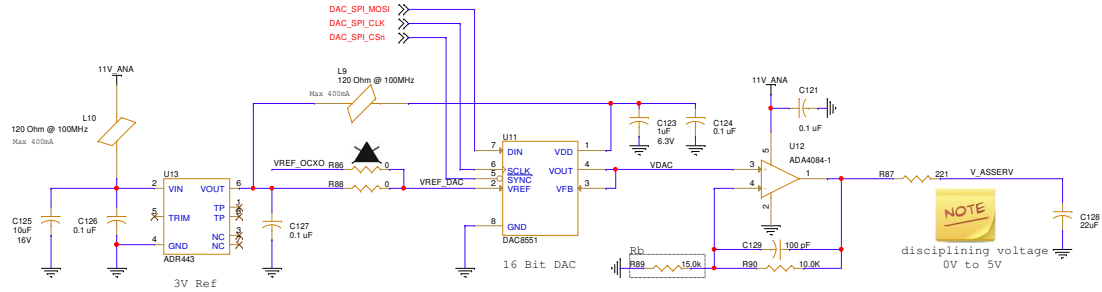
52x42mm NCOCXO
Power : 3W (nom.) to 7.5W (Startup)



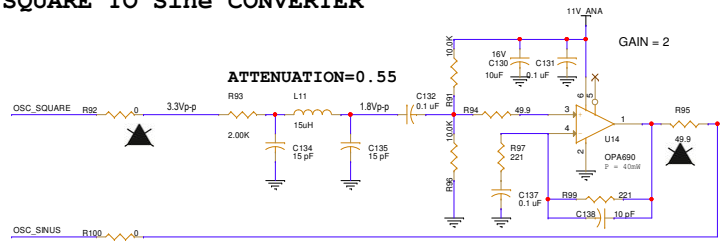
I2C VOLTAGE-LEVEL TRANSLATOR



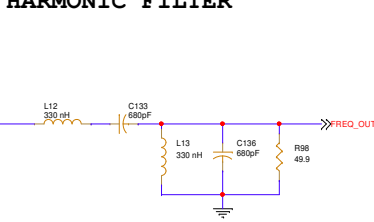
OSCILLATOR CONTROL VOLTAGE



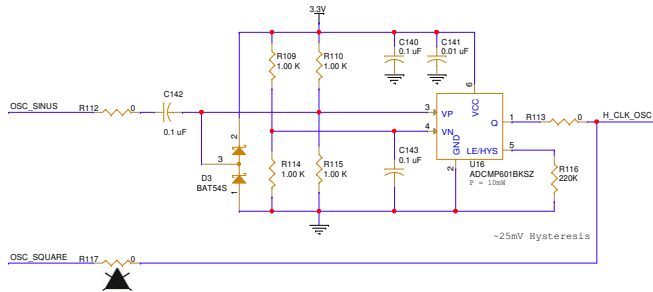
SQUARE TO Sine CONVERTER



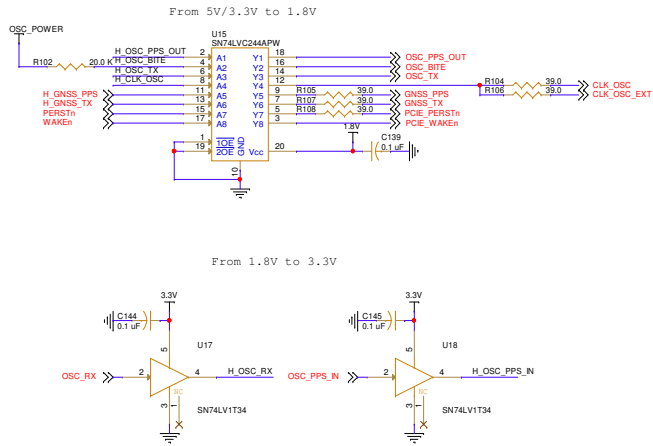
HARMONIC FILTER



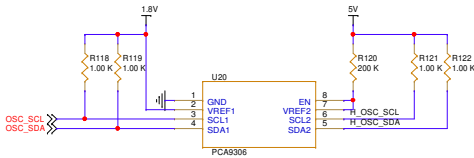
SINUS TO SQUARE CONVERTER



LOGIC VOLTAGE-LEVEL TRANSLATOR



I2C VOLTAGE-LEVEL TRANSLATOR



Chip Scale Atomic Clock

