FILE OROLIA
ART_CARD

Réf PCB : **ART_CARD Rev 4**

⇨	7	SHEETS OF ELECTRICAL SCHEMATICS
⇨	1	ASSEMBLY DRAWING TOP
⇨	1	ASSEMBLY DRAWING BOTTOM
⇨	1	SILKSCREEN TOP
⇨	1	SOLDER MASK TOP
⇨	1	COPPER LAYER TOP
⇨	1	COPPER LAYER INNER 1
⇨	1	COPPER LAYER INNER 2
⇨	1	COPPER LAYER INNER 3
⇨	1	COPPER LAYER INNER 4
⇨	1	COPPER LAYER INNER 5
⇨	1	COPPER LAYER INNER 6
⇨	1	COPPER LAYER BOTTOM
⇨	1	SOLDER MASK BOTOM
⇨	1	SILKSCREEN BOTTOM
⇨	1	DRILL DRAWING
⇨	1	CIRCUIT BOARD SPECIFICATION

Artémis CAO ELECTRONIQUE

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49070 BEAUCOUZÉ
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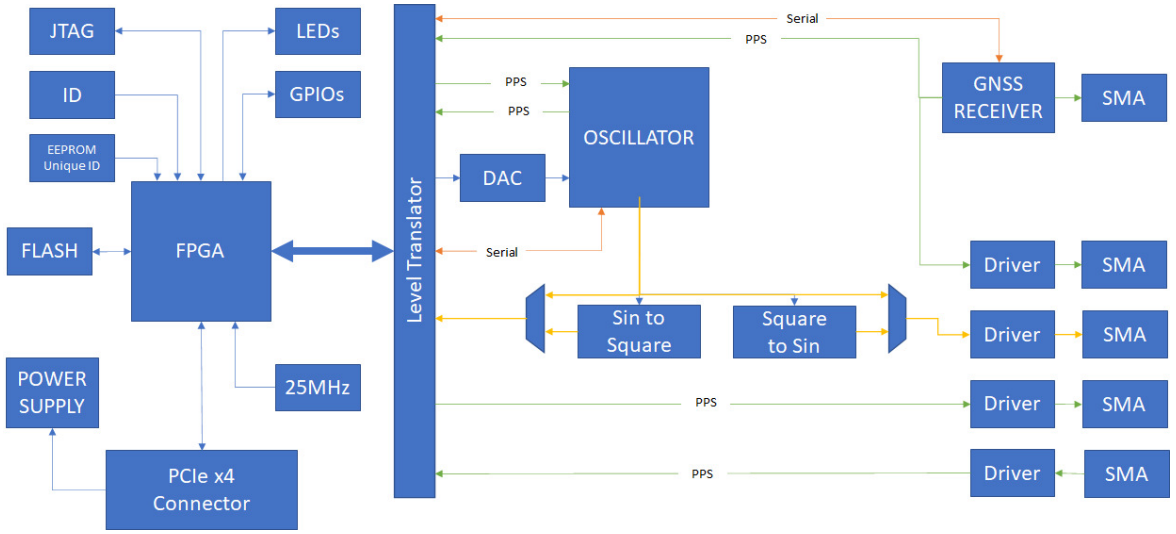

<Core Design>

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Title: OVERVIEW		
Size: A2	Document Number: ART_CARD	Rev: 4
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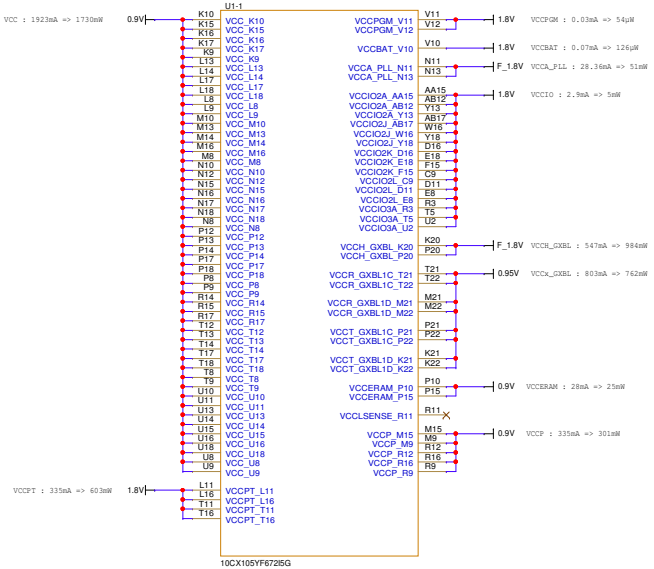
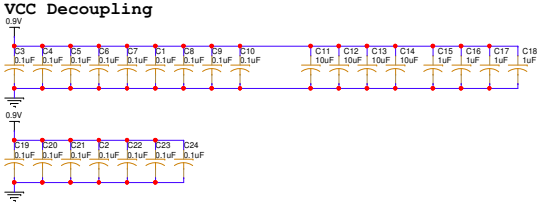
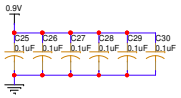
FPGA POWER SUPPLY



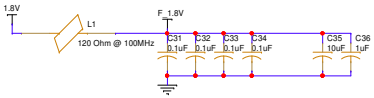
VCC Decoupling



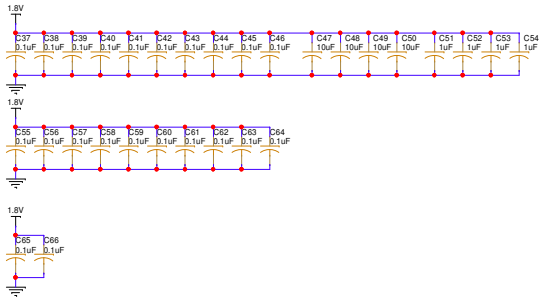
VCCP and VCCERAM Decoupling



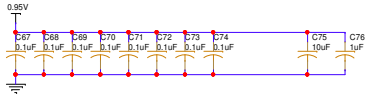
VCCA_PLL and VCCH_GXBL Decoupling

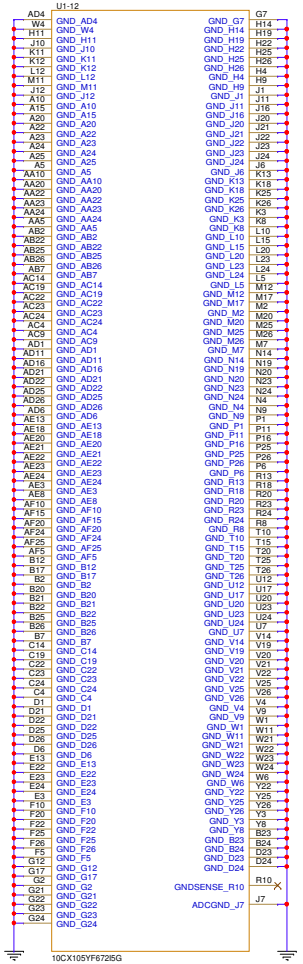


VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling



VCCR/VCCT Decoupling





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Size: A2	Document Number: ART_CARD	Rev: 4
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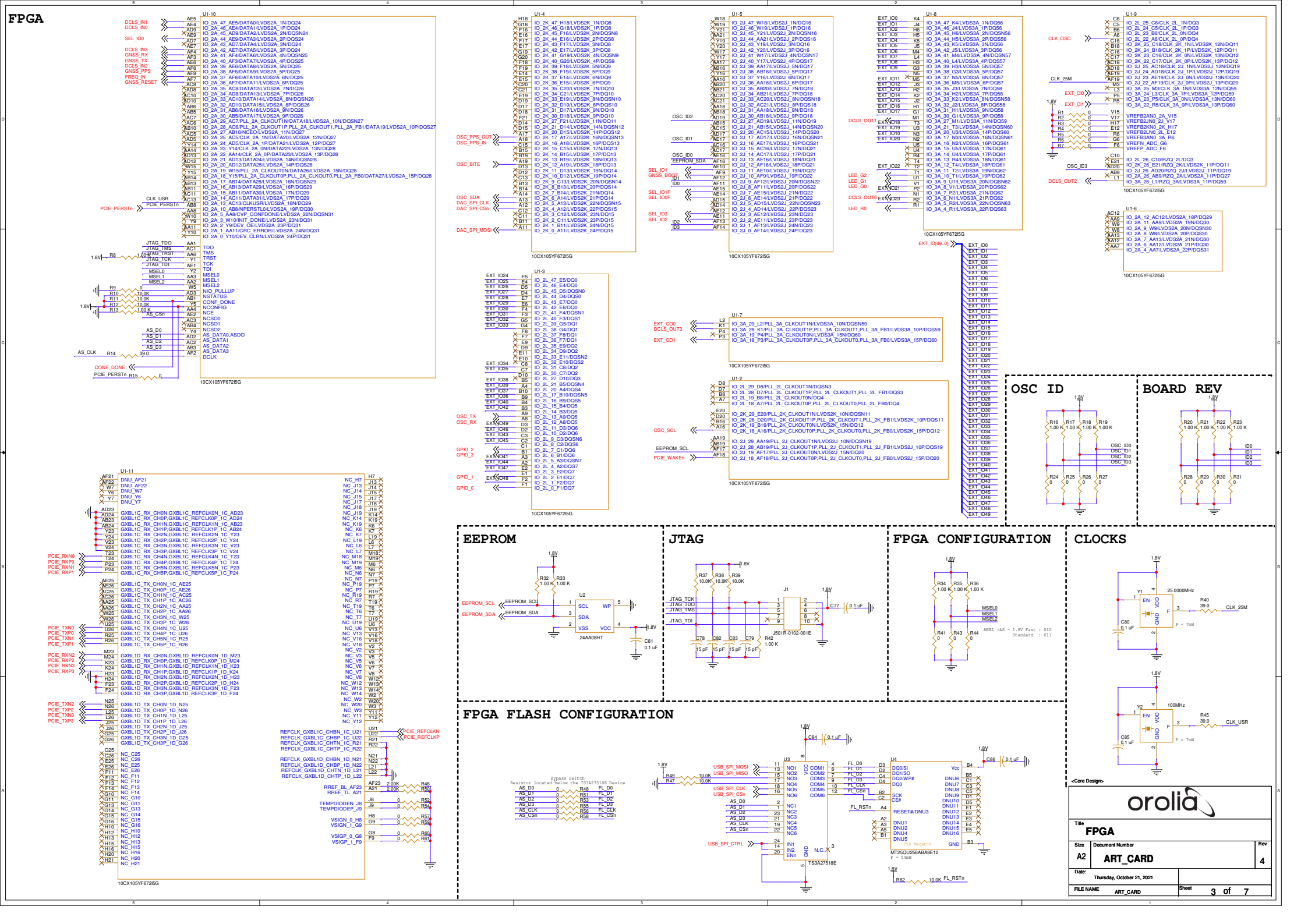
FPGA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U1-9
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U1-6
10CX105YF672I5G
U1-3
10CX105YF672I5G
U1-7
10CX105YF672I5G
U1-2
10CX105YF672I5G
U1-11
10CX105YF672I5G
OSC ID
BOARD REV
EEPROM
JTAG
FPGA CONFIGURATION
CLOCKS
FPGA FLASH CONFIGURATION
24AA08HT
J501R-0102-001E
MT25QU256ABA8E12
TS3A27518E
Bypass Switch
Resistor located below the TS3A27518E Device
MSEL :AS - 1.8V Fast : 010
Standard : 011
<Core Design>
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Title
FPGA
Size
A2
Document Number
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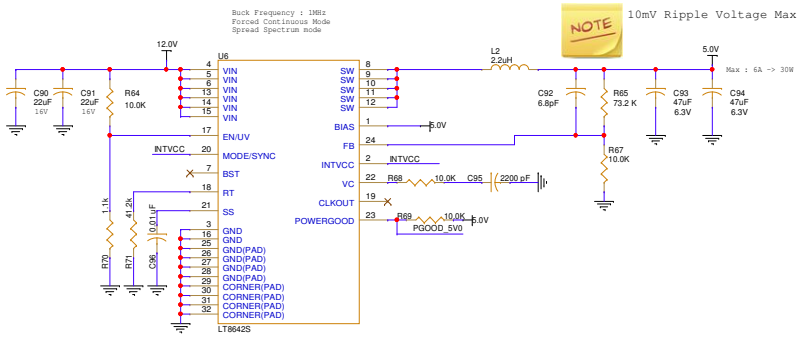
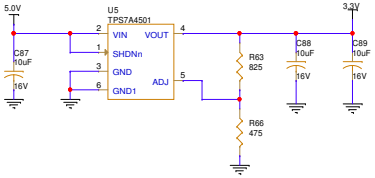
```
POWER NEED  : FPGA : OCXO : Comp : TOTAL
on 12V      :      : 7500 :      : 7500 mW
On 11V_ANA  :      :      :   80 :   80 mW
On 5.0V     :      :      :  350 :  350 mW
On 3.3V     :      :      :  243 :  243 mW
On 1.8V     : 1643 :      :   61 : 1704 mW
On 0.95V    :  762 :      :      :  762 mW
On 0.9V     : 2056 :      :      : 2056 mW
                                  -> 12695 mW
```

12V to 5V Switch Converter

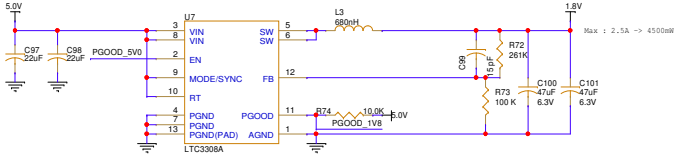


5V to 3.3V LDO Converter

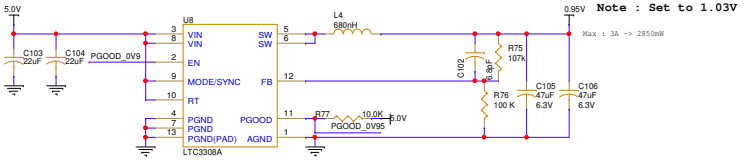


Output : 3.3V
MAX : 0.46A / 1.53W @ Tamb = 85°C
MAX : 0.73A / 2.42W @ Tamb = 60°C

5V to 1.8V Switch Converter

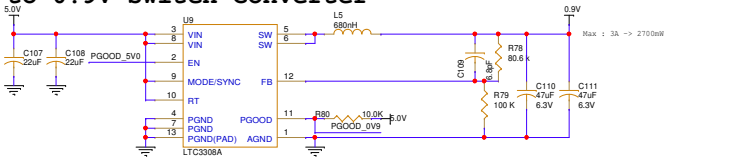


5V to 0.95V Switch Converter

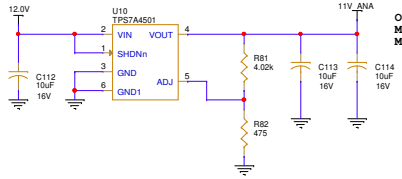


Note : Set to 1.03V

5V to 0.9V Switch Converter

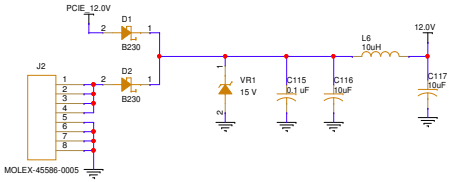


ANALOG POWER SUPPLY



OUTPUT : 11V
MAX : 0.79A / 8.69W @ Tamb = 85°C
MAX : 1.25A / 13.75W @ Tamb = 60°C

POWER CONNECTOR



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Title: POWER SUPPLY		
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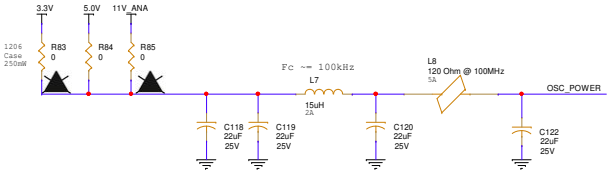
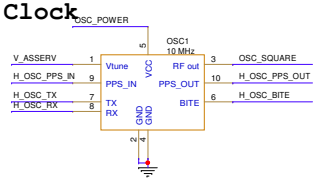
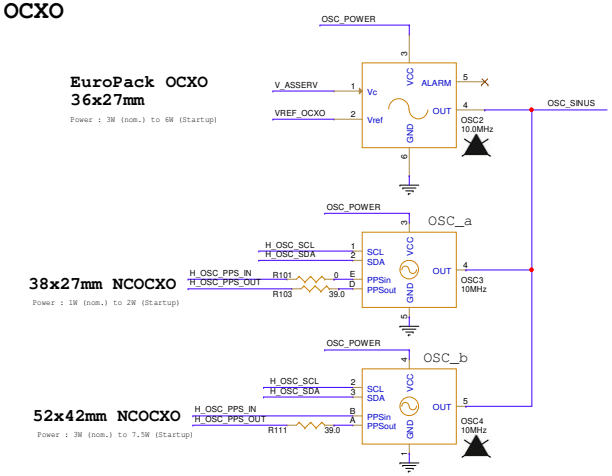
OSCILLATOR POWER SUPPLY



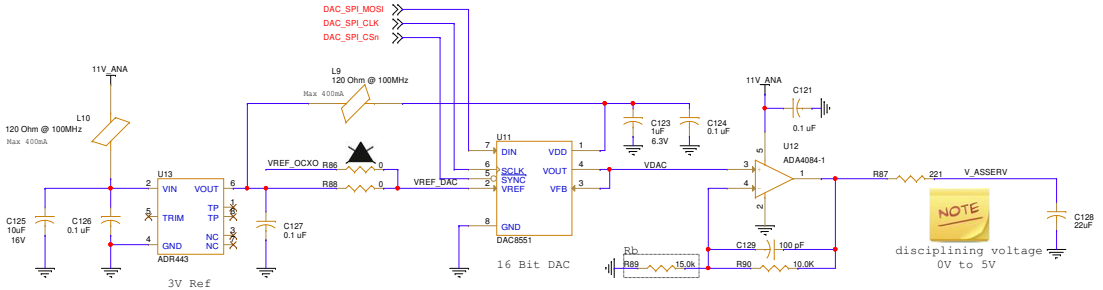
MiniRubidium
Miniature Atomic Clock



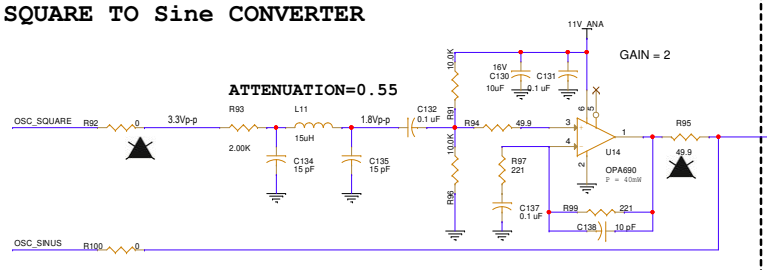
OCXO



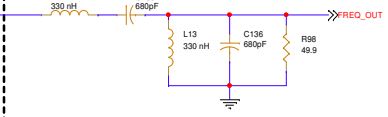
OSCILLATOR CONTROL VOLTAGE



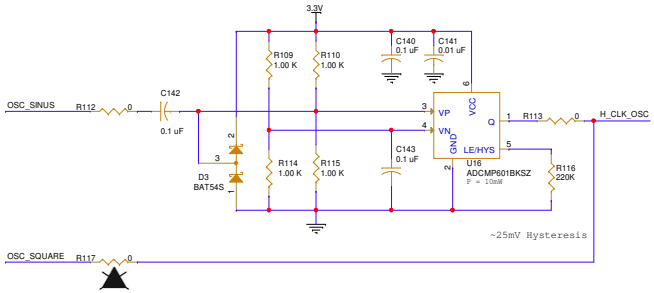
SQUARE TO Sine CONVERTER



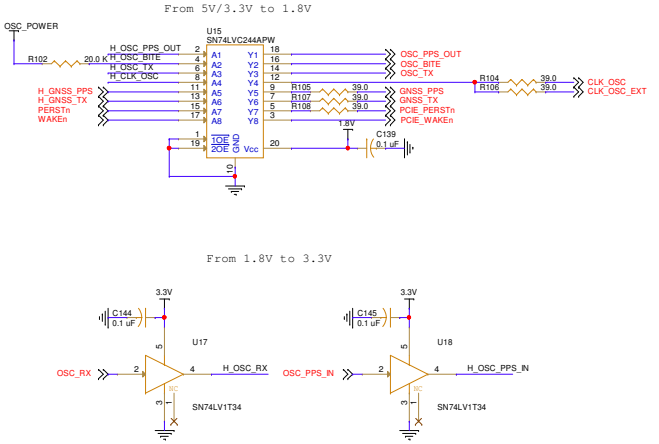
HARMONIC FILTER



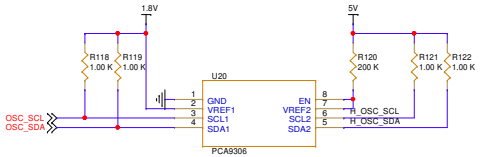
SINUS TO SQUARE CONVERTER



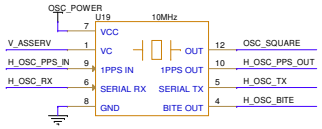
LOGIC VOLTAGE-LEVEL TRANSLATOR



I2C VOLTAGE-LEVEL TRANSLATOR



Chip Scale Atomic Clock



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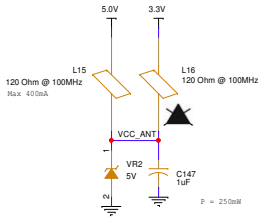
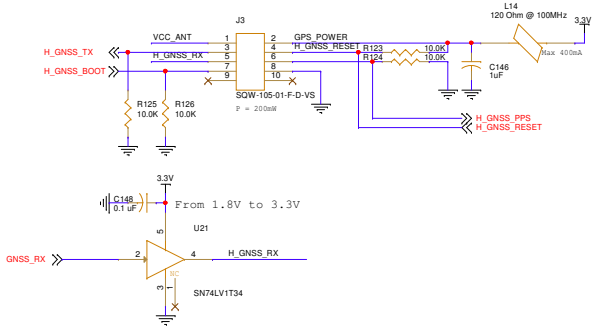
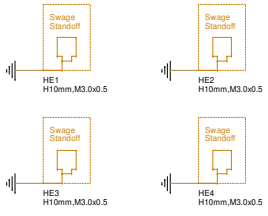
ANTENNA POWER SUPPLY



GNSS RECEIVER

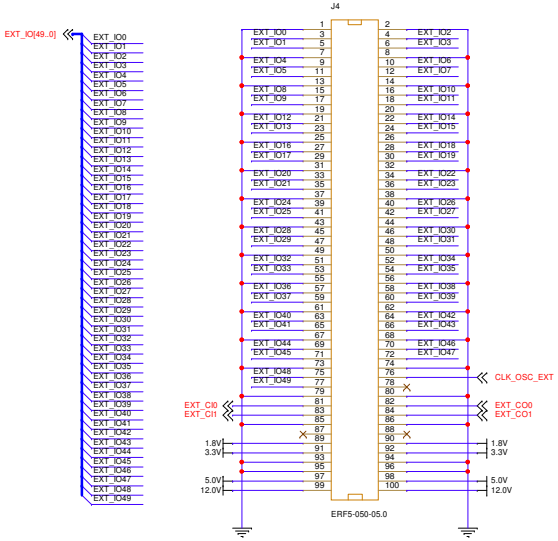


GNSS STANDOFF



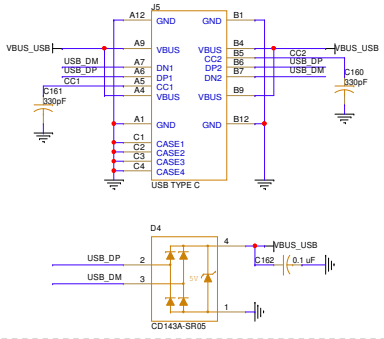
BRACKET HOLES

EXTENSION CONNECTOR

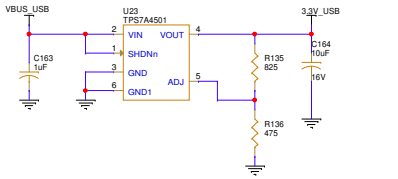


USB-C CONNECTOR

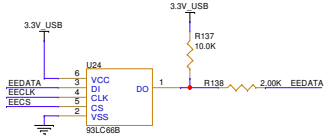
Support USB2.0



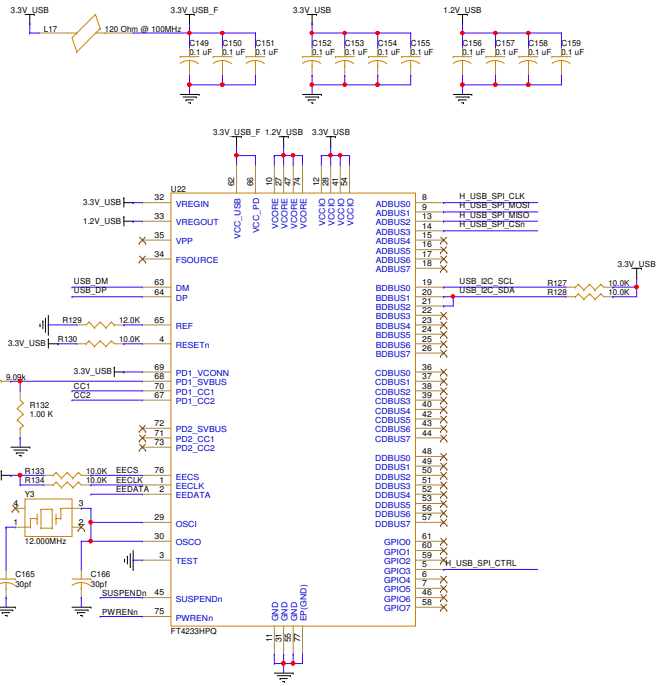
USB SELF-POWERED



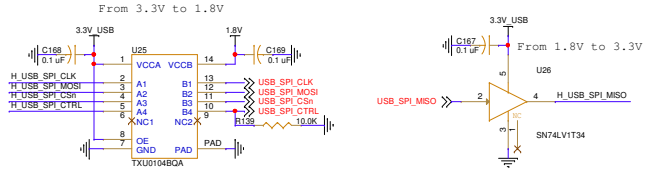
EEPROM FTDI



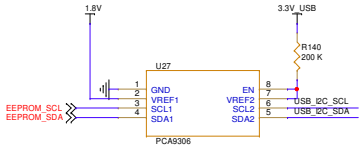
EEPROM FTDI



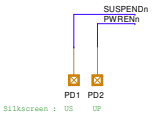
SPI VOLTAGE-LEVEL TRANSLATOR



I2C VOLTAGE-LEVEL TRANSLATOR



TEST POINTS



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Title: GNSS - EXTENSION

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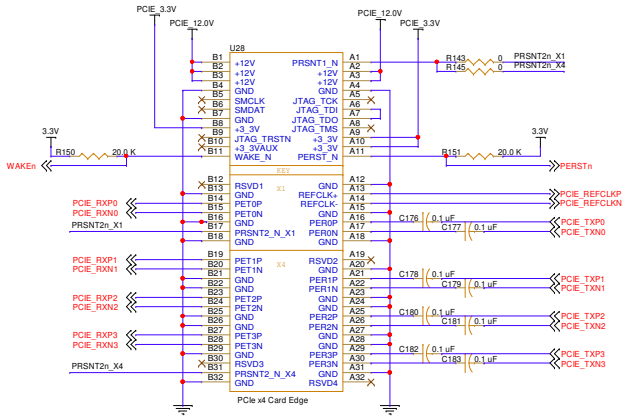
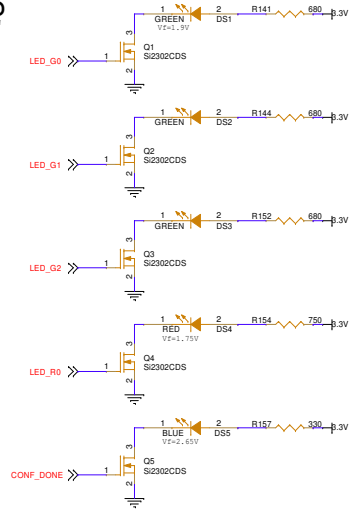
PCIe CONNECTOR



LED



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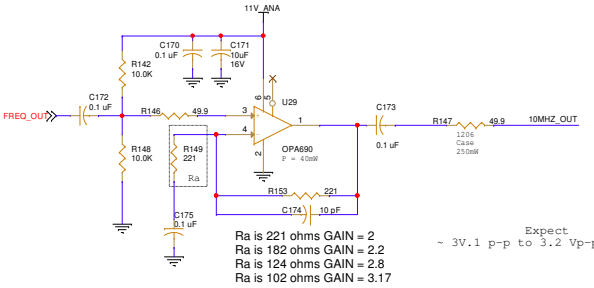

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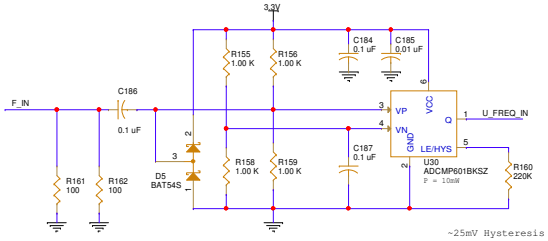
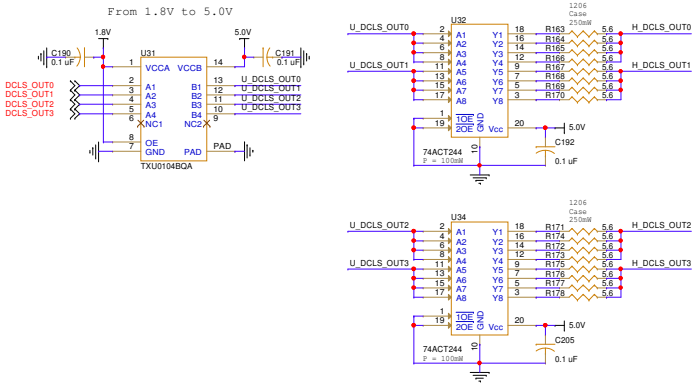
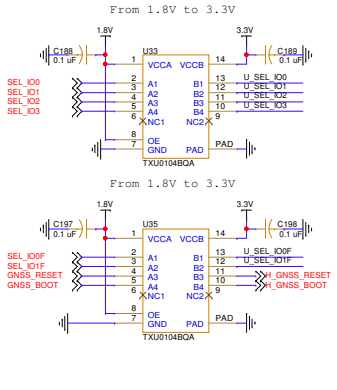
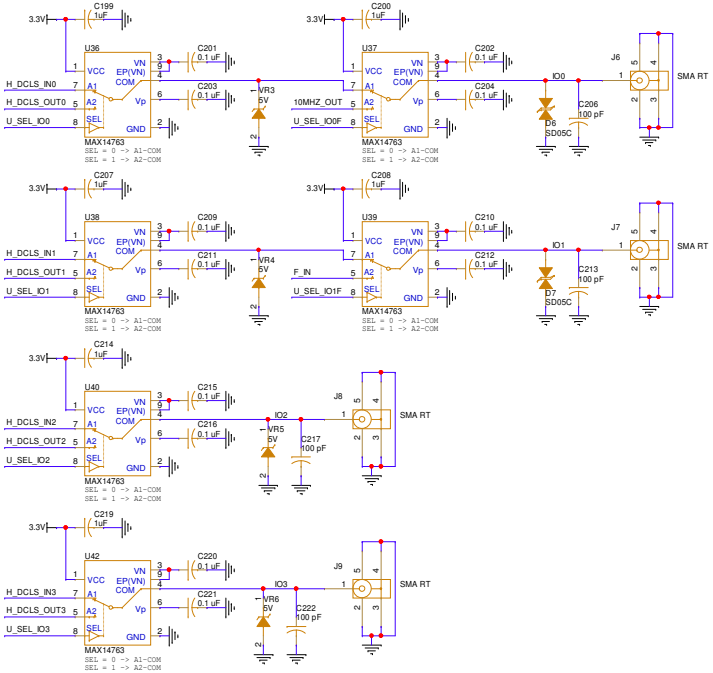


DCLS OUTPUT DRIVER

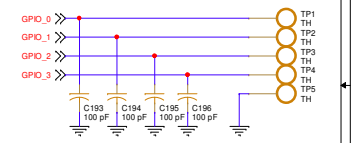




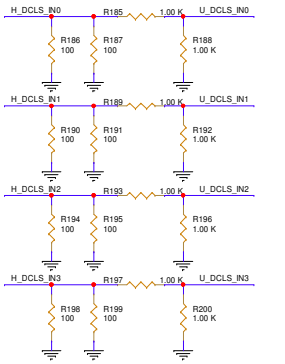
IO CONNECTORS / SWITCH

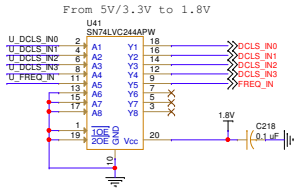


GPIO

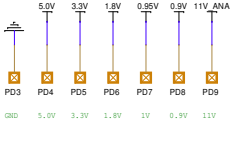


DCLS INPUT DRIVER





TEST POINTS



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Title	CONNECTORS	
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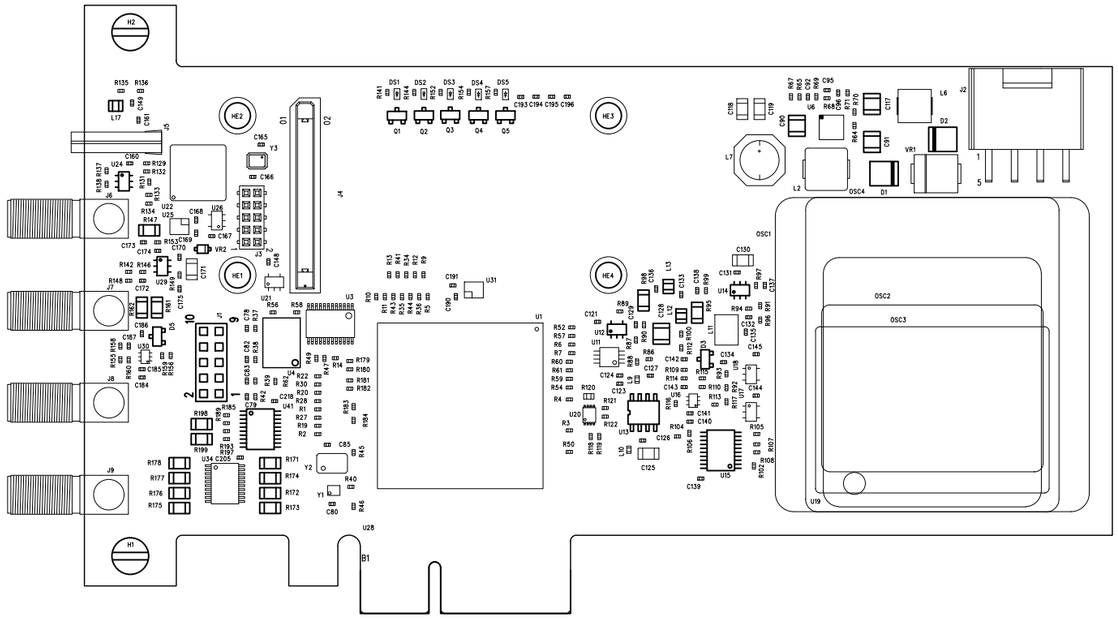
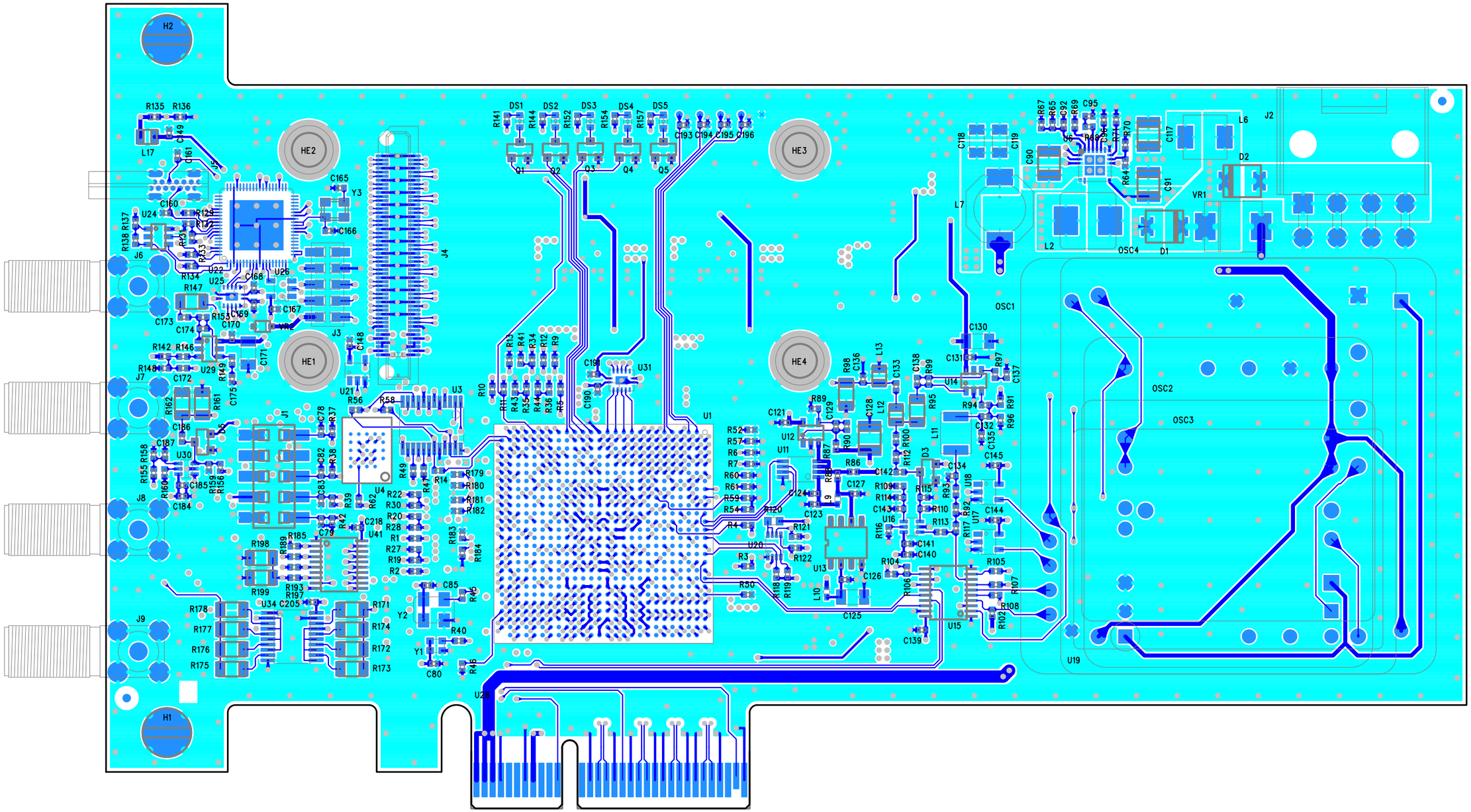
Rev	DESCRIPTION	DATE	APPROVED
1			



UNLESS OTHERWISE SPECIFIED:		NAME	DATE	OROLIA FRANCE
	DRAWN	H ECHELARD	17/11/2021	PART NUMBER: ART_CARD_PCB
	THE INFORMATION CONTAINED IN THIS DOCUMENT IS THE SOLE PROPERTY OF OROLIA. ANY REPRODUCTION, DISCLOSURE OR MANUFATURE OF THIS INFORMATION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF OROLIA GROUP IS PROHIBITED.			TITLE: ART_CARD
MATERIAL: PCB	CHANGE RESTRICTED NO MANUAL CHANGES			SIZE A3 / DWG. NO. ART_CARD_PCB / REV 4
FINISH	THIRD ANGLE PROJECTION			SCALE: 1:1 / DO NOT SCALE / SHEET 1 OF 1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HE1
HE2
HE3
HE4
DS1
DS2
DS3
DS4
DS5
Q1
Q2
Q3
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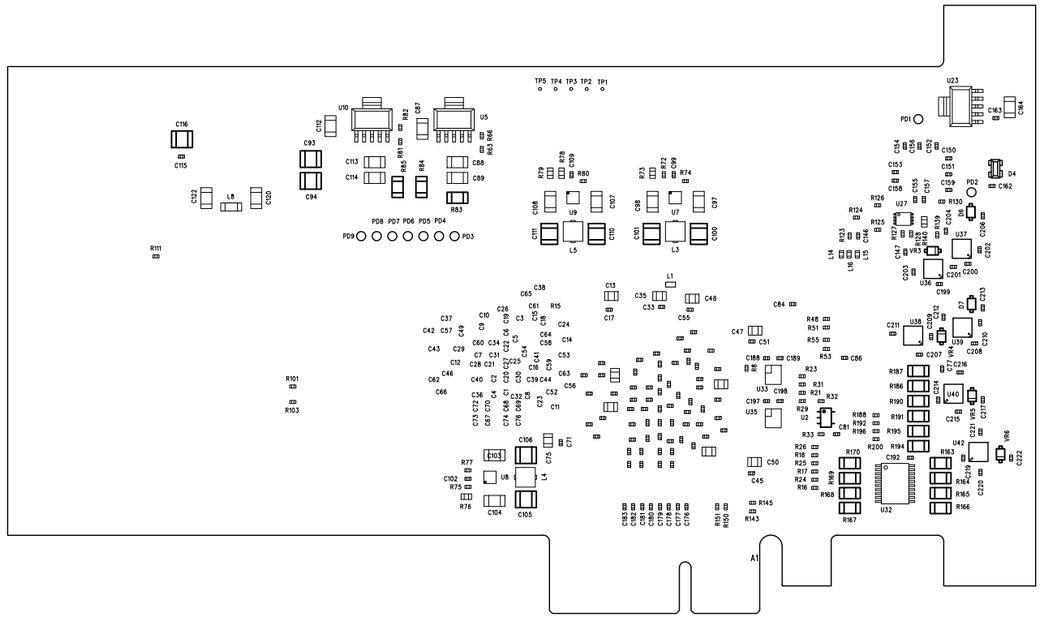
Q5
U1
U2
U3
U4
U11
U12
U13
U14
U15
U16
U19
U20
U21
U22
U24
U25
U26
U28
U29
U30
U31
U34
U41
J1
J2
J3
J4
J5
J6
J7
J8
J9
L2
L6
L7
D1
D2
D3
VR1
VR2
OSC1
OSC2
OSC3
OSC4
Y1
Y2
Y3

Rev	DESCRIPTION	DATE	APPROVED
1			



UNLESS OTHERWISE SPECIFIED:		NAME	DATE
	DRAWN	H ECHELARD	17/11/2021
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MATERIAL: PCB	CHANGE RESTRICTED NO MANUAL CHANGES		
FINISH	THIRD ANGLE PROJECTION		

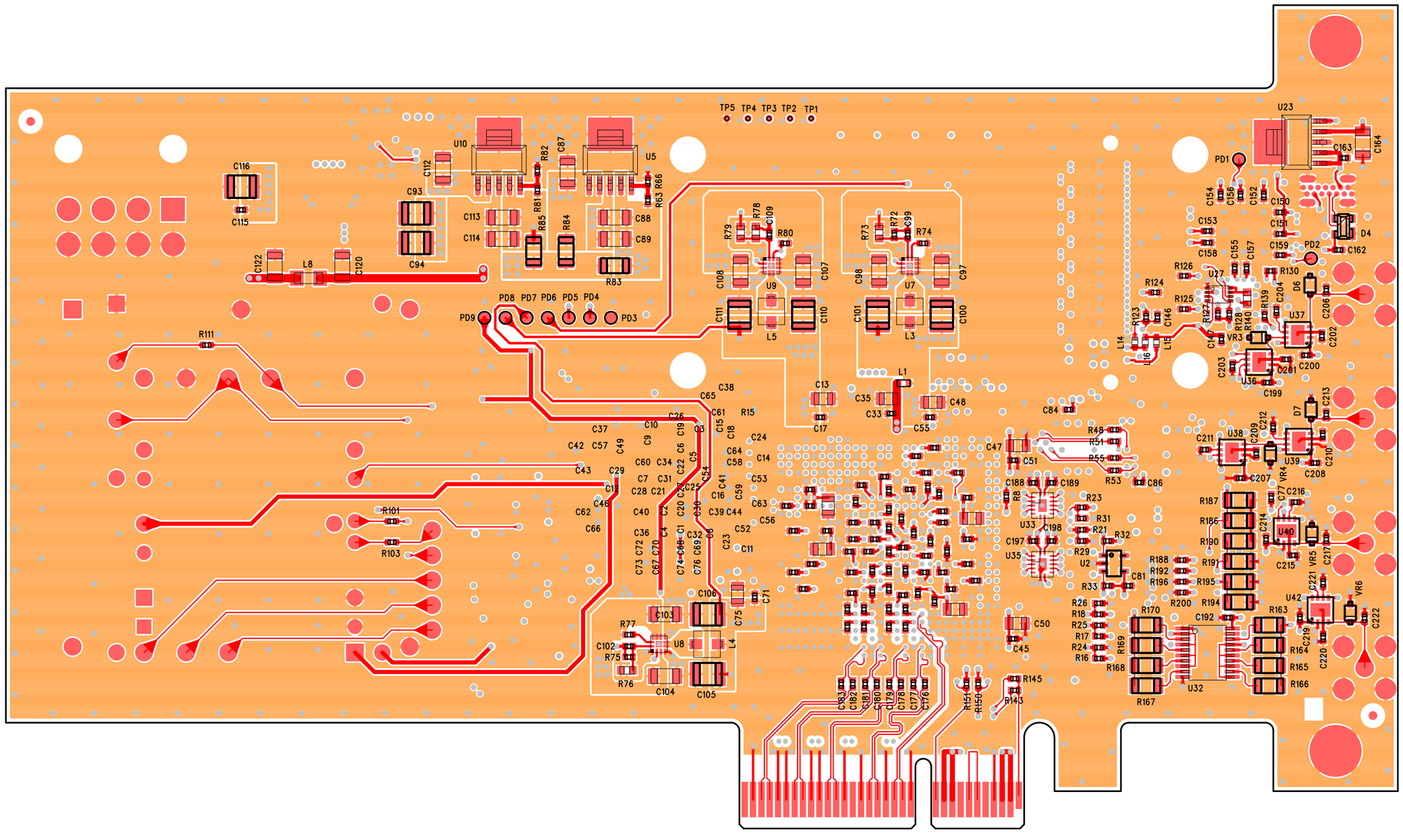
OROLIA FRANCE

PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

SIZE A3 | DWG. NO. ART_CARD_PCB | REV 4

SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1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U10
U5
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C115
C112
C93
C94
C113
C114
R82
C87
R81
R85
R84
C88
C89
R83
R63 R66
C122
L8
C120
PD9
PD8 PD7 PD6 PD5 PD4
PD3
R111
R101
R103
C38
C65
C61
R15
C26
C10
C19
C3
C15
C18
C24
C37
C42 C57 C49
C9
C64
C58
C14
C60 C34
C22 C6 C5
C54
C43
C29
C12
C7 C31
C28 C21
C25
C41
C16
C59
C53
C63
C62
C46
C40
C2
C20 C27
C30
C39 C44
C56
C66
C36
C4
C1
C32
C6
C23
C52
C11
C73 C72
C67 C70
C74 C68
C76 C69
C71
C106
C103
C75
R77
C102
R75
U8
L4
R76
C104
C105
C13
C17
C35
C33
L1
C48
C55
C47
C51
C84
R48
R51
R55
R53
C86
C188
C189
R8
U33
C198
C197
U35
R23
R31
R21
R32
R29
U2
R33
C81
R26
R18
R25
R17
R24
R16
C50
C45
R145
R143
R151
R150
C183
C182
C181
C180
C179
C178
C177
C176
R79
R78
C109
R80
C108
C107
U9
C111
C110
L5
R73
R72
C99
R74
C98
C97
U7
C101
C100
L3
U23
PD1
C163
C164
C154
C156
C152
C150
C153
C151
C158
C155
C157
C159
PD2
C162
D4
R126
R124
R125
R123
C146
L14
L15
L16
U27
R127
R128
R140
R139
C204
D6
R130
VR3
U37
C206
C202
C203
U36
C201
C200
C199
D7
C213
C211
U38
C209
C212
U39
C210
C208
C207
VR4
C77
C216
R187
R186
R190
U40
C214
C215
VR5
C217
R188
R192
R196
R191
R195
R200
R194
R170
C192
R169
R168
R167
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C221
U42
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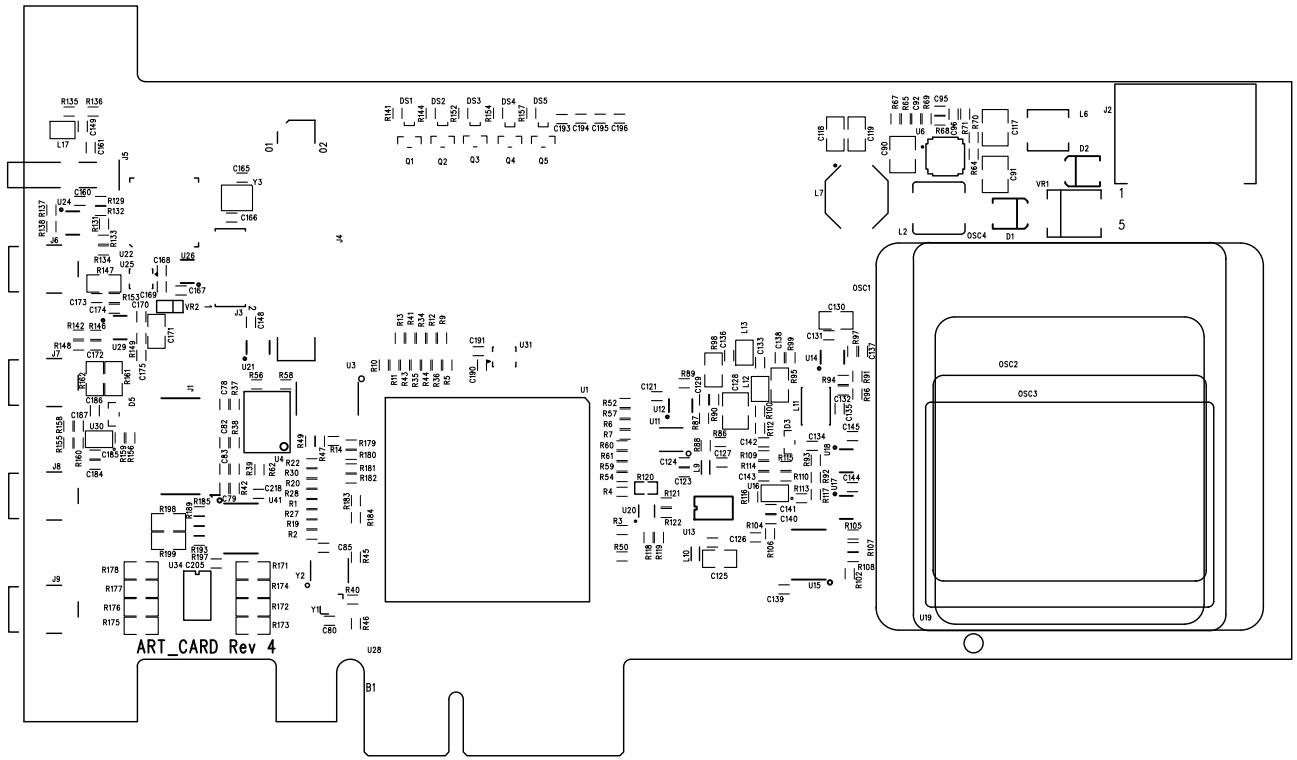
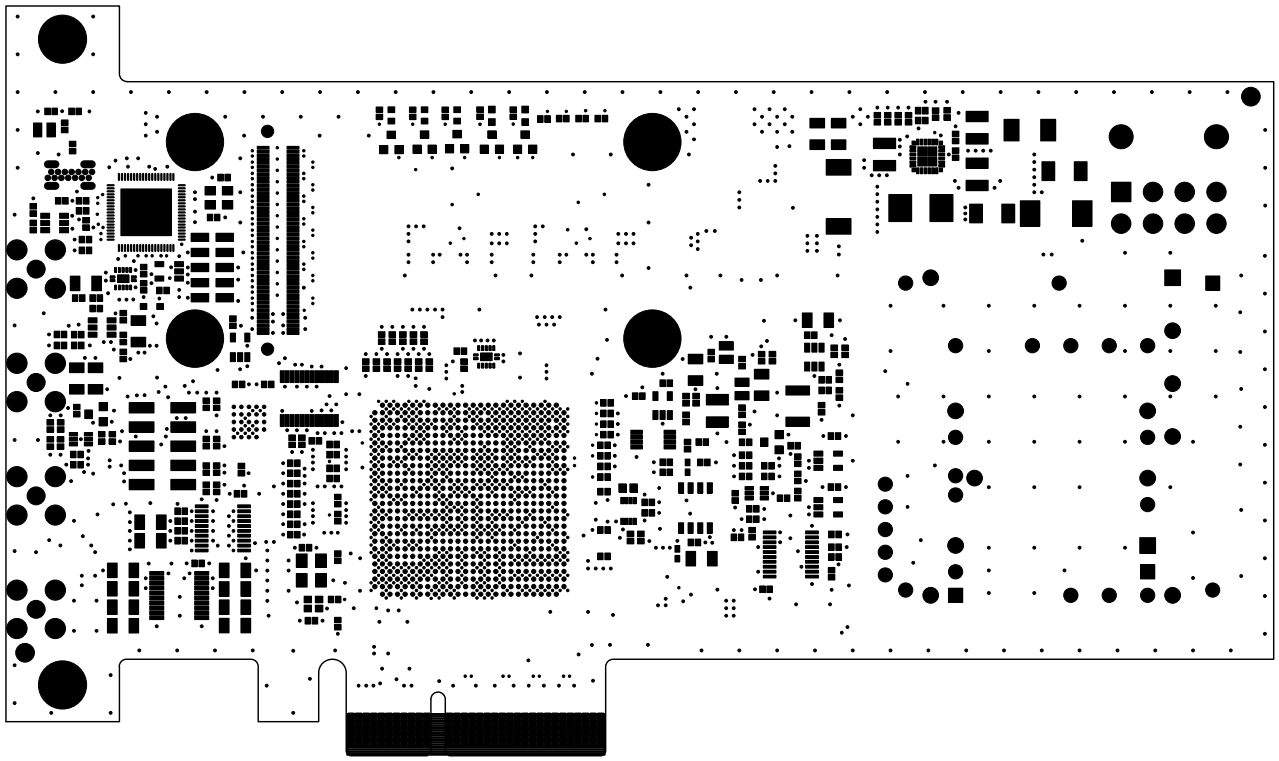
R163
R164
R165
R166
C219
C220
C222



FILM: SERIGRAPHIE COMPOSANT	ARTEMIS
DOSSIER: ART_CARD Rev 4	17/11/21



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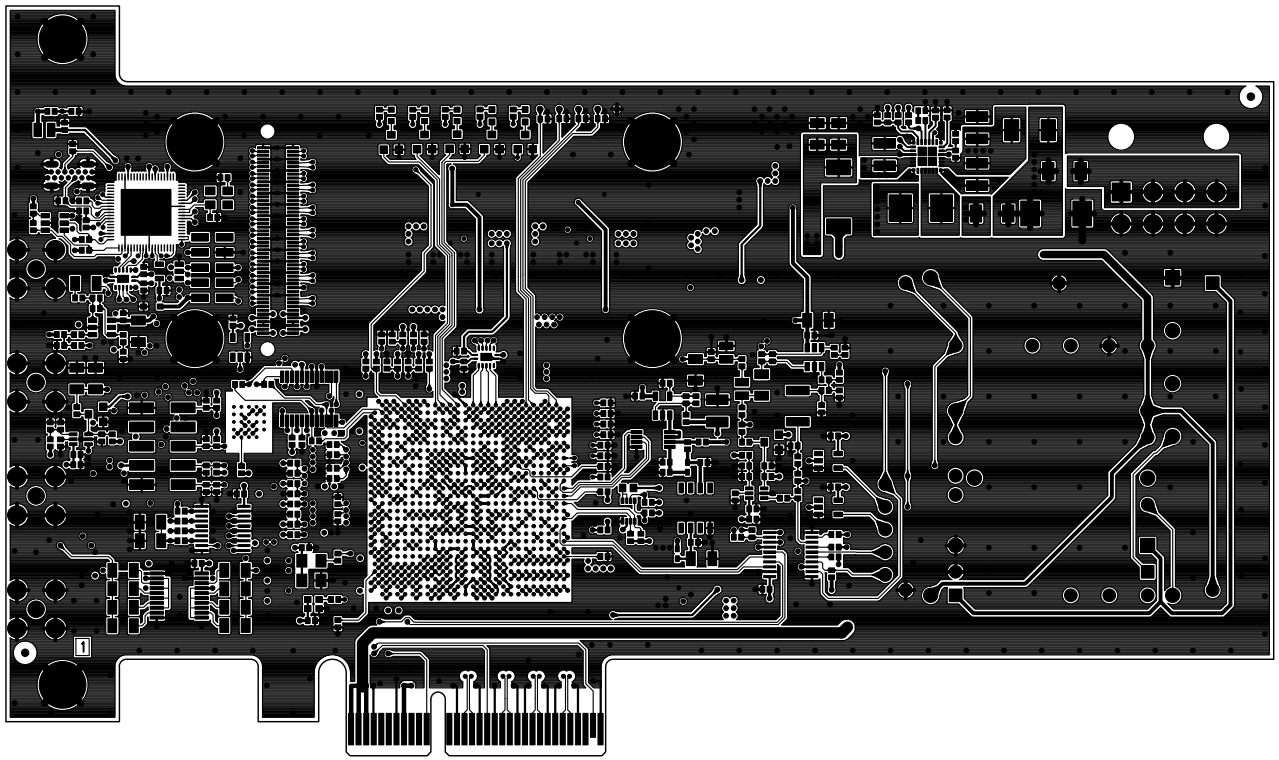
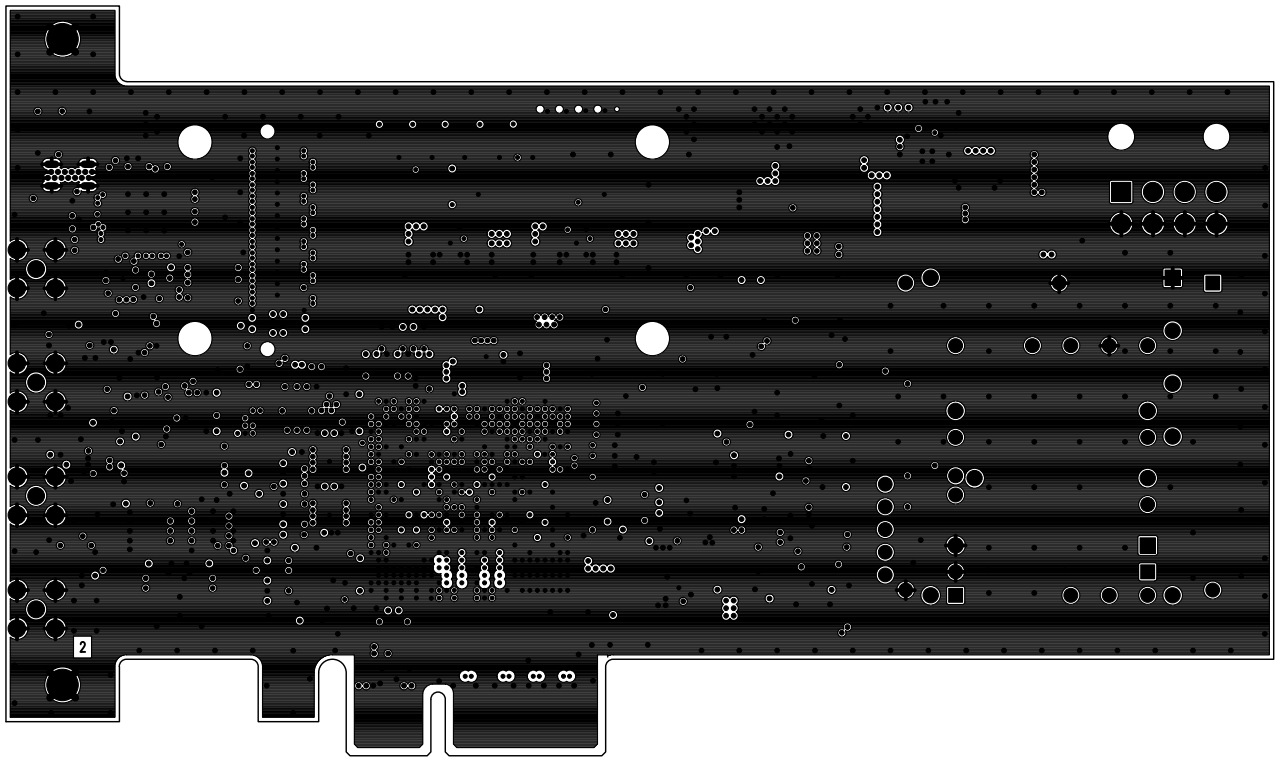
DOSSIER: ART_CARD Rev 4	17/11/21



FILM: COMPOSANT	ARTEMIS
DOSSIER: ART_CARD Rev 4	17/11/21



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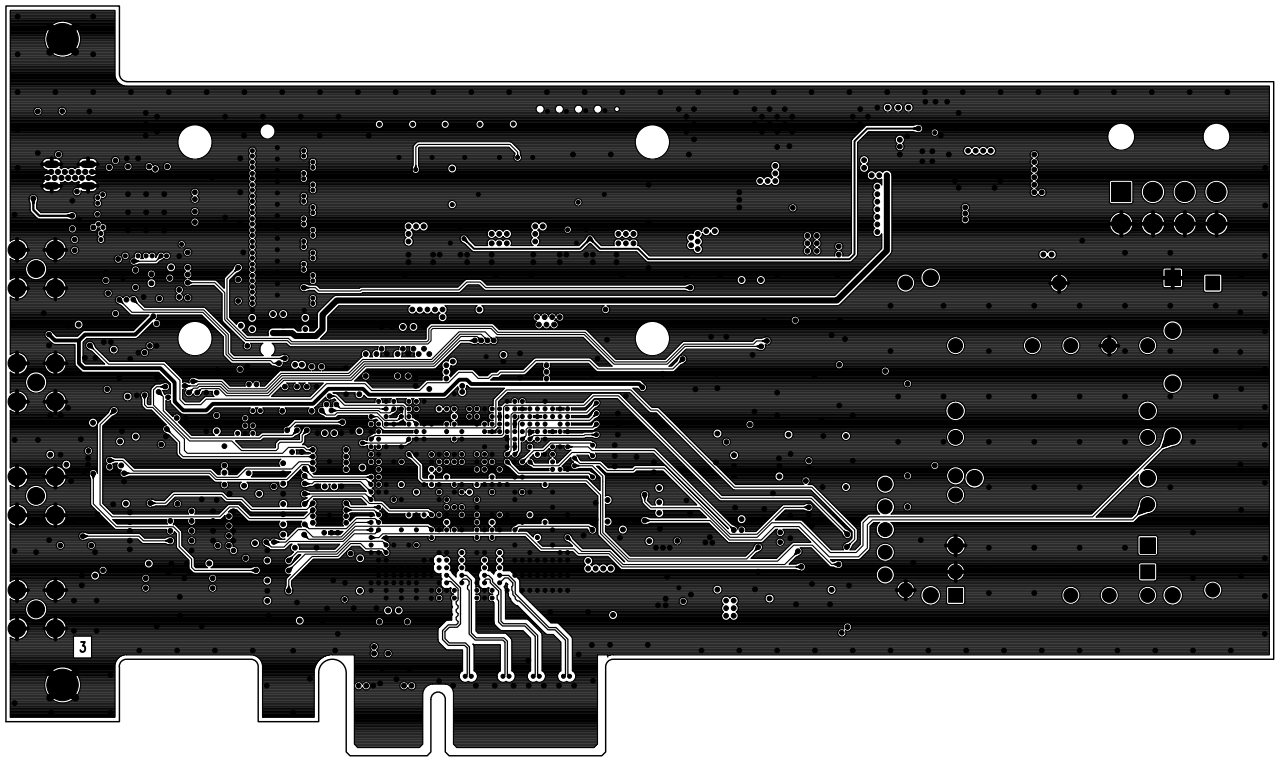
DOSSIER: ART_CARD Rev 4	17/11/21



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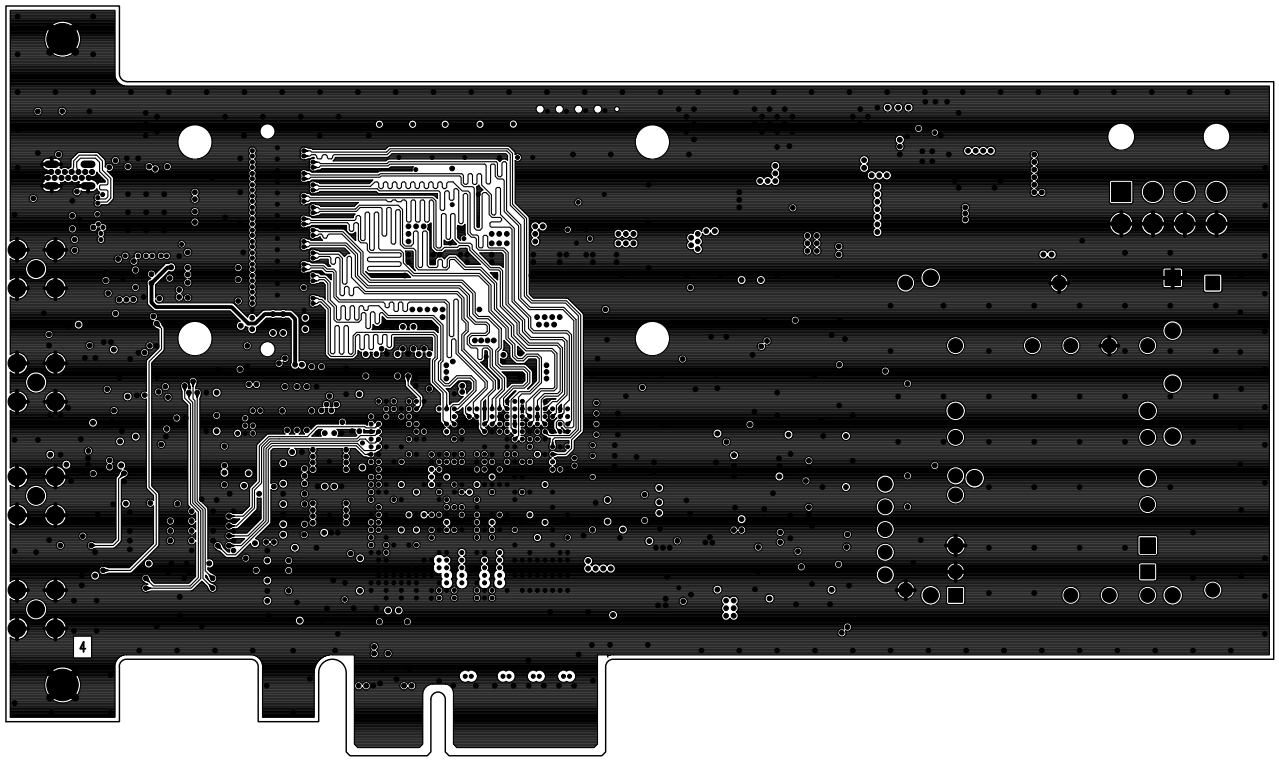
DOSSIER: ART_CARD Rev 4	17/11/21



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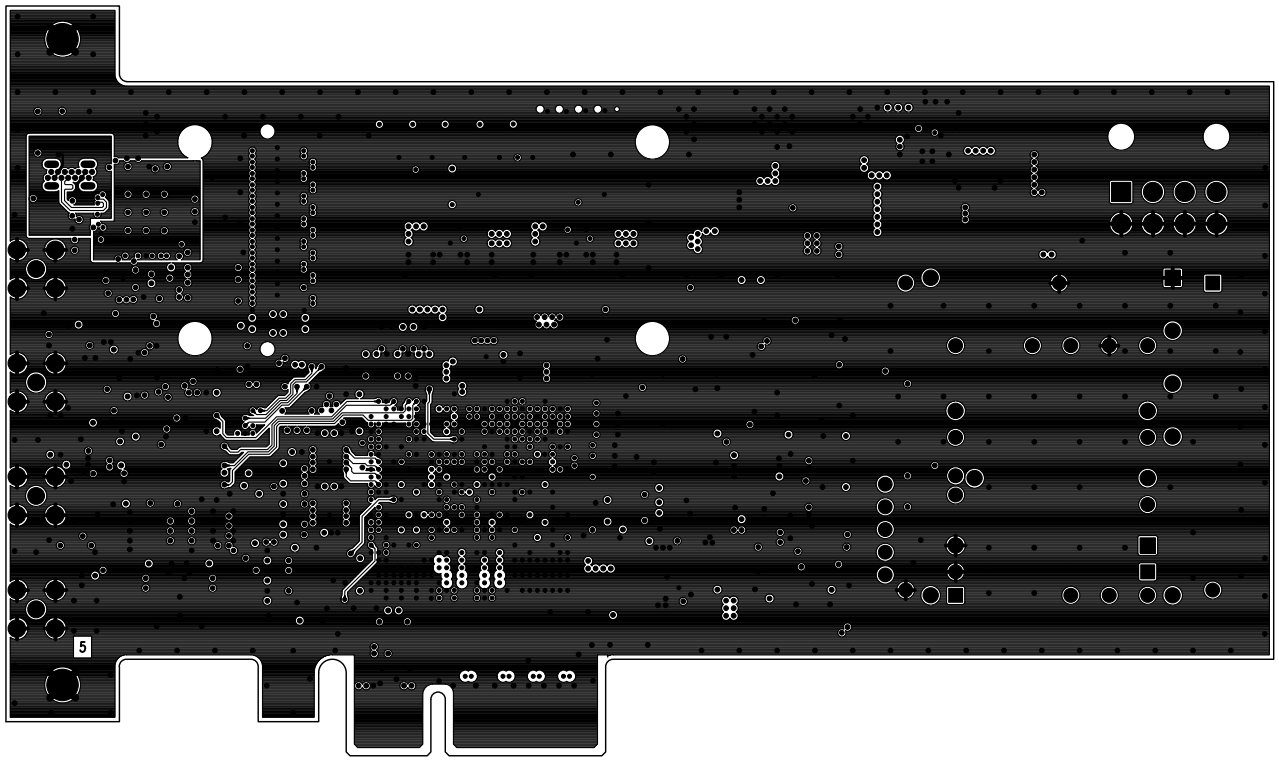
DOSSIER: ART_CARD Rev 4	17/11/21



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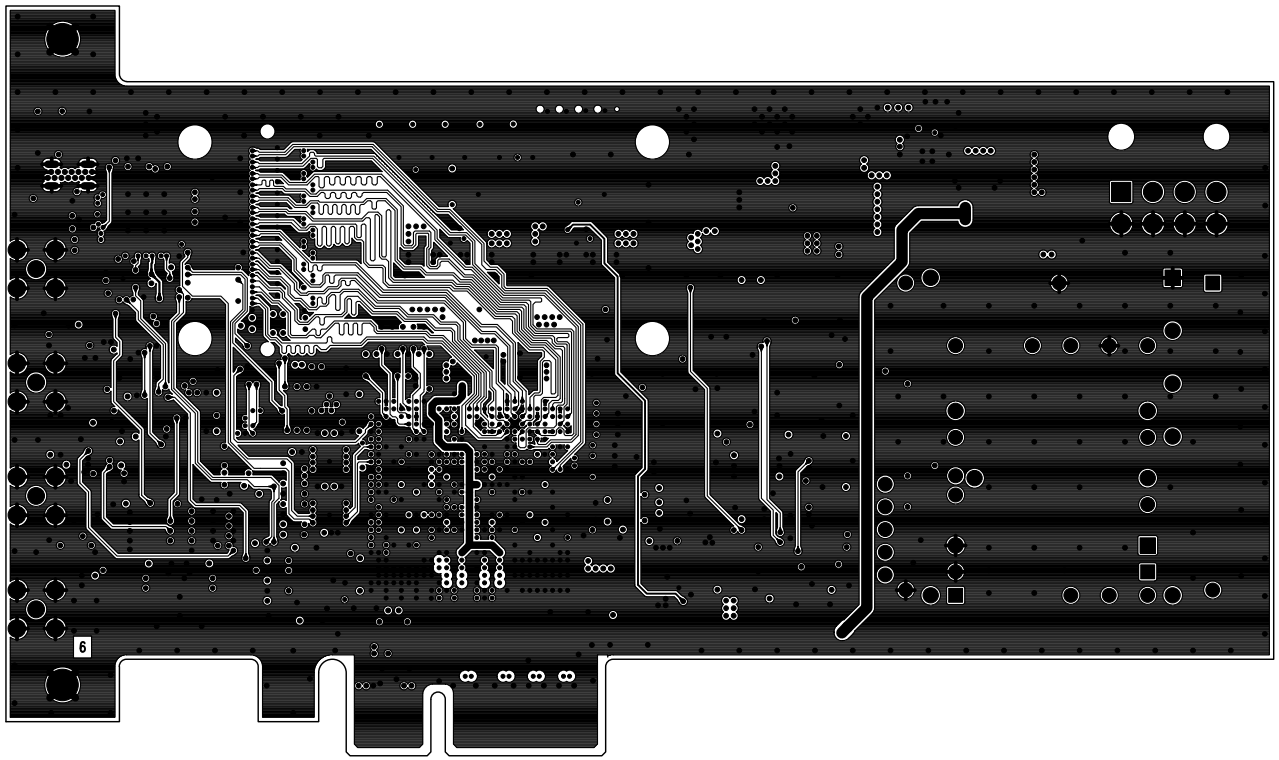
DOSSIER: ART_CARD Rev 4	17/11/21



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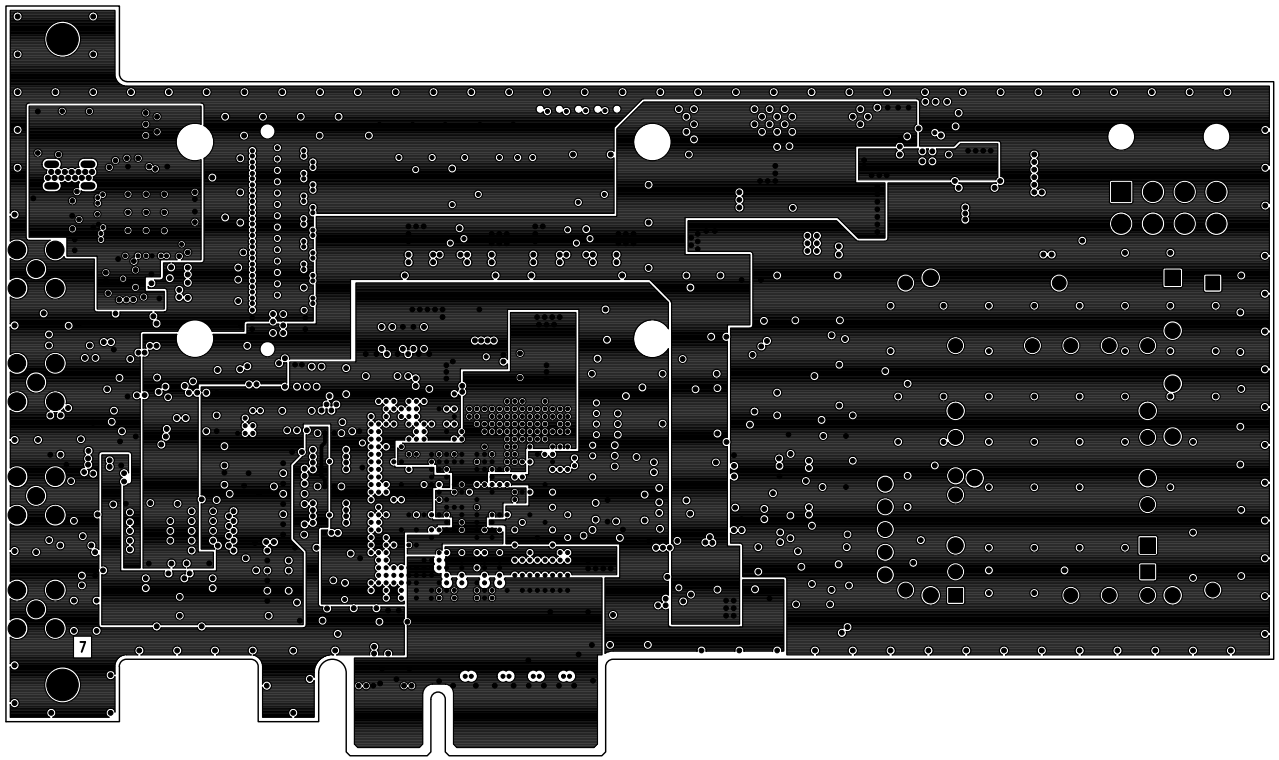
DOSSIER: ART_CARD Rev 4	17/11/21



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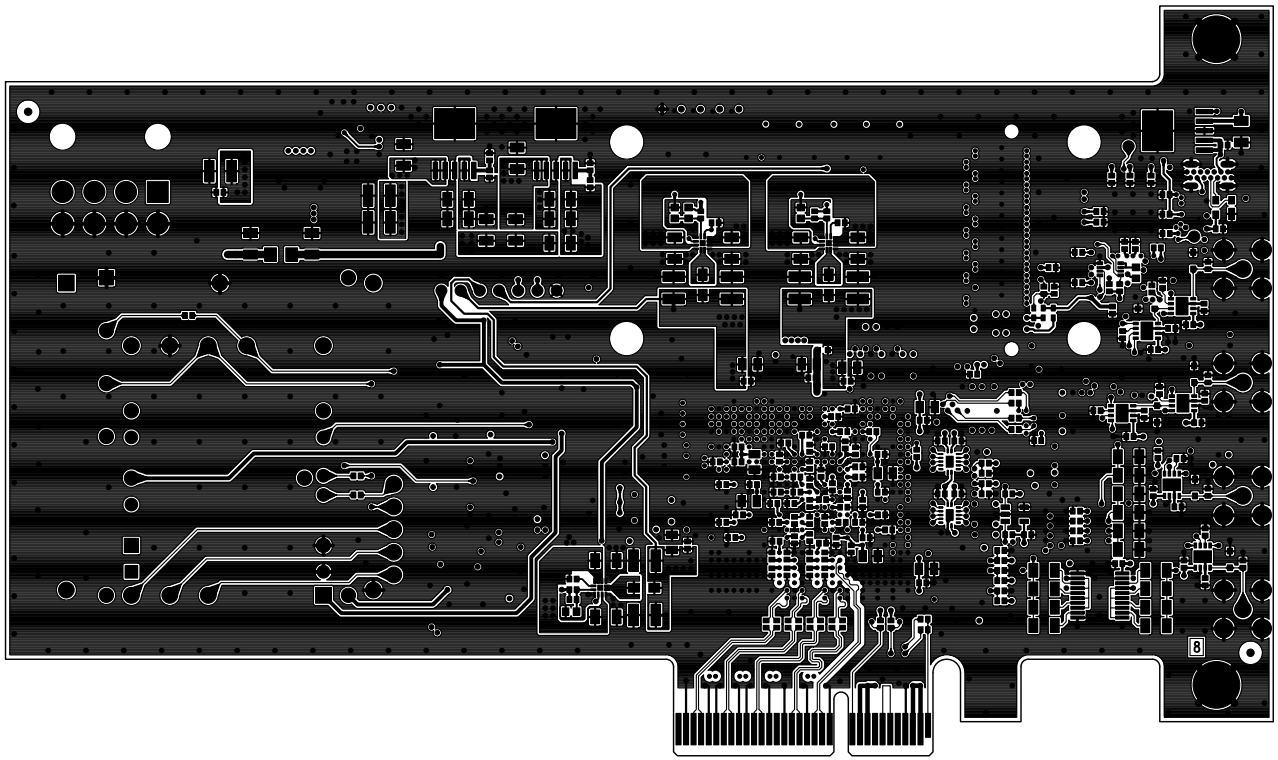
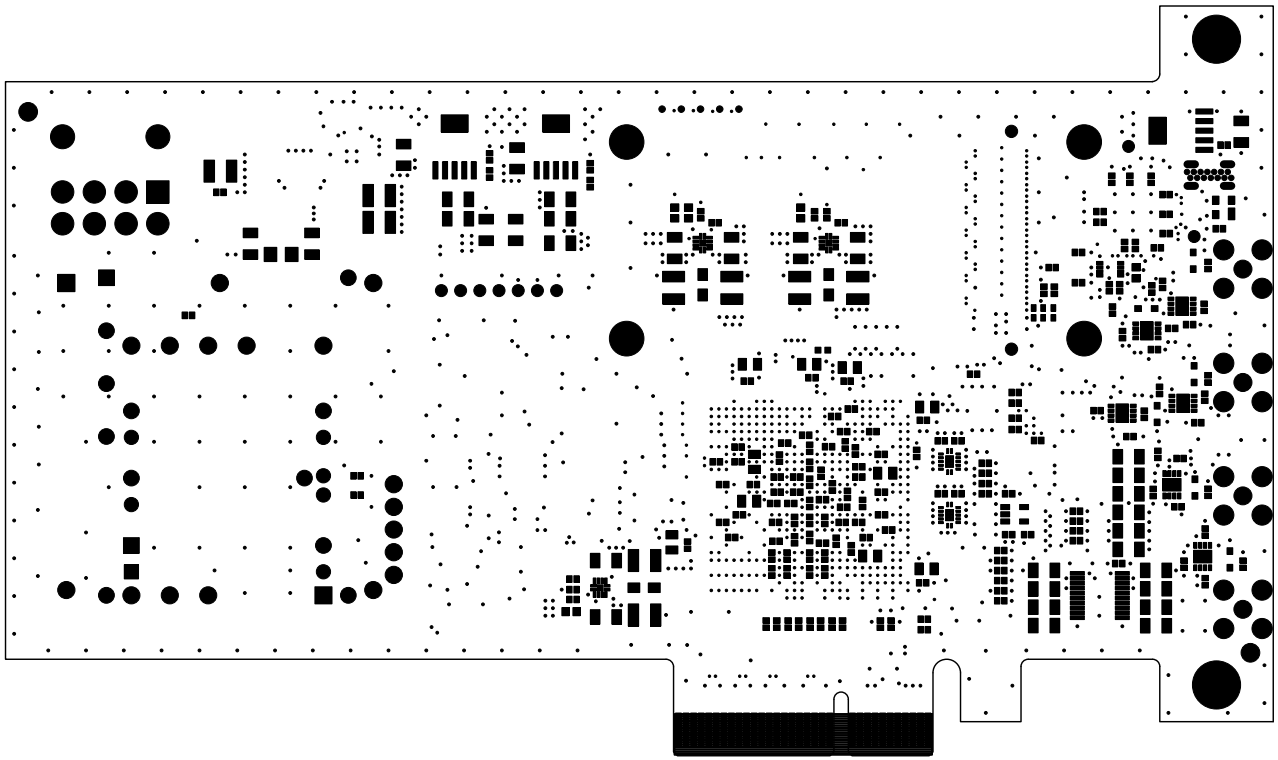
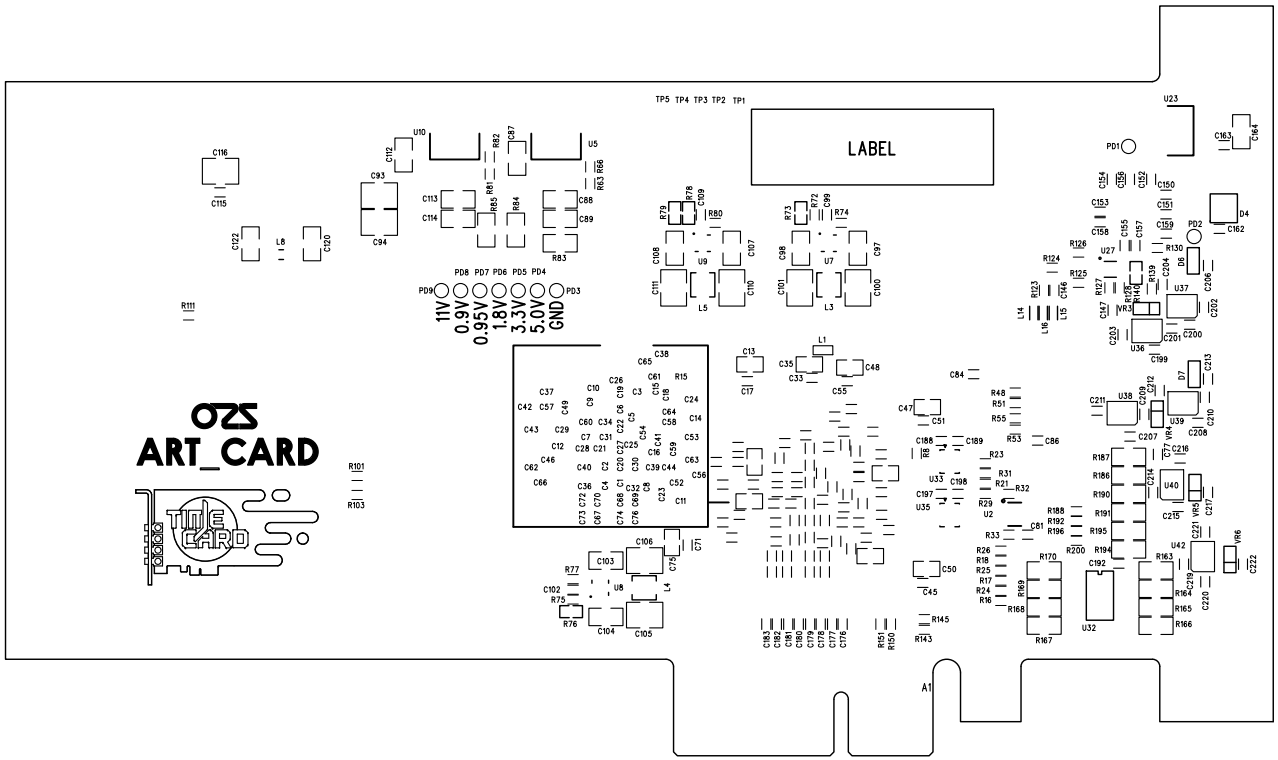
DOSSIER: ART_CARD Rev 4	17/11/21



FILM: SOUDURE	ARTEMIS
DOSSIER: ART_CARD Rev 4	17/11/21



FILM: EPARGNE SOUDURE	ARTEMIS
DOSSIER: ART_CARD Rev 4	17/11/21



OZS

ART_CARD

TIME CARD

FILM: SERIGRAPHIE SOUDURE	ARTEMIS
DOSSIER: ART_CARD Rev 4	17/11/21

Rev	DESCRIPTION	DATE	APPROVED
1			

NOTES:

1. FABRICATE BOARD PER:
Latest revision of IPC-A-600 Class 2. Electrical integrity testing required, per section 5.2 of IPC-A-600.

2. MATERIAL : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
Rigid laminate and prepeg shall be per IPC-4101/99/101/126. As described in the StackUp.
Laminate must meet latest RoHS directive subject to Orolia Engineering Approval.

3. FINISH : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
ENIG (Electroless Nickel, Immersion Gold) per IPC-4552

4. SOLDER MASK : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
LPI per IPC-SM-840 (current rev) COLOR : GREEN
Soldermask provided as 1 to 1 and shall be oversized at the fabricator as required in order to insure that soldermask does not encroach upon thru hole and SMT pads.
0.008 DIA Vias shall be plugged/tented from top and bottom side per artwork supplied unless mask is removed by artwork. These vias are required to be filled and copper capped. It is acceptable to use and epoxy fill after initial plating, followed by a copper cap process to cap the via fill.
Continuous copper plate is required.

5. SILKCREEN : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
White (All silkscreen to be removed from any exposed plated areas)

6. DIMENSIONING AND TOLERANCING PER ANSI-Y-14.5 (LATEST REV).

7. 94V-0 Min is required and shall be marked on top or bottom side silkscreen or copper

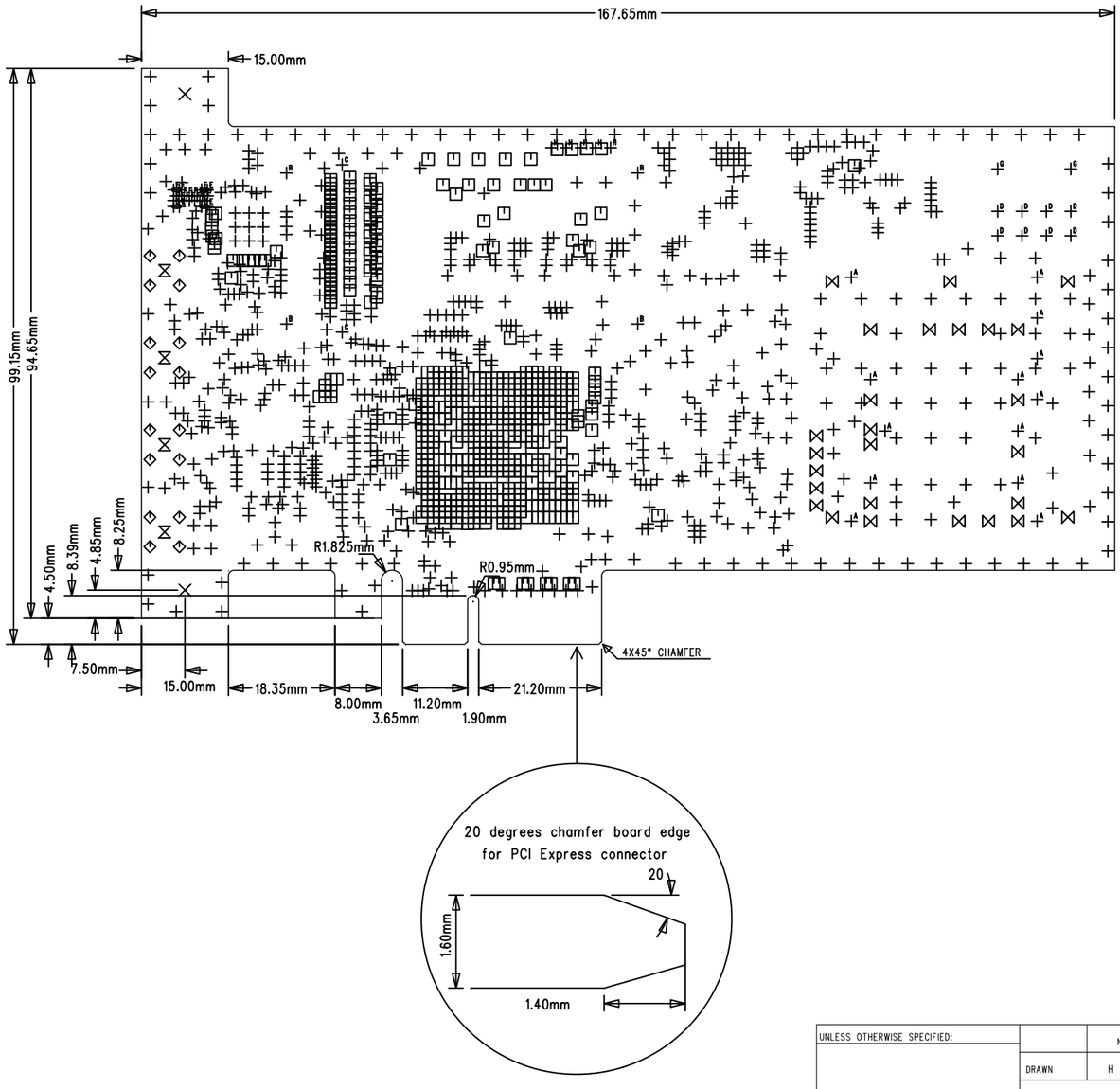
8. All copper on any layer shall be trimmed back 0.015 from the board edge as required.

9. All internal unused pads shall be removed

10. Teardrops shall be added where possible

11. All holes sizes shown are expected finished hole sizes after processing.

12. This board shall be supplied in array format that shall be determined/approved by the purshaser of the bare board



SIZE	QTY	SYM	PLATED	TOL
0.25	512	□	YES	+/-0.1
0.3	864	+	YES	+/-0.1
0.4	14	+F	YES	+/-0.1
0.45	5	+H	YES	+/-0.1
0.6 x 1.6	4	+E	YES	+/-0.1
1.1	26	⋈	YES	+/-0.1
1.3	13	+A	YES	+/-0.1
1.6	4	⧖	YES	+/-0.1
1.7	16	◇	YES	+/-0.1
1.8	8	+D	YES	+/-0.1
3.5	2	×	YES	+/-0.1
1.45	2	+C	NO	+/-0.1
3	2	+G	NO	+/-0.1
4.4	4	+B	NO	+/-0.1

UNLESS OTHERWISE SPECIFIED:

MATERIAL: PCB

FINISH:

	NAME	DATE
DRAWN	H ECHELARD	17/11/2021

CHANGE RESTRICTED
NO MANUAL CHANGES

THIRD ANGLE PROJECTION

OROLIA FRANCE

PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

SIZE A3 | DWG. NO. ART_CARD_PCB | REV 4

SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1

Angers Technopole
1 bis Avenue du Bois l'Abbé
49070 BEAUCOUZÉ FRANCE
Phone : +33(0)2-41-48-98-68
p.benoit@artemis-cad.com
www.artemis-cad.com

TECHNICAL SPECIFICATION
IPC-A-600

CUSTUMER : OROLIA
MANUFACTURER :

PCB Reference :	ART_CARD	**Index :**	Rev 4

☑	**PCB Unit**	**Unit PCB dimensions :**	167.65	X	99.15	mm	
☐	**Panel PCB : 0**	**Panel dimensions :**	0	X	0	mm	
Material :	FR4	**Surface :**	1.66	**dm²**	**Track / Gap :**	0.15 / 0.15	mm

PCB Type :	MC8	Finish Copper Thikness (µm) :	12µ	17,5µ	35µ	40µm
PCB Thickness (mm) :	16/10	External Layer :	☐	☐	☐	☑
		Intern Layer :	☐	☑	☐	☐

Technology	☑ Plated Trough Hole	**Via type :**	Hole / pads ratio :	0,25/0,55	
☑ Traditional	☐ Press-fit Hole	☑ Traditional Via	☐ Via in pad		
☑ SMT	☐ Autre	☐ Laser Via	☐ Stacked	☐ Staggered	
Surface Treatement Finished		☐ Blinded Via	Couche départ et d'arrivée		
☑ Ni/Au Chemical	☐ Sn/Pb surfondu	☐ Buried Via	Couche départ et d'arrivée		
☐ Sn/Cu HAL	☐ Autre	☐ Filled Via	☐ Resin	☐ Copper	

Peelable Solder Mask	☐ Standard		☐ TOP	☐ BOTTOM
Solder Mask	☑ Photo-imageable	Green	☑ TOP	☑ BOTTOM
Silkscreen	☑ Ink	White	☑ TOP	☑ BOTTOM
Electrical Test			☑ Yes	☐ No

☑ **Impedance control :** ☑ Produced ☐ Measured
50 ohms

☑ **Differential Pairs :** ☑ Produced ☐ Measured
85 ohms on layer 1, 3 and 8 ; 90 ohms on layer 4, 5 and 8

☑ **Stack-up :** voir avec le fabricant PCB et selon contraintes.

☐ **Milling** Milling Diameter : 0 mm

Comments :

Construire un empilage pour avoir avoir des lignes 50 ohms en 150µm (classe de la carte)
Pour les lignes 85 et 90 ohms, ajuster les largeurs si necessaire en gardant les isolations.