FILE OROLIA
ART_CARD

Réf PCB : **ART_CARD Rev 1**

⇨	7	SHEETS OF ELECTRICAL SCHEMATICS
⇨	1	ASSEMBLY DRAWING TOP
⇨	1	ASSEMBLY DRAWING BOTTOM
⇨	1	SILKSCREEN TOP
⇨	1	SOLDER MASK TOP
⇨	1	COPPER LAYER TOP
⇨	1	COPPER LAYER INNER 1
⇨	1	COPPER LAYER INNER 2
⇨	1	COPPER LAYER INNER 3
⇨	1	COPPER LAYER INNER 4
⇨	1	COPPER LAYER BOTTOM
⇨	1	SOLDER MASK BOTOM
⇨	1	SILKSCREEN BOTTOM
⇨	1	DRILL DRAWING
⇨	1	STACK-UP
⇨	1	CIRCUIT BOARD SPECIFICATION

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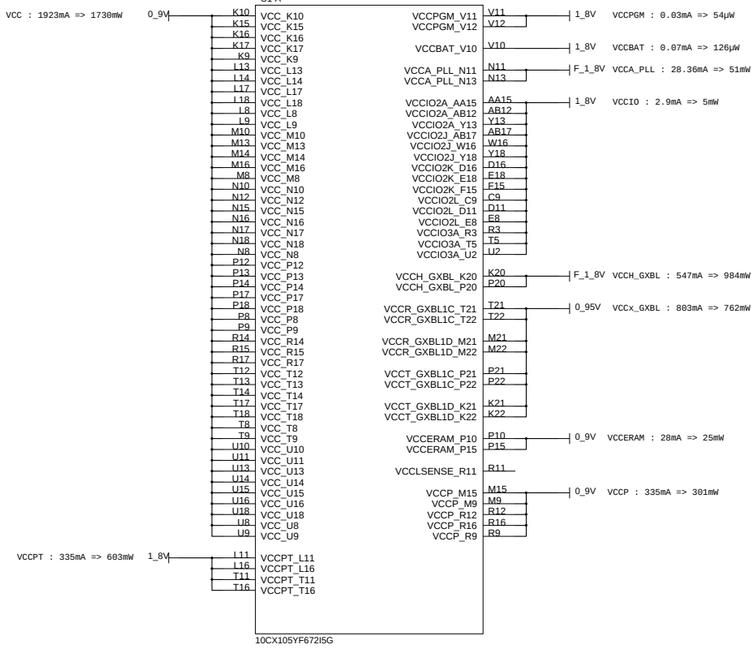
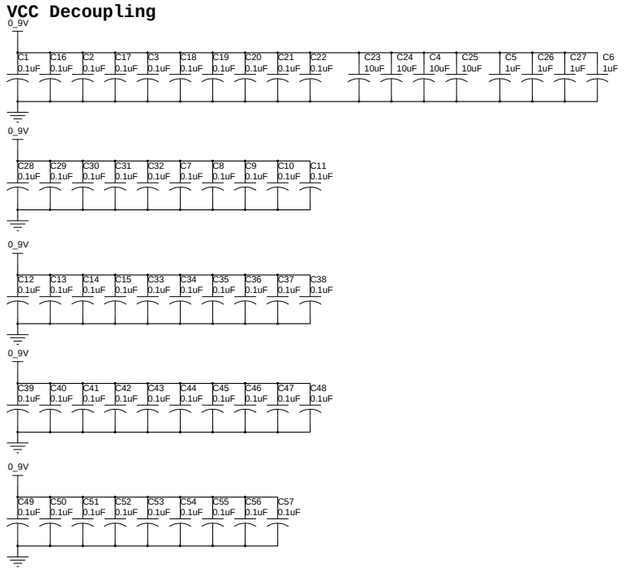
Title	**OVERVIEW**
Size: A1	Document Number: **ART_CARD**
Rev: 1	
Date: Monday, January 25, 2021	
FILE NAME: ART_CARD	Sheet: 1 of 7

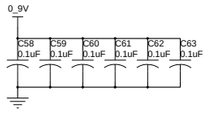
FPGA POWER SUPPLY



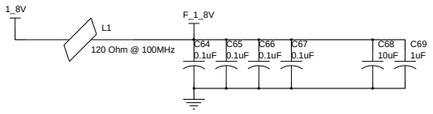
VCC Decoupling



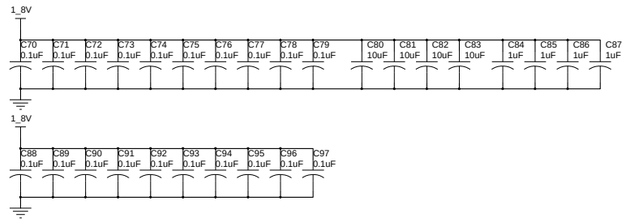
VCCP and VCCERAM Decoupling



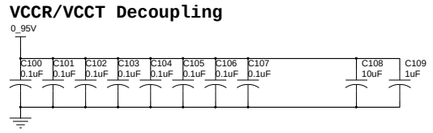
VCCA_PLL and VCCH_GXBL Decoupling

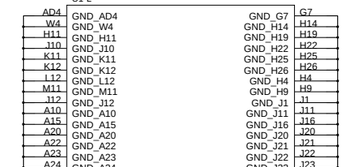


VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling



VCCR/VCCT Decoupling





Title	FPGA POWER
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FPGA

U1-J

AE5	IO_2A_47_AE5/DATA0/LVDS2A_1N/DQ24	
AE4	IO_2A_46_AE4/DATA1/LVDS2A_1P/DQ24	
AD9	IO_2A_45_AD9/DATA2/LVDS2A_2N/DQSN24	
AE9	IO_2A_44_AE9/DATA3/LVDS2A_2P/DQS24	
AD7	IO_2A_43_AD7/DATA4/LVDS2A_3N/DQ24	
AE7	IO_2A_42_AE7/DATA5/LVDS2A_3P/DQ24	
AE4	IO_2A_41_AF4/DATA6/LVDS2A_4N/DQSN25	GNSS_RX
AE3	IO_2A_40_AF3/DATA7/LVDS2A_4P/DQS25	GNSS_TX
AE6	IO_2A_39_AE6/DATA8/LVDS2A_5N/DQ25	
AF6	IO_2A_38_AF6/DATA9/LVDS2A_5P/DQ25	GNSS_PPS
AF8	IO_2A_37_AF8/DATA10/LVDS2A_6N/DQ25	
AE7	IO_2A_36_AF7/DATA11/LVDS2A_6P/DQ25	DCLS_IN
AC8	IO_2A_35_AC8/DATA12/LVDS2A_7N/DQ26	
AD8	IO_2A_34_AD8/DATA13/LVDS2A_7P/DQ26	
AC10	IO_2A_33_AC10/DATA14/LVDS2A_8N/DQSN26	
AD10	IO_2A_32_AD10/DATA15/LVDS2A_8P/DQS26	
AB6	IO_2A_31_AB6/DATA16/LVDS2A_9N/DQ26	
AB5	IO_2A_30_AB5/DATA17/LVDS2A_9P/DQ26	
AC7	IO_2A_29_AC7/PLL_2A_CLKOUT1N/DATA18/LVDS	
AC6	IO_2A_28_AC6/PLL_2A_CLKOUT1P_PLL_2A_CLKO	
AB10	IO_2A_27_AB10/NCEO/LVDS2A_11N/DQ27	
AC5	IO_2A_25_AC5/CLK_2A_1N/DATA20/LVDS2A_12N	
AD5	IO_2A_24_AD5/CLK_2A_1P/DATA21/LVDS2A_12P	
Y14	IO_2A_23_Y14/CLK_2A_0N/DATA22/LVDS2A_13N	
AA14	IO_2A_22_AA14/CLK_2A_0P/DATA23/LVDS2A_13	
AD13	IO_2A_21_AD13/DATA24/LVDS2A_14N/DQSN28	
AD12	IO_2A_20_AD12/DATA25/LVDS2A_14P/DQS28	
W15	IO_2A_19_W15/PLL_2A_CLKOUT0N/DATA26/LVDS	
Y15	IO_2A_18_Y15/PLL_2A_CLKOUT0P_PLL_2A_CLKO	
AB14	IO_2A_17_AB14/DATA28/LVDS2A_16N/DQSN29	
AB13	IO_2A_16_AB13/DATA29/LVDS2A_16P/DQS29	
AB11	IO_2A_15_AB11/DATA30/LVDS2A_17N/DQ29	
AC11	IO_2A_14_AC11/DATA31/LVDS2A_17P/DQ29	
AC13	IO_2A_13_AC13/CLKUSR/LVDS2A_18N/DQ29	
AB8	IO_2A_10_AB8/NPERSTL0/LVDS2A_19P/DQ30	PCIE_PERSTN
AA8	IO_2A_5_AA8/CVP_CONFDONE/LVDS2A_22N/DQSN	
W10	IO_2A_3_W10/INIT_DONE/LVDS2A_23N/DQ31	
Y9	IO_2A_2_Y9/DEV_OE/LVDS2A_23P/DQ31	
AA11	IO_2A_1_AA11/CRC_ERROR/LVDS2A_24N/DQ31	
Y10	IO_2A_0_Y10/DEV_CLRN/LVDS2A_24P/DQ31	

U1-D

H18	IO_2K_47_H18/LVDS2K_1N/DQ8	
G18	IO_2K_46_G18/LVDS2K_1P/DQ8	
F16	IO_2K_45_F16/LVDS2K_2N/DQSN8	
E16	IO_2K_44_E16/LVDS2K_2P/DQS8	
F17	IO_2K_43_F17/LVDS2K_3N/DQ8	
E17	IO_2K_42_E17/LVDS2K_3P/DQ8	
G19	IO_2K_41_G19/LVDS2K_4N/DQSN9	
G20	IO_2K_40_G20/LVDS2K_4P/DQS9	
F18	IO_2K_39_F18/LVDS2K_5N/DQ9	
F19	IO_2K_38_F19/LVDS2K_5P/DQ9	
E14	IO_2K_37_E14/LVDS2K_6N/DQ9	
E15	IO_2K_36_E15/LVDS2K_6P/DQ9	
C20	IO_2K_35_C20/LVDS2K_7N/DQ10	
C21	IO_2K_34_C21/LVDS2K_7P/DQ10	
E19	IO_2K_33_E19/LVDS2K_8N/DQSN10	
D19	IO_2K_32_D19/LVDS2K_8P/DQS10	
D17	IO_2K_31_D17/LVDS2K_9N/DQ10	
D18	IO_2K_30_D18/LVDS2K_9P/DQ10	
F21	IO_2K_27_F21/LVDS2K_11N/DQ11	
D14	IO_2K_21_D14/LVDS2K_14N/DQSN12	
D15	IO_2K_20_D15/LVDS2K_14P/DQS12	
A17	IO_2K_17_A17/LVDS2K_16N/DQSN13	OSC_PPS_OUT
A18	IO_2K_16_A18/LVDS2K_16P/DQS13	OSC_PPS_IN
C15	IO_2K_15_C15/LVDS2K_17N/DQ13	
B15	IO_2K_14_B15/LVDS2K_17P/DQ13	
B19	IO_2K_13_B19/LVDS2K_18N/DQ13	
A19	IO_2K_12_A19/LVDS2K_18P/DQ13	OSC_BITE
D13	IO_2K_11_D13/LVDS2K_19N/DQ14	
D12	IO_2K_10_D12/LVDS2K_19P/DQ14	
C13	IO_2K_9_C13/LVDS2K_20N/DQSN14	
B13	IO_2K_8_B13/LVDS2K_20P/DQS14	
B14	IO_2K_7_B14/LVDS2K_21N/DQ14	
A14	IO_2K_6_A14/LVDS2K_21P/DQ14	OSC_SDA
A13	IO_2K_5_A13/LVDS2K_22N/DQSN15	DAC_SPI_CLK
A12	IO_2K_4_A12/LVDS2K_22P/DQS15	DAC_SPI_CSN
C12	IO_2K_3_C12/LVDS2K_23N/DQ15	
C11	IO_2K_2_C11/LVDS2K_23P/DQ15	
B11	IO_2K_1_B11/LVDS2K_24N/DQ15	
A11	IO_2K_0_A11/LVDS2K_24P/DQ15	DAC_SPI_MOSI

U1-E

W18	IO_2J_47_W18/LVDS2J_1N/DQ16	
W19	IO_2J_46_W19/LVDS2J_1P/DQ16	
Y21	IO_2J_45_Y21/LVDS2J_2N/DQSN16	
AA21	IO_2J_44_AA21/LVDS2J_2P/DQS16	
Y19	IO_2J_43_Y19/LVDS2J_3N/DQ16	
Y20	IO_2J_42_Y20/LVDS2J_3P/DQ16	
W17	IO_2J_41_W17/LVDS2J_4N/DQSN17	
Y17	IO_2J_40_Y17/LVDS2J_4P/DQS17	
AA17	IO_2J_39_AA17/LVDS2J_5N/DQ17	
AB16	IO_2J_38_AB16/LVDS2J_5P/DQ17	
Y16	IO_2J_37_Y16/LVDS2J_6N/DQ17	
AA16	IO_2J_36_AA16/LVDS2J_6P/DQ17	
AB20	IO_2J_35_AB20/LVDS2J_7N/DQ18	
AB21	IO_2J_34_AB21/LVDS2J_7P/DQ18	
AC20	IO_2J_33_AC20/LVDS2J_8N/DQSN18	
AC21	IO_2J_32_AC21/LVDS2J_8P/DQS18	
AA18	IO_2J_31_AA18/LVDS2J_9N/DQ18	
AB18	IO_2J_30_AB18/LVDS2J_9P/DQ18	
AD19	IO_2J_27_AD19/LVDS2J_11N/DQ19	
AB15	IO_2J_21_AB15/LVDS2J_14N/DQSN20	
AC15	IO_2J_20_AC15/LVDS2J_14P/DQS20	
AD17	IO_2J_17_AD17/LVDS2J_16N/DQSN21	
AE17	IO_2J_16_AE17/LVDS2J_16P/DQS21	
AC16	IO_2J_15_AC16/LVDS2J_17N/DQ21	
AC17	IO_2J_14_AC17/LVDS2J_17P/DQ21	
AF16	IO_2J_13_AF16/LVDS2J_18N/DQ21	
AE16	IO_2J_12_AF16/LVDS2J_18P/DQ21	EEPROM_SDA
AE10	IO_2J_11_AE10/LVDS2J_19N/DQ22	
AF9	IO_2J_10_AF9/LVDS2J_19P/DQ22	
AF12	IO_2J_9_AF12/LVDS2J_20N/DQSN22	ID1
AF11	IO_2J_8_AF11/LVDS2J_20P/DQS22	ID0
AE15	IO_2J_7_AE15/LVDS2J_21N/DQ22	
AE14	IO_2J_6_AE14/LVDS2J_21P/DQ22	
AD15	IO_2J_5_AD15/LVDS2J_22N/DQSN23	
AD14	IO_2J_4_AD14/LVDS2J_22P/DQS23	
AE12	IO_2J_3_AE12/LVDS2J_23N/DQ23	
AF11	IO_2J_2_AE11/LVDS2J_23P/DQ23	
AF13	IO_2J_1_AF13/LVDS2J_24N/DQ23	ID2
AF14	IO_2J_0_AF14/LVDS2J_24P/DQ23	ID3

U1-H

K4	IO_3A_47_K4/LVDS3A_1N/DQ56	
J4	IO_3A_46_J4/LVDS3A_1P/DQ56	
H6	IO_3A_45_H6/LVDS3A_2N/DQSN56	
H5	IO_3A_44_H5/LVDS3A_2P/DQS56	
K5	IO_3A_43_K5/LVDS3A_3N/DQ56	
J5	IO_3A_42_J5/LVDS3A_3P/DQ56	
M4	IO_3A_41_M4/LVDS3A_4N/DQSN57	
L4	IO_3A_40_L4/LVDS3A_4P/DQS57	
H3	IO_3A_39_H3/LVDS3A_5N/DQ57	
G3	IO_3A_38_G3/LVDS3A_5P/DQ57	
N5	IO_3A_37_N5/LVDS3A_6N/DQ57	
M5	IO_3A_36_M5/LVDS3A_6P/DQ57	
J3	IO_3A_35_J3/LVDS3A_7N/DQ58	
H2	IO_3A_34_H2/LVDS3A_7P/DQ58	
K2	IO_3A_33_K2/LVDS3A_8N/DQSN58	
J2	IO_3A_32_J2/LVDS3A_8P/DQS58	
H1	IO_3A_31_H1/LVDS3A_9N/DQ58	
G1	IO_3A_30_G1/LVDS3A_9P/DQ58	
M1	IO_3A_27_M1/LVDS3A_11N/DQ59	DCLS_OUT1
T3	IO_3A_21_T3/LVDS3A_14N/DQSN60	
U3	IO_3A_20_U3/LVDS3A_14P/DQS60	
N3	IO_3A_17_N3/LVDS3A_16N/DQSN61	
N2	IO_3A_16_N2/LVDS3A_16P/DQS61	
U5	IO_3A_15_U5/LVDS3A_17N/DQ61	
U4	IO_3A_14_U4/LVDS3A_17P/DQ61	
R4	IO_3A_13_R4/LVDS3A_18N/DQ61	
T4	IO_3A_12_T4/LVDS3A_18P/DQ61	
T2	IO_3A_11_T2/LVDS3A_19N/DQ62	
T1	IO_3A_10_T1/LVDS3A_19P/DQ62	LED_G2
U1	IO_3A_9_U1/LVDS3A_20N/DQSN62	LED_G1
V1	IO_3A_8_V1/LVDS3A_20P/DQS62	LED_G0
P2	IO_3A_7_P2/LVDS3A_21N/DQ62	
N1	IO_3A_6_N1/LVDS3A_21P/DQ62	DCLS_OUT0
R2	IO_3A_5_R2/LVDS3A_22N/DQSN63	
R1	IO_3A_4_R1/LVDS3A_22P/DQS63	LED_R0

U1-I

C6	IO_2L_25_C6/CLK_2L_1N/DQ3	
C5	IO_2L_24_C5/CLK_2L_1P/DQ3	
B6	IO_2L_23_B6/CLK_2L_0N/DQ4	
A6	IO_2L_22_A6/CLK_2L_0P/DQ4	CLK_OSC
C18	IO_2K_25_C18/CLK_2K_1N/LVDS2K_12N/DQ11	
B18	IO_2K_24_B18/CLK_2K_1P/LVDS2K_12P/DQ11	
C16	IO_2K_23_C16/CLK_2K_0N/LVDS2K_13N/DQ12	
C17	IO_2K_22_C17/CLK_2K_0P/LVDS2K_13P/DQ12	
AC18	IO_2J_25_AC18/CLK_2J_1N/LVDS2J_12N/DQ19	
AD18	IO_2J_24_AD18/CLK_2J_1P/LVDS2J_12P/DQ19	
AE19	IO_2J_23_AE19/CLK_2J_0N/LVDS2J_13N/DQ20	
AF19	IO_2J_22_AF19/CLK_2J_0P/LVDS2J_13P/DQ20	CLK_25M
M3	IO_3A_25_M3/CLK_3A_1N/LVDS3A_12N/DQ59	
L3	IO_3A_24_L3/CLK_3A_1P/LVDS3A_12P/DQ59	
P5	IO_3A_23_P5/CLK_3A_0N/LVDS3A_13N/DQ60	
R5	IO_3A_22_R5/CLK_3A_0P/LVDS3A_13P/DQ60	
C10	IO_2L_26_C10/RZQ_2L/DQ3	
E21	IO_2K_26_E21/RZQ_2K/LVDS2K_11P/DQ11	
AD20	IO_2J_26_AD20/RZQ_2J/LVDS2J_11P/DQ19	
AB9	IO_2A_26_AB9/RZQ_2A/LVDS2A_11P/DQ27	
L1	IO_3A_26_L1/RZQ_3A/LVDS3A_11P/DQ59	

1_8V — R1 R2 R3 R4 R5 R6 R7 0 — V15 V17 H17 E12 R6 G6 F6

V15	VREFB2AN0_2A_V15	
V17	VREFB2JN0_2J_V17	
H17	VREFB2KN0_2K_H17	
E12	VREFB2LN0_2L_E12	
R6	VREFB3AN0_3A_R6	
G6	VREFN_ADC_G6	
F6	VREFP_ADC_F6	

U1-F

AC12	IO_2A_12_AC12/LVDS2A_18P/DQ29	
AA9	IO_2A_11_AA9/LVDS2A_19N/DQ30	
W9	IO_2A_9_W9/LVDS2A_20N/DQSN30	
W8	IO_2A_8_W8/LVDS2A_20P/DQS30	
AA13	IO_2A_7_AA13/LVDS2A_21N/DQ30	
AA12	IO_2A_6_AA12/LVDS2A_21P/DQ30	
AA7	IO_2A_4_AA7/LVDS2A_22P/DQS31	

U1-G

L2	IO_3A_29_L2/PLL_3A_CLKOUT1N/LVDS3A_10N/D	
K1	IO_3A_28_K1/PLL_3A_CLKOUT1P_PLL_3A_CLKOU	
P4	IO_3A_19_P4/PLL_3A_CLKOUT0N/LVDS3A_15N/D	
P3	IO_3A_18_P3/PLL_3A_CLKOUT0P_PLL_3A_CLKOU	

U1-B

D8	IO_2L_29_D8/PLL_2L_CLKOUT1N/DQSN3	
D7	IO_2L_28_D7/PLL_2L_CLKOUT1P_PLL_2L_CLKOU	
B8	IO_2L_19_B8/PLL_2L_CLKOUT0N/DQ4	
A7	IO_2L_18_A7/PLL_2L_CLKOUT0P_PLL_2L_CLKOU	
E20	IO_2K_29_E20/PLL_2K_CLKOUT1N/LVDS2K_10N/	
D20	IO_2K_28_D20/PLL_2K_CLKOUT1P_PLL_2K_CLKO	
B16	IO_2K_19_B16/PLL_2K_CLKOUT0N/LVDS2K_15N/	
A16	IO_2K_18_A16/PLL_2K_CLKOUT0P_PLL_2K_CLKO	OSC_SCL
AA19	IO_2J_29_AA19/PLL_2J_CLKOUT1N/LVDS2J_10N	
AB19	IO_2J_28_AB19/PLL_2J_CLKOUT1P_PLL_2J_CLK	
AE17	IO_2J_19_AF17/PLL_2J_CLKOUT0N/LVDS2J_15N	EEPROM_SCL
AF18	IO_2J_18_AF18/PLL_2J_CLKOUT0P_PLL_2J_CLK	PCIE_WAKEN

U1-C

E5	IO_2L_47_E5/DQ0	
E4	IO_2L_46_E4/DQ0	
D5	IO_2L_45_D5/DQSN0	
D4	IO_2L_44_D4/DQS0	
E7	IO_2L_43_E7/DQ0	
E6	IO_2L_42_E6/DQ0	
F4	IO_2L_41_F4/DQSN1	
F3	IO_2L_40_F3/DQS1	
G5	IO_2L_39_G5/DQ1	
G4	IO_2L_38_G4/DQ1	
F8	IO_2L_37_F8/DQ1	
F7	IO_2L_36_F7/DQ1	
E9	IO_2L_35_E9/DQ2	
D9	IO_2L_34_D9/DQ2	
E11	IO_2L_33_E11/DQSN2	
E10	IO_2L_32_E10/DQS2	
C8	IO_2L_31_C8/DQ2	
C7	IO_2L_30_C7/DQ2	
D10	IO_2L_27_D10/DQ3	
B5	IO_2L_21_B5/DQSN4	
A4	IO_2L_20_A4/DQS4	
B10	IO_2L_17_B10/DQSN5	
B9	IO_2L_16_B9/DQS5	
B4	IO_2L_15_B4/DQ5	
B3	IO_2L_14_B3/DQ5	
A9	IO_2L_13_A9/DQ5	OSC_TX
A8	IO_2L_12_A8/DQ5	OSC_RX
D3	IO_2L_11_D3/DQ6	
D2	IO_2L_10_D2/DQ6	
C3	IO_2L_9_C3/DQSN6	
C2	IO_2L_8_C2/DQS6	
C1	IO_2L_7_C1/DQ6	GPIO_2
B1	IO_2L_6_B1/DQ6	GPIO_3
A3	IO_2L_5_A3/DQSN7	
A2	IO_2L_4_A2/DQS7	
F2	IO_2L_3_E2/DQ7	
E1	IO_2L_2_E1/DQ7	GPIO_1
F2	IO_2L_1_F2/DQ7	
F1	IO_2L_0_F1/DQ7	GPIO_0

U1-K

AF21	DNU_AF21	
AF22	DNU_AF22	
W7	DNU_W7	
Y6	DNU_Y6	
Y7	DNU_Y7	
AD23	GXBL1C_RX_CH0N_GXBL1C_REFCLK0N_1C_AD23	
AD24	GXBL1C_RX_CH0P_GXBL1C_REFCLK0P_1C_AD24	
AB23	GXBL1C_RX_CH1N_GXBL1C_REFCLK1N_1C_AB23	
AB24	GXBL1C_RX_CH1P_GXBL1C_REFCLK1P_1C_AB24	
Y23	GXBL1C_RX_CH2N_GXBL1C_REFCLK2N_1C_Y23	
Y24	GXBL1C_RX_CH2P_GXBL1C_REFCLK2P_1C_Y24	
V23	GXBL1C_RX_CH3N_GXBL1C_REFCLK3N_1C_V23	
V24	GXBL1C_RX_CH3P_GXBL1C_REFCLK3P_1C_V24	
T23	GXBL1C_RX_CH4N_GXBL1C_REFCLK4N_1C_T23	PCIE_RXN0
T24	GXBL1C_RX_CH4P_GXBL1C_REFCLK4P_1C_T24	PCIE_RXP0
P23	GXBL1C_RX_CH5N_GXBL1C_REFCLK5N_1C_P23	PCIE_RXN1
P24	GXBL1C_RX_CH5P_GXBL1C_REFCLK5P_1C_P24	PCIE_RXP1
AE25	GXBL1C_TX_CH0N_1C_AE25	
AE26	GXBL1C_TX_CH0P_1C_AE26	
AC25	GXBL1C_TX_CH1N_1C_AC25	
AC26	GXBL1C_TX_CH1P_1C_AC26	
AA25	GXBL1C_TX_CH2N_1C_AA25	
AA26	GXBL1C_TX_CH2P_1C_AA26	
W25	GXBL1C_TX_CH3N_1C_W25	
W26	GXBL1C_TX_CH3P_1C_W26	
U25	GXBL1C_TX_CH4N_1C_U25	PCIE_TXN0
U26	GXBL1C_TX_CH4P_1C_U26	PCIE_TXP0
R25	GXBL1C_TX_CH5N_1C_R25	PCIE_TXN1
R26	GXBL1C_TX_CH5P_1C_R26	PCIE_TXP1
M23	GXBL1D_RX_CH0N_GXBL1D_REFCLK0N_1D_M23	PCIE_RXN2
M24	GXBL1D_RX_CH0P_GXBL1D_REFCLK0P_1D_M24	PCIE_RXP2
K23	GXBL1D_RX_CH1N_GXBL1D_REFCLK1N_1D_K23	PCIE_RXN3
K24	GXBL1D_RX_CH1P_GXBL1D_REFCLK1P_1D_K24	PCIE_RXP3
H23	GXBL1D_RX_CH2N_GXBL1D_REFCLK2N_1D_H23	
H24	GXBL1D_RX_CH2P_GXBL1D_REFCLK2P_1D_H24	
F23	GXBL1D_RX_CH3N_GXBL1D_REFCLK3N_1D_F23	
F24	GXBL1D_RX_CH3P_GXBL1D_REFCLK3P_1D_F24	
N25	GXBL1D_TX_CH0N_1D_N25	PCIE_TXN2
N26	GXBL1D_TX_CH0P_1D_N26	PCIE_TXP2
L25	GXBL1D_TX_CH1N_1D_L25	PCIE_TXN3
L26	GXBL1D_TX_CH1P_1D_L26	PCIE_TXP3
J25	GXBL1D_TX_CH2N_1D_J25	
J26	GXBL1D_TX_CH2P_1D_J26	
G25	GXBL1D_TX_CH3N_1D_G25	
G26	GXBL1D_TX_CH3P_1D_G26	
C25	NC_C25	
C26	NC_C26	
E25	NC_E25	
E26	NC_E26	
F11	NC_F11	
F12	NC_F12	
F13	NC_F13	
E14	NC_F14	
G10	NC_G10	
G11	NC_G11	
G13	NC_G13	
G14	NC_G14	
G15	NC_G15	
G16	NC_G16	
H10	NC_H10	
H12	NC_H12	
H13	NC_H13	
H15	NC_H15	
H16	NC_H16	
H20	NC_H20	
H21	NC_H21	
H7	NC_H7	
J13	NC_J13	
J14	NC_J14	
J15	NC_J15	
J17	NC_J17	
J18	NC_J18	
J19	NC_J19	
K14	NC_K14	
K19	NC_K19	
K6	NC_K6	
K7	NC_K7	
L19	NC_L19	
L6	NC_L6	
L7	NC_L7	
M18	NC_M18	
M19	NC_M19	
M6	NC_M6	
N6	NC_N6	
N7	NC_N7	
P19	NC_P19	
P7	NC_P7	
R19	NC_R19	
R7	NC_R7	
T19	NC_T19	
T6	NC_T6	
T7	NC_T7	
U19	NC_U19	
U6	NC_U6	
V13	NC_V13	
V16	NC_V16	
V18	NC_V18	
V2	NC_V2	
V3	NC_V3	
V5	NC_V5	
V6	NC_V6	
V7	NC_V7	
V8	NC_V8	
W12	NC_W12	
W13	NC_W13	
W14	NC_W14	
W2	NC_W2	
W20	NC_W20	
W3	NC_W3	
Y11	NC_Y11	
Y12	NC_Y12	
U21	REFCLK_GXBL1C_CHBN_1C_U21	PCIE_REFCLKN
U22	REFCLK_GXBL1C_CHBP_1C_U22	PCIE_REFCLKP
R21	REFCLK_GXBL1C_CHTN_1C_R21	
R22	REFCLK_GXBL1C_CHTP_1C_R22	
N21	REFCLK_GXBL1D_CHBN_1D_N21	
N22	REFCLK_GXBL1D_CHBP_1D_N22	
L21	REFCLK_GXBL1D_CHTN_1D_L21	
L22	REFCLK_GXBL1D_CHTP_1D_L22	
AF23	RREF_BL_AF23	
A21	RREF_TL_A21	
J8	TEMPDIODEN_J8	
J9	TEMPDIODEP_J9	
H8	VSIGN_0_H8	
G9	VSIGN_1_G9	
G8	VSIGP_0_G8	
F9	VSIGP_1_F9	

1_8V — R8 1.00 K — JTAG_TDO AC1; JTAG_TMS AA6; JTAG_TRST Y1; JTAG_TCK AE1; JTAG_TDI Y2; MSEL0 AA3; MSEL1 AA2; MSEL2 W5

R9 0; R10 10.0K; R11 10.0K; R12 10.0K; R13 1.00 K — NIO_PULLUP AD3; NSTATUS AB1; CONF_DONE Y5; NCONFIG AA4; NCE AE2; NCSO0 AC3; NCSO1 AB4; NCSO2 Y4

AS_CSN — AS_DATA0_ASDO; AS_D0 AD2; AS_D1 AC2; AS_D2 AB3; AS_D3 AE2

AS_CLK — R14 39.0 — DCLK

CONF_DONE

ID

1_8V — R15 R16 R17 R18 1.00 K — ID0; ID1; ID2; ID3

R19 R20 R21 R22 0

FPGA FLASH CONFIGURATION

U2

1_8V — C110 0.1 uF

AS_D0 D3; AS_D1 D2; AS_D2 C4; AS_D3 D4; AS_CLK B2; AS_CSN C2; AS_RESETN A4

1_8V — R24 10.0K

DQ0/SI; DQ1/SO; DQ2/WP#; DQ3; SCK; CE#; RESET#/DNU3; DNU1 A2; DNU2 A3; DNU4 A5; DNU5 B1

VCC B4; DNU6 B5; DNU7 C1; DNU8 C3; DNU9 C5; DNU10 D1; DNU11 D5; DNU12 E1; DNU13 E2; DNU14 E3; DNU15 E4; DNU16 E5; GND B3

256 Megabit

IS25WP256D-RHLE

P = 54mW

CLOCK

1_8V

Y1 — 1 EN; 4 VDD; 2 GND; 3 F — 25.0000MHz

R23 39.0 — CLK_25M

C111 0.1 uF

P = 7mW

FPGA CONFIGURATION

1_8V — R25 R26 R27 1.00 K — MSEL0; MSEL1; MSEL2

MSEL :AS - 1.8V Fast : 010
Standard : 011

R28 R29 R30 0

EEPROM WITH UNIQUE ID

1_8V — R36 R37 1.00 K

U3

EEPROM_SCL 1 SCL; EEPROM_SDA 3 SDA; 2 VSS; WP 5; VCC 4

24LC08B

1_8V — C115 0.1 uF

JTAG

3_3V — R32 R33 R35 10.0K

JTAG_TCK; JTAG_TDO; JTAG_TMS; JTAG_TDI

J1 — 1 2 3 4 5 6 7 8 9 10 — 3_3V — C112 0.1 uF

J501R-0102-001E

C113 C116 C117 C114 15 pF

R44 1.00 K

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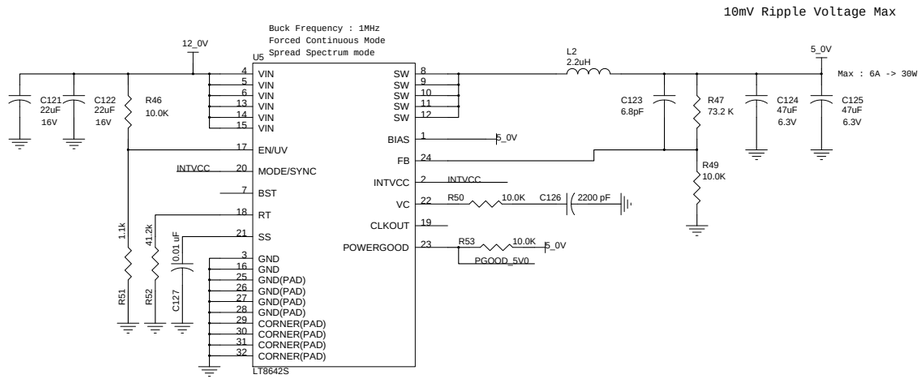
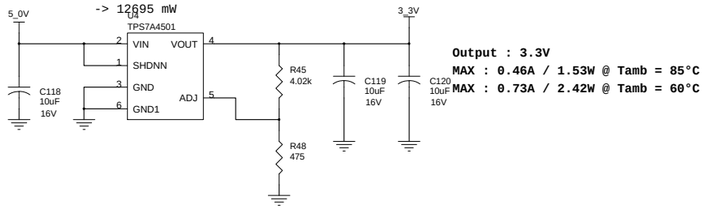
12V to 5V Switch Converter

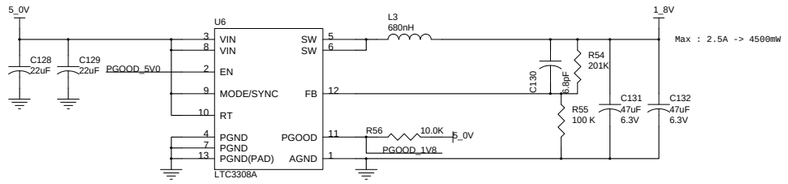


POWER NEED : FPGA : OCXO : Comp : TOTAL
On 12V : : 7500 : : 7500 mW
On 11V_ANA : : : 80 : 80 mW
On 5.0V : : 450 : : 450 mW
On 3.3V : : : 243 : 243 mW
On 1.8V : 1643 : : 61 : 1704 mW
On 0.95V : 762 : : : 762 mW
On 0.9V : 2056 : : : 2056 mW
-> 12695 mW

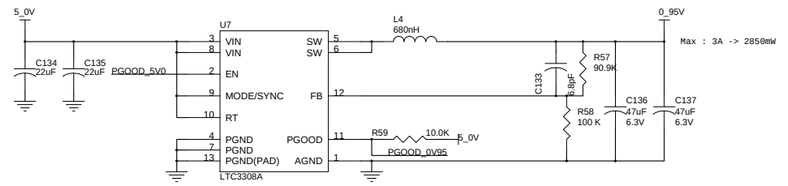
5V to 3.3V LDO Converter



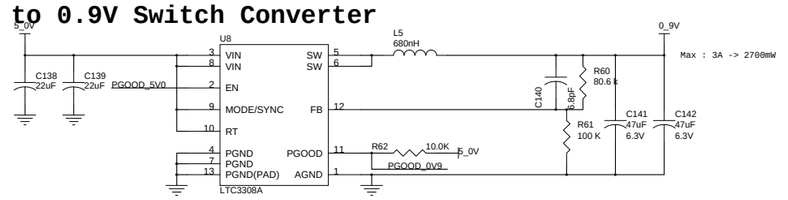
5V to 1.8V Switch Converter



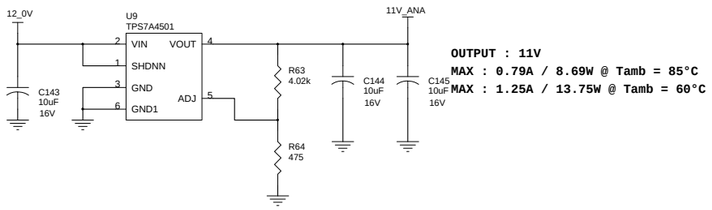
5V to 0.95V Switch Converter



5V to 0.9V Switch Converter



ANALOG POWER SUPPLY



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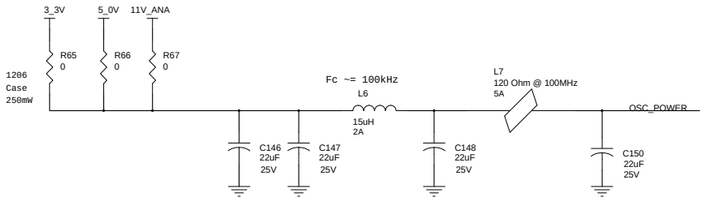
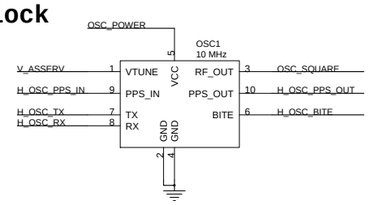
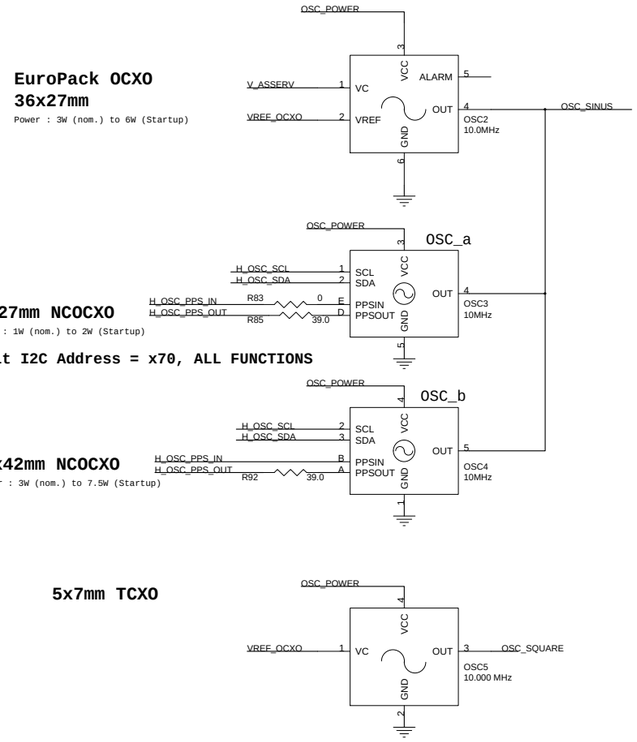
OSCILLATOR POWER SUPPLY



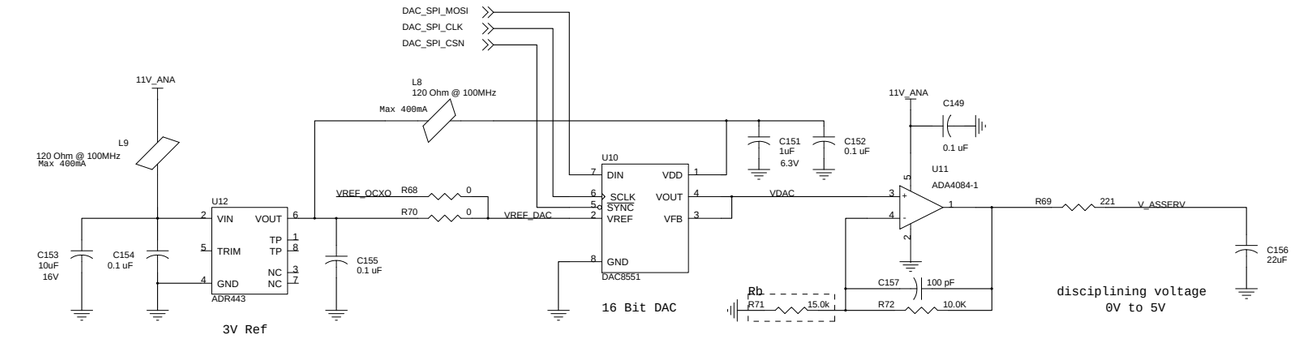
MiniRubidium
Miniature Atomic Clock



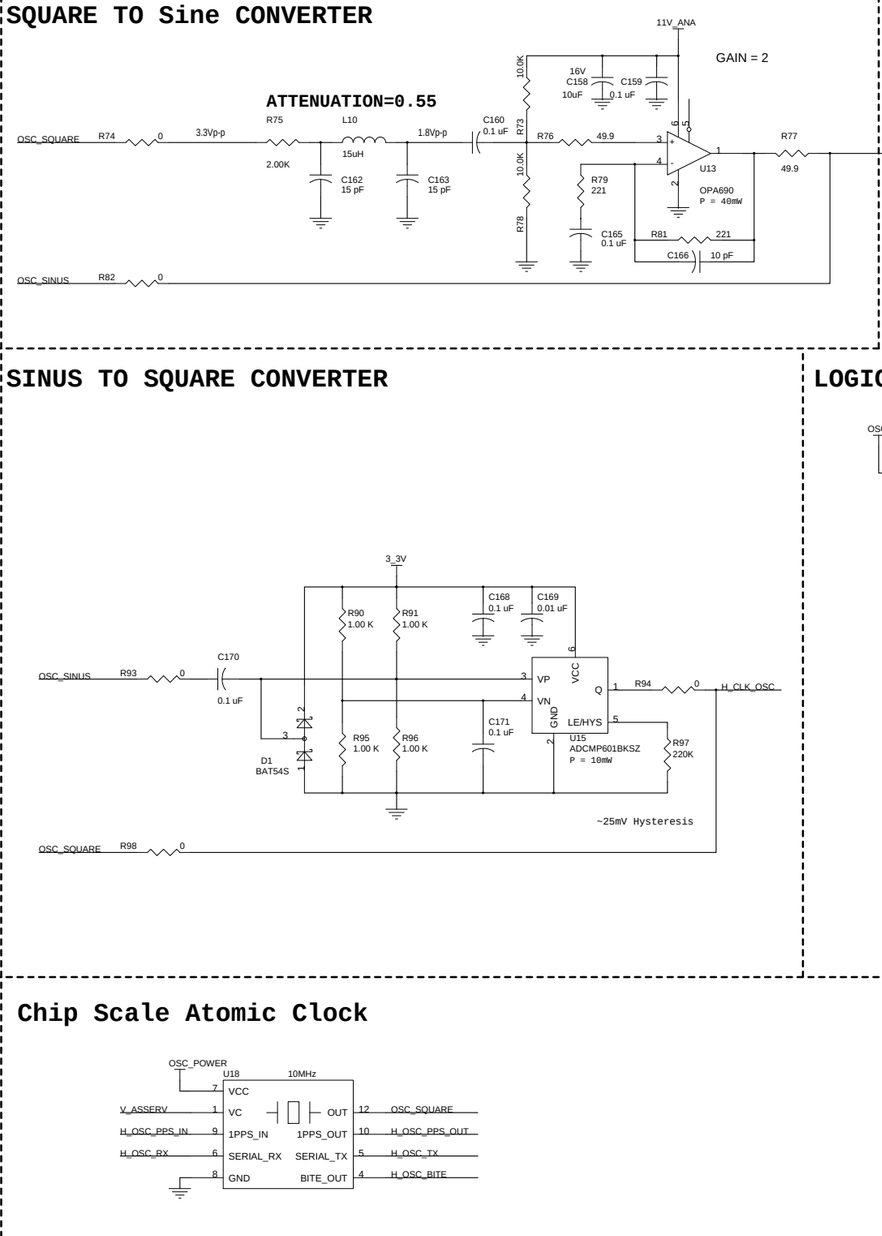
OCXO



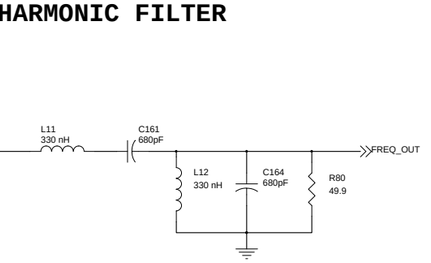
OSCILLATOR CONTROL VOLTAGE



SQUARE TO Sine CONVERTER



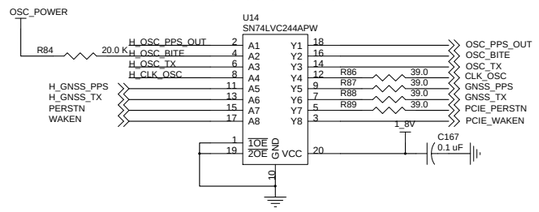
HARMONIC FILTER



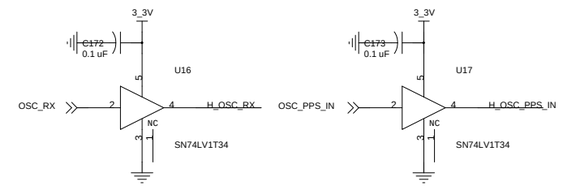
SINUS TO SQUARE CONVERTER

LOGIC VOLTAGE-LEVEL TRANSLATOR

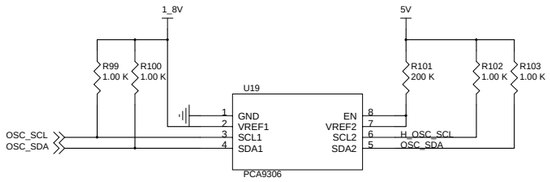
From 5V/3.3V to 1.8V



From 1.8V to 3.3V



I2C VOLTAGE-LEVEL TRANSLATOR



Chip Scale Atomic Clock

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TIMING

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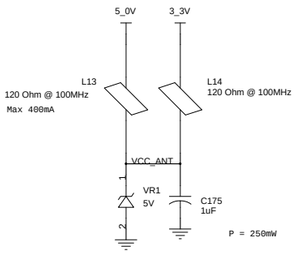
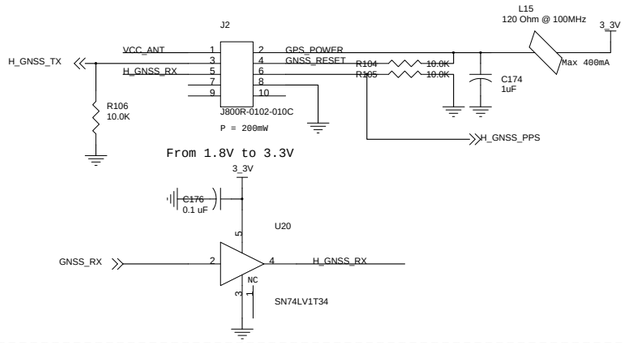
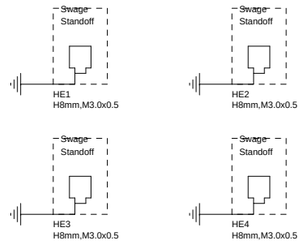
ANTENNA POWER SUPPLY



GNSS RECEIVER



GNSS STANDOFF



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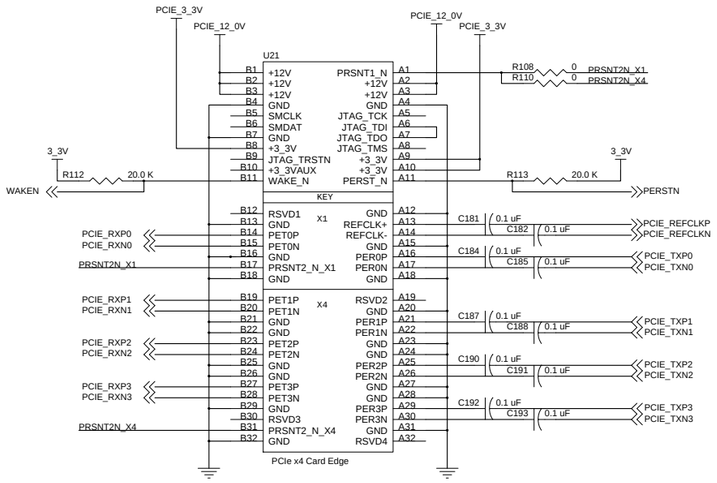
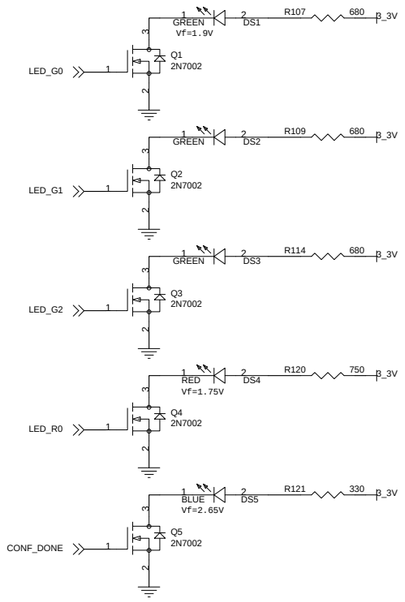
PCIe CONNECTOR



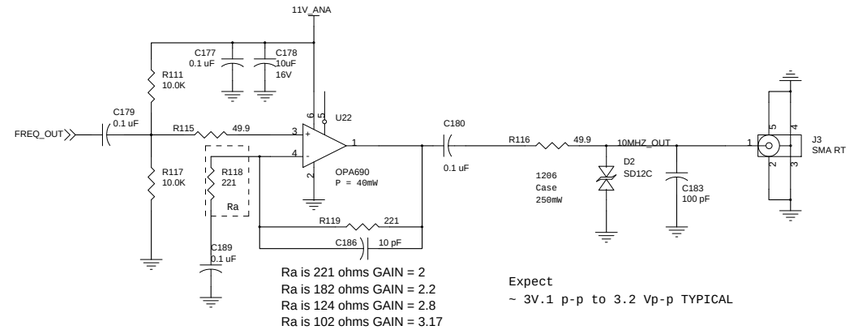
LED

P = 33mW



FREQ OUTPUT DRIVER

10MHZ OSC Buffer Driver

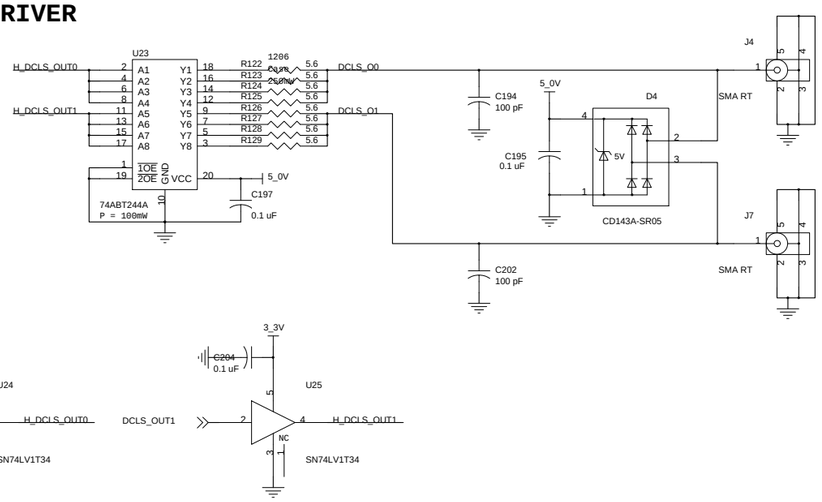


Ra is 221 ohms GAIN = 2
Ra is 182 ohms GAIN = 2.2
Ra is 124 ohms GAIN = 2.8
Ra is 102 ohms GAIN = 3.17

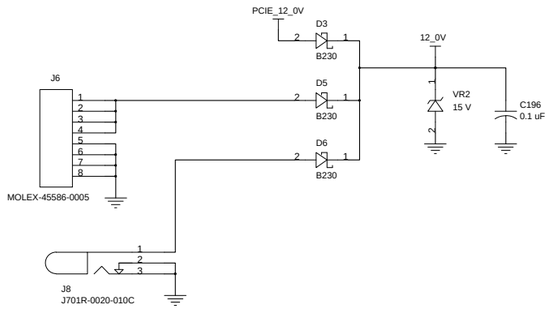
Expect
~ 3V.1 p-p to 3.2 Vp-p TYPICAL

Ra = 221 ohms for Y100R-0002-PH05, Y100R-0002-PH10
Ra = 182 ohms for Y100R-0002-TS01
Ra = 124 ohms for Y100R-0002-PH15, Y100R-0002-PH17
Ra = 102 ohms for Y100R-0002-PH13

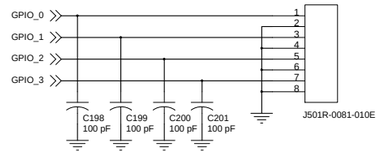
DCLS OUTPUT DRIVER



POWER CONNECTOR



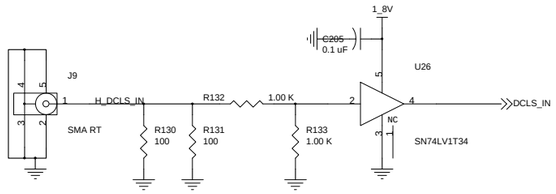
GPIO



BRACKET HOLES / MOUNT HOLES

DCLS INPUT DRIVER

From 5V input to 1.8V



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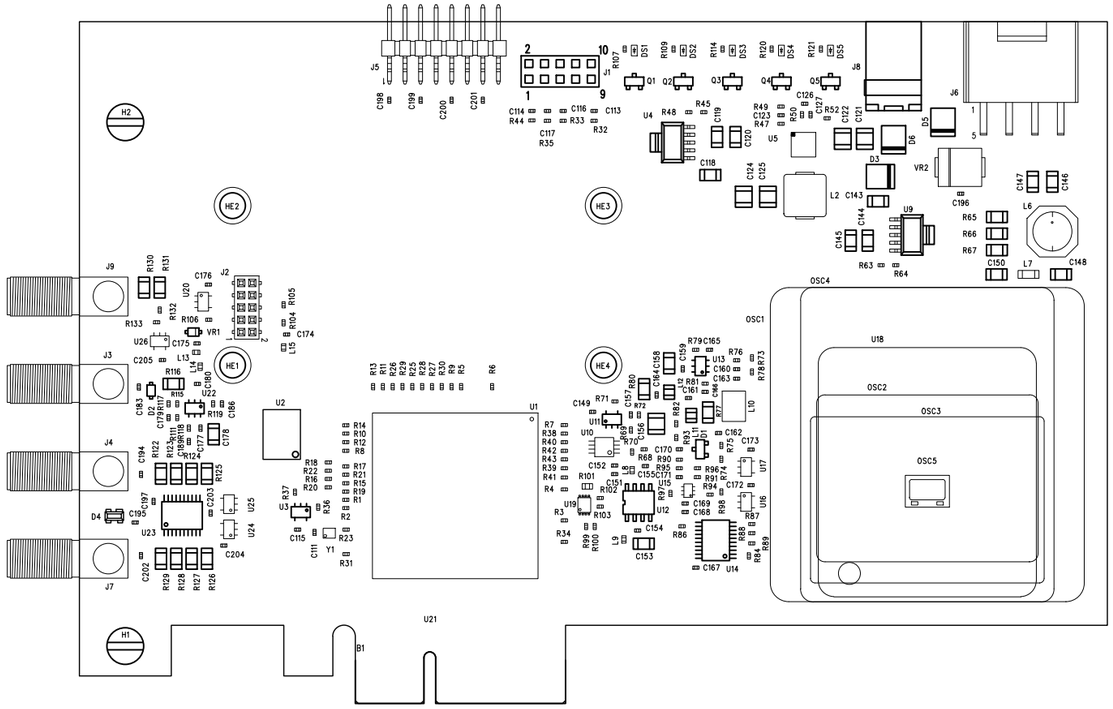
1			



UNLESS OTHERWISE SPECIFIED:		NAME	DATE
	DRAWN	H ECHELARD	03/02/2021
MATERIAL: PCB			
FINISH			

CHANGE RESTRICTED
NO MANUAL CHANGES

THIRD ANGLE PROJECTION

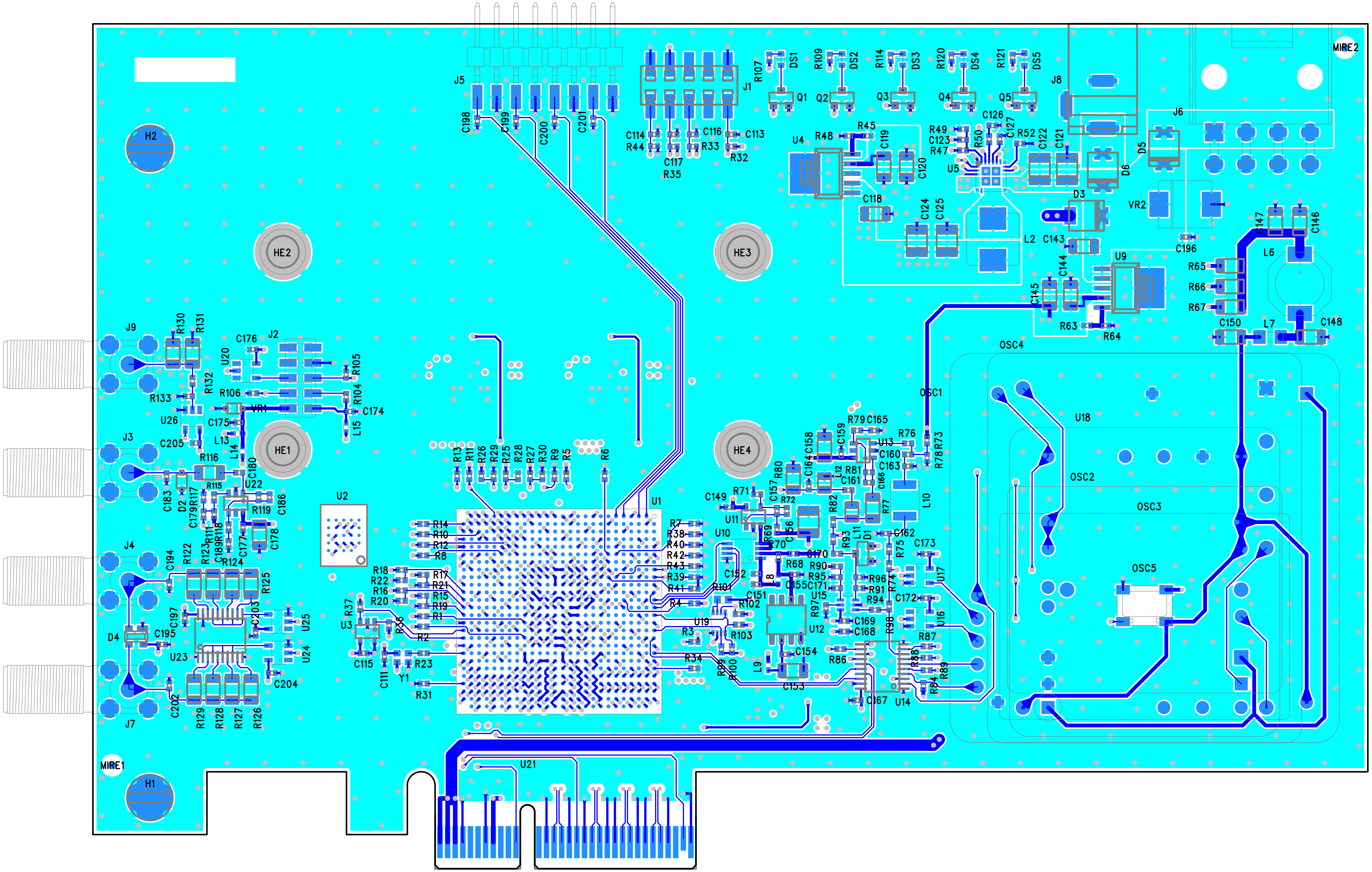
OROLIA FRANCE

PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

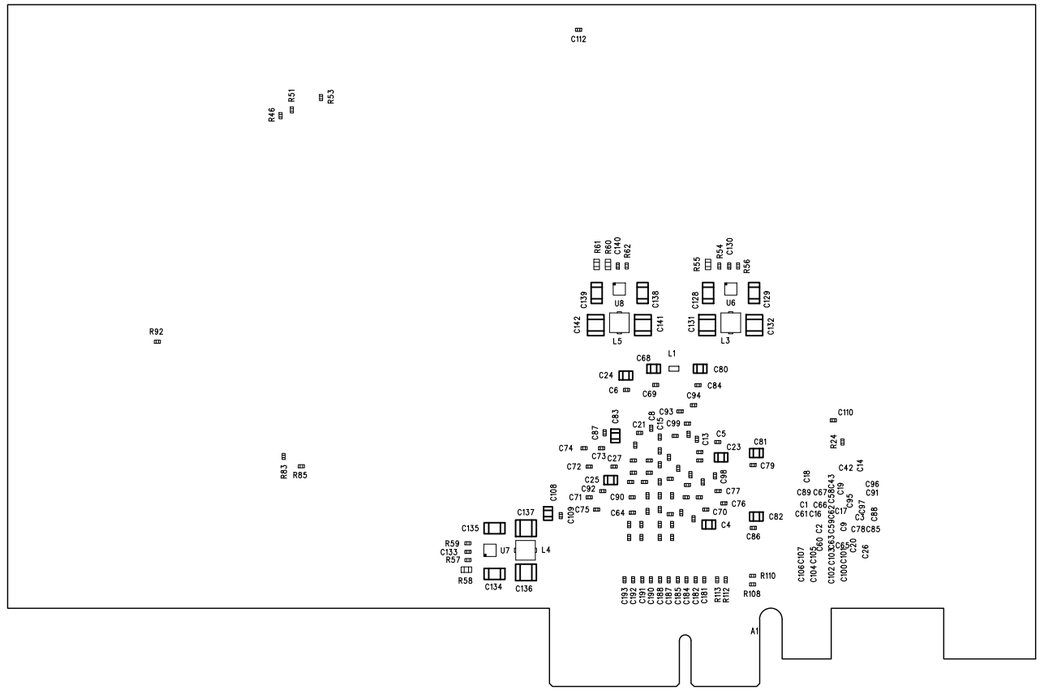
SIZE	DWG. NO.	REV
A3	ART_CARD_PCB	1

SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1

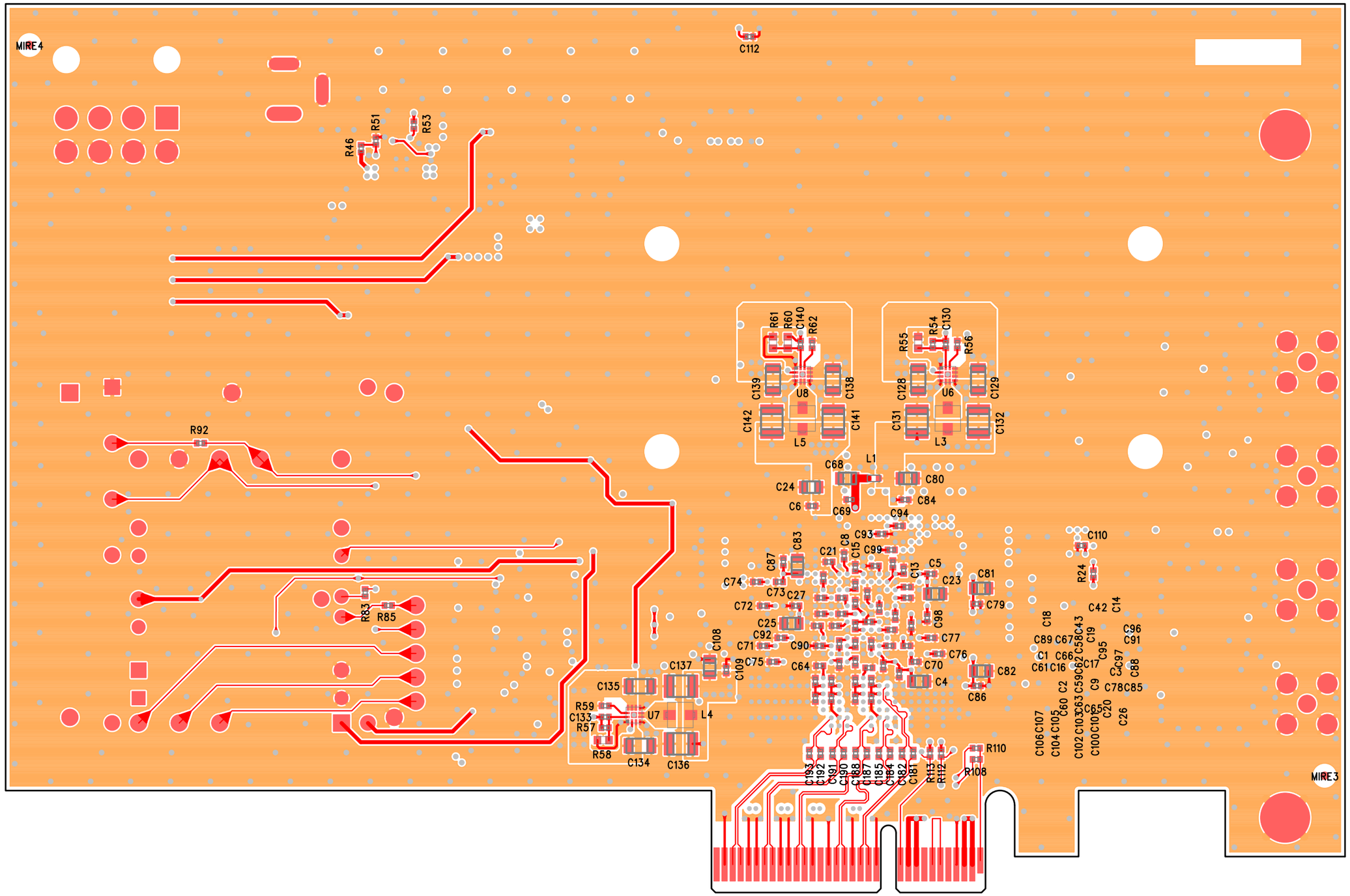


MIRE1
MIRE2
H1
H2
HE1
HE2
HE3
HE4
J1
J2
J3
J4
J5
J6
J7
J8
J9
U1
U2
U3
U4
U5
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
OSC1
OSC2
OSC3
OSC4
OSC5
DS1
DS2
DS3
DS4
DS5
Q1
Q2
Q3
Q4
Q5
D1
D2
D3
D4
D5
D6
VR1
VR2
Y1
L2
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15

Rev	DESCRIPTION	DATE	APPROVED
1			



UNLESS OTHERWISE SPECIFIED:		NAME	DATE	OROLIA FRANCE
	DRAWN	H ECHELARD	03/02/2021	PART NUMBER: ART_CARD_PCB
	THE INFORMATION CONTAINED IN THIS DOCUMENT IS THE SOLE PROPERTY OF OROLIA. ANY REPRODUCTION, DISCLOSURE OR MANUFATURE OF THIS INFORMATION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF OROLIA GROUP IS PROHIBITED.			TITLE: ART_CARD
MATERIAL: PCB	CHANGE RESTRICTED NO MANUAL CHANGES			SIZE A3 / DWG. NO. ART_CARD_PCB / REV 1
FINISH	THIRD ANGLE PROJECTION			SCALE: 1:1 / DO NOT SCALE / SHEET 1 OF 1


MIRE4
C112
R46
R51
R53
R61
R60
C140
R62
R55
R54
C130
R56
C139
U8
C138
U6
C128
C129
C142
C141
C131
C132
L5
L3
L1
C68
C24
C80
C6
C84
C69
C94
C93
C110
C83
C8
C87
C21
C15
C99
C13
C5
C74
C23
C81
C73
C27
C79
R24
C72
C42
C14
C25
C98
C18
C43
C92
C77
C89
C67
C58
C19
C96
C71
C90
C76
C1
C66
C95
C91
C108
C109
C75
C64
C70
C61
C16
C62
C17
C97
C88
C137
C82
C4
C59
C9
C78
C85
C135
C86
C2
C63
C20
R59
C133
U7
L4
C65
C26
R57
C60
C107
C106
C105
C103
C102
C104
C100
C101
R58
C134
C136
C193
C192
C191
C190
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C185
C184
C182
C181
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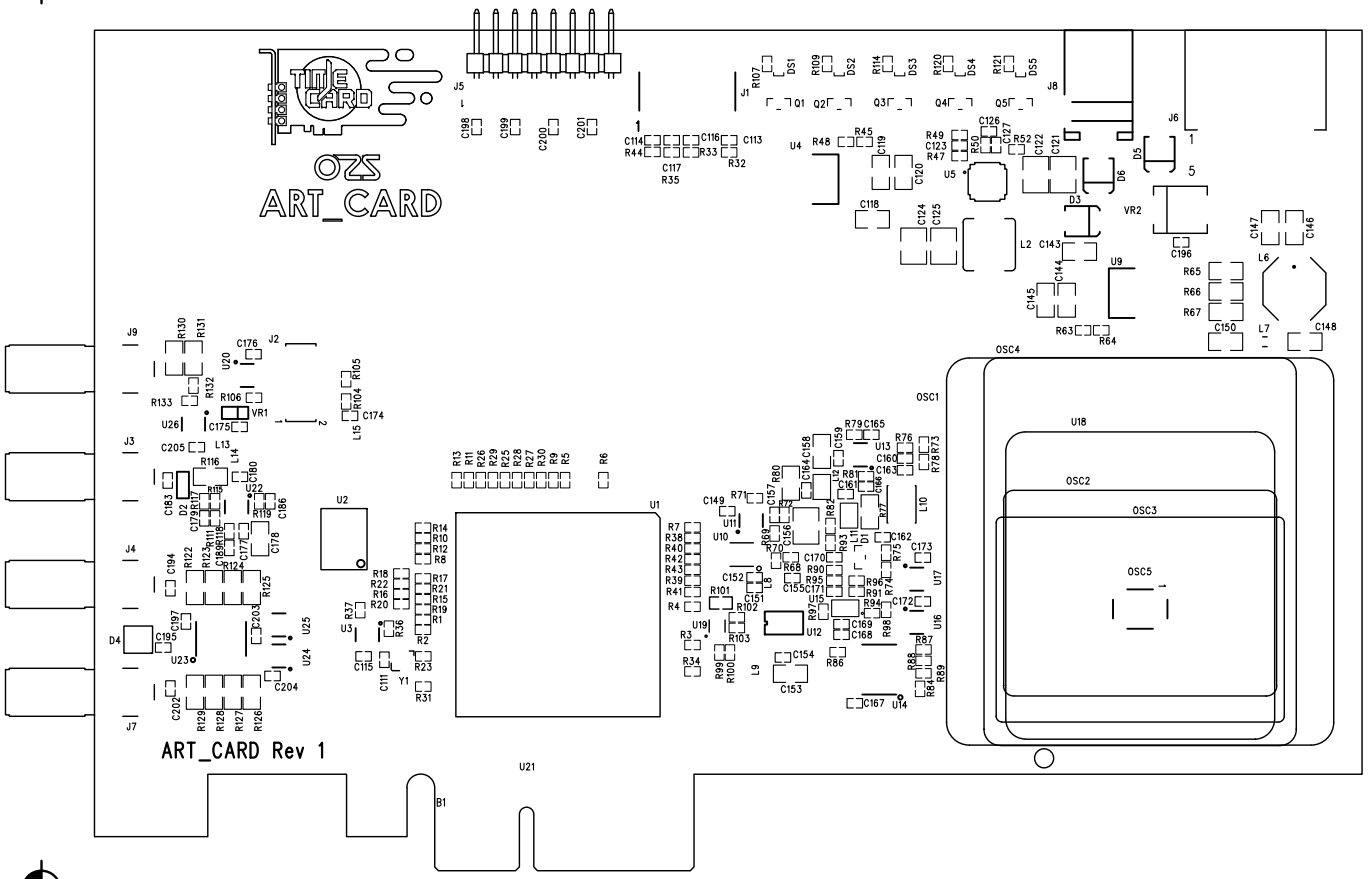
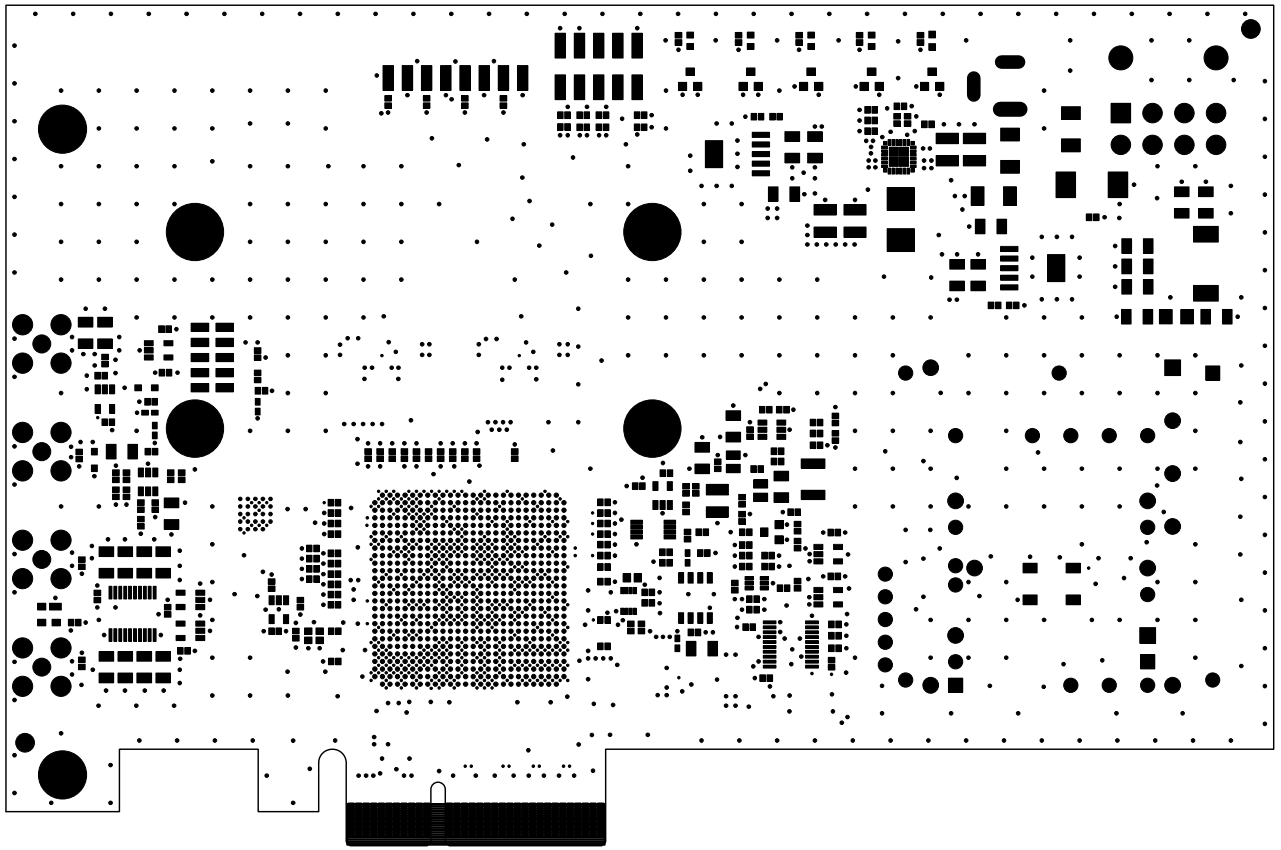
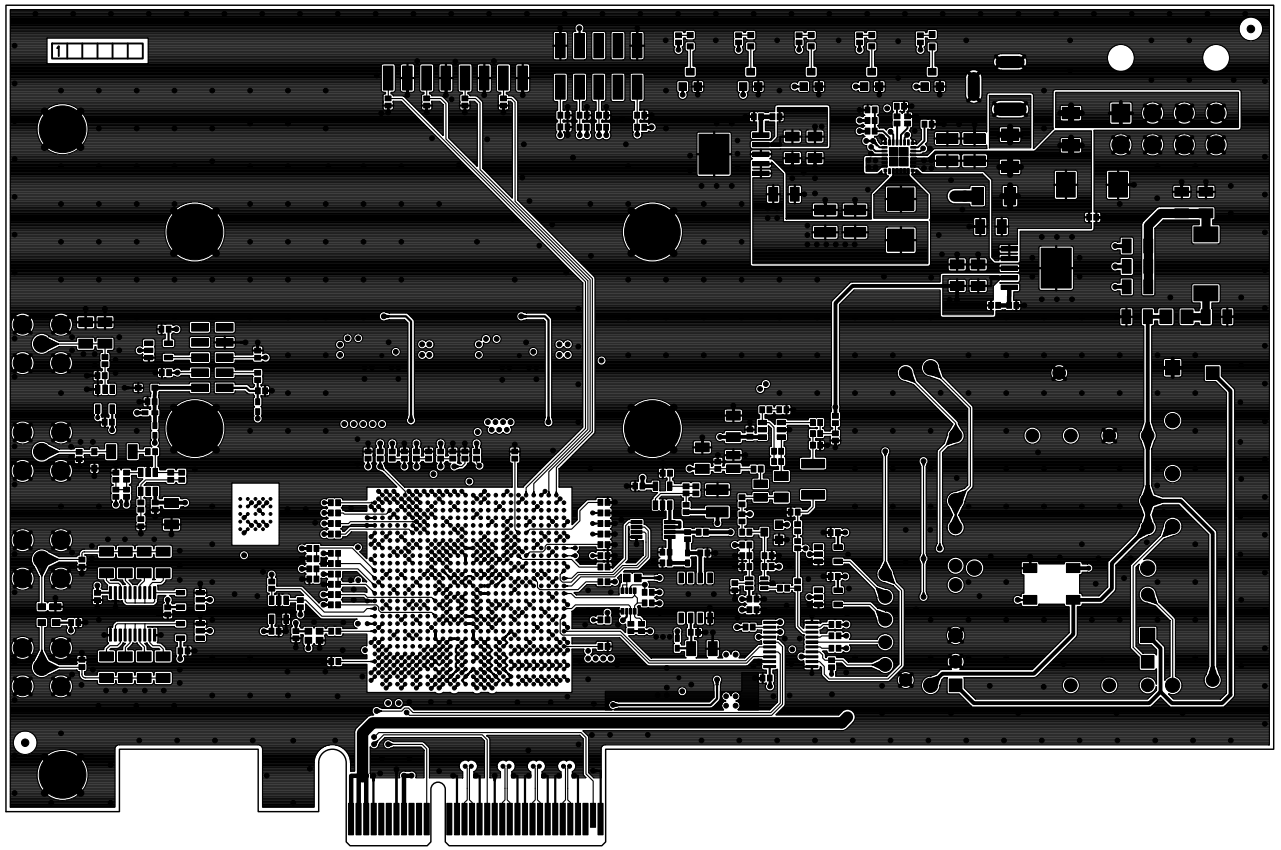
R110
R108
R92
R83
R85
MIRE3



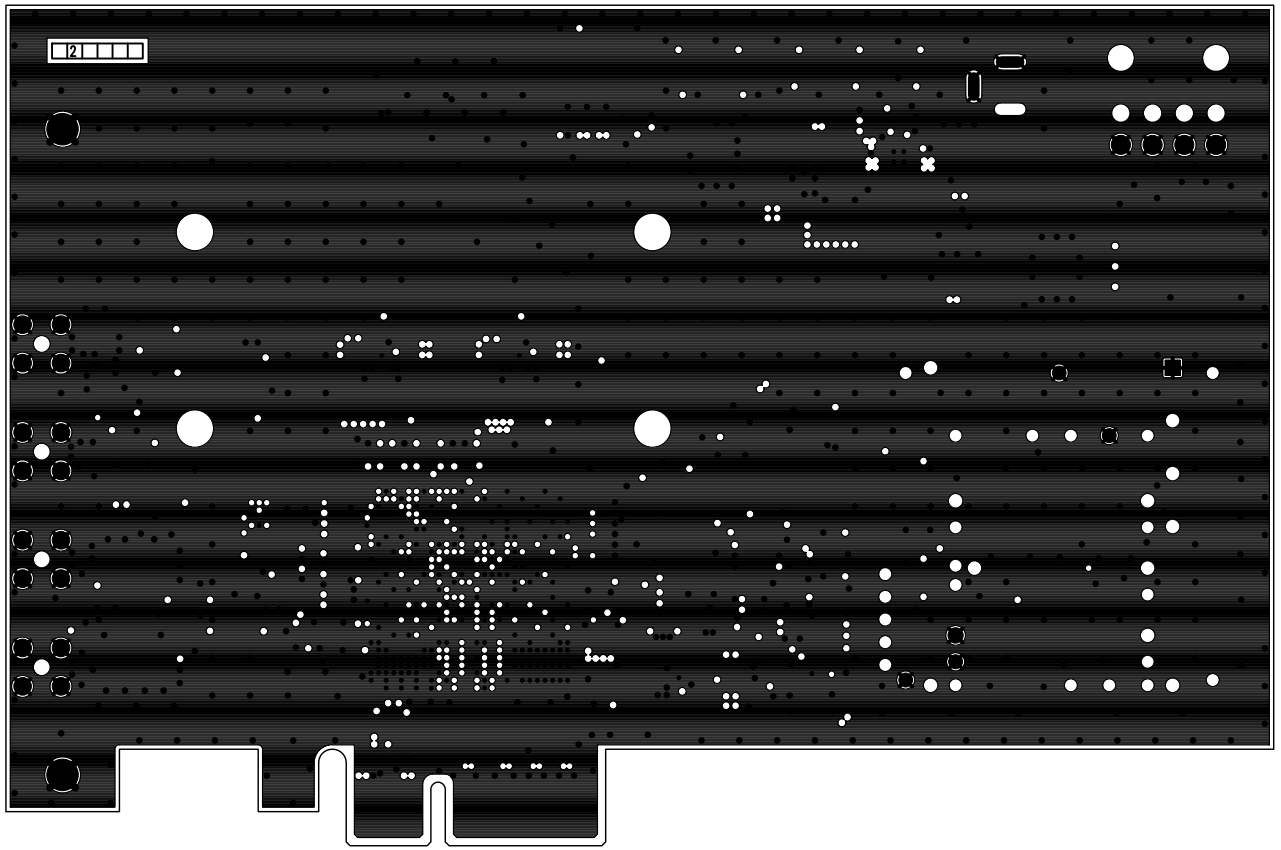
SILKSCREEN TOP	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



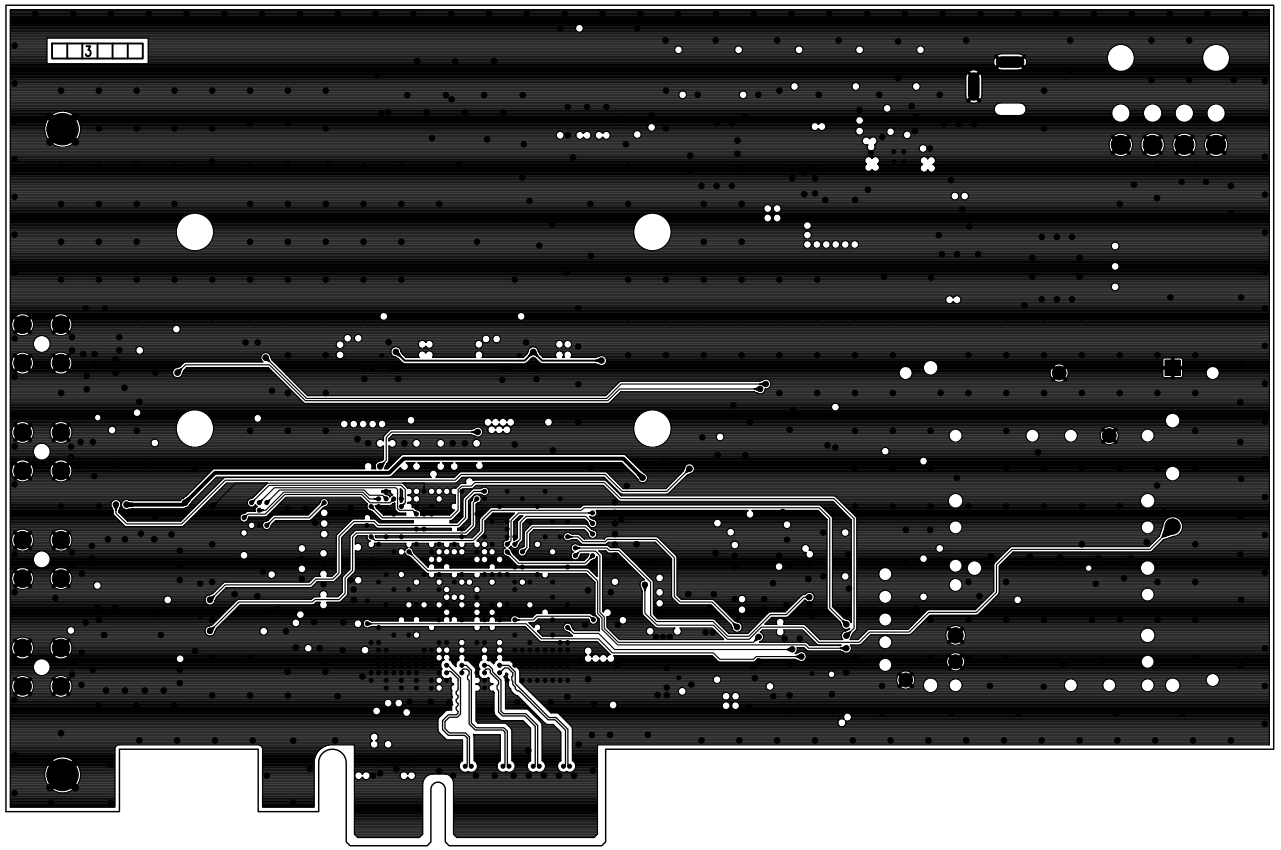
SOLDER MASK TOP	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



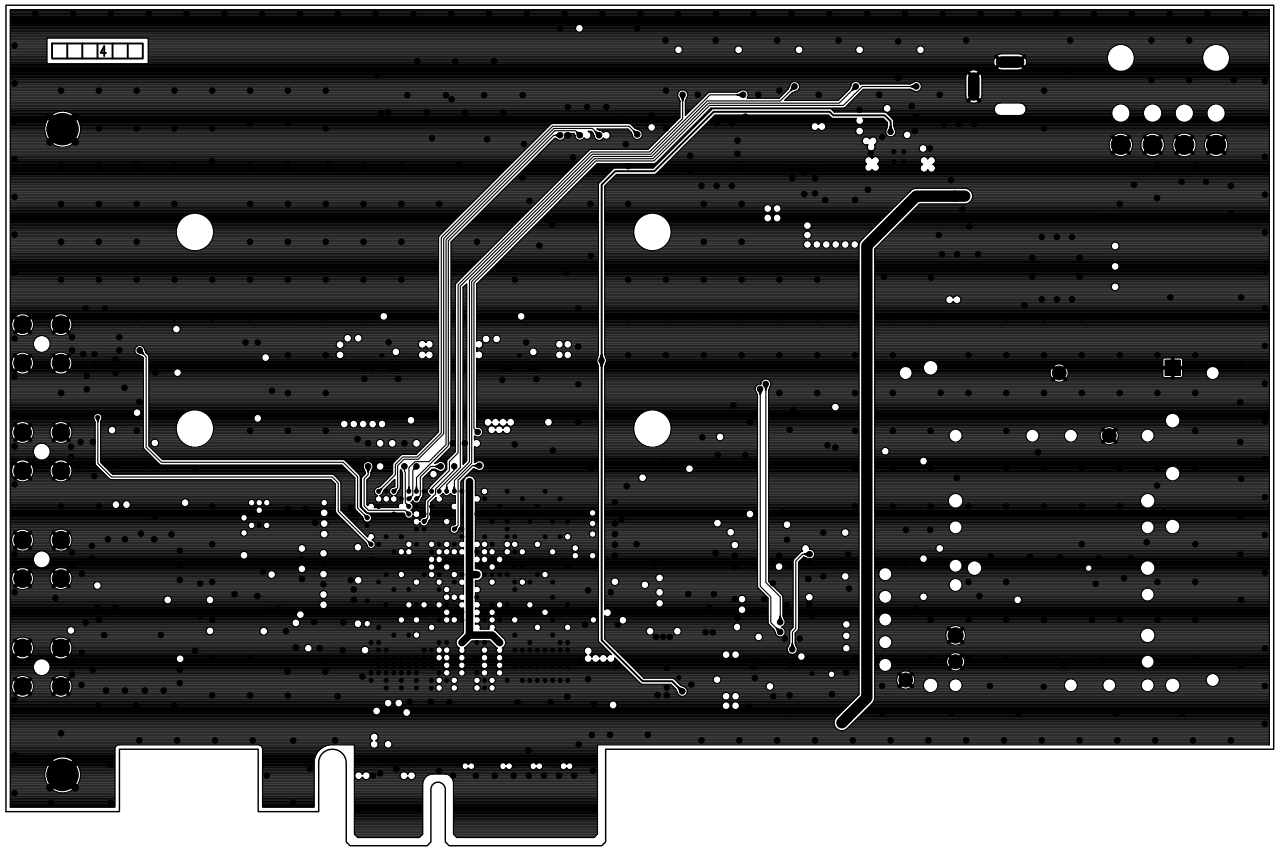
TOP LAYER	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



INTERNAL 1 LAYER	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



INTERNAL 2 LAYER	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



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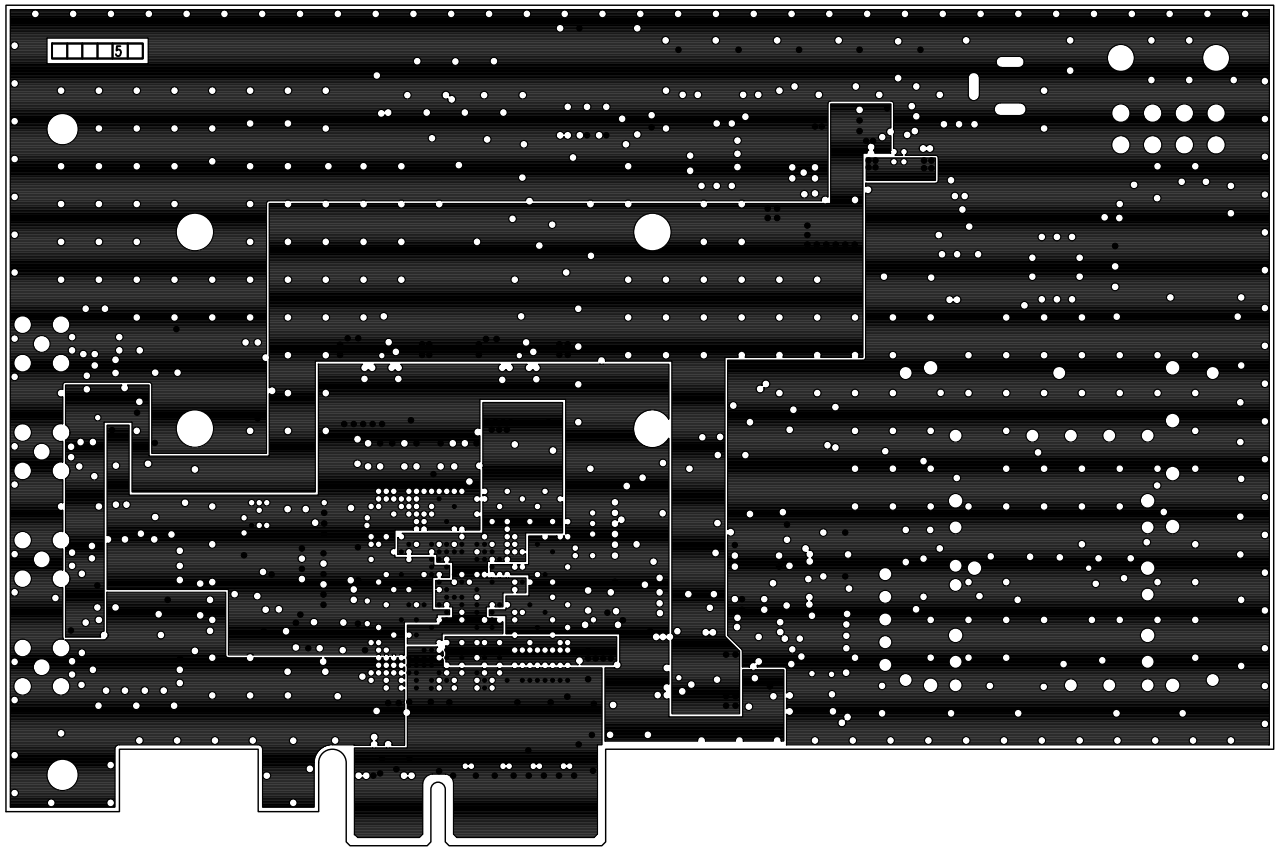
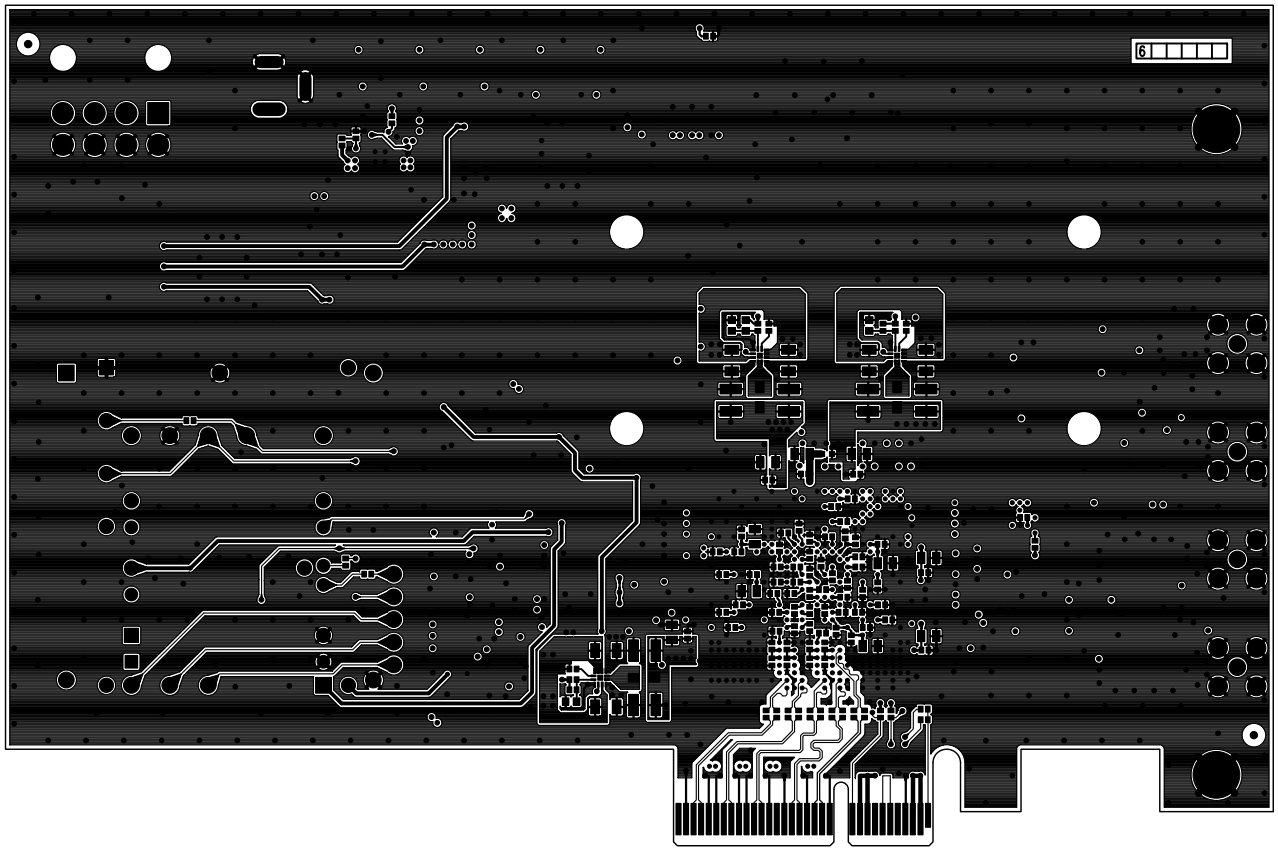
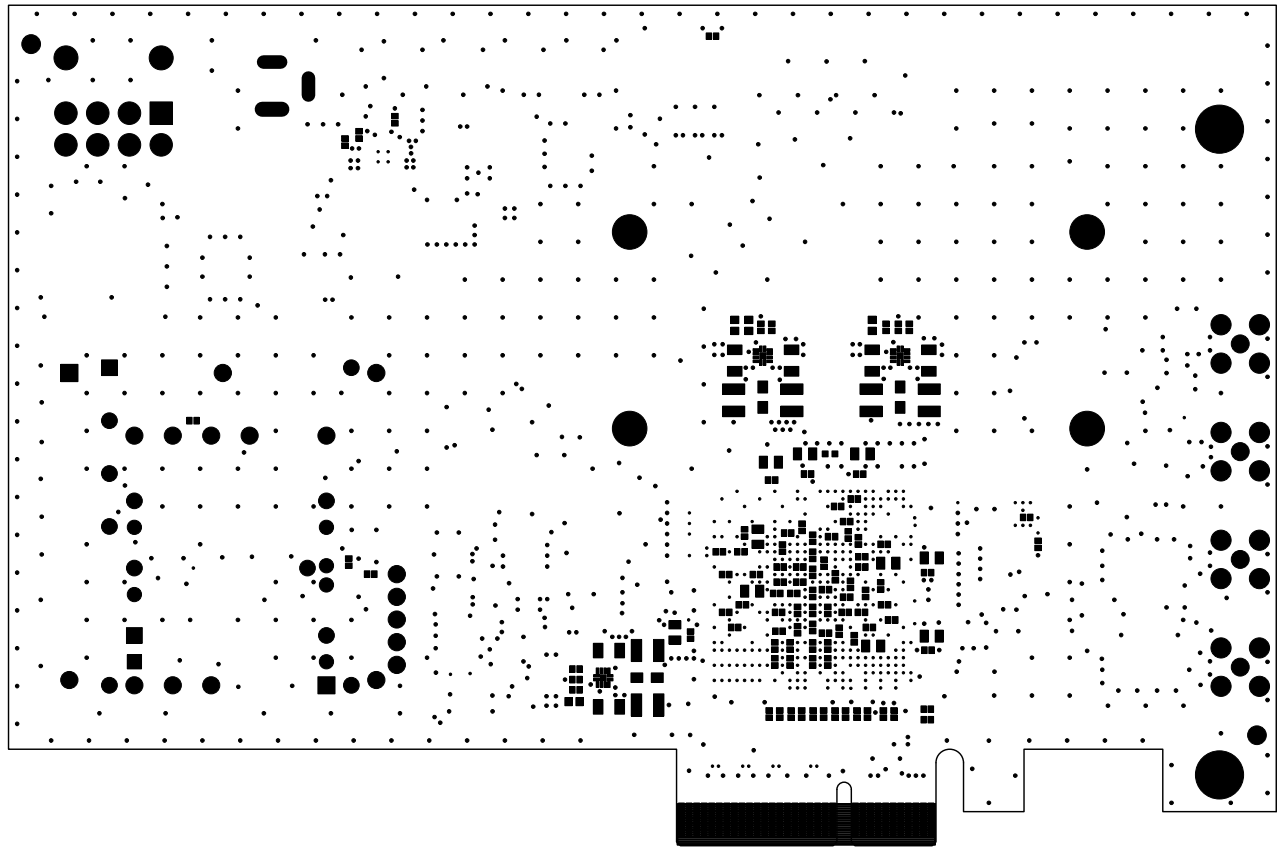
FILE: ART_CARD REV 1	02/04/21



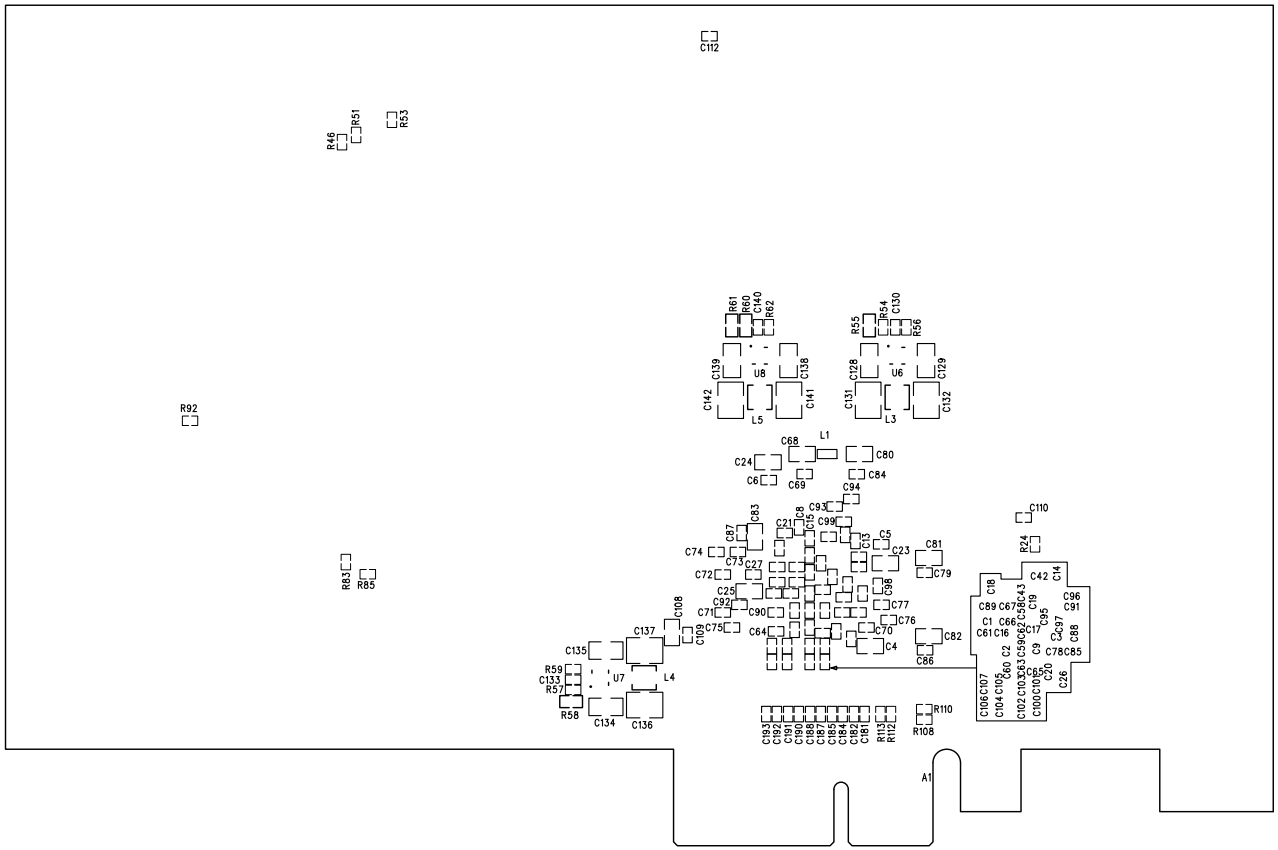
FILM: COUCHE INTERNE 4	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



BOTTOM LAYER	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



SOLDER MASK BOTTOM	ARTEMIS
FILE: ART_CARD REV 1	02/04/21



SILKSCREEN BOTTOM	ARTEMIS
FILE: ART_CARD REV 1	02/04/21

Rev	DESCRIPTION	DATE	APPROVED
1			

NOTES:

1. FABRICATE BOARD PER:
Latest revision of IPC-A-600 Class 2. Electrical integrity testing required, per section 5.2 of IPC-A-600.

2. MATERIAL : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
Rigid laminate and prepeg shall be per IPC-4101/99/101/126. As described in the StackUp.
Laminate must meet latest RoHS directive subject to Orolia Engineering Approval.

3. FINISH : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
ENIG (Electroless Nickel, Immersion Gold) per IPC-4552

4. SOLDER MASK : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
LPI per IPC-SM-840 (current rev) COLOR : GREEN
Soldermask provided as 1 to 1 and shall be oversized at the fabricator as required in order to insure that soldermask does not encroach upon thru hole and SMT pads.
0.008 DIA Vias shall be plugged/tented from top and bottom side per artwork supplied unless mask is removed by artwork. These vias are required to be filled and copper capped. It is acceptable to use and epoxy fill after initial plating, followed by a copper cap process to cap the via fill.
Continuous copper plate is required.

5. SILKCREEN : MUST BE "LEAD-FREE PROCESS COMPATIBLE"
White (All silkscreen to be removed from any exposed plated areas)

6. DIMENSIONING AND TOLERANCING PER ANSI-Y-14.5 (LATEST REV).

7. 94V-0 Min is required and shall be marked on top or bottom side silkscreen or copper

8. All copper on any layer shall be trimmed back 0.015 from the board edge as required.

9. All internal unused pads shall be removed

10. Teardrops shall be added where possible

11. All holes sizes shown are expected finished hole sizes after processing.

12. This board shall be supplied in array format that shall be determined/approved by the purshaser of the bare board

SIZE	QTY	SYM	PLATED	TOL
0.25	331	□	YES	+/-0.1
0.4	871	+	YES	+/-0.1
0.8 x 3.05	2	+C	YES	+/-0.1
1 x 3.56	1	+D	YES	+/-0.1
1.1	26	⧖	YES	+/-0.1
1.3	13	⋈	YES	+/-0.1
1.6	4	+A	YES	+/-0.1
1.7	16	◇	YES	+/-0.1
1.8	8	+E	YES	+/-0.1
3.5	2	×	YES	+/-0.1
3	2	+F	NO	+/-0.1
4.4	4	+B	NO	+/-0.1

UNLESS OTHERWISE SPECIFIED:

MATERIAL
PCB

FINISH

	NAME	DATE
DRAWN	H ECHELARD	03/02/2021

CHANGE RESTRICTED
NO MANUAL CHANGES

THIRD ANGLE PROJECTION

OROLIA FRANCE

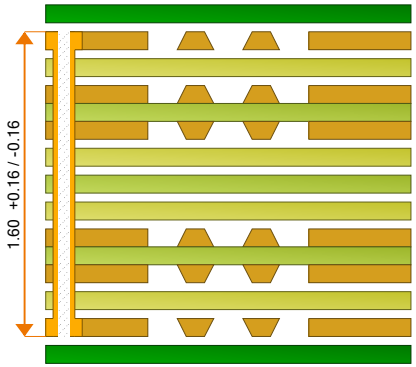
PART NUMBER: ART_CARD_PCB

TITLE: ART_CARD

SIZE A3 | DWG. NO. ART_CARD_PCB | REV 1

SCALE: 1:1 | DO NOT SCALE | SHEET 1 OF 1

Layer	Stack up	Supplier	Description	Supplier Description	Type	Base Thickness	Finish Thickness	Mask Thickness	εr	Loss Tangent	Resin Content	Impedance ID
			Solder resist	LPI	Solder resist			0.020	4.100	0.0000		
1			Foil	17um Copper Foil	Foil	0.018	0.040					1, 2
		VENTEC	VT47-2113	VT-47	PREPREG	0.106	0.095		4.060	0.0000	57.000	
2						0.017	0.017					
		VENTEC	VT-47	0.127mm	Core	0.127	0.127		4.350	0.0000	0.000	
3						0.017	0.017					3, 4
		VENTEC	VT47-2116	VT-47	PREPREG	0.132	0.121		4.150	0.0000	54.000	
		VENTEC	VT-47	0.711mm	Core	0.711	0.711		4.400	0.0000	0.000	
		VENTEC	VT47-2116	VT-47	PREPREG	0.132	0.121		4.150	0.0000	54.000	
4						0.017	0.017					5, 6
		VENTEC	VT-47	0.127mm	Core	0.127	0.127		4.350	0.0000	0.000	
5						0.017	0.017					
		VENTEC	VT47-2113	VT-47	PREPREG	0.106	0.095		4.060	0.0000	57.000	
6			Foil	17um Copper Foil	Foil	0.018	0.040					7, 8
			Solder resist	LPI	Solder resist			0.020	4.100	0.0000		



Copper Thickness = 0.148 | Dielectric Thickness = 1.399 | Solder Mask Thickness = 0.040 | Stack Up Thickness = 1.546 | Stack Up Thickness with Soldermask = 1.586

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 2 in Layer	Ref. Plane 1 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)	Coating Between Traces (C3)
1		Coated Microstrip 1B	1	0	2	0.150	0.000	0.000	0	50.090	50.000	10.000	0.000
2		Edge Coupled Coated Microstrip 1B	1	0	2	0.150	0.150	0.000	0	87.470	85.000	10.000	0.020
3		Offset Stripline 1B1A	3	5	2	0.160	0.000	0.000	0	50.950	50.000	10.000	0.000
4		Edge Coupled Offset Stripline 1B1A	3	5	2	0.160	0.150	0.000	0	85.010	85.000	10.000	0.000
5		Offset Stripline 1B1A	4	5	2	0.160	0.000	0.000	0	50.950	50.000	10.000	0.000
6		Edge Coupled Offset Stripline 1B1A	4	5	2	0.160	0.150	0.000	0	85.010	85.000	10.000	0.000
7		Coated Microstrip 1B	6	0	5	0.150	0.000	0.000	0	50.090	50.000	10.000	0.000

StackName: Ouestronic_PCI Express_246183-Q_6L_VT47	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 1/2
Date: 28/01/2021	Associated Documents:					
Author: Mostefa Abdali						
Department: IDS						
Site: Tewkesbury						

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 2 in Layer	Ref. Plane 1 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)	Coating Between Traces (C3)
8		Edge Coupled Coated Microstrip 1B	6	0	5	0.150	0.150	0.000	0	87.470	85.000	10.000	0.020

Column Position	Drill Image	1st Layer	2nd Layer	Drill Type	Minimum Size	Fill Type	Data Filenames	Minimum Pad Size
1		1	6	Mechanical PTH	0.250	None		0.500

Notes

StackName: Ouestronic_PCI Express_246183-Q_6L_VT47	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 2/2	
Date: 28/01/2021	Associated Documents:						
Author: Mostefa Abdali							
Department: IDS							
Site: Tewkesbury							

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Phone : +33(0)2-41-48-98-68
p.benoit@artemis-cad.com
www.artemis-cad.com

TECHNICAL SPECIFICATION

IPC-A-600

CUSTUMER : OROLIA
MANUFACTURER :

PCB Reference :	ART_CARD	**Index :**	Rev 1

☑ **PCB Unit**	**Unit PCB dimensions :**	167.65	X	106.65	mm	
☐ **Panel PCB :** 0	**Panel dimensions :**	0	X	0	mm	
Material : FR4	**Surface :**	1.79 **dm²**	**Track / Gap :**	0.15	/	0.15 mm

PCB Type :	MC6	Finish Copper Thikness (µm) :	12µ	17,5µ	35µ	40µm
PCB Thickness (mm) :	16/10	External Layer :	☐	☐	☐	☑
		Intern Layer :	☐	☑	☐	☐

Technology	☑ Plated Trough Hole	**Via type :**	Hole / pads ratio : 0,25/0,55
☑ Traditional	☐ Press-fit Hole	☑ Traditional Via	☐ Via in pad
☑ SMT	☐ Autre	☐ Laser Via	☐ Stacked ☐ Staggered
Surface Treatement Finished		☐ Blinded Via	Couche départ et d'arrivée
☑ Ni/Au Chemical	☐ Sn/Pb surfondu	☐ Buried Via	Couche départ et d'arrivée
☐ Sn/Cu HAL	☐ Autre	☐ Filled Via	☐ Resin ☐ Copper

Peelable Solder Mask	☐ Standard		☐ TOP	☐ BOTTOM
Solder Mask	☑ Photo-imageable	Green	☑ TOP	☑ BOTTOM
Silkscreen	☑ Ink	White	☑ TOP	☑ BOTTOM
Electrical Test			☑ Yes	☐ No

☑ **Impedance control :**	☑ Produced	☐ Measured
50 ohms on layer 1, 3 and 4		
☑ **Differential Pairs :**	☑ Produced	☐ Measured
85 ohms on layer 1, 3 and 6		
☑ **Stack-up :**	Ouestronic_PCI Express_246183-Q_6L_VT47.pdf	
☐ **Milling**	Milling Diameter : 0 mm	

Comments :