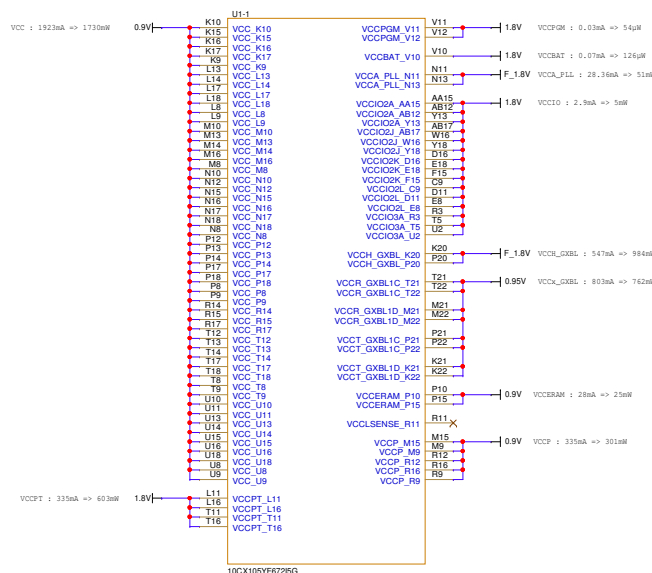
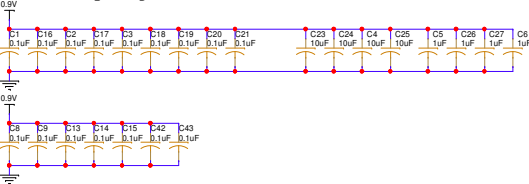


orolia		
Title: <b>OVERVIEW</b>		
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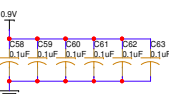
FPGA POWER SUPPLY



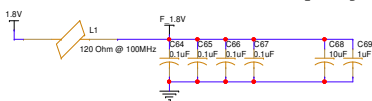
VCC Decoupling



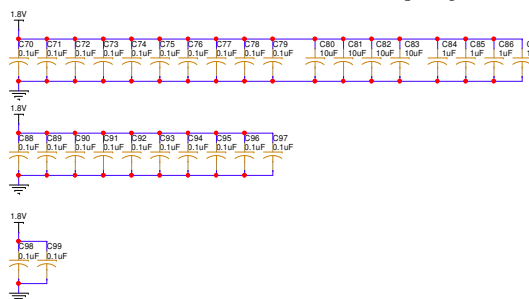
VCCP and VCCERAM Decoupling



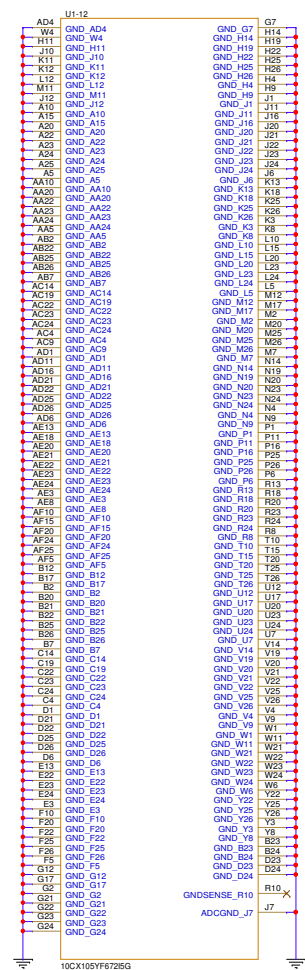
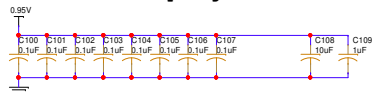
VCCA\_PLL and VCCB\_GXBL Decoupling



VCCPT, VCCPGM, VCCBAT and VCCIO Decoupling



VCCR/VCCT Decoupling



**FPGA**

**EEPROM WITH UNIQUE ID**

**JTAG**

**CLOCK**

**FPGA CONFIGURATION**

**orolia**

**ART CARD**

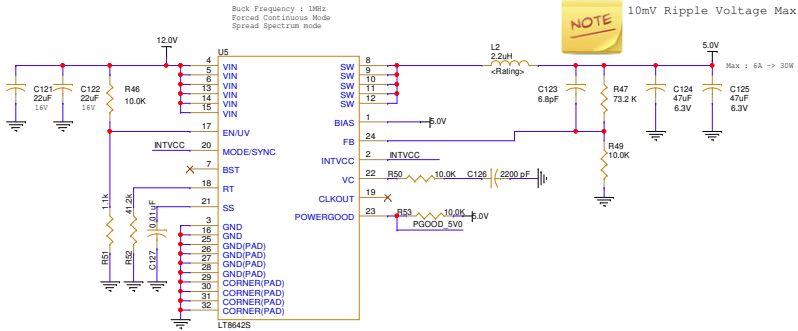
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ART\_CARD

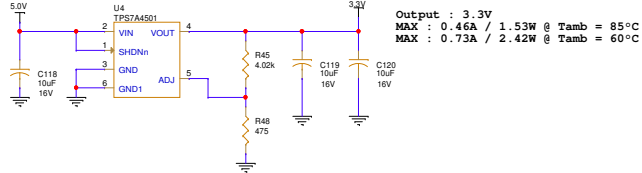
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POWER NEED	:	FPGA	:	OCXO	:	Comp	:	TOTAL	
On 12V	:	:	:	7500	:	:	:	7500	mW
On 11V_ANA	:	:	:	:	:	80	:	80	mW
On 5.0V	:	:	:	:	:	350	:	350	mW
On 3.3V	:	:	:	:	:	243	:	243	mW
On 1.8V	:	1643	:	:	:	61	:	1704	mW
On 0.95V	:	762	:	:	:	:	:	762	mW
On 0.9V	:	2056	:	:	:	:	:	2056	mW
								-> 12695	mW

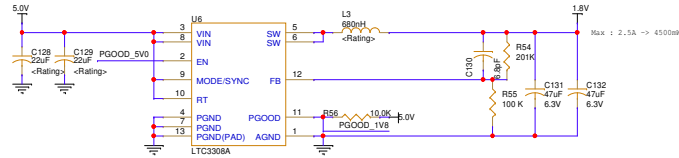
## 12V to 5V Switch Converter



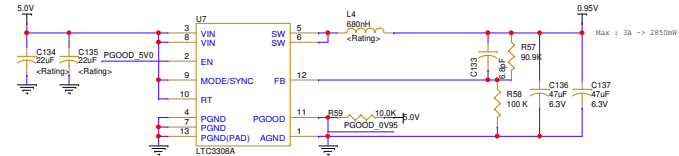
## 5V to 3.3V LDO Converter



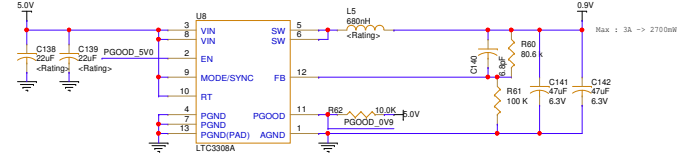
## 5V to 1.8V Switch Converter



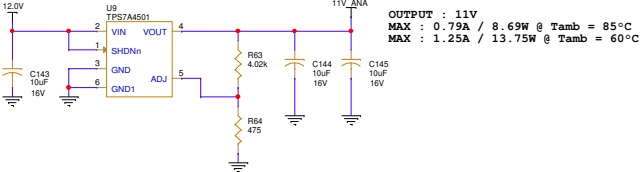
## 5V to 0.95V Switch Converter



## 5V to 0.9V Switch Converter



## ANALOG POWER SUPPLY



**DEFAULT**



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# OSCILLATOR POWER SUPPLY

3.3V 5.0V 11V ANA

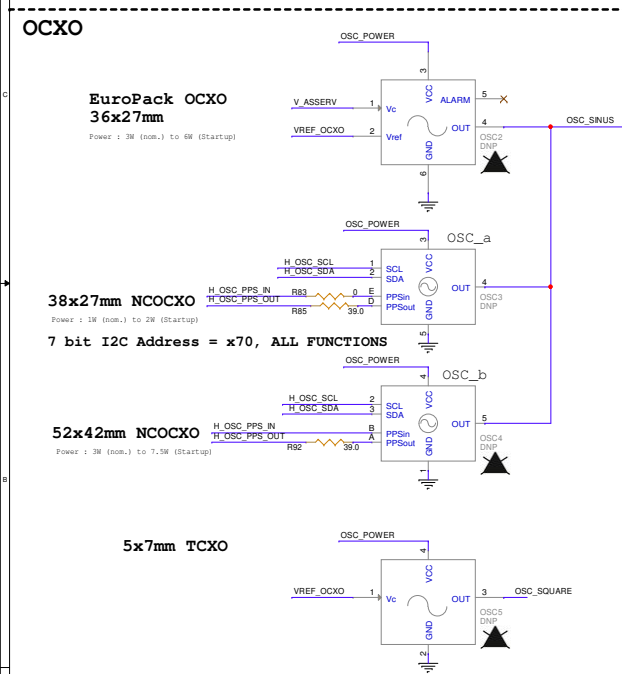
1206 C165 250nF 1206 C166 0 1206 C167 0 1206 C168 0

OSC\_POWER

Fc ~ 100kHz

L6 15uH 2A L7 120 Ohm @ 100MHz 5A

C146 22uF 25V C147 22uF 25V C148 22uF 25V C150 22uF 25V



## I2C VOLTAGE-LEVEL TRANSLATOR

The diagram illustrates the connection of a PCA9306 I2C voltage-level translator. The chip is shown with its pins and internal components. The input side (left) is connected to a 1.8V supply and includes a 100k pull-up resistor (R99) and a 100k resistor (R100). The output side (right) is connected to a 5V supply and includes a 100k pull-up resistor (R101), a 100k resistor (R102), and a 100k resistor (R103). The chip's pins are labeled: 1 (GND), 2 (VREF1), 3 (SCL1), 4 (SDA1), 5 (SCL2), 6 (SDA2), 7 (EN), and 8 (VREF2). The chip is identified as PCA9306.

## OSCILLATOR CONTROL VOLTAGE

DAC\_SPL\_MOSI  
DAC\_SPL\_CLK  
DAC\_SPL\_CS $\bar{n}$

11V\_ANA

120 Ohm @ 100MHz  
L9  
Max 400nA

C153 10uF 16V  
C154 0.1 uF

3V Ref

U12  
VIN  
VOUT  
TRIM  
TP  
GND  
ADR443  
NC  
NC

VREF\_OCXO  
R88  
VREF\_DAC  
R70

L8 120 Ohm @ 100MHz  
Max 400nA

16 Bit DAC

U10  
DIN  
VDD  
VOUT  
VREF  
VFB  
GND  
DAC6551

C151 0.1 uF 6.3V  
C152 0.1 uF

VDAC

U11  
ADA4084-1  
VOUT  
VASSERV  
R69  
221  
V\_ASSERV  
C156 22uF

NOTE  
disciplining voltage 0V to 5V

C157 100 nF  
R71 15.0k  
R72 10.0k

# SQUARE TO Sine CONVERTER

# SINUS TO SQUARE CONVERTER

# HARMONIC FILTER

The diagram illustrates a harmonic filter circuit. The input signal passes through a series combination of inductor L11 (330 nH) and capacitor C161 (680pF). Following C161, the circuit branches into two parallel paths. The first path contains inductor L12 (330 nH). The second path contains capacitor C164 (680pF) in series with resistor R80 (49.9 ohms). Both paths recombine and lead to the output terminal REQ\_OUT. A ground connection is shown at the bottom of the circuit.

# LOGIC VOLTAGE-LEVEL TRANSLATOR

From 5V/3.3V to 1.8V

From 5V/3.3V to 1.8V

OSC\_POWER

R84 20.0 kΩ

H OSC\_PPS\_OUT

H OSC\_BITE

H OSC\_TX

H CLK\_OSC

H GNSS\_PPS

H GNSS\_TX

PERSTn

WAKEn

U14 SN74LVC244APW

A1 V1 18

A2 V2 16

A3 V3 12

A4 V4 8

A5 V5 7

A6 V6 5

A7 V7 3

A8 V8 3

OSC\_PPS\_OUT

OSC\_BITE

OSC\_TX

CLK\_OSC

GNSS\_PPS

GNSS\_TX

PCIE\_PERSTn

PCIE\_WAKEn

1.8V

C167 0.1 μF

From 1.8V to 3.3V

OSC\_RX

U16 SN74LV1T34

H OSC\_RX

OSC\_PPS\_N

U17 SN74LV1T34

H OSC\_PPS\_N

3.3V

C172 0.1 μF

3.3V

C173 0.1 μF

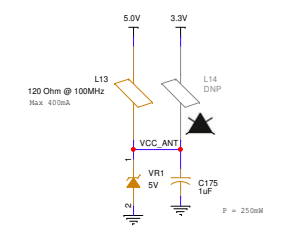
### Chip Scale Atomic Clock

The diagram shows a central component with various pins. On the left, pins 1 through 8 are connected to V.ASSERV, H.OSC\_PPS\_IN, H.OSC\_RX, and GND. On the right, pins 4 through 12 are connected to H.OSC\_BITE, H.OSC\_TX, H.OSC\_PPS\_OUT, and OSC\_SQUARE. The top pins are connected to OSC\_POWER, GND, and VCC. A crystal symbol is shown between pins 9 and 10.

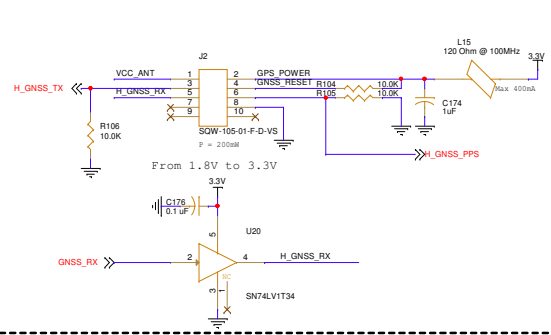
DEFAULT

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ANTENNA POWER SUPPLY



GNSS RECEIVER



GNSS STANDOFF

