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SENSIM: An Event-driven Parallel Simulator for Multi-core Neuromorphic Systems



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Timing Param Value Comm Param Value

Technology

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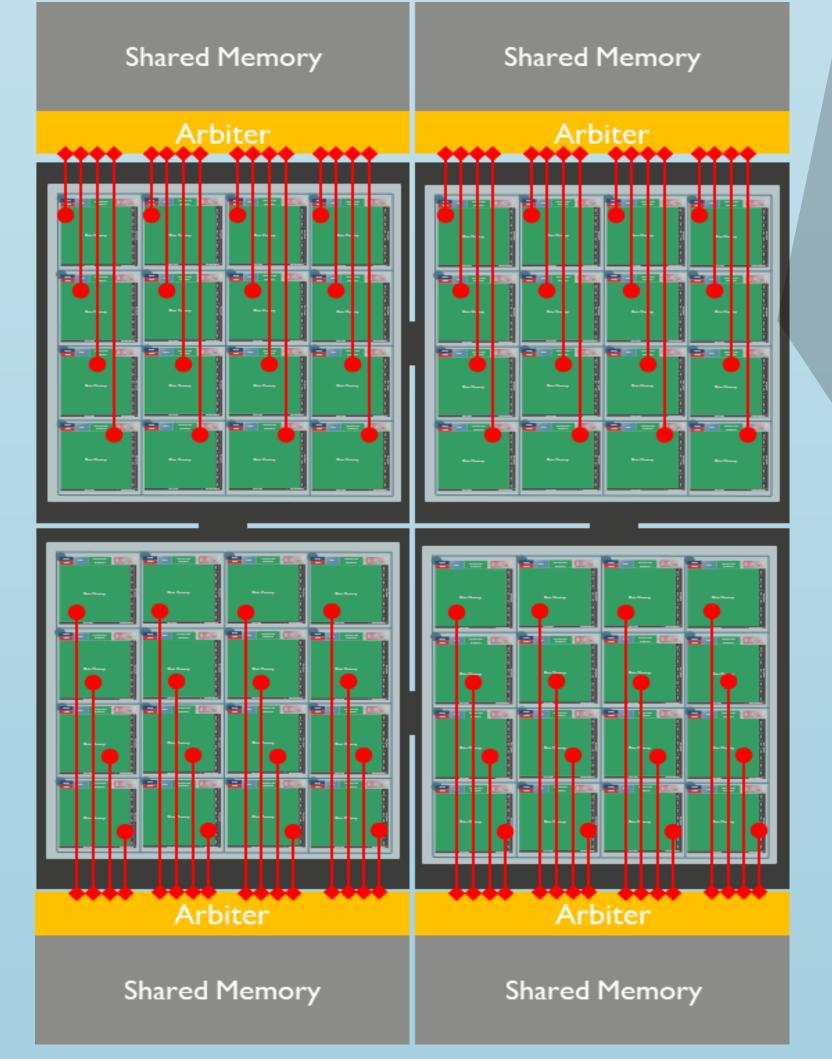
Abstract

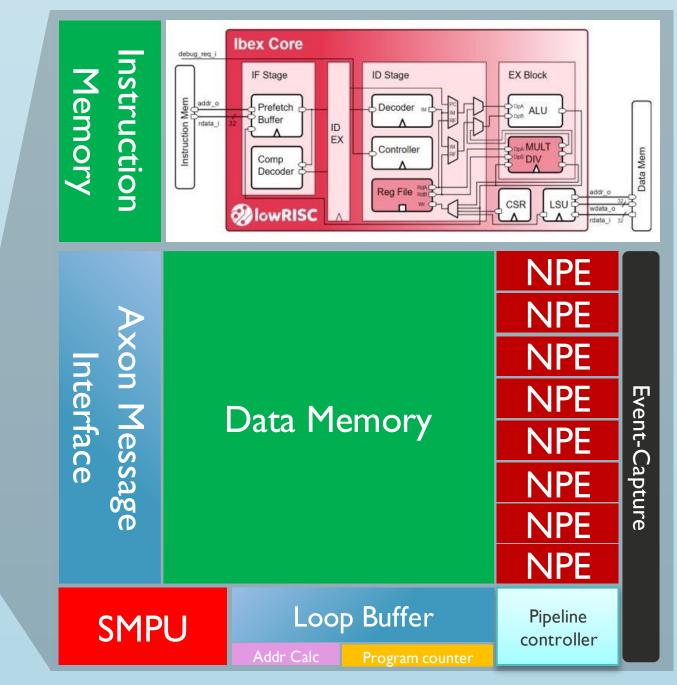
In this paper, we present SENSIM, which is an open-source simulator designed specifically for the SENECA neuro-morphic processor. This simulator is unique in that it combines features from both hardwarespecific and hardware-agnostic spiking neural network simulators, resulting in a hybrid event- driven and time-step-driven simulation approach. This allows for flexibility between accuracy and speed during different stages of simulation. Our work highlights the open-source SENSIM platform, which enables the mapping of large-scale SNN/DNN models to the SENECA cores, as well as the benchmarking of crucial KPIs such as power and latency estimation.

Objectives

- ✓ Open-source SENECA Simulation Platform
- ✓ Hybrid event-driven Design
- ✓ Scaling up the Flexible SENECA Neuro Synaptic Core
- ✓ Faster design space exploration and energy/latency estimation
- ✓ Easy Integration with SNN/DNN models
- ✓ Customization for Future Research

SENECA





Neuro-Synaptic Interconnect core Seg. Bus Neuron Models Application Quantization Event/Spike Temporal PilotNet SNN Compression Input events MNIST DNN Queuing framework Utilies Layer Types Neron/Weights Frame2Event Mapping Event2Frame Snapshot Cap Application SENSIM Model Mapping L1 L2 L3

t npe

t interconect

t_ext_mem

Parallel research & References

Energy Param

e_dmem_rd

e_dmem_wr

e fifo rd

e fifo wr

e_ext_mem_rd

e_ext_mem_wr

e_interconnect

1.5

e_npe

- ✓ Amirreza Yousefzadeh, et al. Multiplexing AER Asynchronous Channels over LVDS Links with Flow-Control and Clock-Correction for Scalable Neuromorphic Systems. May 2017.
- ✓ Amirreza Yousefzadeh et al. Delta Activation Layer exploits temporal sparsity for efficient embedded video processing. July 2022
- Guangzhi Tang, et al. Open the box of digital neuromorphic processor: Towards effective algorithm-hardware co-design, March 2023. arXiv:2303.15224
- ✓ Guangzhi Tang, et al. SENECA: building a fully digital neuromorphic processor, design trade-offs and challenges. Frontiers in Neuroscience, 17, 2023

Parameters

max event flit 9

flit width (fw) 32

bw_ext_mem 32

F_flow control Strict

Architecture

Parameters

Architectural

Quantization

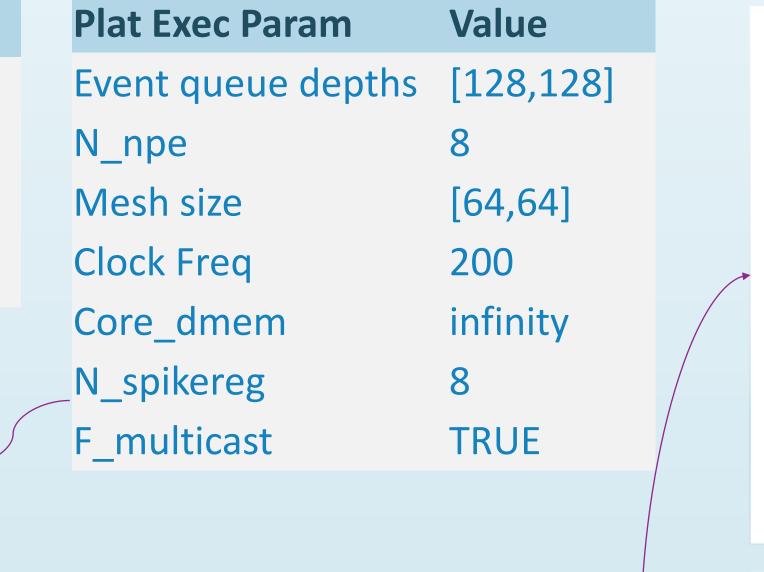
Platform Exec.

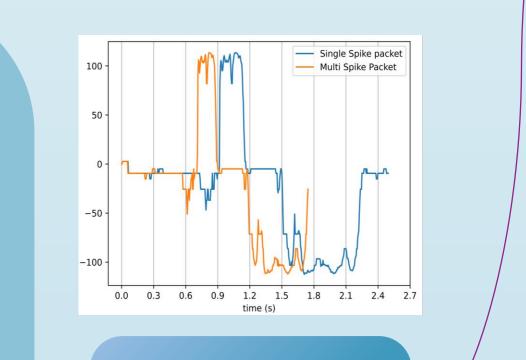
GUI

Communication

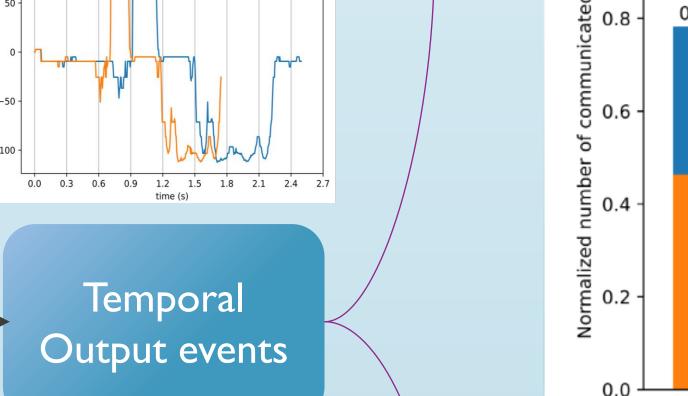
Energy

Timing

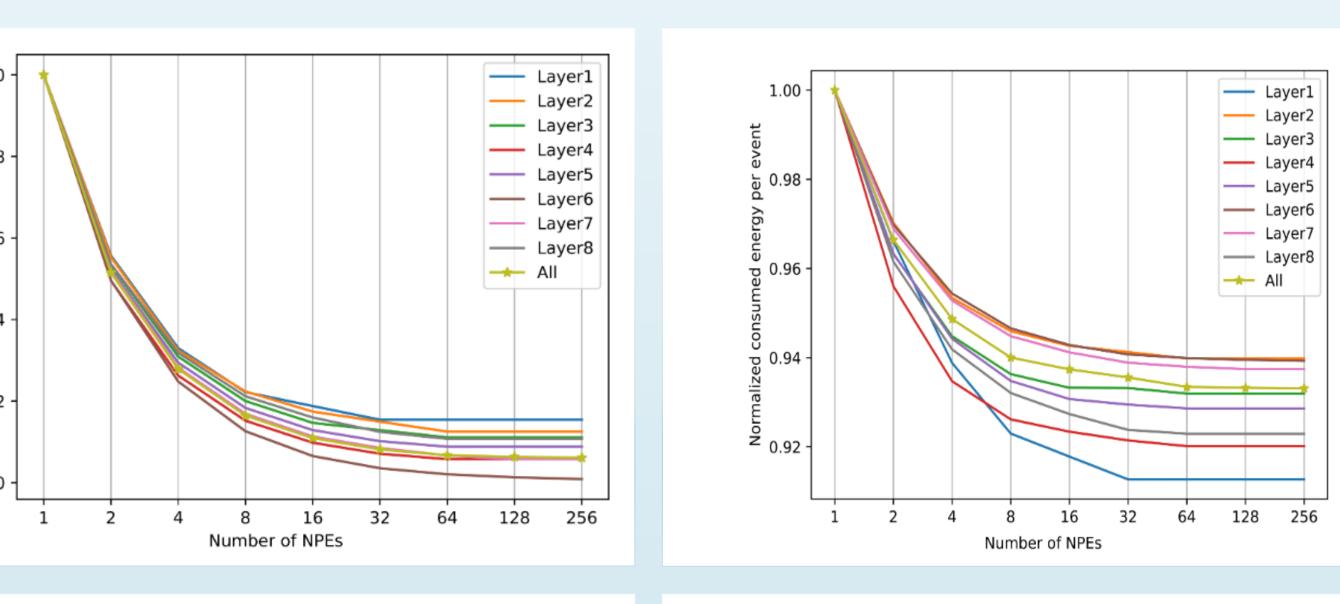


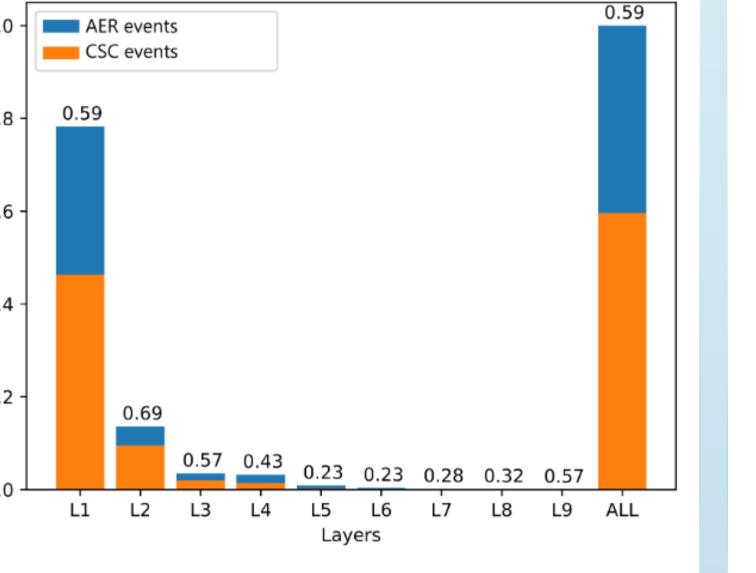


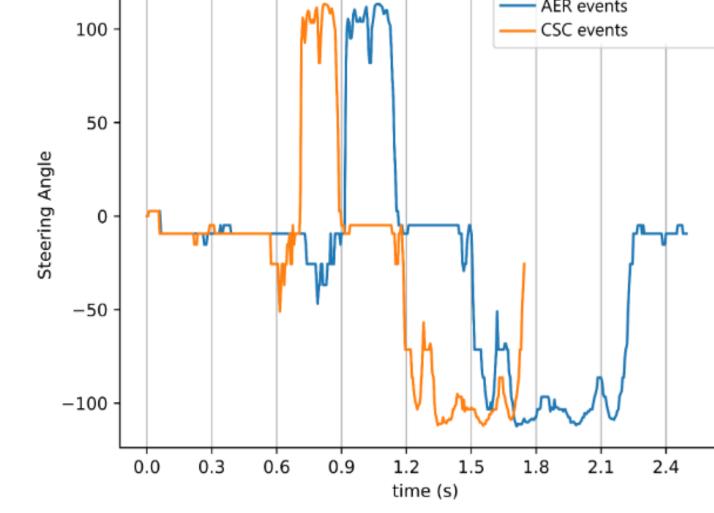
SENSIM GUI

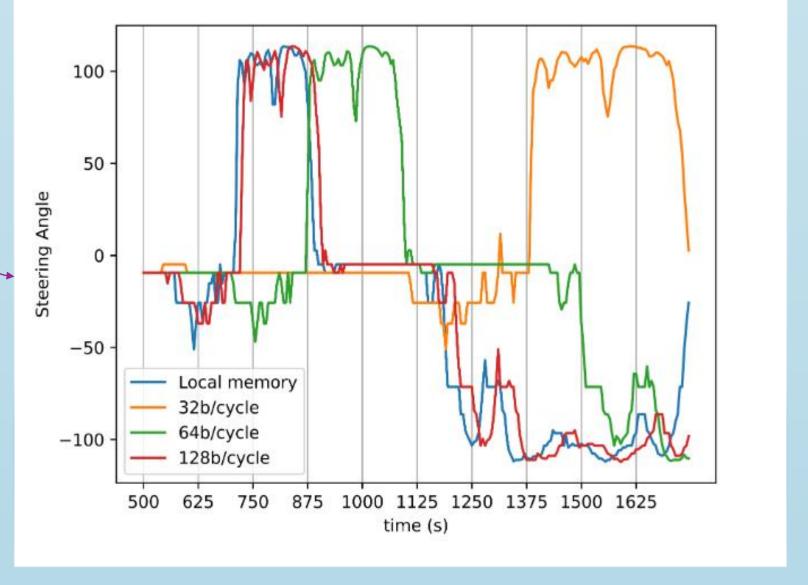


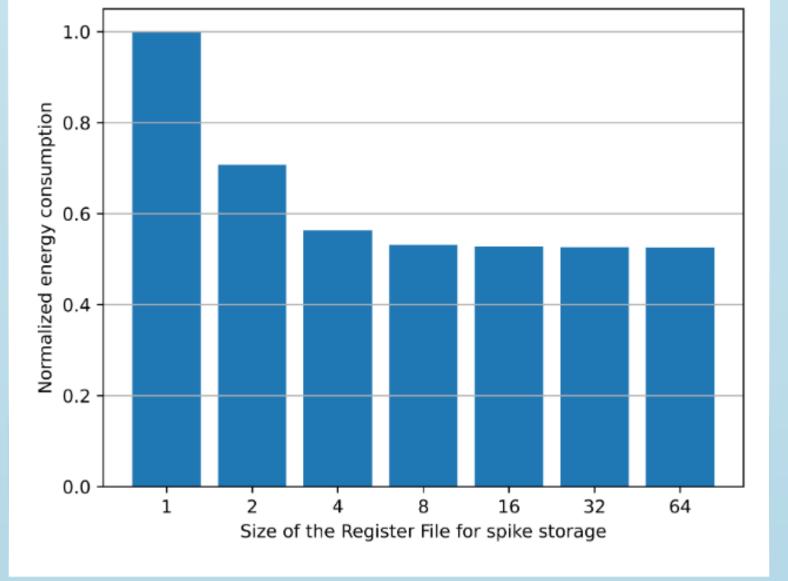
Experimentation & Results











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