SENSIM: An Event-driven Parallel Simulator for Multi-core Neuromorphic Systems

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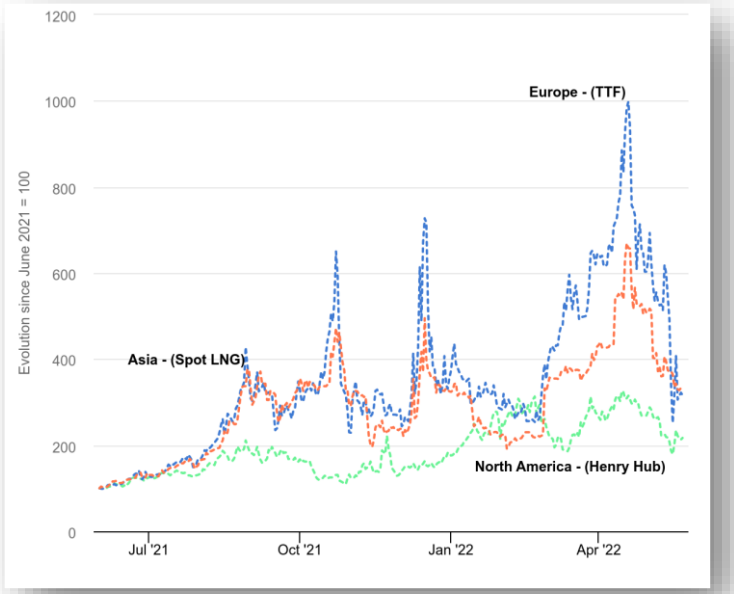
Agenda

- Global Importance
- Neuromorphic computing / engineering
- SENeCA (brief overview)
- Motivation behind SENSIM
- SENSIM: Model
- SENSIM: Graphical User Interface
- SENSIM: Experimentation and Results
- Future Scope

Primary motivation (global importance)



Global Energy Crisis Report

International Energy Agency

Industrial Automation

Automotive Industry

Smart Cities

imec

UNIVERSITY OF TWENTE. TU Delft

Neuromorphic computing/engineering (general overview)

Artificial Intelligence

- With AI revolution – DNN became the primary workload
- DNN were wasteful and consume a lot of energy
- Temporal and spatial sparsity can be extracted from DNN – SNN

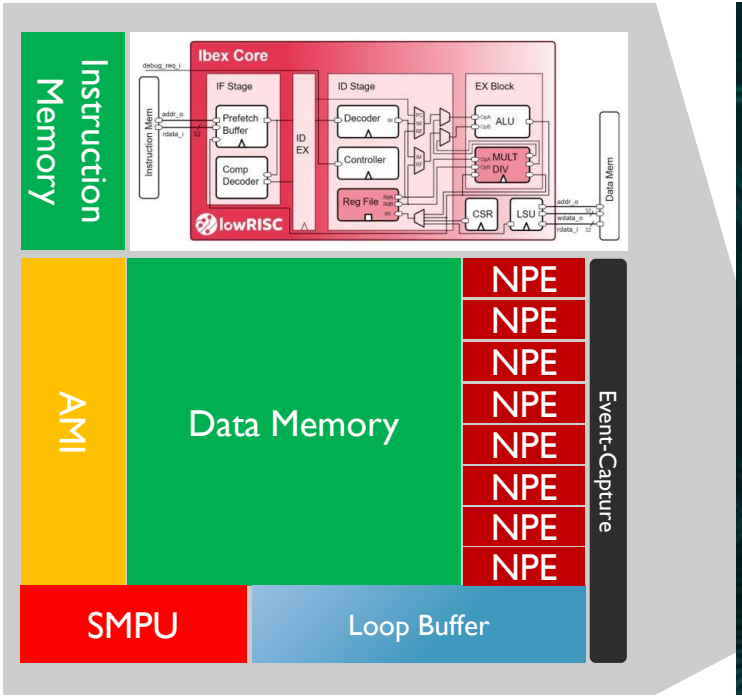
Neuroscience

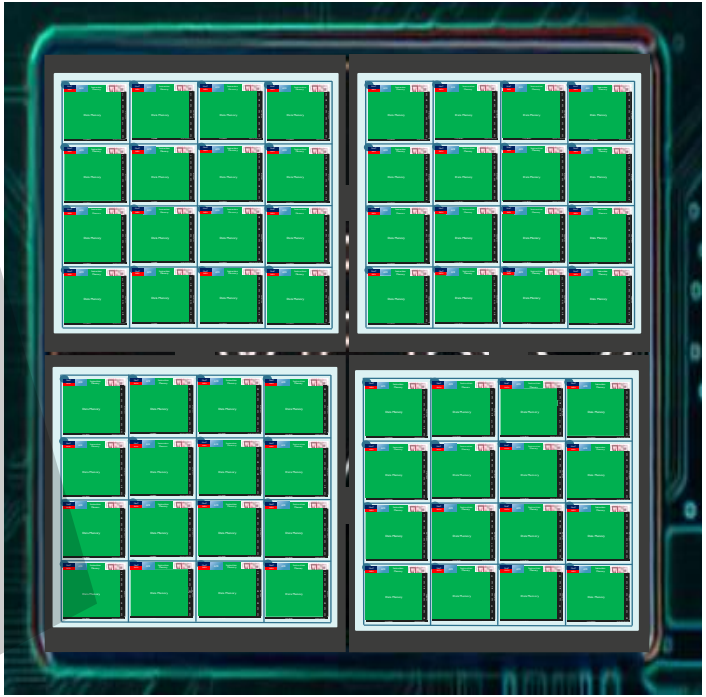
- Brain performs cognitive tasks more efficiently – consumes very less energy
- Several models were developed to model the working of a brain

Computer Architecture

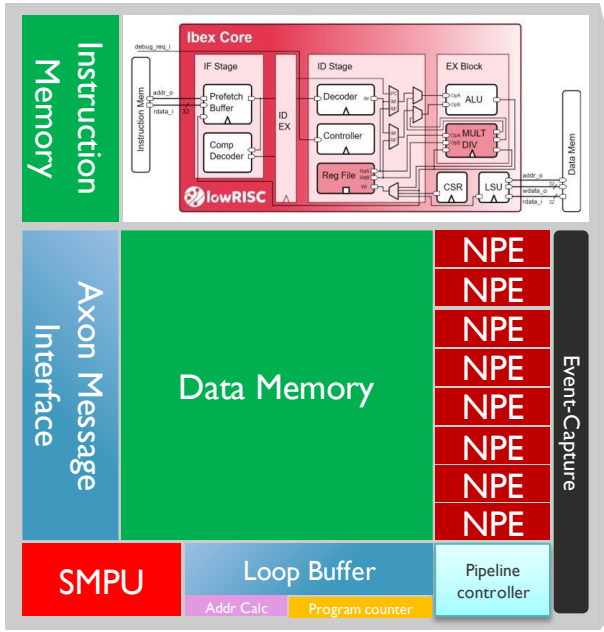
- Reduce the communication latency
- Memory centric computing
- In-Memory, Near-Memory

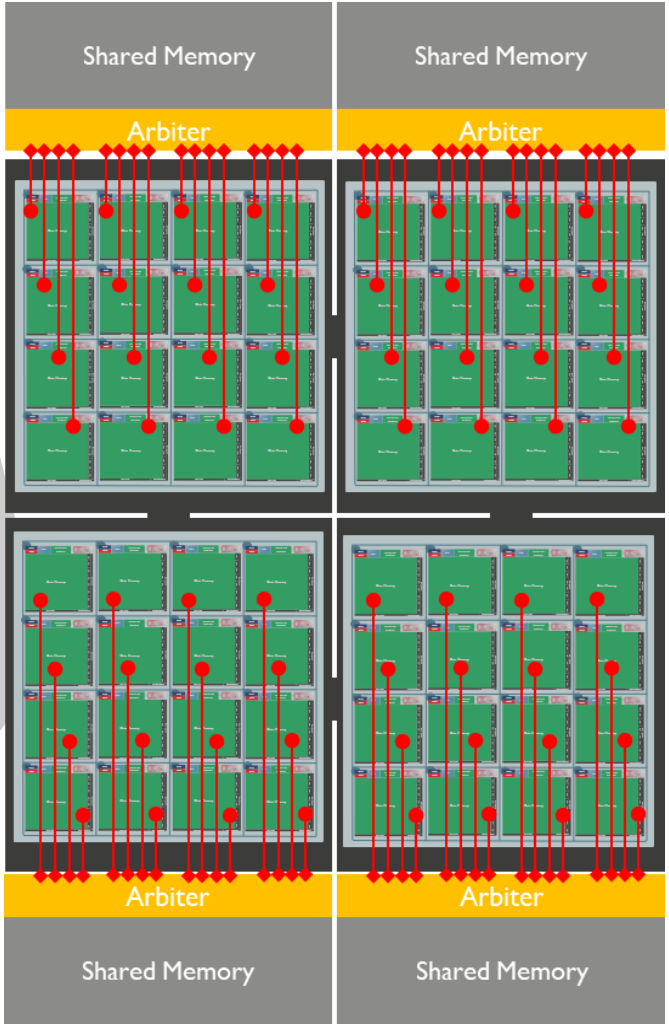
SENeCA: Scalable Energy-efficient Neuromorphic computing architecture: ReCAP





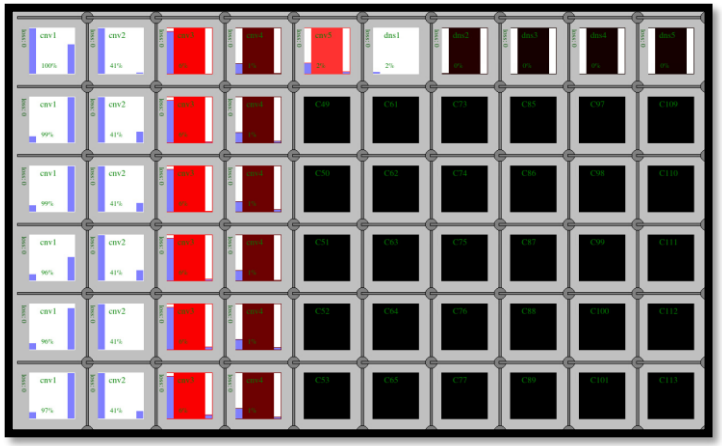
SENeCA ReCAP

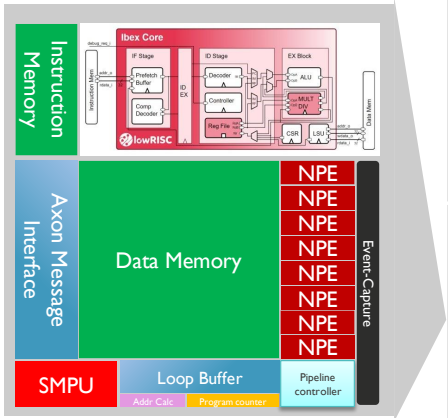


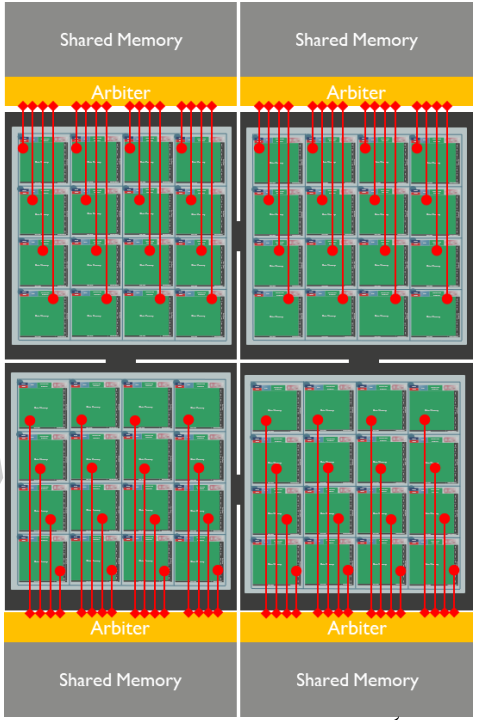


Motivation behind SENSIM

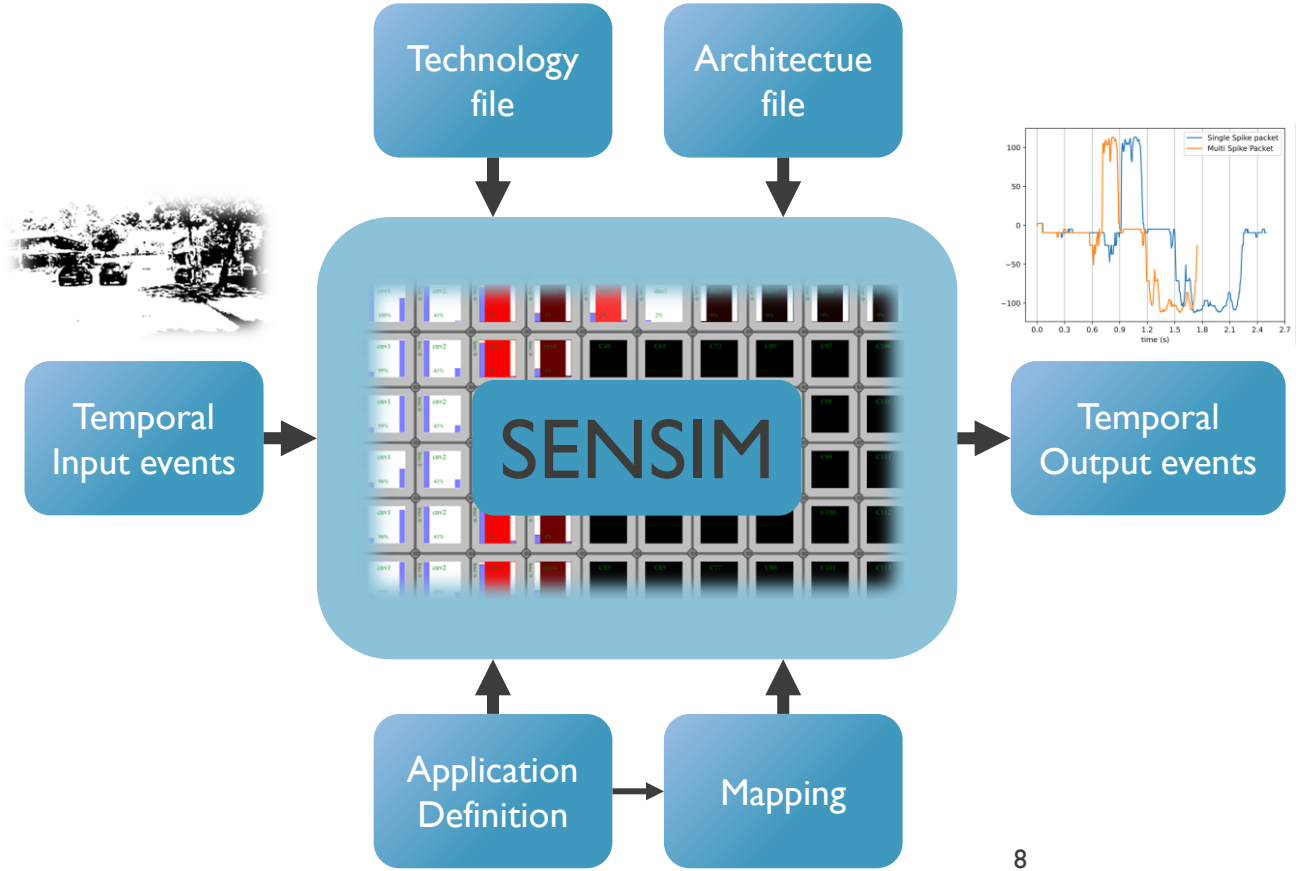
- ✓ Faster design space exploration and estimation of energy and time
- ✓ Implementation of Large-Scale Spiking Neural Networks for SENeCA and other scaled up neuromorphic chips
- ✓ SENSIM was designed in python enabling easy DNN/SNN integration







SENSIM: SENeCA Simulator



SENSIM: SENeCA Simulator

Temporal Input events

Technology file

Architectue file

Neuro-Synaptic core

- Neuron Models
- Quantization
- Event/Spike Compression
- Queuing framework
- Layer Types
- Neron/Weights Mapping

Interconnect

- Seg. Bus
- NoC

Application

- PilotNet SNN
- MNIST DNN

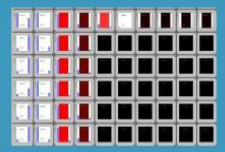
Utilies

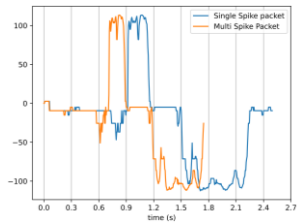
- Frame2Event
- Event2Frame
- Snapshot Cap.

Parameters

- Energy
- Timing
- Architectural
- Communication
- Quantization
- Platform Exec.

GUI



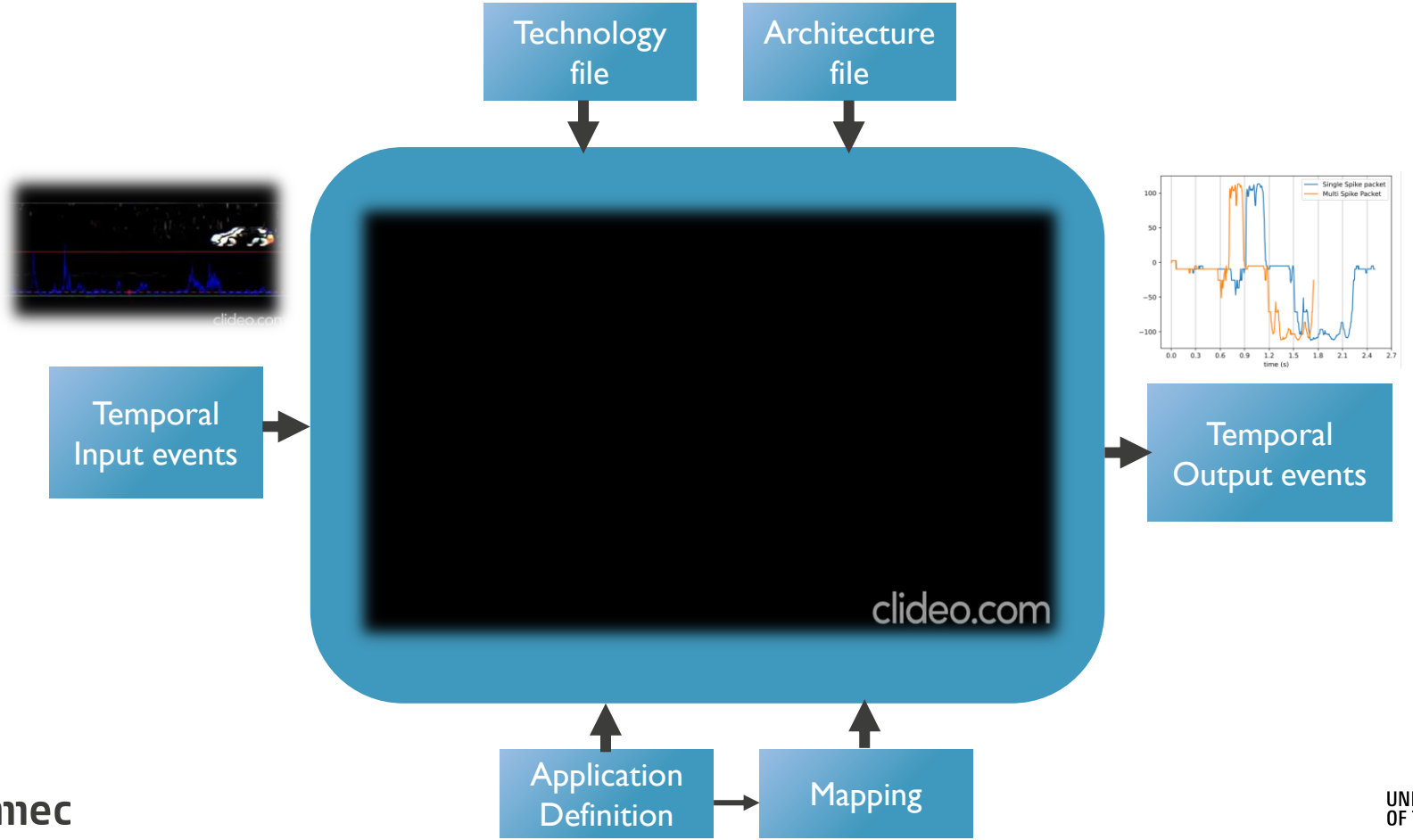


Temporal Output events

Application Definition

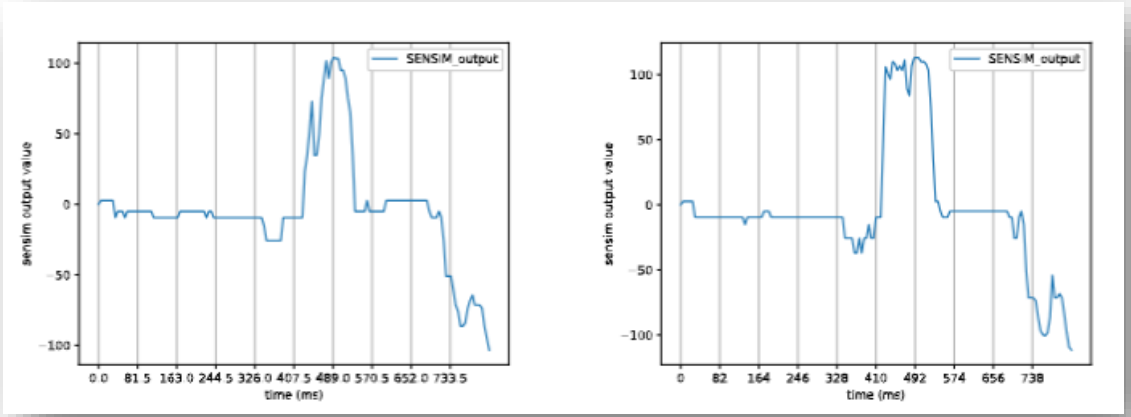
Mapping

SENSIM GUI

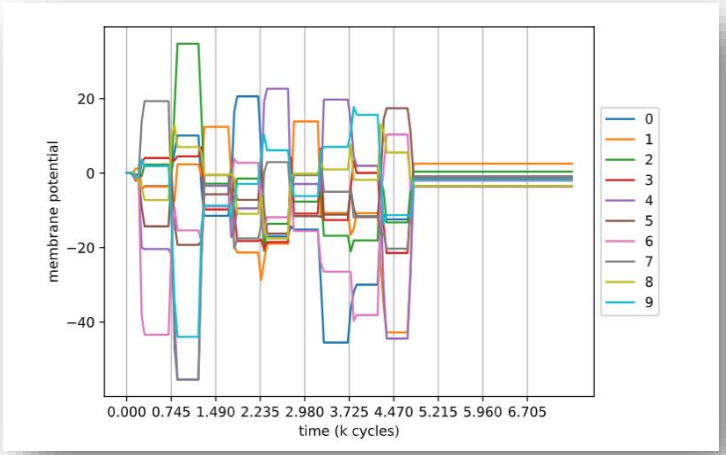

Technology file
Architecture file
Temporal Input events
clideo.com
Single Spike packet
Multi Spike Packet
time (s)
Temporal Output events
Application Definition
Mapping

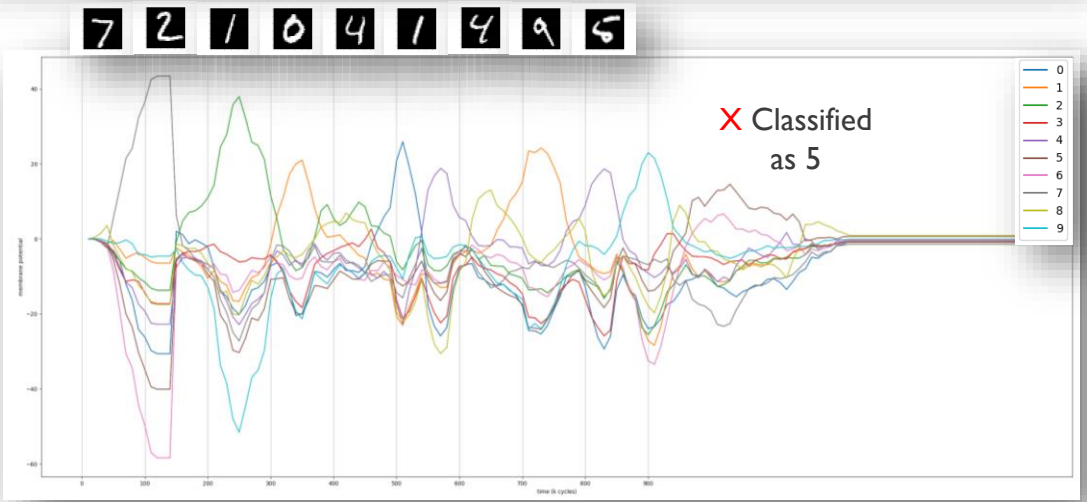
SENSIM Application

PilotNet: Inter Spike Distortion



MNIST: Output validation





SENSIM Parameters

Architectural/Simulation Parameters

Parameter	Value	Description
Event queue depths	[128,128]	Sizes of the input and output queues (in flits) of every core on the chip.
N_npe	8	a global parameter that sets the total number of processing elements on every core on the chip.
Mesh size	[64,64]	a parameter which decides to total number of cores (x,y) on the neuromorphic chip in the simulation
Clock Freq	200	Clock frequency at which each processor is running (in MHz)
Core_dmem	infinity	local data memory of each core (in bits)
N_spikereg	8	number of spike registers for every processing element
F_multicast	TRUE	Flag to control the multicasting and uni-casting of events in the network on chip

Communication Parameters

Parameter	Value	Description
max event flit	9	Maximum limit the max number of flits per event
flit width (fw)	32	Bandwidth (bits) per flit
bw_ext_mem	32	Shared memory bandwidth (bits per cycle)
F_flow control	Strict	The flow control can be controlled by dropping packets in the interconnect or ensuring complete delivery of packets.

SENSIM Parameters

Energy Parameters

Parameter	Value	Description
e_con	3	energy unit per each controller operation and instruction memory read
e_npe	1	energy unit for each NPE operation
e_dmem_rd	3	energy unit for every local data memory bit read
e_dmem_wr	3	energy unit for every local data memory bit write
e_ext_mem_rd	300	energy unit for every shared memory bit read
e_ext_mem_wr	300	energy unit for every shared memory bit write
e_fifo_rd	1.5	energy unit per each event queue bit read
e_fifo_wr	1.5	energy unit per each event queue bit write
e_interconnect	6	energy unit for sending a bit of data on a interconnect

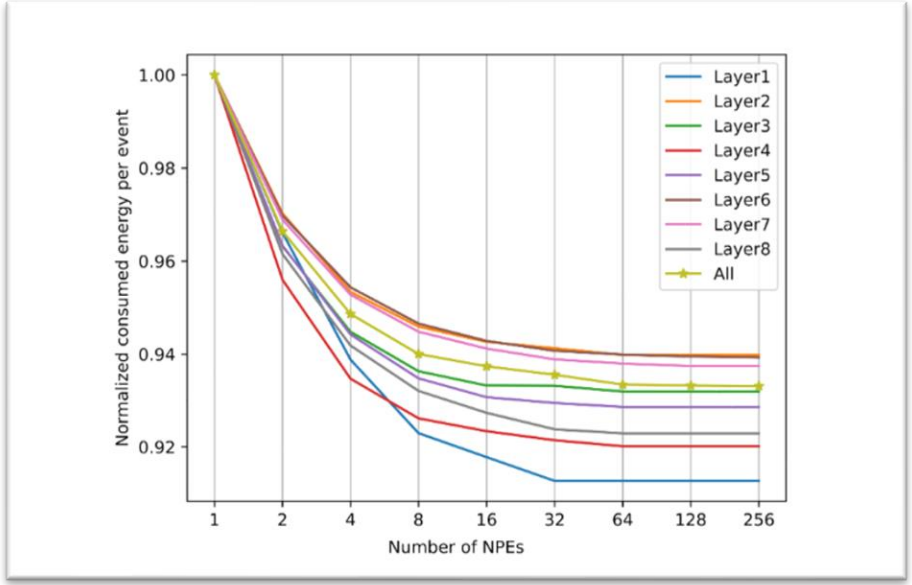
Timing Parameters

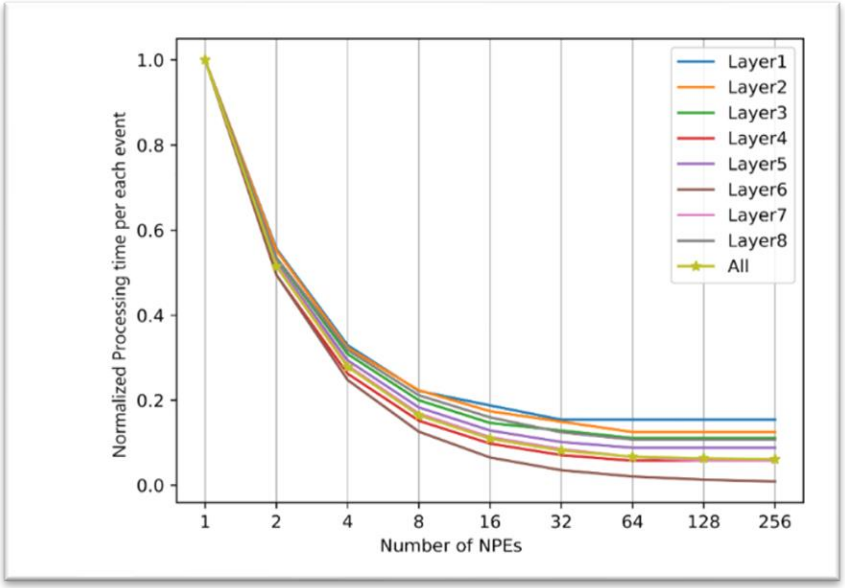
Parameter	Value	Description
t_npe	1	time units (in cc) per each NPE operation
t_fifo	1	time units (in cc) per each event queue access
t_interconect	1	time units (in cc) for sending a flit of data on the interconnect
t_ext_mem	100	time units (in cc) for accessing the shared memory

SENSIM: Simulator Comparison

Simulator	Programming language support	Execution Platform	Emulation Platform	Learning support	Event/Time-step driven	energy/power estimates	Latency estimates
Lava	Python	CPU, GPU, Loihi, Loihi2	NA	Yes	Event	No	Yes
Carlsim	C/C++	CPU,GPU	TrueNorth, Loihi, Dynapse	Yes	Time-step	Yes	Yes
PyCarl	Python	CPU, GPU	TrueNorth, Loihi, Dynapse	Yes	Time-step	Yes	Yes
Brian2Loihi	Python	CPU, GPU	Loihi	Yes	Time-step	No	Yes
SpyNNaker	Python	CPU, GPU	SpiNNaker	NA	Event	No	Yes
BindsNet	Python	CPU, GPU	NA	Yes	Time-step	No	No
Py(NEST)	Python, SLI	CPU	NA	Yes	Time-step	No	Yes
Core(NEURON)	Python, NMODL	CPU, GPU	NA	Yes	Hybrid	No	Yes
Nengo	Python	CPU, GPU	NA	Yes	Time-step	Yes	Yes
Brian/2	Python	CPU, GPU	NA	Yes	Time-step	No	No
EvtSNN	Python	CPU	NA	Yes	Event	No	Yes
EDHA	Java	CPU (cross-platform)	NA	Yes	Event	No	Yes
SENSIM	Python	CPU	SENECA	No	Hybrid	Yes	Yes

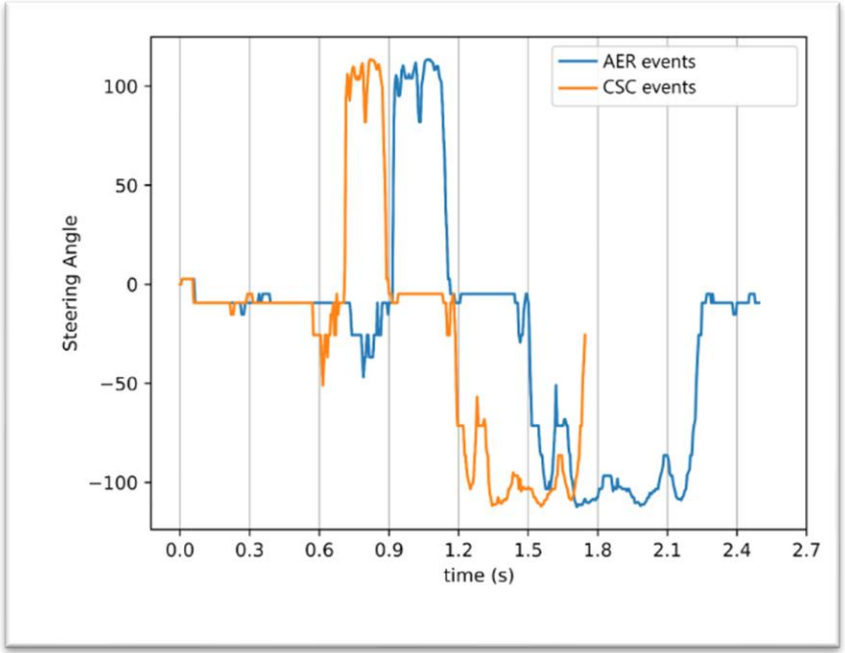
SENSIM: Experiments & Results

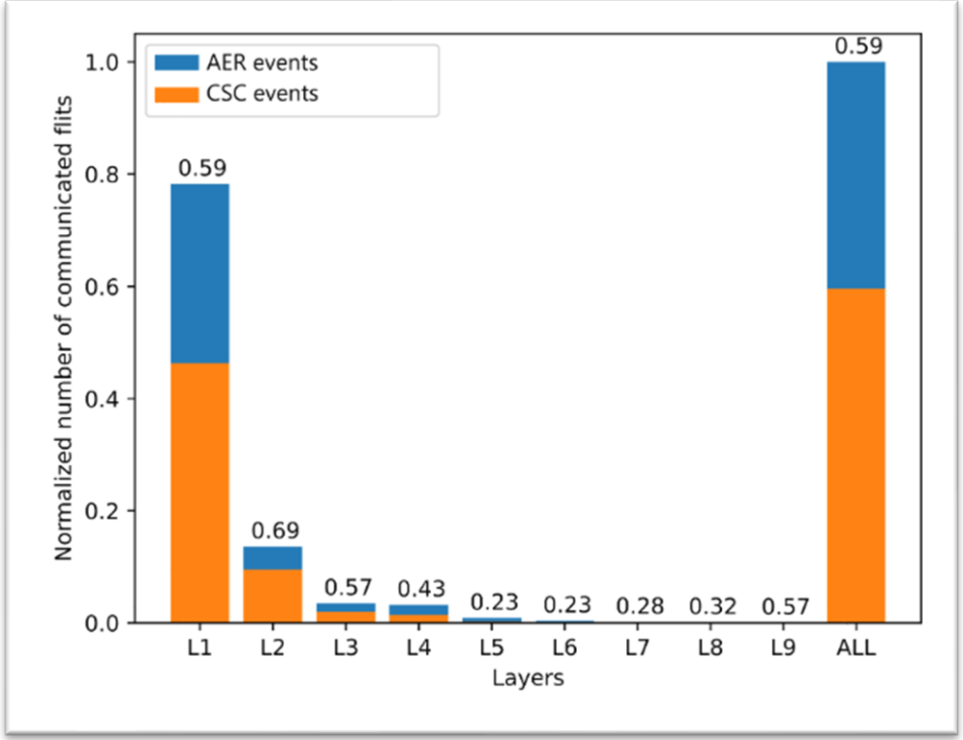




Varying the number of NPEs in the core

SENSIM: Experiments & Results

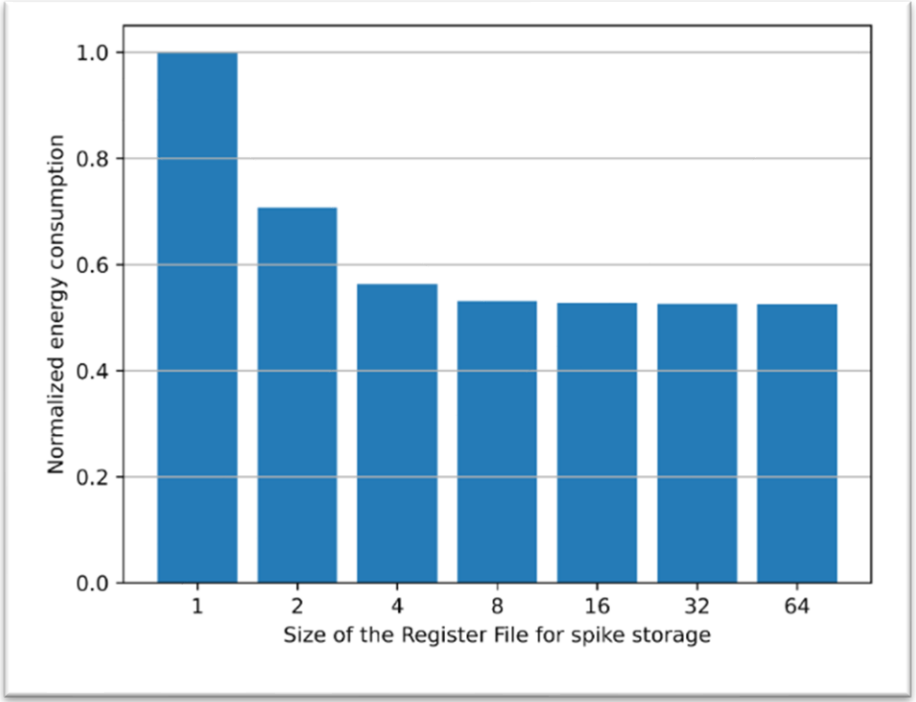




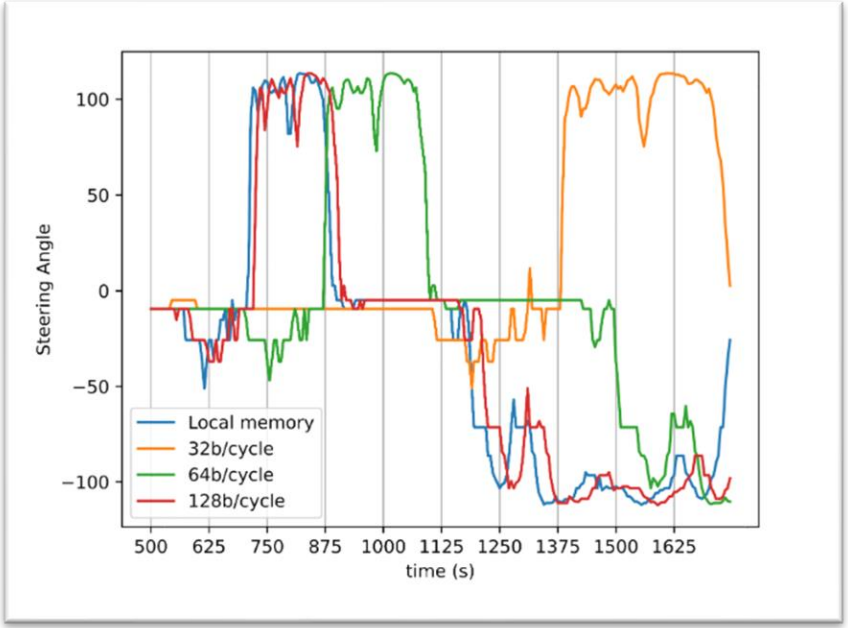
Varying the Spike compression scheme

SENSIM: Experiments & Results

Varying the Spike Register size in the NPE



SENSIM: Experiments & Results



Varying the Shared Memory Bandwidth

Future scope

- SENMap : SENSIM/ SENeCA Mapper – designed for optimal SNN mappings on SENeCA / SENSIM
- Scale SENSIM / SENeCA to a 3rd dimension
- SNN/ DNN fusion and mapping.
- Support different type of neuron models

Open source and Collaboration

- SENSIM is open source @
  - https://github.com/Prithvish04/SENSIM_paper_submission
- Issues and bugs SENSIM –
  - Prithvish V N prithvish.n13@gmail.com
- Collaboration on SENeCA –
  - Amirreza Yousefzadeh a.yousefzadeh@utwente.nl
  - Manolis Sifalakis Manolis.Sifalakis@imec.nl

Thankyou

¿ Open for Questions ?