

Design Rules Verification Report

Filename : C:\Users\Asteria\Dropbox\Satellite\Pumpkin PCBs\Battery Bus Interface (01573B)\Battery Bus Interface REVB.PcbDoc

Warnings 0
Rule Violations 84

Warnings	
Total	0

Rule Violations	
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mm) (All)	0
Silk to Silk (Clearance=0.254mm) (All),(All)	6
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	67
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	10
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Width Constraint (Min=0.254mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Clearance Constraint (Gap=0.178mm) (All),(All)	1
Un-Routed Net Constraint (All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Clearance Constraint (Gap=0.254mm) (InNet('BAT_POS')), (All)	0
Total	84

Silk to Silk (Clearance=0.254mm) (All),(All)	
Silk To Silk Clearance Constraint: (0.111mm < 0.254mm) Between Text "TM" (-23.159mm,4.825mm) on Top Overlay And Trac	
Silk To Silk Clearance Constraint: (0.111mm < 0.254mm) Between Text "TM" (-23.159mm,4.825mm) on Top Overlay And Trac	
Silk To Silk Clearance Constraint: (0.223mm < 0.254mm) Between Text "J164" (18.316mm,21.544mm) on Bottom Overlay And Trac	
Silk To Silk Clearance Constraint: (0.149mm < 0.254mm) Between Text "J164" (18.316mm,21.544mm) on Bottom Overlay And Trac	
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "J165" (19.662mm,-8.075mm) on Bottom Overlay And Trac	
Silk To Silk Clearance Constraint: (0.021mm < 0.254mm) Between Text "J165" (19.662mm,-8.075mm) on Bottom Overlay And Trac	

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.057mm < 0.254mm) Between Track (13.793mm,-2.591mm)(13.793mm,0.787mm) on Bottom Overlay
Silk To Solder Mask Clearance Constraint: (0.047mm < 0.254mm) Between Track (17.197mm,-2.591mm)(17.197mm,0.787mm) on Bottom Overlay
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Track (13.793mm,-2.591mm)(18.009mm,-2.591mm) on Bottom Overlay
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Track (13.972mm,0.787mm)(17.197mm,0.787mm) on Bottom Overlay And
Silk To Solder Mask Clearance Constraint: (0.137mm < 0.254mm) Between Track (-22.749mm,32.984mm)(-22.749mm,35.016mm) on Top Overlay
Silk To Solder Mask Clearance Constraint: (0.137mm < 0.254mm) Between Track (-20.717mm,32.984mm)(-20.717mm,35.016mm) on Top Overlay
Silk To Solder Mask Clearance Constraint: (0.137mm < 0.254mm) Between Track (-22.749mm,32.984mm)(-20.717mm,32.984mm) on Top Overlay
Silk To Solder Mask Clearance Constraint: (0.137mm < 0.254mm) Between Track (-22.749mm,35.016mm)(-20.717mm,35.016mm) on Top Overlay
Silk To Solder Mask Clearance Constraint: (0.137mm < 0.254mm) Between Track (-21.733mm,32.476mm)(-21.733mm,32.984mm) on Top Overlay
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Text "TP51" (29.067mm,-6.5mm) on Top Overlay And Pa
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Text "TP52" (24.967mm,-6.5mm) on Top Overlay And Pa

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)

Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(51.311mm,-30.811mm) on Multi-Layer Actual Hole Size = 3.175mm
Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(-34.408mm,46.654mm) on Multi-Layer Actual Hole Size = 3.175mm
Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(51.317mm,42.842mm) on Multi-Layer Actual Hole Size = 3.175mm
Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(-34.408mm,-33.358mm) on Multi-Layer Actual Hole Size = 3.175mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-24(-29.004mm,-1.062mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-25(-29.004mm,33.228mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-26(35.766mm,33.228mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-27(35.766mm,-1.062mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-24(-15.233mm,18.5mm) on Multi-Layer Actual Hole Size = 3.2mm
Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-24(-15.233mm,7mm) on Multi-Layer Actual Hole Size = 3.2mm

Clearance Constraint (Gap=0.178mm) (All),(All)

Clearance Constraint: (0.108mm < 0.178mm) Between Track (-5.983mm,-1.95mm)(-4.004mm,-3.929mm) on Bottom Layer And Pa
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