Design Rules Verification Report

Filename : C:\Users\Asteria\Dropbox\Pumpkin PCBs\Battery Module Dev Cells (02190A0)\BM Dev Cells.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=8mil) (HasFootprint('Spark_Gap')),(inPolygon)	0
Clearance Constraint (Gap=10mil) (All),(OnLayer('Keep-Out Layer'))	0
Clearance Constraint (Gap=8mil) (InNet('BAT_POS') and not HasFootprint('Spark_Gap')),(All	0
Clearance Constraint (Gap=8mil) (All),(All)	0
Clearance Constraint (Gap=6mil) (HasFootprint('Spark_Gap')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=8mil) (Max=100mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4	0
Hole Size Constraint (Min=1mil) (Max=314.961mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=6mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Silk primitive without silk layer	0
Total	0