Design Rules Verification Report

Filename : C:\Pumpkin\Altium_docs\test folder (01234A)\Battery Bus Interface REVB.Pcb
Doc

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (InNet('BAT_POS')),(All)	0
Clearance Constraint (Gap=0.178mm) (All),(All)	19
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	10
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	65
Silk to Silk (Clearance=0.254mm) (All),(All)	5
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	99

Clearance Constraint (Gap=0.178mm) (All),(All)

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-23.233mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-23.233mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-24.983mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-24.983mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-26.733mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-26.733mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-28.483mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-28.483mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-28.483mm,40mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-28.483mm,40mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-30.233mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-30.233mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-30.233mm,40mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-30.233mm,40mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-31.983mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-31.983mm,-10.25mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-31.983mm,40mm) on Multi-Layer And Trac

Clearance Constraint: (Collision < 0.178mm) Between Pad Free-28(-31.983mm,40mm) on Multi-Layer And Trac

Clearance Constraint: (0.108mm < 0.178mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Trac

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)

Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(-34.408mm,-33.358mm) on Multi-Layer Actual Hole Size = 3.175mn

Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(-34.408mm,46.654mm) on Multi-Layer Actual Hole Size = 3.175mn

Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(51.311mm,-30.811mm) on Multi-Layer Actual Hole Size = 3.175mn

Hole Size Constraint: (3.175mm > 2.54mm) Pad Free-(51.317mm,42.842mm) on Multi-Layer Actual Hole Size = 3.175mn

Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-24(-16.114mm,18.5mm) on Multi-Layer Actual Hole Size = 3.2mn

Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-24(-16.114mm,7mm) on Multi-Layer Actual Hole Size = 3.2mn

Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-24(-29.004mm,-1.062mm) on Multi-Layer Actual Hole Size = 3.2mn

Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-25(-29.004mm,33.228mm) on Multi-Layer Actual Hole Size = 3.2mn

Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-26(35.766mm,33.228mm) on Multi-Layer Actual Hole Size = 3.2mn

Hole Size Constraint: (3.2mm > 2.54mm) Pad Free-27(35.766mm,-1.062mm) on Multi-Layer Actual Hole Size = 3.2mn

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Free-24(-16.114mm,7mm) on Multi-Layer And Text "OFF_VCC
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Free-24(-16.114mm,7mm) on Multi-Layer And Text "OFF_VCC
Silk To Solder Mask Clearance Constraint: (0.229mm < 0.254mm) Between Pad Free-24(-16.114mm,7mm) on Multi-Layer And Text "This device

the FCC rules. Operation is subject

to the following conditions." (-24.579mm,2.473mm) on Bottom Overlay [Bottom Overlay] to [Bottom Solder] clearance [

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-1(12.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-1(12.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-12(4.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-12(4.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-13(2.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-13(2.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-14(0.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-14(0.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-5(4.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-5(4.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-6(2.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-6(2.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-7(0.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-7(0.017mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-8(12.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J164-8(12.017mm,15.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.047mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.057mm < 0.254mm) Between Pad J164-MNT(15.517mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.057mm < 0.254mm) Between Pad J164-MNT(-3.483mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Pad J164-MNT(-3.483mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Pad J164-MNT(-3.483mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.047mm < 0.254mm) Between Pad J164-MNT(-3.483mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Pad J164-MNT(-3.483mm,14.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-1(0mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-1(0mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-12(8mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-12(8mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-13(10mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-13(10mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-14(12mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-14(12mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-5(8mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-5(8mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-6(10mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-6(10mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-7(12mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-7(12mm,0mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-8(0mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad J165-8(0mm,-2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Pad J165-MNT(15.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.057mm < 0.254mm) Between Pad J165-MNT(15.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Pad J165-MNT(15.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.063mm < 0.254mm) Between Pad J165-MNT(15.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.047mm < 0.254mm) Between Pad J165-MNT(15.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.047mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.136mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.063mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.037mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.057mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.041mm < 0.254mm) Between Pad J165-MNT(-3.5mm,-0.9mm) on Multi-Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.205mm < 0.254mm) Between Pad T100-1(-21.733mm,34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.182mm < 0.254mm) Between Pad T100-1(-21.733mm,34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad T100-1(-21.733mm,34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.205mm < 0.254mm) Between Pad T100-1(-21.733mm,34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad T100-1(-21.733mm,34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.221mm < 0.254mm) Between Pad TP52-1(26.767mm,-7.5mm) on Multi-Layer And Text "TP52

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.157mm < 0.254mm) Between Text "J164" (18.316mm,21.544mm) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (0.23mm < 0.254mm) Between Text "J164" (18.316mm,21.544mm) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (0.186mm < 0.254mm) Between Text "J165" (21.844mm,-8.001mm) on Bottom Overlay And Track
Silk To Silk Clearance Constraint: (0.113mm < 0.254mm) Between Text "TM" (-23.159mm,4.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.111mm < 0.254mm) Between Text "TM" (-23.159mm,4.825mm) on Top Overlay And Track