Design Rules Verification Report

Filename : C:\Pumpkin\Altium_docs\test folder (02190A)\BM Dev Cells.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.203mm) (HasFootprint('Spark_Gap')),(inPolygon)	0
Clearance Constraint (Gap=0.254mm) (All),(OnLayer('Keep-Out Layer'))	0
Clearance Constraint (Gap=0.203mm) (InNet('BAT_POS') and not HasFootprint('Spark_Gap')),(All	0
Clearance Constraint (Gap=0.203mm) (All),(All)	0
Clearance Constraint (Gap=0.152mm) (HasFootprint('Spark_Gap')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=0.203mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm	0
Hole Size Constraint (Min=0.025mm) (Max=8mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.152mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Silk primitive without silk layer	0
Total	0