1			2	3		4		5	6
									,
	Configuration (T			Test Point		
Bit	Value) case		1 case		Number	Net	Function
0 1 2 3 4	1 Not 2 ce 2 Not 3 ce 4 Not 4 ce 8 -; 16 -;	l operation; l operation; l operation;		2 cell operation, place JP10 in position B 3 cell operation, place JP10 in position B 4 cell operation, Place JP10 in position A Two Board stacking confirguration, top b MTMM-102-07-S-D-196; Two Board stacking confirguration, botto	and DNP R65 and R73; , DNP B3, R52, R53 and R76; , DNP R52, R53, R73 and R76; yoard. Place H2 and H3 as MTM! ym board. Place H1, H2 and H3 as	vI-103-09-S-D-243 and H1 as ESQT-108-03-F-D-709;	TP43 TP44 TP45 TP58 TP59	VC2 VC3 VC4 VC1 VC5	3rd center-tap, 2nd center-tap, positive side of second lowest cell 1st center-tap, positive side of lowest cell negative side of bottom cell positive side of highest cell
ECO Li		iber		Action Summary					
Change	s from REVA(/ BM2-F1							
No previous									
									PUMPKIN 750 Naples Street San Francisco, Calife
									Title: Battery Module Development Board Cells - Modification Information Part Number: Revision:
							(C) 2001-20	Doc. Rev: 01 017 Pumpkin, Inc.	705-02190 File: MOD.SchDoc Sheet: