Basics of ARM Cortex

A ⇒Advanced
R ⇒Reduced Instruction Set Computer[RISC]
M ⇒Machine

CISC ⇒ Complex Instruction Set Computer

1 MB Flash memory, 4 GB of Memory space
Flash memory stores code and this memory does not wipe out data even after power loss.

STM32F-Discovery board uses following processors: Cortex-M33F, Cortex-M7F, Cortex-M4F, Cortex-M3, Cortex-M0+, or Cortex-M0.

TOPS ⇒ Tera Operations Per Seconds.

NVIC ⇒ Nested Vector Interrupt Controller sets interrupt priority.

In ARM, Lower the number, Higher the priority.
In Others, Higher the number, Higher the priority.

T ⇒ Thumb Instructions.
D ⇒ JTAG Debug.
M ⇒ Multiplier.
I ⇒ ICE

ICE ⇒ In Circuit Emulator.

Pipelining ⇒ Multiple Instructions in single cycle.
3 stage pipelining is provided by ARM.

Memory mapping for 32 bit uP/µC

0x0000
0x0004
0x0008
0x000C
0x0010
0x0014
0x0018
0x001C
0x0020
0x0024
0x0028
0x002C

.
.
.
..
0xFFFFFFFF

Stack grows in downward direction.
Stack has a memory allocated in a memory mapping.
PUSH ops ⇒ SP = SP-1 ..... 1 is 4bytes
POP ops ⇒ SP = SP+1 ..... 1 is 4bytes

Naming conventions of ARM

- ARMv& M [Microcontroller series]
- ARMv7 A [Application series]
- ARMv7 R [Real time]

RaspPi3 ⇒ A8
RaspPi4 ⇒ A72

MMU ⇒ Memory Management Unit.

CPU works on virtual addr space.

Types of RESETs

- Power On Reset ⇒ Resets process the moment power turns on.

- Brownout Reset ⇒ If the supply power drops below a particular voltage, This resets process.
- Watchdog Reset ⇒ If process does not respond in a particular time, This resets process.
- Thermal Reset ⇒ If a processor temperature drops or goes above the specified temperature, This resets process.

SIMD ⇒ Single Instruction Multiple Data.

CoreMarks per MHz.

- Cortex-M4 ARMv7-M 3.42
- Cortex-M3 ARMv7-M 3.34
- Cortex-M7 ARMv7-M 5

DMIPS ⇒ Dhrystone Million Instructions Per Seconds.

CMSIS ⇒ Cortex µC S/w Interface Standard.

FPGA ⇒ Field Programmable Git Arrays.

PLL ⇒ Phase Locked Loop modulates frequency of Input signal. It is used to change clock frequency of µC / µP.

HSI ⇒ High Speed Internal [16 MHz **default]

ISR Vector holds all the addresses of ISR.

Linker [.ld] files contains memory mapp specification.

Terms	Size
Byte	8-bit
Half Word	16-bit
Word	32-bit
Double Word	64-bit

M0 follows von-nueman architecture.
M3,M4 follows harward architecture.

Load and store method ⇒ First load the data in register, operate or execute on it and then store it in a memory space.

Only two Instructions works on memory space.

- LDR ⇒ Load Register.
- SDR ⇒ Store Register.

Disadvantage of ARM7TDMI

- Latency due to switching between the ARM state and Thumb state.

ARM mode ⇒ 32 bit
Thumb mode ⇒ 16 bit

BLX is used to enter ARM state.
BXLR is used to return from ARM state to Thumb sate.

Dark colored boxes are for debug support features.

NVIC is closely embeded with the core. helps to execute nested interrupt.

Fetch ⇒ Read the data from ptogram memory.

Decode ⇒ Read the register placed in data memory.

Execute ⇒ Execution of instruction/s.

Register bank has 18 registers, each of 32 bit.

Memory interface connects external memory to core.

SysTick ⇒ Provides timer for OS.
Ex. RTOS Task Schedular.

WIC ⇒ This helps processor to wakeup on Interrupt if it is in a sleep mode.

Instruction Trace interface contains details of Instructions that are being executed.

Software trace holds the amount of memory used.[Stack, Heap, RAM]

MPU provides excess level privileges to actions.

- User space will have full privilege.
- Kernel space will have less privilege.

During Interrupt, vector addresses will be fetched by I-CODE and stacking and unstackig will be provided by D-CODE.

AMBA ⇒ Advance µC Bus Architectur.

APB ⇒ Advance Peripheral BUS(UART,SPI,I2C)

AHB ⇒ Advance High Performance(USB, Ethernet, Memory, DMA,RAM)
DMA ⇒ Direct Memory Access

AXI ⇒ Advance eXtansible Interface

PPB ⇒ Private Peripheral Bus

- Internal PPB (For connect Core to NVIC,SB)
- External PPB

Burst support

The buses will provide error free data transmission even after having data burst from different peripherals. The data may be of 8/16/32 bit.

Multiple Bus Master

This allows multiple MASTER-SLAVE configurations. By default core is Master.
