Basics of ARM Cortex part 3

Part 2

linker files [.ld] contains base addresses.

startup file [.s] contains vector address for interrupt.

BIST → Built-In Self Test.

IVT is mapped closer to wherever booting program is stored. [Internal SRAM]

Commonly Used CMSIS-Core Fxns

Functions	Usage
void NVIC_EnableIRQ (IRQn_Type IRQn) void NVIC_DisableIRQ (IRQn_Type IRQn) void NVIC_SetPriority (IRQn_Type IRQn, uint32_t priority)	Enable an external interrupt Disable an external interrupt Set the priority of an interrupt
voidenable_irq(void) voiddisable_irq(void) void NVIC_SetPriorityGrouping(uint32_t PriorityGroup)	Clear PRIMASK to enable interrupts Set PRIMASK to disable all interrupts Set priority grouping configuration

Sub priority exception is used if same priority exceptions from that group occurs at a same time.

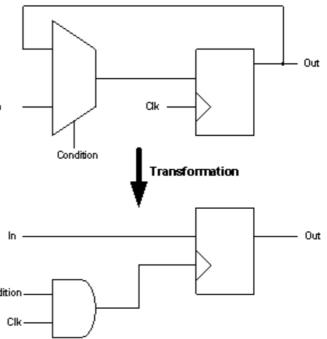
Stacking and **unstacking** is done on **D-bus** and **Vector fetch** i.e fetching of address of interrupt from IVT takes place on **I-bus**.

Three Methods of setting interrupt priority:

- using SetPriority()
- using PRIMASK
- · using Grouping and sub-priority level

Clock Gating

- Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation.
- Clock gating saves power by adding more logic to a circuit to prune the clock tree.
- Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states because Conc Switching states consumes power.
- When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.



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