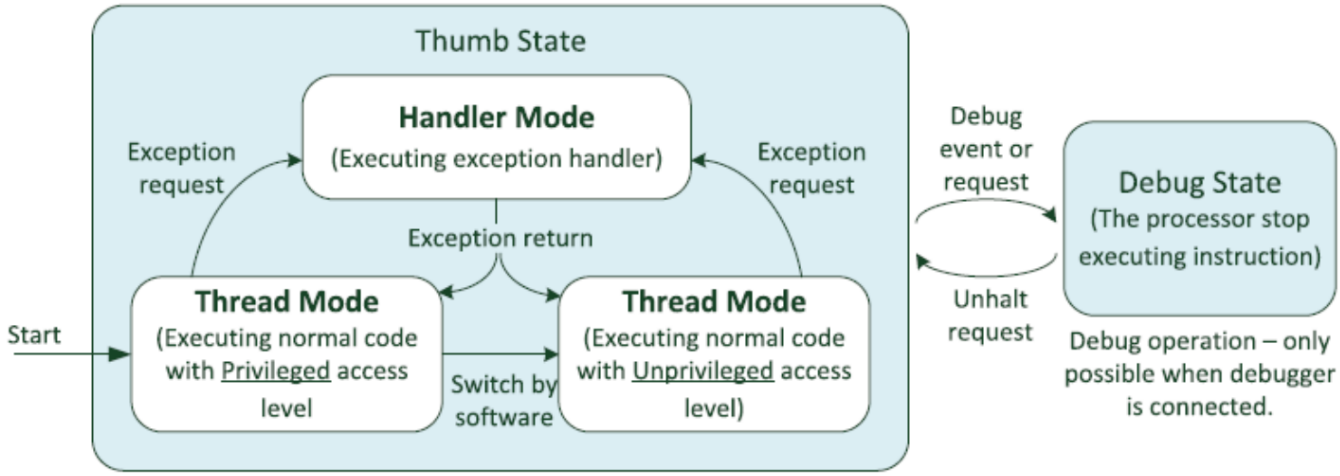
Basics of ARM Cortex part 2

Part 1

Architecture of ARM

Programmer's Model

Operation states and Modes



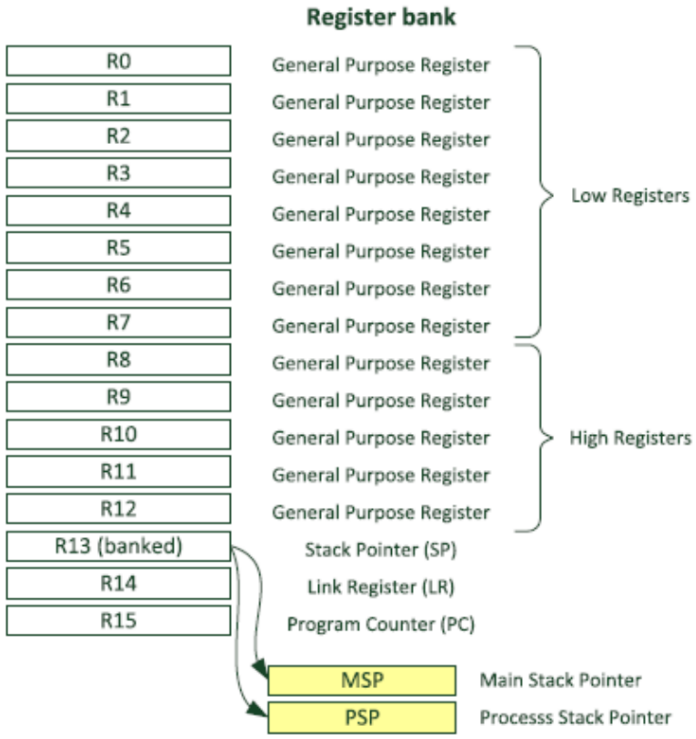
M3 has Thumb state and Debug State.

Thread mode and Handler mode.

OR operation is used for setting a bit; AND operation is used for clearing a bit.

Register Set

- R0-R12
- General Purpose registers
- R0-R7 low registers due to limited space available in IS , many 16 bit instruction can only access the low registers.
- R8-R12 high registers can be used by 32-bit instruction
- Initial Value of R0-R12 are undefined.
- R13 Stack Pointer
- R14 Link Register
- R15 Program Counter



Stack Pointer –R13

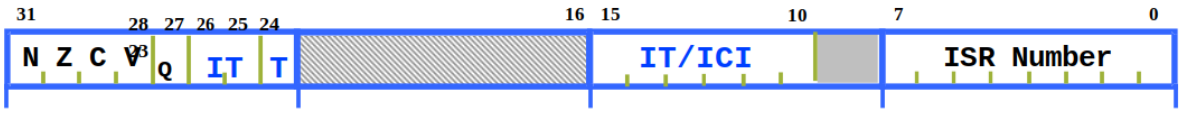
Physically there are two different Stack Pointers:

- Main Stack Pointer is the default Stack Pointer. It is selected after reset, or when the processor is in Handler Mode.
- The other Stack Pointer is called the Process Stack Pointer. The PSP can only be used in Thread Mode. The selection of Stack Pointer is determined by a special register called CONTROL.
- The PSP is normally used when an embedded OS is involved, where the stack for the OS kernel and application tasks are separated.

Link Register – R14

- This is used for holding the return address when calling a function, subroutine or Exceptions.
- At the end of the function or subroutine, the program control can return to the calling program and resume by loading the value of LR into the Program Counter (PC).
- When a function or subroutine call is made, the value of LR is updated automatically.
- If a function needs to call another function or subroutine, it needs to save the value of LR in the stack first. Otherwise, the current value in LR will be lost when the function call is made.

Program Status Register



Program Status Register is of 32 bit.

Application PSR, Execution PSR, Interrupt PSR.

APSR has ALU flags and it has 5 bits.

- N - Negative
- Z - Zero
- C - Carry
- V - Overflow
- Q - Saturation

- T - Thumb state [Always 1]

- IT - If/Then bit.

IPSR uses 8 bits and these are read only bits.

PSR, PRIMASK, FAULTMASK, BASEPRI, CONTROL registers are not memory mapped.

Memory mapped means mappin to memory and getting register address.

MSR and MRS are two instructions used to access above registers.

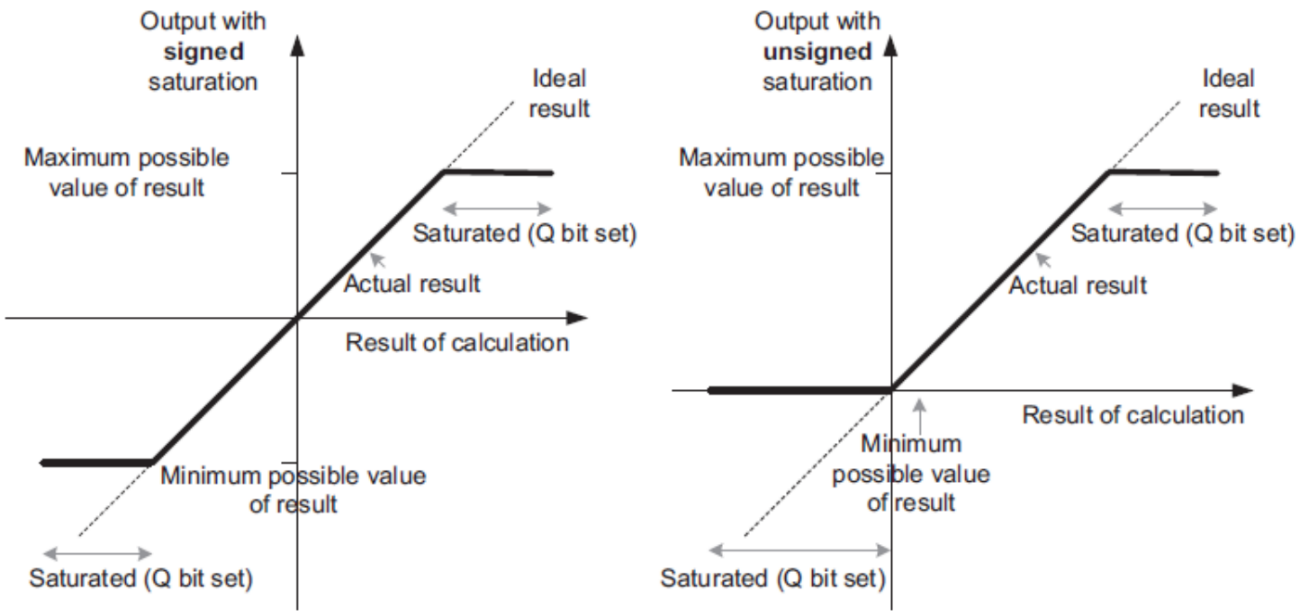
```
MRS - it will copy PSR to the ARM register. [R0-R12]
READING
R0 = PSR
Now, It is possible to modify or operate on copy of PSR i.e. R0

It can be done only in priviledged access mode.
```

```
MSR - it will copy the ARM register to PSR
WRITING
PSR = R0
New modified data can be stored in PSR.

It can be done in both priviledged access mode as well as unpriviledged
access mode.
```

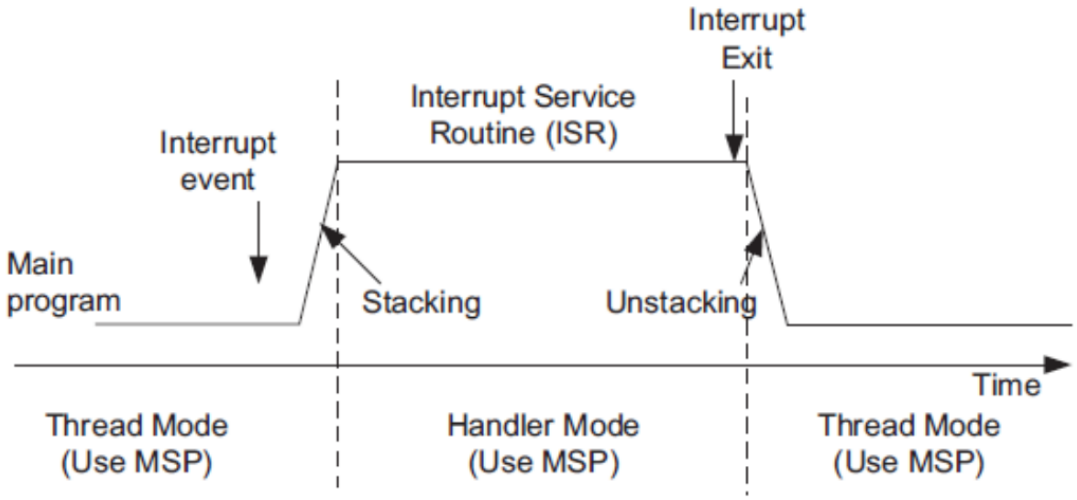
Q Flag – Signed & Unsigned Saturation



HIGHER the number, LOWER the priority.

- PRIMASK - Priority Masking is 1 bit register. It disables all the interrupts with positive priority.
- FaultMask is 1 bit register. It will disable all the interrupts with positive priority and Including FaultMask / Hard fault.
- Non Maskable Interrupt and RESET can not be masked; but NMI is programmable.
- BASEPRI - Base Priority is 8 bit register. Changes the priority level required for preemption. If it is set to 60 then all the interrupts having between 61 - 255 will be disabled.
- **Interrupt Preemption** - If LOWER priority ISR has HIGHER priority ISR then execution of LOWER priority stops and HIGHER priority gets executed first and once this is done then execution of LOWER priority begins.
  If HIGHER priority ISR has LOWER priority ISR then HIGHER priority gets executed first and once this is done then execution of LOWER priority begins.

Both Thread and Handler using MSP



In case of normal OS
Thread uses MSP → Handler uses MSP → Thread uses MSP

In case of custom OS
Thread uses PSP → Handler uses MSP → Thread uses PSP

When interupt X is triggered, jump to the ISR for interrupt X.($1 \leq X \leq 255$)

In an interrupt vector table addresses, last bit i.e bit-0 will always be 1 to indicate the THUMB state.

Example,
0x0800030C is the actual address but the address stored will be 0x0800030D. [IRQ3]

Vector table can be relocated either in CODE segment or in SRAM.

JTAG → Joint Test Action Group is a standard for debugging and it works on 4 pins.

SWV → Serial Wire Viewer uses 2 pin and it is also a debugger.

Embedded Trace Macrocell

Instrumentation Trace Macrocell

Bit banding - If a particular bit needs to be accessed from n-bits, that process is called as bit banding.
