Basics of ARM Cortex part 3

Part 2

linker files [.ld] contains base addresses.

startup file [.s] contains vector address for interrupt.

BIST → Built-In Self Test.

IVT is mapped closer to wherever booting program is stored. [Internal SRAM]

Commonly Used CMSIS-Core Fxns

Functions	Usage
void NVIC_EnableIRQ (IRQn_Type IRQn)	Enable an external interrupt
void NVIC_DisableIRQ (IRQn_Type IRQn)	Disable an external interrupt
void NVIC_SetPriority (IRQn_Type IRQn, uint32_t priority)	Set the priority of an interrupt
void __enable_irq(void)	Clear PRIMASK to enable interrupts
void __disable_irq(void)	Set PRIMASK to disable all interrupts
void NVIC_SetPriorityGrouping(uint32_t PriorityGroup)	Set priority grouping configuration

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Sub priority exception is used if same priority exceptions from that group occurs at a same time.

Stacking and **unstacking** is done on **D-bus** and **Vector fetch** i.e fetching of address of interrupt from IVT takes place on **I-bus**.

Three Methods of setting interrupt priority:

- using SetPriority()
- using PRIMASK
- using Grouping and sub-priority level

Clock Gating

- **Clock gating** is a popular technique used in many synchronous circuits for reducing dynamic power dissipation.
- Clock gating saves power by adding more logic to a circuit to prune the clock tree.
- Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states because Switching states consumes power.
- When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.