UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, ECE 894, Fall 1399
Computer Assignment 1
Basic Switch and Gate Structures in Verilog
Week 3-4

Name:
Date:

1. You are to use nMOS and pMOS transistors in various forms for the realization of the following functions. The functions describe a circuit that we refer to as BCS, or Bit Compare Slice. Use #(3, 4, 5) delay for the nMOS transistors and #(5, 6, 7) for the pMOS transistors. The inputs of BCS are e0, g0, a0, and b0, and its outputs are e1 and g1. For the implementation of these functions you may decide to generate the complement of a function that is not the output (i.e., j1 and k1) for a better transistor-level implementation. For example, it may be better to form complement of j1 instead of j1 as shown below.

```
j1 = a1 ~^ b1
e1 = j1 & e0
k1 = ~a1 & b1 & e0
g1 = k1 | g0
```

Implement j1 or its complement (as you decide) using a Mux based pass-transistor realization. Implement k1 or its complement using a 3-input NAND or an OAI. Implement e1 and g1 using NAND or NOR gates. For these four structures use transistors are specified above. We refer to this circuit as Transistor-level BCS.

2. Generate a testbench for the Transistor-level BCS and apply various test vectors to verify its functionality and the circuit internal structure worst-case delays and its output delays. For the delay values, first estimate the delays manually and then apply test vectors that you come up with in the simulation to adjust the delay values.

3. Replace the four structures of Part 1 with **assign** statements or Verilog primitives. Extract these delay values with those found in Part 2. Generate a new Gate-level BCS circuit.

4. Generate a testbench to examine the Transistor-level BCS and the Gate-level BCS circuits alongside each other. Run simulations and compare the delay values and the differences in the outputs of these circuits.