UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, ECE 894, Fall 1399
Computer Assignment 2
Basic Switch and Gate Structures in Verilog
Week 5-6

Name:
Date:

1. In Assignment 1, you created two versions of a BCS and compared their delay values. Using **assign** statements create a model that mimics the transistor model as closely as possible.

2. As discussed in Lecture 16a, you can cascade several BCS structures to create an n-bit comparator. Using a SystemVerilog **generate** statement build an 8-bit comparator that is composed of eight BCS units of Part 1. Simulate this circuit and calculate its output delays as caused by changes in bits 7 to 0 of the inputs.

3. Instead of a BCS, build a TCS (Two-bit Compare Slice) using basic logic gates. Make sure the longest path from eq and gt inputs to EQ and GT outputs remains at a maximum of two logic levels. Combine gates as much as possible to reduce delays. You do not have to write the gate description in SystemVerilog, and just a circuit schematic is sufficient. Based on the transistor delays of Assignment 1, estimate the delays of the outputs of this circuit and describe a TCS using SystemVerilog **assign** statements. Write a testbench to test this circuit and verify its operation.

4. Using a SystemVerilog **generate** statement build an 8-bit comparator that is composed of four TBCS units of Part 3. Simulate this circuit and calculate its output delays as caused by changes in bits 7 to 0 of the inputs.

5. In a testbench, simulate the two circuits of Part 2 and Part 4 and compare their operations and timing. Explain pros and cons of circuit of Part 4 as compared with that of Part 2.