UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design ECE 367 / Digital System I ECE 894

Fall 1399

Computer Assignment 5-Preparation

Counters, Shifters, State machines - Week 13

Name:	**Date:**
Username:	

In this assignment you will design a Moore sequence detector that detects 1011 on its J input. The W output becomes 1 when the sequence is detected.

Problem Description: A Moore machine that detects 1011 on its J input.

1. Show state diagram of the Moore1011 machine.
2. Describe your machine in SystemVerilog and simulate it to verify its operation. Use a testbench in ModelSim. This phase of simulation is referred to as pre-synthesis simulation.
3. Take your design into Quartus and implement using its SystemVerilog description. It is recommended that you describe this sequence detector in SystemVerilog using Huffman modeling style.
4. Synthesize your design in Quartus and obtain .vo and .sdo files. These files are your post-synthesis netlist and timing files.
5. See synthesis reports, view various diagrams that the synthesis tool generates.
6. Add the post-synthesis output of Part 4 to the testbench of Part 2 and simulate these two implementations of Moore1011 alongside each other.
7. Provide simulation reports and compare the timings of the two implementations.