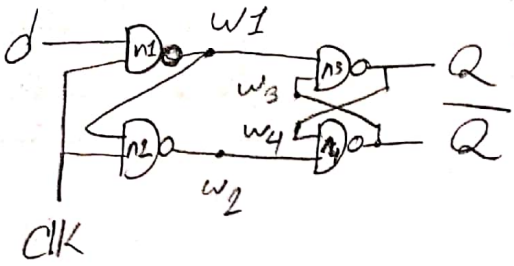
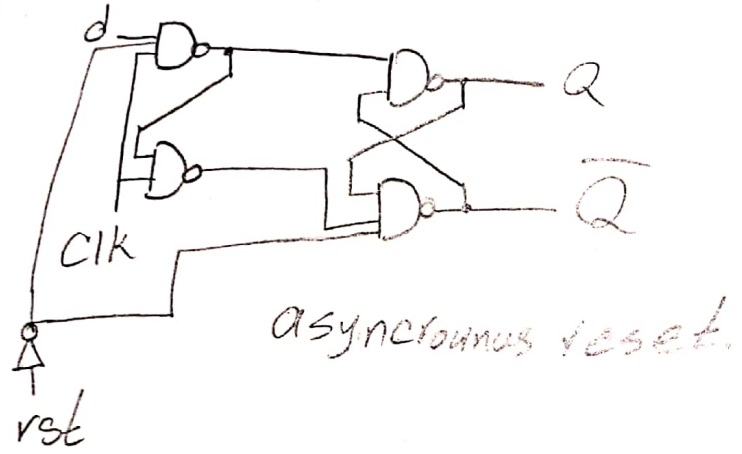
(1)



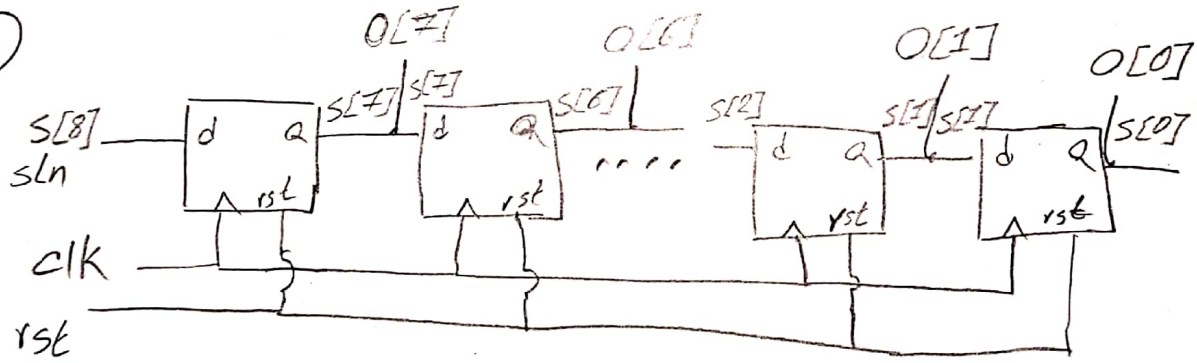
(2) each nand have delay of 8ns.

(3) if d=1 and clk=1 we have 8ns static 1 Hazard.

(4)



(5)



(6) while clk=1 the sln will go to all latches.

(7)