UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design ECE 367 / Digital System I ECE 894
Fall 1399

Small-scale RT Level Components, Iterative Logic - Week 7

Name:	**Date:**
Username:	

In this assignment, you will be using the TCS comparator of Assignment 2, multiplexer-based 2-bit adder of Homework 7 (we will refer to this as Two-bit Multiplexer-based Adder, TMA), a multiplexer-based 2-bit adder incrementor (we will refer to this as Two-bit Multiplexer-based Incrementor, TMI), and discrete logic gates. In all structures delay values from Assignment 1 are used.

1. Describe the TCS circuit as a SystemVerilog module using an **always** statement. Annotate this description by delay values found in Assignment 2 as closely as possible.
2. Using a **generate** statement describe a parameterized n-bit comparator. We refer to this as NCS.
3. In a testbench simulate and test an 8-bit version of the NCS circuit (N8CS). Find the worst-case delay of this circuit.

4. Write multiplexer-based description of TMA.
   A. Write **assign** statements for the necessary multiplexers used in TMA. Use delay values based on gates and transistors used in Assignment 1. The sum outputs can be based on pass-transistor logic, but the carry output must be based on multiplexers that use CMOS structures. Annotate the multiplexer **assign** statements with the corresponding delay values.
   B. Describe the TMA circuit as a SystemVerilog module using the above multiplexers.
5. Using a **generate** statement describe a parameterized n-bit adder. We refer to this as NMA.
6. In a testbench simulate and test an 8-bit version of the NMA circuit (N8MA). Find the worst-case delay of this circuit.

7. Write multiplexer-based description of TMI.
   A. Write assign statements for the necessary multiplexers used in TMI. Use delay values based on gates and transistors used in Assignment 1. The sum outputs can be based on pass-transistor logic, but the carry output must be based on multiplexers that use CMOS structures. Annotate the multiplexer assign statements with the corresponding delay values.
   B. Describe the TMI circuit as a SystemVerilog module using the above multiplexers.
8. Using a **generate** statement describe a parameterized n-bit incrementor. We refer to this as NMI.

9. In a testbench simulate and test an 8-bit version of the NMI circuit (N8MI). Find the worst-case delay of this circuit.

10. Using an N8MI, an N8MA, and discrete logic gates with delays based on delay values of Assignment 1, describe a circuit that calculates the absolute value of the difference of its two unsigned 8-bit inputs. We refer to this circuit as *AbsDiff* and its inputs are *ref* and *data*.

11. Simulate the *AbsDiff* circuit in a testbench. Make sure you exercise the circuit for various data types and corner cases. Use multiple concurrent statements and use constructs such as **repeat** and **$random()** for test data generation.

12. Using the *AbsDiff* of the above part, build a circuit with a reference input (*refI*) and two data inputs (*dataA* and *dataB*). The output of the circuit becomes the data input with a lesser distance from the reference. You can use other structures such a multiplexer and discrete logic gates. We refer to this circuit as *LessDistance*.

13. Write a testbench for the above structural *LessDistance*. Make sure you exercise the circuit for various data types and corner cases. Use multiple concurrent statements and use constructs such as **repeat** and **$random()** for test data generation.

14. Based on the above simulation, develop a behavioral description of the *LessDistance* circuit and in a testbench, instantiate the structural and behavioral versions of this circuit. Make sure you exercise the circuit for various data types and corner cases. Use multiple concurrent statements and use constructs such as **repeat** and **$random()** for test data generation.

Deliverables: For each of the above 6 parts (i.e., 1-3, 4-6, 7-9, 10-11, 12-13, and 14) three tasks A, B and C must be completed and demonstrated.

A. Show a diagram for the circuit you are designing and/or simulating. This must be in form of a document.
B. Show simulation project file and run the simulation. This is an oral presentation.
C. Show the test procedure and your choice of SystemVerilog constructs for developing the test bench. This is an oral presentation.