Fall 99

CA1 Report

Digital Logic Design

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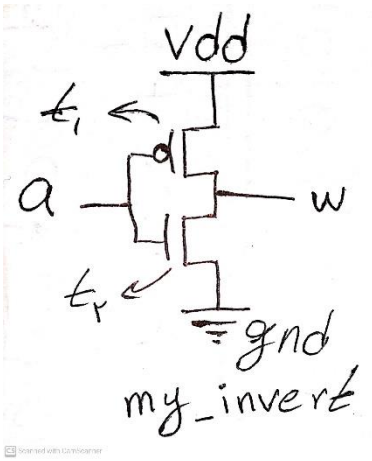
Part 1

I implemented all needed gates of part one using transistors (P1-1 to P1-8).

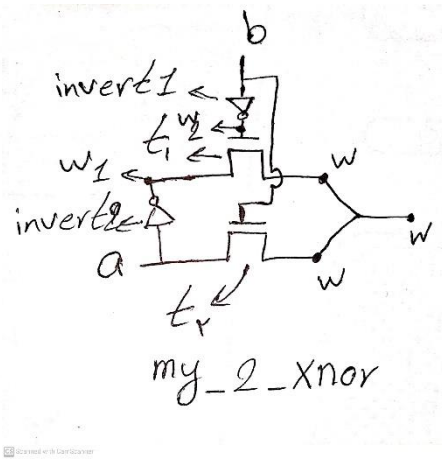
Then by combining them I created whole structure of part one (P1-9).

The truth table of Part one structure(P1-10).

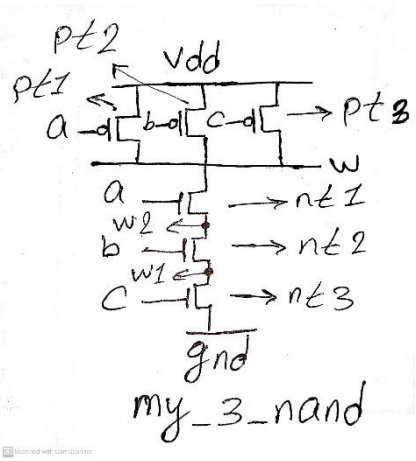
All of these structures is available in one.v file. (Name of each module is under the picture)



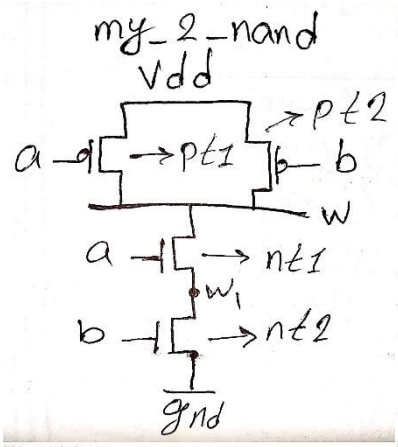
(P1-1)



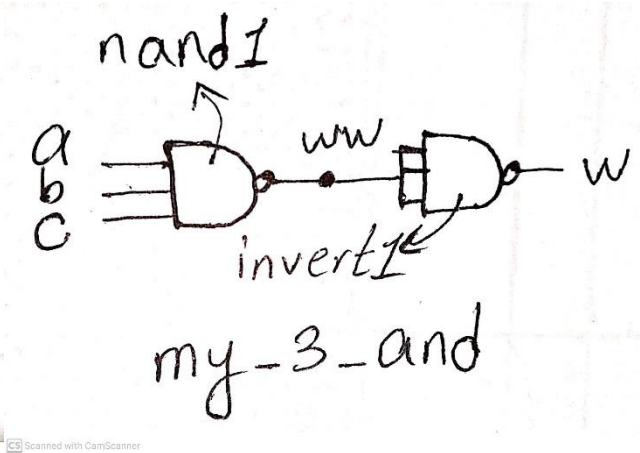
(P1-2)



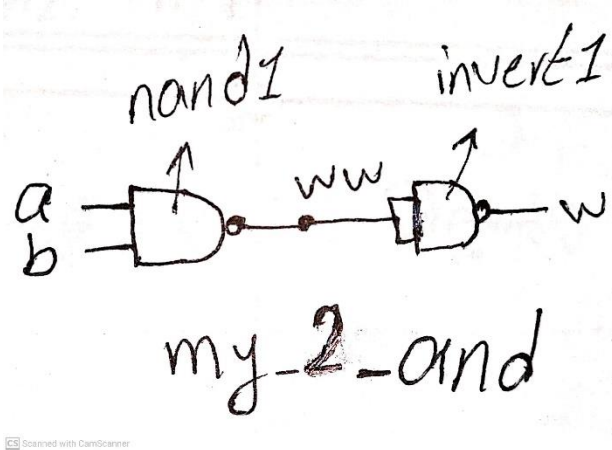
(P1-3)



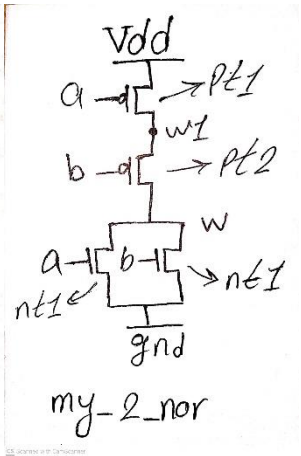
(P1-4)



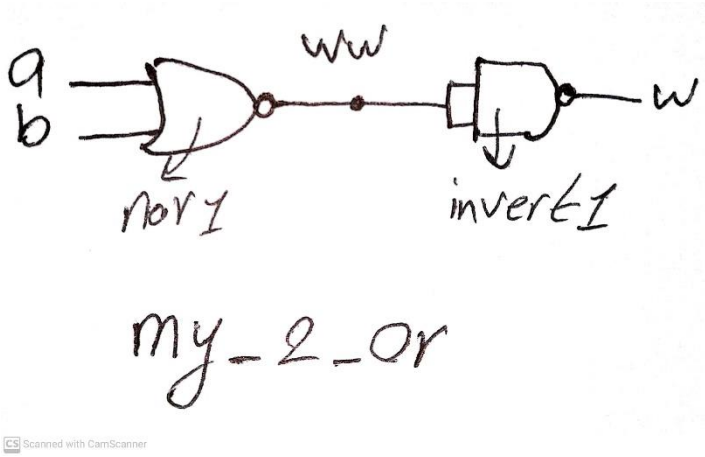
(P1-5)



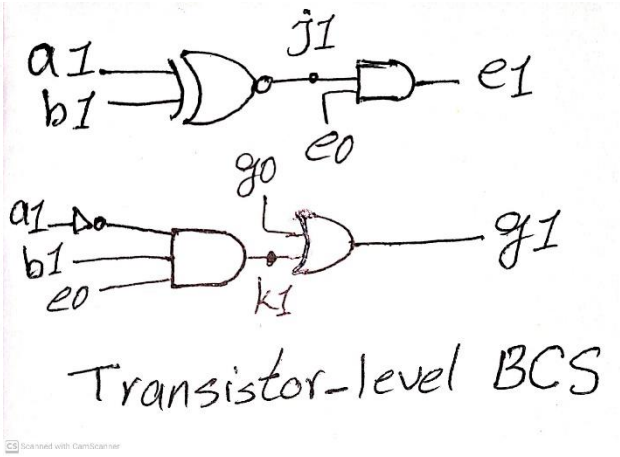
(P1-6)



(P1-7)



(P1-8)



(P1-9)

a1	b1	e0	g0	e1	g1
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	1	1

(P1-10)

Part 2

Manual delay calculation (to1, to0)

my_invert → (5,7) my_2_xnor → (12,12) my_3_nand → (15,12) my_2_nand → (10,8)

my_3_and → (27,27) my_2_and → (18,18) my_2_nor → (10,14) my_2_or → (24,18)

transistor_level_bcs → (51,45)

Simulation delay (to1, to0)

my_invert → (5,7) my_2_xnor → (12,12) my_3_nand → (15,12) my_2_nand → (10,8)

my_3_and → (27,17) my_2_and → (13,18) my_2_nor → (10,15) my_2_or → (19,18)

transistor_level_bcs → (37,45)

There is some few differences between manual and simulation delays witch is caused by not calculating all possible input changes.