On Timing Closure with OpenCPI

Shep Siegel, Atomic Rules LLC

Contemporary FPGA synthesis and place and route (P&R) tools are timing-driven. They attempt to satisfy a timing constraint provided by the user. In synthesis, these results can only be estimates as the placement and routing, and thus the actual wire-delays, have not been determined. In P&R, the circuit is fully established and an exact measure of delays can be observed. This note specifically addresses the exact timing results produced by P&R.

Sequential circuits can be characterized by an Fmax and its reciprocal period. For example, a 125 MHz Fmax has an associated 8 nS clock period. To function correctly under worst-case conditions of process, temperature, and voltage (PVT); every sequential arc must complete in less the clock period. Common contributors to each arc include, but are not limited to:

- The clock-Q of the source DFF
- The combinatorial logic of the LUTs
- The wire-delay of the interconnect (routing)
- The setup time of the destination DFF

Anytime the sum of these contributors exceeds the clock period, a setup violation is present. This is reported as “negative slack” in the signal arrival vs. clock race. Regardless of the magnitude of the violation, how negative the slack is, this is called a timing error.

There are many scenarios for timing errors. One of the most common scenarios arises from a combination of poor placement and/or too many combinatorial LUT stages between DFFs. The common remedies are better placement and/or bisecting the critical path with another DFF.

In OpenCPI, we classify timing errors in to “serious” and “marginal” violations. We discriminate between the two when the violation exceeds 10% of the clock period. When negative setup slack exceeds 800 pS of an 8 nS clock period, we say this is a serious violation. When it is less, we say it is a marginal violation. Marginal violations are less likely to fail than serious violations, especially under lab conditions for temperature and voltage. Make no mistake: **all timing violations are errors**; and unacceptable in any production bitstream.

Many marginal violations may be cleared by floor planning, pipelining, or both. In some cases simply re-running P&R with different conditions (tool versions, other IPs) will cause marginal violations to be cleared or appear. Serious violations often require a step back to understand the inherent structural cause. Because of this, it is one common, but not mandatory or singular, development tactic to look past marginal violations when first achieving functional correctness; then to later clear the remaining errors.

A Path Showing > 10% Serious Violation (> 800pS negative slack on 8 nS clock period)

```
Slack (setup path):     -1.183ns (requirement - (data path - clock path skew + uncertainty))
  Source:               ftop/ctop/inf/dp1/tlp_inF/pos_3 (FF)
  Destination:          ftop/ctop/inf/dp1/tlp_outF/Mshreg_D_OUT_31_0 (FF)
  Requirement:          8.000ns
  Data Path Delay:      8.774ns (Levels of Logic = 9)
  Source Clock:         ftop/trnClk rising at 0.000ns
  Destination Clock:    ftop/trnClk rising at 8.000ns
  Maximum Data Path: ftop/ctop/inf/dp1/tlp_inF/pos_3 to
ftop/ctop/inf/dp1/tlp_outF/Mshreg_D_OUT_31_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X28Y57.AQ      Tcko                  0.471   ftop/ctop/inf/dp1/tlp_inF/pos<3>
                                                       ftop/ctop/inf/dp1/tlp_inF/pos_3
    SLICE_X29Y59.C3      net (fanout=4)        0.881   ftop/ctop/inf/dp1/tlp_inF/pos<3>
    SLICE_X29Y59.C       Tilo                  0.094   ftop/ctop/inf/dp1/tlp_fabMetaAddr<23>
    SLICE_X28Y60.D5      net (fanout=130)      0.551   ftop/ctop/inf/dp1/tlp_inF/_COND_126<3>
    SLICE_X28Y60.D       Tilo                  0.094   ftop/ctop/inf/dp1/tlp_inF_D_OUT<62>

...
    SLICE_X33Y70.B6      net (fanout=7)        0.639   ftop/ctop/inf/dp1/tlp_outF_ENQ
    SLICE_X33Y70.B       Tilo                  0.094   ftop/ctop/inf/dp1/tlp_outF_D_IN<114>
                                                       ftop/ctop/inf/dp1/tlp_outF/dat_15_not00011
    SLICE_X36Y72.CE      net (fanout=37)       0.802   ftop/ctop/inf/dp1/tlp_outF/dat_15_not0001
    SLICE_X36Y72.CLK     Tceck                 0.325   ftop/ctop/inf/dp1_server_response_get<31>
-------------------------------------------------  ---------------------------
    Total                                      8.774ns (1.642ns logic, 7.132ns route)
                                                       (18.7% logic, 81.3% route
```