Verifying that ML555 boards are recognized as OpenCPI PCIe devices

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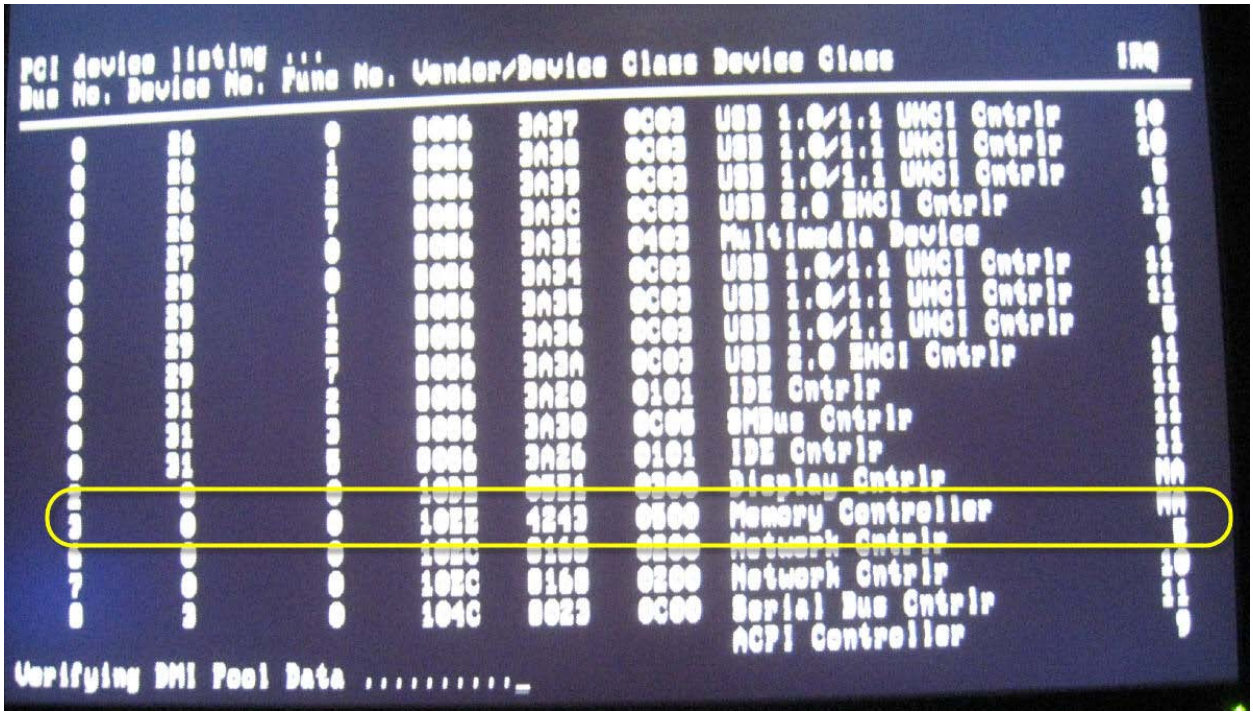
In all OpenCPI bitstreams, certain choices are made and programmed into the PCIe endpoint device to allow the BIOS and OpenCPI driver to recognize it. These choices include setting the following:

Parameter	Value	Meaning
VendorId	0x1055	Xilinx
DeviceId	0x4243	OpenCPI Device
Class Code	0x0500	Memory Controller

And others that can be seen in the file $OCPI/coregen/endpoint/endpoint.xco file used to build the bitstream.

Prior to OS Boot, the motherboard BIOS scans for PCIe devices and assigns them configuration data such as Bus 3, as shown in the screen photo below:



If for some reason the device is not detected, inspect D1 on the ML555 board to see if the PCIe link is up (lit means link is up). Lack of the link being up could be due to factors including: board not programmed with OCPI default bitstream, jumpers or dip switches set incorrectly, defective hardware.

Before any OS software can act on the board; the BIOS must have seen it at boot time.