

### OpenCPI FPGA Boards at Atomic Rules

| ID  | Board Vendor                 | Board Model              | Board Name  | FPGA      | PCIe    | FTop    | Status                      |
|-----|------------------------------|--------------------------|-------------|-----------|---------|---------|-----------------------------|
| 101 | <a href="#">Xilinx</a>       | <a href="#">ML555</a>    | ml 555      | V5-LX50T  | Gen1 x8 | FTopV5  | B,H(3),R,W <sub>12.4</sub>  |
| 102 | <a href="#">Abekas</a>       | <a href="#">Alder</a>    | al der      | V5-LX50T  | Gen1 x8 | FTopV5  | B,H(1), W <sub>12.4</sub>   |
| 103 | Generic                      | Generic                  | schi st     | V5-SX95T  | Gen1 x8 | FTopV5  | B,P(1),R, W <sub>12.4</sub> |
| 104 | <a href="#">Xilinx</a>       | <a href="#">XUPV5</a>    | xupv5       | V5-LX110T | Gen1 x1 | FTopV5  | B,H(2),R, W <sub>12.4</sub> |
| 105 | Generic                      | Generic                  | bi ot i t e | V5-FX130T | Gen1 x8 | FTopV5  | U1                          |
| 106 | <a href="#">HiTechGlobal</a> | <a href="#">Net10G</a>   | nf10        | V5-TX240T | Gen1 x8 | FTopV5  | B, H(0)                     |
| 107 | Generic                      | Generic                  | ill i t e   | V5-LX330T | Gen1 x8 | FTopV5  | B,P(0)                      |
| 108 | <a href="#">Xilinx</a>       | <a href="#">ML605</a>    | ml 605      | V6-LX240T | Gen2 x4 | FTopV6  | B,H(1),R, W <sub>12.4</sub> |
| 109 | <a href="#">Xilinx</a>       | <a href="#">SP605</a>    | sp605       | S6-LX45T  | Gen1 x1 | FTopS6  | B,H(1)                      |
| 110 | <a href="#">Altera</a>       | <a href="#">4CGX15N</a>  | al cy4      | 4CGX-12   | Gen1 x1 | FTopCGX | H(1)                        |
| 111 | <a href="#">HiTechGlobal</a> | <a href="#">S4GX-230</a> | htgs4       | 4SGX-230  | Gen2 x8 | FTopSGX | U2, H(0)                    |

#### Status Codes:

B = In OpenCPI build

H = Hardware in Use (number of boards located at AR-Auburn)

P = Proprietary Hardware (number of boards located at AR-Auburn)

R = In Test Regressions

U1 = Under Consideration; U2 = Planning Phase

W = Known Working (ISE or Quartus Tool Version)

### Development/Target Machines for PCIe at Atomic Rules

| Machine Name | OS             | Chipset | GPU    | DRAM (GB) |
|--------------|----------------|---------|--------|-----------|
| core980      | RHEL6.0 WS 64b | X58     | GTX470 | 12        |
| core960      | RHEL5.3 WS 64b | X58     | GTX285 | 12        |
| core920      | RHEL5.3 WS 64b | X58     | GTX280 | 12        |
| amd790 [1]   | RHEL5.3 WS 64b | 790FX   | 8800GT | 4         |
| Q9550        | XP-SP3 32b     | X48     | GTX280 | 4         |
| XP8500       | XP-SP3 32b     | X48     | 8800GT | 4         |

#### Note Codes:

[1] = On loan to OpenCPI development partner in Exeter, NH