OpenCPI FPGA Boards/Platforms at Atomic Rules

ID	Board Vendor	Board Model	Platform Name	FPGA	PCIe	Status
101	Xilinx	ML555	ml555	V5-LX50T	Gen1 x8	A, B, H(3), R,$W_{13.3}$
102	Abekas	Alder	alder	V5-LX50T	Gen1 x8	B, H(1), R,$W_{13.3}$
103	Generic	Generic	schist	V5-SX95T	Gen1 x8	A, B, P(1), R, $W_{13.3}$
104	Xilinx	XUPV5	xupv5	V5-LX110T	Gen1 x1	B, H(2), R, $W_{13.3}$
105	Generic	Generic	biotite	V5-FX130T	Gen1 x8	U1
106	HiTechGlobal	Net10G	nf10	V5-TX240T	Gen1 x8	A, B, H(1), R,$W_{13.3}$
107	Generic	Generic	illite	V5-LX330T	Gen1 x8	B, P(0)
108	Xilinx	ML605	ml605	V6-LX240T	Gen2 x4	A, B, H(5), R, $W_{13.3}$
109	Xilinx	SP605	sp605	S6-LX45T	Gen1 x1	B, H(1)
110	Altera	4CGX15N	alcy4	4CGX-12	Gen1 x1	H(1)
111	Altera	4SGX230N	alst4	4SGX-230	Gen2 x4	A, B, H(1), $W_{11.1}$
112	HiTechGlobal	S4GX-360	htgs4	4SGX-360	Gen2 x4	B, H(1)
113	Xilinx	KC705	kc705	K7-325T	Gen2 x4	B, H(1), $W_{13.3}$
114	Xilinx	VC707	vc707	V7-585T	Gen2 x4	U1
115	HiTechGlobal	TBD	htgs5	5SGX-TBD	Gen2 x4	U1
116	Bittware	S5-PCIE	s5pe	5SGX/GS	Gen2 x8	U1

Status Codes:

A = Active Development and Use (in machines below)
B = In OpenCPI build
H = Hardware in Use (number of boards located at AR-Auburn)
P = Proprietary Hardware (number of boards located at AR-Auburn)
R = In Test Regressions
U1 = Under Consideration; U2 = Planning Phase, expected in Build shortly
W = Known Working (ISE or Quartus Tool Version)

Development/Target Machines for PCIe at Atomic Rules

Machine Name	OS	BIOS	Chipset	GPU	DRAM (GB)	Near PCIe	Far PCIe
core980	RHEL 5.6 WS 64b	E768.82	X58	GTX470	12	ml605	kc705
core960	RHEL 5.6 WS 64b	E758.SZ.2C	X58	GTX285	12	schist	ml605
core920	RHEL 5.6 WS 64b	E758.82	X58	GTX280	12	ml555	alst4
vm121	RHEL 5.6 WS 64b		VM		4		
w7-q9550	Win7 Pro SP1 64b		X48	GTX580	4		
XP8500	XP-SP3 32b		X48	8800GT	4		
amd790 [1]	RHEL 5.6 WS 64b		790FX	8800GT	4	ml605	ml555

Note Codes:

[1] = On loan to OpenCPI development partner in Exeter, NH

Updated: 2011-11-17