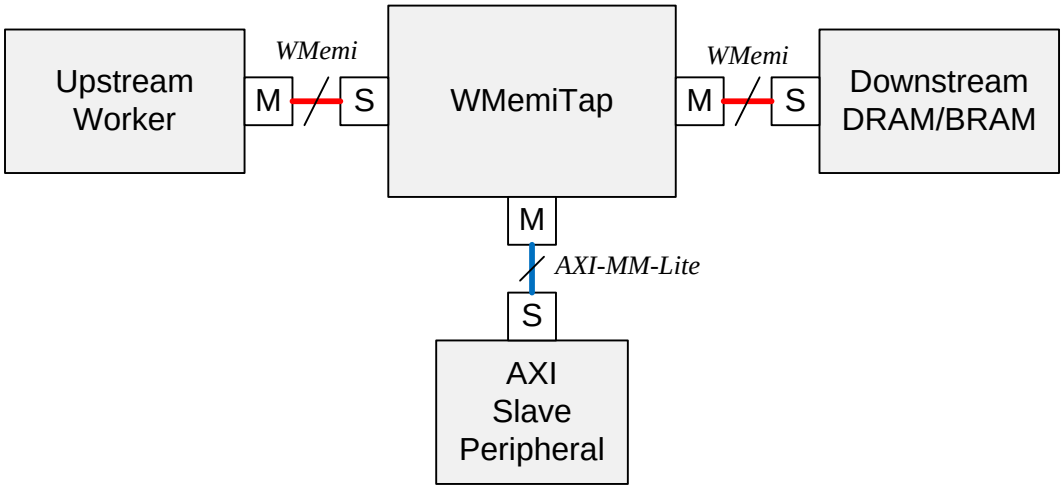
1 WMEMITAP - AN AXI TAP ACROSS A WMEMI LINK

WMemi is one of the five core Worker Interface Profiles (WIPs) used by RTL IPs with OpenCPI [1]. In some OpenCPI use-cases, WMemi is employed as a singleton master-slave link between an application looking to access bulk memory and a device-worker providing memory resource in the form of BRAM or FPGA-attached DRAM. In other use-cases, there is the requirement to use WMemi not just to communicate with memory, but to also communicate with AXI slave peripherals, such as an AXI UART or GMAC. WMemiTap provides a means to serve this second use-case as illustrated in the diagram below:



1.1 SPECIFICATIONS AND FEATURES

- Separate FIFO channels for WMemi Request, Data-Handshake, and Response
- Standard OpenCPI WMemi interfaces: 128b (16B) Data; 36b (64 GB) Address
- Standard AXI-MM-Lite-Master interface: 32b (4B) Data, 32b (4GB) Address

1.2 USAGE

There are no user programmable registers in WMemiTap.

The source code for WMemiTap implements a function isMemoryAddr() that is used to decide if the 36b address on the request is for WMemi Memory or for AXI. In the current implementation, the decision is made simply by looking at address bit 31. If it is 0, the request is for WMemi Memory; if it is 1, the request is for AXI.

Requests targeting WMemi memory pass-through as if WMemiTap were transparent. In reality, there are two cycles of added request and response latency added.

Requests targeting AXI are converted from WMemi requests with the following rules:

- The 36b WMemi address width is truncated to a 32b AXI address width
- The 128b WMemi data width is truncated to a 32b AXI data width (the 32 LSBs are preserved)
- For AXI reads, the 32b AXI read response data is placed in the 32 LSBs of the WMemi 128b data
- AXI access locks the WMemiTap until the response; preventing another cycle until AXI completes

[1] opencpi.org/documentation