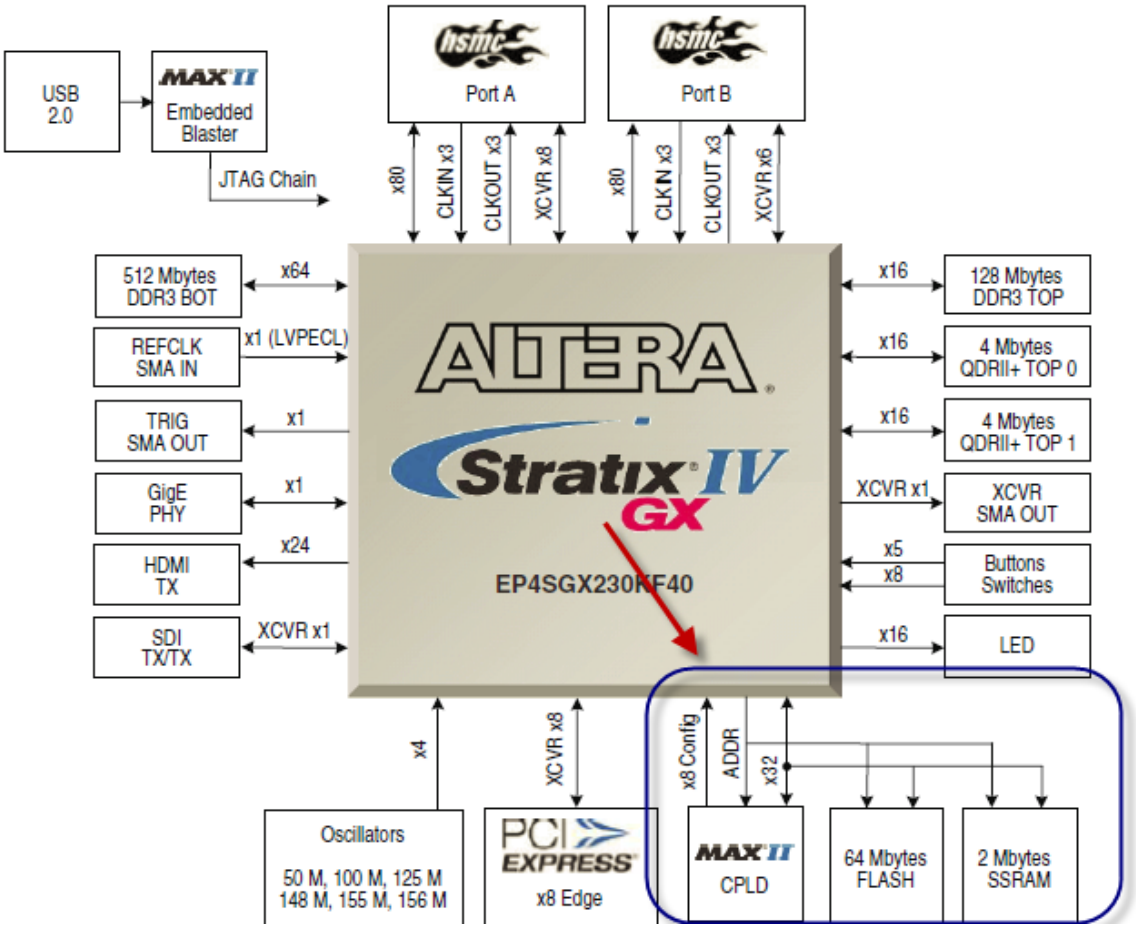
Flash Writing Issue with Altera S4GX ("alst4") Platform

Overview

The Altera S4GX platform "alst4" places an Altera MAXII CPLD in the signal path of the S4GX FPGA and the flash device. Altera does not make source code for the CPLD or their example applications available. It is uncertain what involvement the CPLD is supposed to have. Reads to FLASH appear to work; however writes do not. Without the source code to the CPLD, it is difficult to guess in which cases the Altera MAXII CPLD is active or passive. Further reverse engineering is required to achieve write functionality.

The absence of both CPLD source and a Verification model of the flash device make functional simulation impossible.

The diagram below shows the affected functional block.



According to Altera:

Flash

> *The flash interface consists of a single synchronous flash memory device, providing 64 Mbyte interface with a 16-bit data bus. This device is part of the shared FSM Bus, which connects to flash memory, SSRAM, and the Max II CPLD EPM2210 System Controller.*
>
> *There are two 256 Mbyte die per package with A(25) low selecting the lower die and A(25) high selecting the upper die. Parameter blocks are 32 K and main blocks are 128 K. The parameters of this device are located at both the top and bottom of the address space.*
>
> *This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps. The write performance is 125 µs for a single word and 440 µs for a 32-word buffer. The erase time is 400 ms for a 32 K parameter block and 1200 ms for a 128 K main block.*

Note that the “FSM bus” is not a standard; it is an ad hoc name for the grouping of SRAM and Flash by way of the CPLD.