Data Conversion and the Sample-Message Bounds

Latency and Time Concerns

Shepard.Siegel@atomicrules.com

Designer's Development Notes

2010-02-02

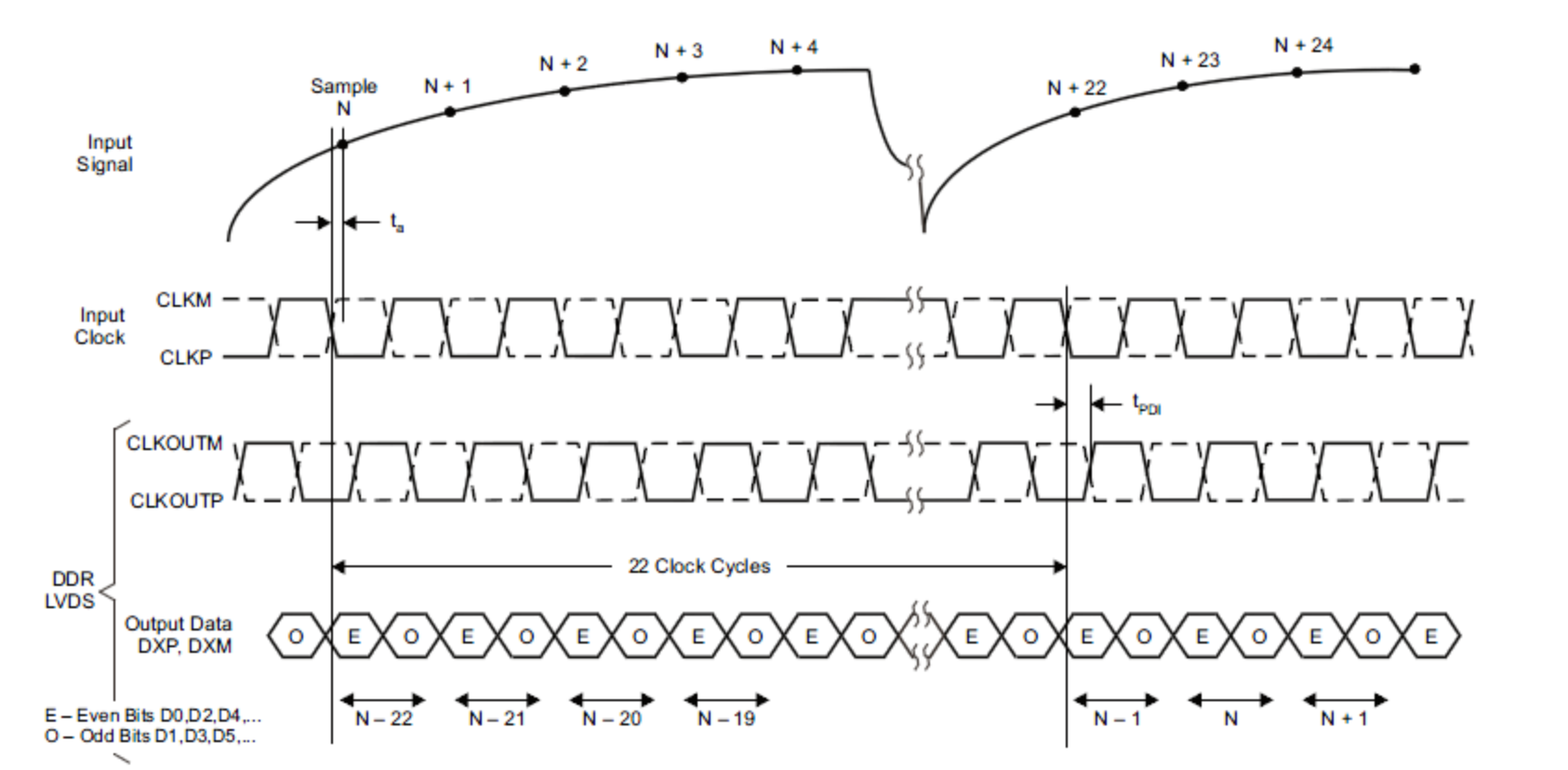
Collection and Emission

- “Collection”: Analog/Digital Converters (ADCs) accept an analog input signal and produce a discrete time series – a “collection” process
- “Emission”: Digital/Analog Converters (DACs) accept a discrete time series and produce an analog output – an “emission” process
- Synonymous with
  - Receive and Transmit (SIGINT/SDR/EW)
  - Acquire and Display (Image Exploitation)
  - Record and Playback (Data/Instrumentation Recording)
  - Ingress and Egress (Networking)
  - In and Out (from the digital system actor’s view)

Latency

- Most converters have a fixed delay between their analog and digital domains
  - TI ADS62P49, 22 cycles@250MHz = 88 nS latency
  - Same device, Aperture Delay = 1.7 nS
  - Same device, Aperture Uncertainty = 1000 pS
  - Same device, Aperture Jitter= 145 fS (RMS)
- Strong motivation to
  - Mitigate the substantial (fixed, known) latency
  - Not to degrade the (superb, small) variation

Converter Latency



Ref: TI ADS62P49 Data Sheet

Time

- Actual Time – Time in the analog domain with regard to an unstoppable timing reference
  - In the preceding figure, when Sample-N is captured
- Signal Time – Time in the digital domain that may advance in synchrony or not; faster or slower, and even stop
  - In the preceding figure, when Sample-N is output

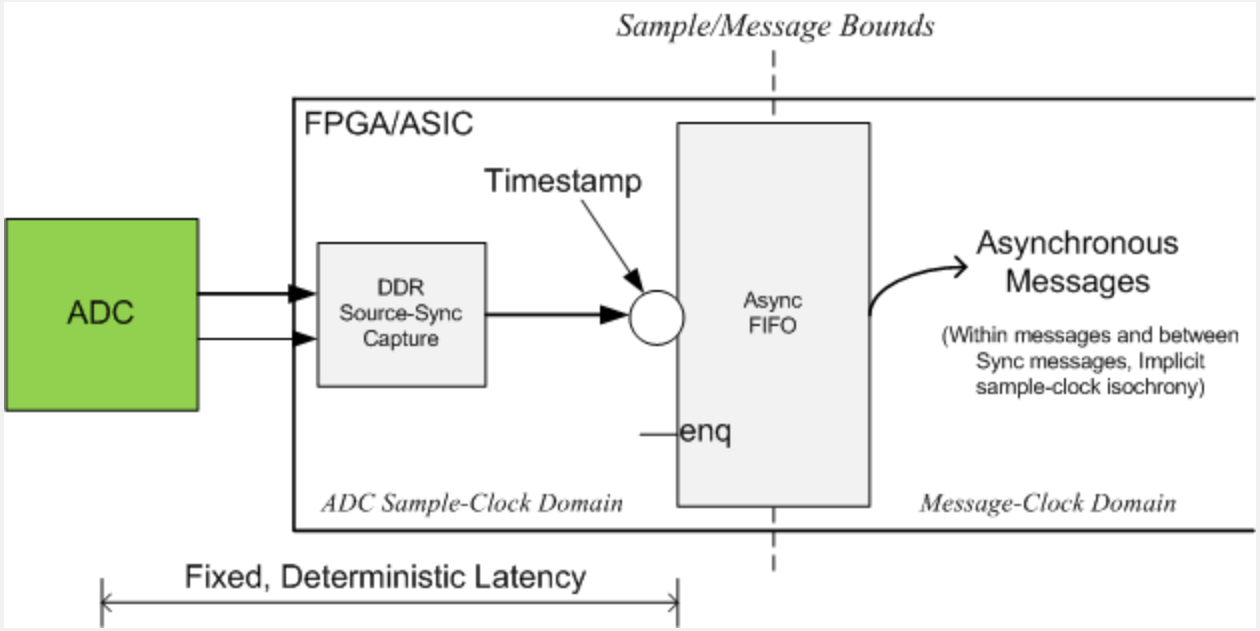
Ref: VITA-49 Appendix B.8

Deterministic Latency

- Discrete, digital samples marching from an ADC or to an DAC generally have a fixed, specified latency
  - Sample time is related to Actual time by the sample rate
- When latency is fixed, actual and signal time relationships can be calculated
  - When latency is uncertain, so too is the actual/signal time relationship

Sample-Message Bounds

- The point in the data collection/emission process where digitized samples are converted to/from messages is termed the “sample-message bounds”
  - Periodic (Isochronous) Samples ↔ Asynchronous Message Stream
  - Practical point of timestamp insertion



Device Interface IP

- ASIC/FPGA design decisions can influence the collection/emission time uncertainty
- Implementations which resolve actual- and signal- time in the sample-clock domain are ***immune*** to FIFO fall-through uncertainties
  - Fall-through uncertainties can be 100s of sample clock periods
- Implementing time-rendezvous in the sample-clock domain can be challenging

OpenCPI ADCWorker – 3 sample delay