Altera Lessons Learned

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Overview

Atomic Rules was subcontracted by MFS as part of OpenCPI Phase 2 to port specific functionality that was previously implemented with Xilinx FPGAs unto Altera FPGAs. Taken together, the Xilinx and Altera duopoly dominate the FPGA (PLD) market as shown below. By adapting key pieces of OpenCPI to work with Altera; OpenCPI is shown to be "vendor-agnostic", at least between Xilinx and Altera. This document captures the "lessons learned" in that process.

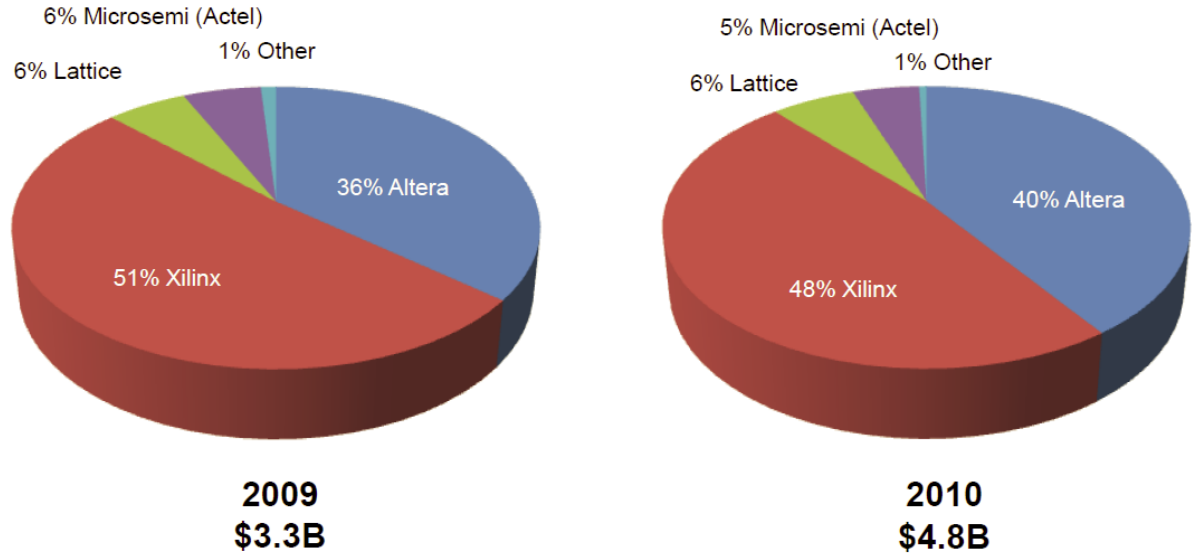


Figure 1 - PLD Market Share

Source: Altera

Tools

Xilinx and Altera offer a similar methodology to transform a circuit represented in RTL to a bitstream that can be run on their FPGA device. Both vendors have their strengths and weaknesses. The table below captures some of the similarities and differences in names and versions.

Attribute	Altera	Xilinx
Tool suite	Quartus	ISE
Version Used (10/2011)	11.0sp1	13.2
Synthesis	Quartus	XST
Simulation	Modelsim “Altera Edition”	ISim
In-Circuit Debug	SignalTap	ChipScope

The Altera Build Process

To build Altera bitstreams, the following ten step process was used. There are most probably other ways to achieve the same result; but this process was use at the suggestion of the Altera FAEs.

Step	Action	Description
1	./cleanit	(script) Remove all prior artifacts from build directory.
2	./pullsrc	(script) Bring into the build directory the clean top-level .v and .qsf files
3	quartus &	(GUI) Launch Quartus GUI
4	Open .qpf	(GUI) Open the .qpf file associated with the project
5	Run Analysis & Synth	(GUI) Run Analysis and Synthesis on the design (button adjacent play)
6	Megafunction .qip	(GUI) Add to the project the .qip file associated with megafunction
7	Megafunction .tcl	(GUI) Add to the project the .tcl “pin assignment” script
8	Run .tcl	(GUI) Run the .tcl pin assignment script (note progress bar)
9	Run Full Compile	(GUI) Click the “play” button (typical 40~60 minute builds)
10	./sof2flash	(script) Convert the .sof bitstream to flash so it can be downloaded

General Observations

Documentation

There were a numerous defects that were either out and out defects in documentation, tacitly incorrect; or were errors of omission.

Avalon

Altera has a proprietary signaling protocol called Avalon, of which there are streaming and memory-mapped variants. However, almost every IP used different variations on the interface. A comment in the Altera documentation paraphrased below, is typical of the variation among standard theme:

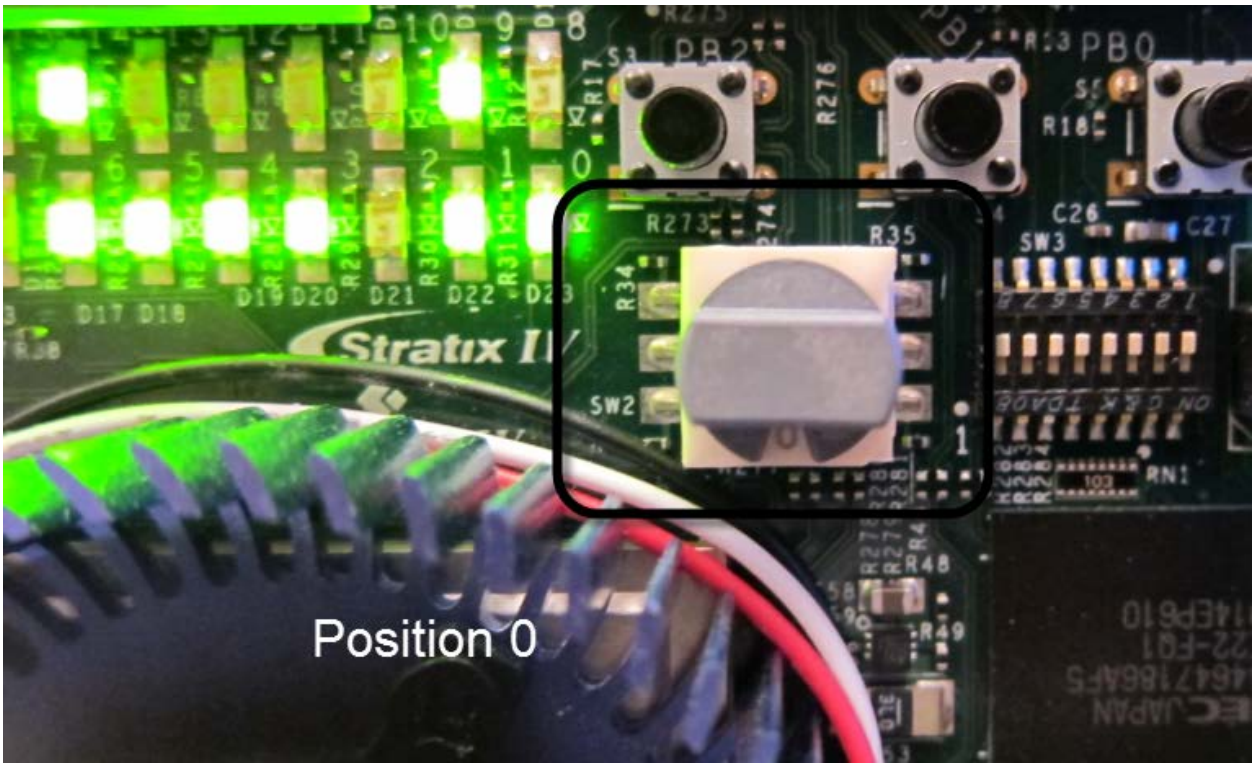
> "… *Unlike other Avalon-MM signals, this signal does not stay asserted if this other signal is de-asserted*."

This deviation from a standard, even a proprietary one such as Avalon, increases complexity and reduces interoperability.

Downloading a Bitstream to Altera Flash

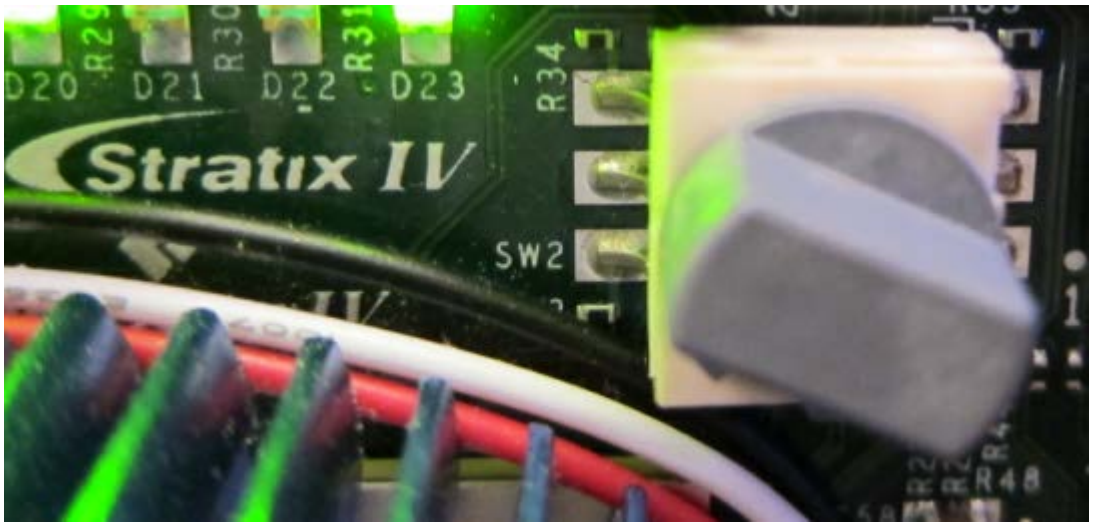
The following process is used to download a .flash file to the “alst4” platform.

Set the board SW2 rotary switch to the horizontal position 0



Use a web browser to connect to the board and download the .flash image

Set the board SW2 to position 1 and reboot. (Position 1 is one click clockwise from horizontal)



Note the LCD will refresh.