1 AXBLUART – AN AXI UART DEVICE

AXBLUART is a simple UART peripheral with a standard AXI-MM-Lite-Slave interface. It is implemented as an AXI wrapper on top of the protocol-agnostic BLUART component. All of the AXI functionality is contained in the wrapper, while all of the UART functionality is contained in the underlying BLUART.

1.1 SPECIFICATIONS AND FEATURES

- AXI-Compliant MM-Lite-Slave interface occupying 4KB of address space
- RO and RW registers for AXI interface validation and debugging
- TX and RX FIFOs are each 16 Bytes deep; their occupancy may be read by the AXI interface
- Programmable Baud Rate setting, common to both TX and RX channels
- Power-On reset default of 115200 baud, 8 data bits, 1 stop bit, no parity
- Power-On reset diagnostic text string sent out TX port without software involvement

1.2 REGISTER MAP

The following table describes the registers accessible through the AXI-MM-Lite Slave interface of AXBLUART. The offset is in Bytes from the base of the 4 KB address space. POR State is the value of the register at Power On Reset.

ADDRESS OFFSET	NAME	ACCESS	POR STATE	FUNCTION
0x000	r0	RW	0	General Purpose RW Register R0
0x004	r4	RW	0	General Purpose RW Register R4
0x008	r8	RW	0	General Purpose RW Register R8
0x00C	rC	RW	0	General Purpose RW Register RC
0x010	const0	RO	0xDEADBEEF	Constant return value
0x014	const1	RO	0xBABECAFE	Constant return value
0x018	const2	RO	0xFOODFACE	Constant return value
0x01C	const3	RO	0xFEEDCODE	Constant return value
0x020	setClkDiv	WO	1085	Sets UART Baud Rate (see text for detail)
0x024	txLevel	RO	0	Number of bytes in UART TX FIFO
0x028	rxLevel	RO	0	Number of bytes in UART RX FIFO
0x02C	txCharPut	WO	-	Write to send ASCII Byte out UART TX FIFO
0x030	rxCharGet	RO	-	Read to receive ASCII Byte from UART RX FIFO
0x034	bluartCtl	RW	0	BLUART control (reserved use)
0x038-FFC	*reserved*	-	-	-

Notes: All accesses are of type UInt32_t, little-endian DWORDs, unless noted otherwise.

The correct setting of the baud rate clock divider is determined by dividing the AXBLUART module's AXI clock, typically 125 MHz, by the desired baud rate. The result is written to this register. The POR value of 1085 = 125E6/115200.

The txCharPut and rxCharGet registers have write and read side effects as they enqueue and dequeue their respective FIFOs. As such, the AXI bus should not attempt to write txCharPut when txLevel is non-zero; nor should the AXI bus attempt to read rxCharGet when the rxLevel is zero.