RPL Time Service

Shepard Siegel
Atomic Rules LLC

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What RPL Time Service Provides

- Absolute Time in "Seconds, not samples"
 Pure, continuous, binary time, Independent of any clock domain, available consistently in every clock domain
- Application-Specific Range and Precision
 m-Integer bits of Seconds : n-Fractional bits of Seconds
- Precision Synchronization Discipline
 Time Servo Loops drive measured phase-errors to zero
- A simple, standard way of accessing time
 OCP-IP Worker Interface Profile: Worker Time Interface

Seconds, not samples

• Time, purposefully divorced from signal sample rates

- At any point in space, "now" is absolute
 - Relativity of simultaneity
 - Practical need to know "now" in any clock domain

Representation of Time

- Fixed-Point binary m-bits integer, n-bits fraction
- Application specifies range and precision
- Infrastructure provides required resources

Example: timeSeconds[32.32]

Bit[63] of the 64b timeSeconds field is equal to 2³¹ seconds (~68 years)

Bit[32] of the 64b timeSeconds field is equal to 20 seconds (one second)

Bit[31] of the 64b timeSeconds field is equal to 2⁻¹ seconds (one half second)

Bit[00] of the 64b timeSeconds field is equal to 2⁻³² seconds (~232 picoseconds)

WIP:: Worker Time Interface (WTI)

- Allows any worker to easily observe "now"
- Worker chooses which clock domain they wish to observe time in
- Worker chooses how much range and precision (SecondsWidth.FractionWidth)
- Infrastructure provides Time "now"
- Also, provides associated quality of time
 - Unknown, Tracking, Locked

Quality Of Time

- "Unknown" The time is unknown
 - At reset, and until the time is explicitly set
- "Tracking" The time is known, loop settling
 - The time servo loop is attempting frequency-lock
 - Accuracy of time is only as good as using the uncompensated local worker clock since last set
 - When locked criteria achieved, transition to Locked
- "Locked" The time is known, loop locked
 - The time servo loop has stabilized
 - Accuracy as good as it will get
 - Loss of sync, or explicit time set outside window, transition to Tracking

Spec Sheet - Tracking

 Worst-Case, single-sample, error while Tracking is bound by the sum of Time Quantization Error and Worker Clock Drift

Time Quantization Error
$$\leq \frac{2}{Fwrkclk}$$

Wrkclk Drift
$$\leq \left(\frac{Fwrkclk}{Fsync}\right) \left(\frac{PPMwrkclk}{Fwrkclk \times 1E6}\right)$$

Wrkclk Drift
$$\leq \left(\frac{PPMwrkclk}{Fsync \times 1E6}\right)$$

Spec Sheet - Locked

 Worst-Case, single-sample, error while Locked is bound by the sum of Time Quantization Error and Worker Clock Short Term (per Fsync interval) Drift

Time Quantization Error
$$\leq \frac{2}{Fwrkclk}$$

Wrkclk ST Drift
$$\leq \left(\frac{PPMwrkclkST}{Fsync \times 1E6}\right)$$

Spec Sheet: Example 1

Consider Fwrkclk=250 MHz; Fsync=1 Hz; PPMwrkclk=200; PPMwrkclkST=1;

Time Quantization Error: <=8nS Time Quantization Error $\leq \frac{2}{Fwrkclk}$ Wrkclk Drift: <=200 uS Wrkclk Drift: $\leq \left(\frac{PPMwrkclk}{Fsync \times 1E6}\right)$ Wrkclk ST Drift: $\leq \left(\frac{PPMwrkclkST}{Fsync \times 1E6}\right)$

- Tracking: Time accurate to +/- 200. uS 200uS swamps 8ns by ~25,000:1 ratio
- Locked: Time accurate to +/- 1.008 uS
 1uS bests 8 nS by ~125:1 ratio

Precision Synchronization

- RPL Time Service may be implemented with one or more Time Servo Loops (TSL)
- Each TSL contains a phase-accumulator state variable that integrates a particular clock over time $\varphi(t) = \int \omega(t)$

 With sufficient precision, the phase-accumulator may function as a time-accumulator, converting angular-frequency to time

TSL Phase Detector (1/2)

- Each TSL contains a phase-detector that measures the difference between a TSL's current state and an input time signal. That signal can be implicit or explicit about time:
 - A periodic event, with *implicit* phase
 e.g. 1PPS GPS Sync Pulse, 10 MHz Freq, TCXO
 - A (possibly) aperiodic event with explicit phase
 e.g. Time message from grandmaster, master, or another TSL
- At least one explicit time message is required to bring a TSL to a known phase-time
 - Until then, only its 1st derivative, frequency, is known

TSL Phase Detector (2/2)

- The TSL phase-detector measures "Big Phase"
 - Linear over all time (Compared with PLL 2π)
 - Allows infinite capture window (w/explicit phase)
 - All digital down to $\frac{1}{Fwrkclk}$ (2ns for 500 MHz TSL)
 - Sufficient to asymptotically approach F-lock

- Time-to-Digital phase augmentation
 - Adds 5~6 bits of monotonic, sub-sample phase
 - Achieves ~80 pS resolution per sub-sample LSB
 - Analog measurement on FPGA substrate

TSL P/PI Digital Servo

- The Proportional (P) component of the servo provides a non-linear response when the absolute value of the error exceeds a set threshold
- The Proportional-Integral (PI) component of the servo is 1-pole, adjustable- α IIR loop-filter
- The resultant feedback provides a signed bias to the fractional $2\pi/\omega$ phase-increment

TSL Summary

- Exposes time in the worker clock domain
- Improves the accuracy of time provided by an uncompensated local worker clock by several orders-of-magnitude

"Short-term stability provided over the long term"

 When needed for added accuracy, sub-sample phase detector provides meaningful linear compensation data