OpenCPI FPGA Boards at Atomic Rules

ID	Board Vendor	Board Model	Build Code	FPGA	PCIe	FTop	Status
101	Xilinx	ML555	"ml555"	V5-LX50T	Gen1 x8	FTopV5	B,H(3),R,$W_{12.3}$
102	Abekas	Alder	"alder"	V5-LX50T	Gen1 x8	FTopV5	B,H(1), $W_{12.3}$
103	Generic	Generic	"sx95t"	V5-SX95T	Gen1 x8	FTopV5_a	B,P(1),R, $W_{12.3}$
104	Xilinx	XUPV5	"xupv5"	V5-LX110T	Gen1 x1	FTopV5_g	B,H(2),R, $W_{12.3}$
105	Generic	Generic	"fx130"	V5-FX130T	Gen1 x8	FTopV5	U1
106.1	HiTechGlobal	Net10G	"tx240"	V5-TX240T	Gen1 x8	FTopV5	B, $W_{12.3}$
106.2	HiTechGlobal	Net10G	"nf10"	V5-TX240T	Gen1 x8	FTopV5	B, $W_{12.3}$
107	Generic	Generic	"lx330"	V5-LX330T	Gen1 x8	FTopV5	B,P(0), $W_{12.3}$
108	Xilinx	ML605	"ml605"	V6-LX240T	Gen2 x4	FTopV6	B,H(1),R, $W_{12.3}$
109	Xilinx	SP605	"sp605"	S6-LX45T	Gen1 x1	FTopS6	B,H(1)
110	HiTechGlobal	S4GX-230	"s4gx"	4SGX-230	Gen2 x8	FTopSGX	U2
111	Altera	4CGX15N	"c4gx"	4CGX-12	Gen1 x1	FTopCGX	H(1)

Status Codes:

B = In OpenCPI build

H = Hardware in Use (number of boards located at AR-Auburn)

P = Proprietary Hardware (number of boards located at AR-Auburn)

R = In Test Regressions

U1 = Under Consideration; U2 = Planning Phase

W = Known Working (ISE or Quartus Tool Version)

Development/Target Machines for PCIe at Atomic Rules

Machine Name	OS	Chipset	GPU	DRAM (GB)
core960	RHEL5.3 WS 64b	X58	GTX285	12
core920	RHEL5.3 WS 64b	X58	GTX280	12
amd790 [1]	RHEL5.3 WS 64b	790FX	8800GT	4
Q9550	XP-SP3 32b	X48	GTX280	4
XP8500	XP-SP3 32b	X48	8800GT	4

Note Codes:

[1] = On loan to OpenCPI development partner in Exeter, NH

Updated: 2010-11-08