

FT62F21X

Application note

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FT62F21x IO 应用

1 IO 相关寄存器的设置

本芯片共包含 6 个 GPIO。这些 IO 除了作为普通输入/输出端口以外还通常具备一些与内核周边电路通讯的功能。PORTA 是一个 6 位双向端口。与其相应的进出方向寄存器就是 TRISA 寄存器。

相关寄存器的各个位定义如下：

1) PORTA 寄存器

Bit	7	6	5	4	3	2	1	0
Name	-	-	PA5	PA4	PA3	PA2	PA1	PA0
Reset	-	-	x	x	x	x	x	x

Bit7~Bit6: -

Bit5: PORTA5 数据

Bit4: PORTA4 数据

Bit3: PORTA3 数据

Bit2: PORTA2 数据

Bit1: PORTA1 数据

Bit0: PORTA0 数据

2) TRISA 寄存器

Bit	7	6	5	4	3	2	1	0
Name	-	-	TRISA[5]	TRISA[4]	TRISA[3]	TRISA[2]	TRISA[1]	TRISA[0]
Reset	-	-	1	1	1	1	1	1

Bit7~ Bit6: N/A,读 0

Bit5~ Bit0: PORTA<5:0>输入/输出状态控制寄存器

1: 端口为输入状态

0: 端口为输出状态

3) WPUA 寄存器

Bit	7	6	5	4	3	2	1	0
Name	-	-	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
Reset	-	-	1	1	-	1	1	1

Bit7~Bit6、Bit3: N/A,读 0

Bit5~Bit0: Port A 弱上拉使能

1: 使能PORTA 端口弱上拉

0: 关闭PORTA 端口弱上拉

4) OPTION 寄存器

Bit	7	6	5	4	3	2	1	0
Name	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
Reset	1	1	1	1	1	1	1	1

Bit7: PORTA 口上拉使能位

1: 上拉功能被禁止

0: 上拉功能使能

Bit6: 触发中断边沿选择位

1: PA2/INT 上升沿触发中断

0: PA2/INT 下降沿触发中断

Bit5: Timer0 时钟选择位

1: PA2/T0CKI管脚输入时钟

0: 内部指令周期Fosc/4

Bit4: Timer0 时钟边沿选择位

1: PA2/T0CKI管脚由高到底变化时计数增加

0: PA2/T0CKI管脚由低到高变化时计数增加

Bit3: 预分频分配位

1: 预分频器分配给WDT

0: 预分频器分配给Timer0

Bit2~Bit0 预分频大小设置位

Bit2: Bit0	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

2 应用范例

//*****

/* 文件名: Test_62F21X_io.c

* 功能: FT62F21X-IO 功能演示

* IC: FT62F21X SOP8

* 晶振: 16M/4T

* 说明: 当 DemoPortIn 悬空或者高电平时,

* DemoPortOut 输出 50Hz 占空比 50%的波形

* 当 DemoPortIn 接地时,DemoPortOut 输出高电平

* Memory: Flash 1KX14b, EEPROM 128X8b, SRAM 64X8b

* FT62F21X SOP8

*

* DemoPortOut -----|1(PA4) (PA3)8 |-----NC

* NC-----|2(TKCAP) (PA0)7 |-----NC

* NC-----|3(VDD) (PA1)6 |-----NC

* NC-----|4(VSS) (PA2)5 |-----DemoPortIn

*

*/

```

//=====
#include <FT62F21X.INC>;
;=====
;RAM DEFINE
TEMP            EQU      0X40
TEMP1           EQU      0X41
TEMP2           EQU      0X42
W_TMP           EQU      0X4C
S_TMP           EQU      0X4D
;=====
;CONSTANT DEFINE
;=====
INTCON_DEF      EQU      B'00000000'    ;GIE, TMR0IE,
OPTION_DEF      EQU      B'00000000'    ;PORTA pull-ups are enable;Timer0 1:2
OSCCON_DEF      EQU      B'01110000'    ;16MHz INTERNAL OSC
WPUA_DEF        EQU      B'00000100'    ;开启 PA2 上拉功能
TRISA_DEF       EQU      B'00000100'    ;PA4-OUT    PA2-IN

LSB              EQU      0
MSB              EQU      7
;=====
;USER DEFINE
;=====
#define DemoPortOut  PORTA,4
#define DemoPortIn   PORTA,2
;=====
        ORG          0x0000
        LJUMP        RESTART
        ORG          0x0004
        STR          W_TMP
        SWAPR        STATUS,W
        STR          S_TMP
        BCR          STATUS,RP0

INT_RET:
        SWAPR        S_TMP,0
        STR          STATUS
        SWAPR        W_TMP,1
        SWAPR        W_TMP,0
        RETI
;=====
;SYSTEM START
;=====
RESTART:

```

```

    BANKSEL    PORTA
    LCALL      INITIAL
    BCR STATUS, 5    ;->BANK0
MAIN_LOOP:
    BSR        DemoPortOut    ;将寄存器的某位置 1
    LCALL      DELAY_10MS
    BTSS       DemoPortIn     ;若为 1，则跳过
    LJUMP      MAIN_LOOP
    BCR        DemoPortOut
    LCALL      DELAY_10MS
    LJUMP      MAIN_LOOP

```

```

;=====
;SYSTEM INITIAL
;=====

```

```

INITIAL:
    BANKSEL    PORTA    ;
    LDWI       0X00      ;立即数存到 W
    STR        PORTA     ;将 W 存到 PORTA
    BANKSEL    TRISA
    LDWI       TRISA_DEF ;PA5-OUT
    STR        TRISA     ;SET IO Direction
    LDWI       WPUA_DEF
    STR        WPUA
    LDWI       OPTION_DEF
    STR        OPTION_REG ;SET OPTION
    LDWI       OSCCON_DEF
    STR        OSCCON    ;SET OSCCON
    BANKSEL    PORTA
    LDWI       INTCON_DEF
    STR        INTCON

```

```

CLEAR_RAM:

```

```

    LDWI       40H
    STR        FSR

```

```

CLEAR_RAM_LOOP:

```

```

    CLRR       INDF
    INCR       FSR,F
    LDWI       80H
    XORWR      FSR,W
    BTSS       STATUS,Z
    LJUMP      CLEAR_RAM_LOOP
    RET

```

```

;=====

```

```
;DELAY_10MS 16MHZ/4T
```

```
;
```

```
DELAY_10MS:
```

```
    LDWI      H'28'
```

```
    STR       TEMP1
```

```
    LDWI      H'0F'
```

```
    STR       TEMP2
```

```
DELAY_10MSLOOP3:
```

```
    CLRWDT
```

```
    DECRSZ    TEMP2,F    ;TEMP2-1 ->F结果为 0 则跳过下一条语句
```

```
    LJUMP     DELAY_10MSLOOP3
```

```
    DECRSZ    TEMP1,F
```

```
    LJUMP     DELAY_10MSLOOP3
```

```
    RET
```

```
END
```

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