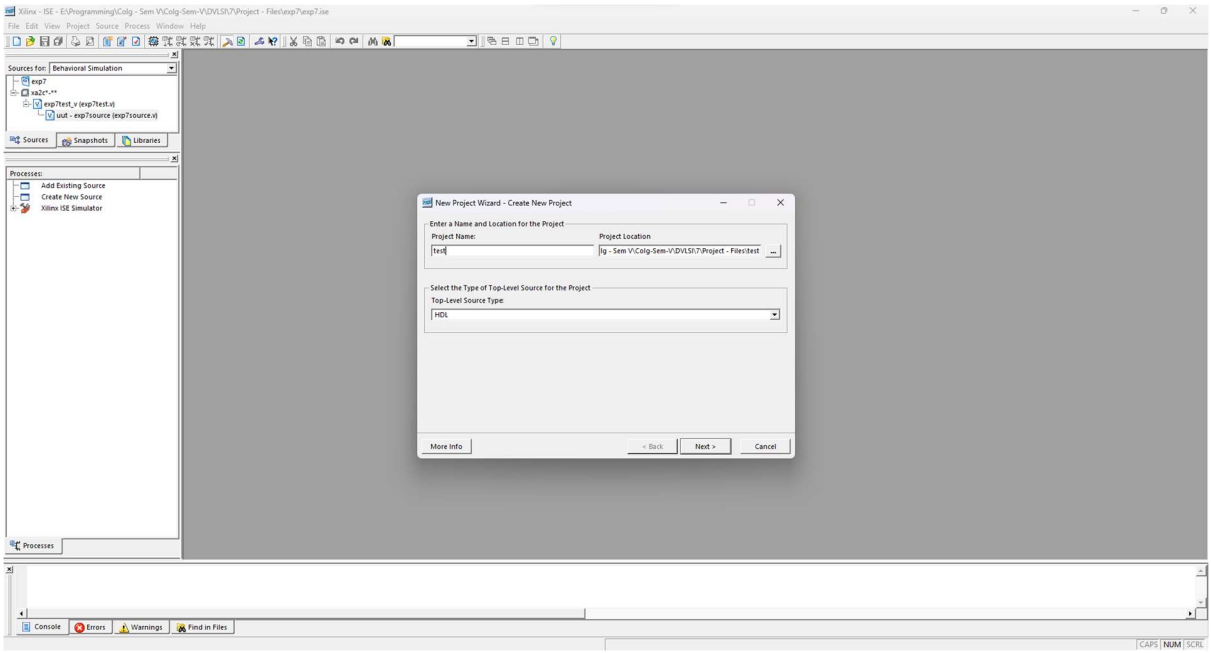
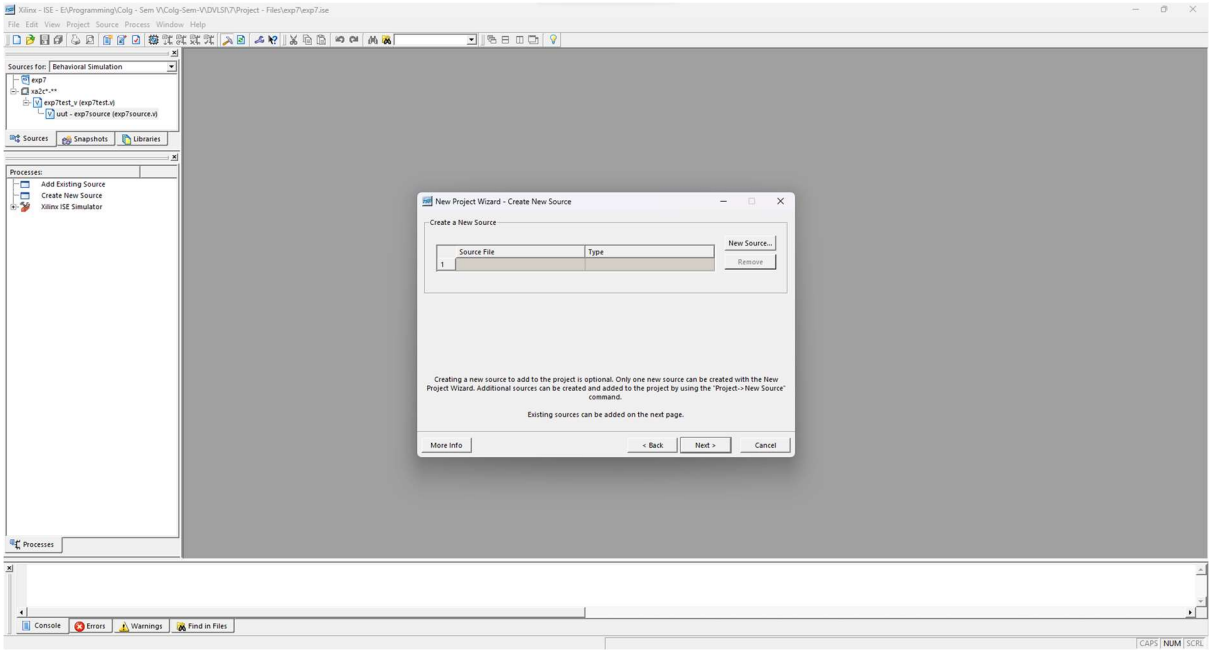
Follow visual steps if necessary: -

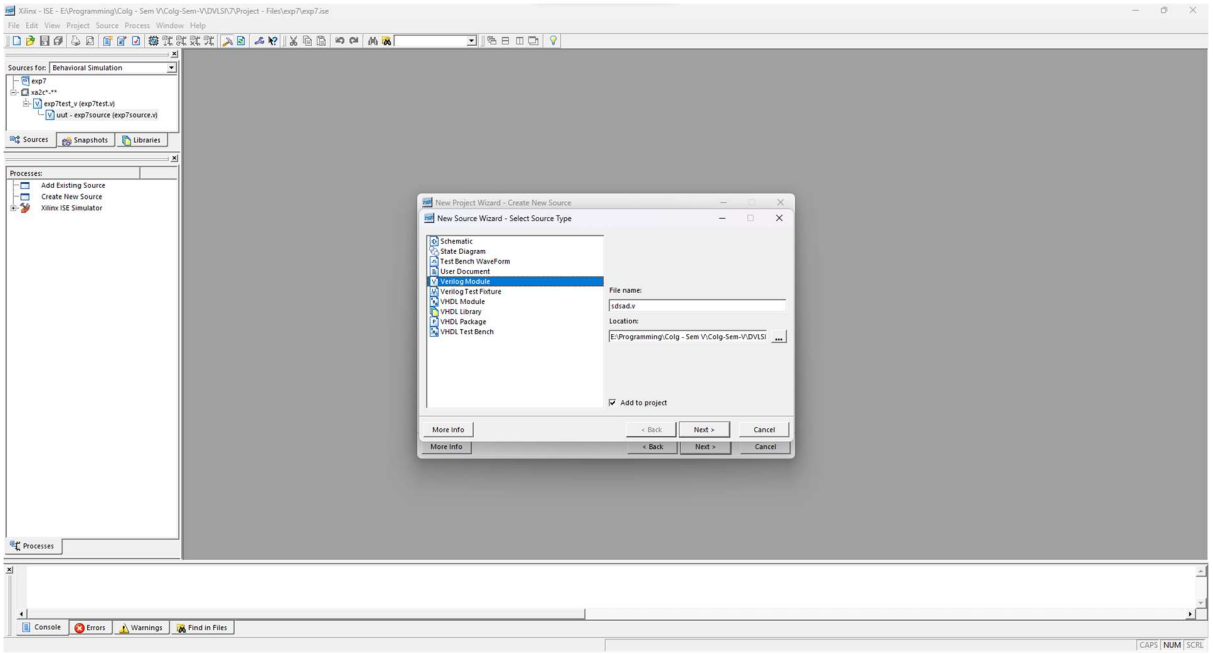
1. Create new project



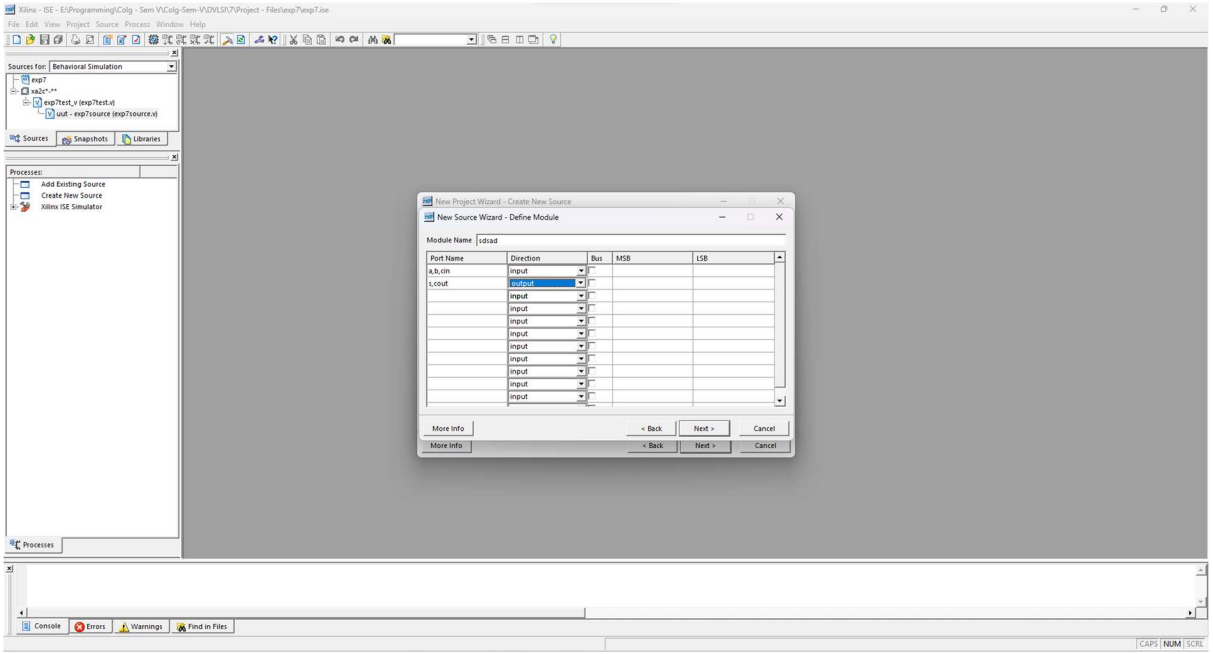
2. Click next then new source



3. Select verilog module (dont include same name as project and any special characters)



4. In first tab, put a, b, cin. For second tab, put s, cout and select output on direction tab.

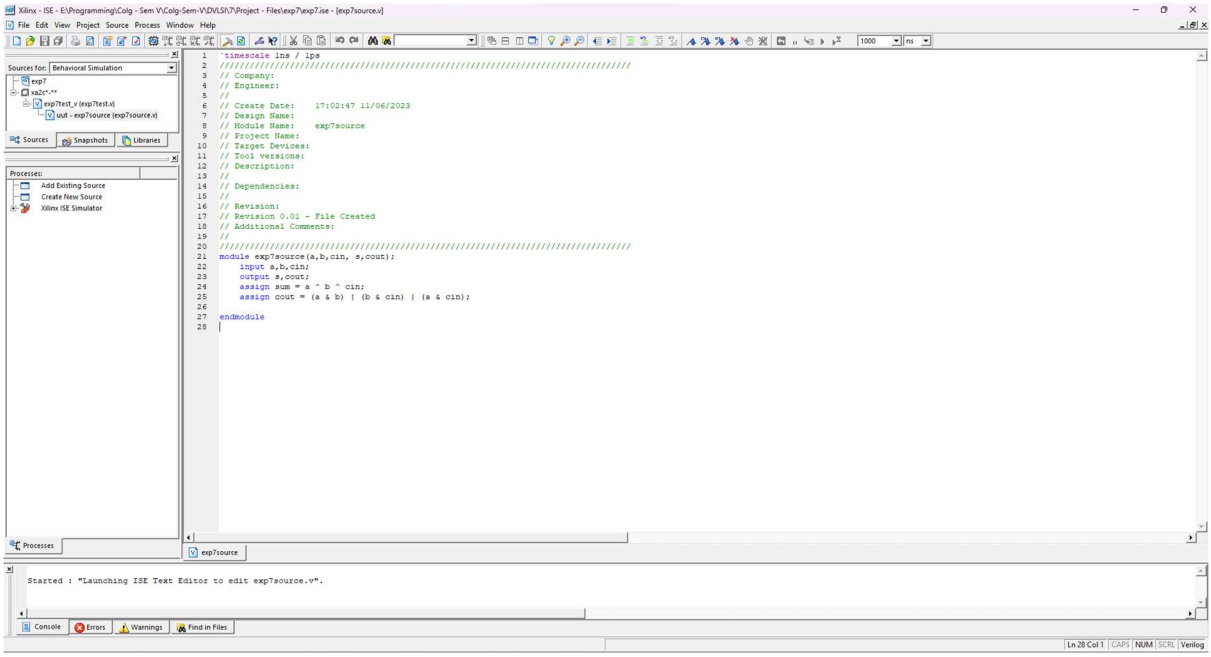


5. Next, Finish on both windows

6. In source file opened automatically copy paste the following (don't replace everything!)

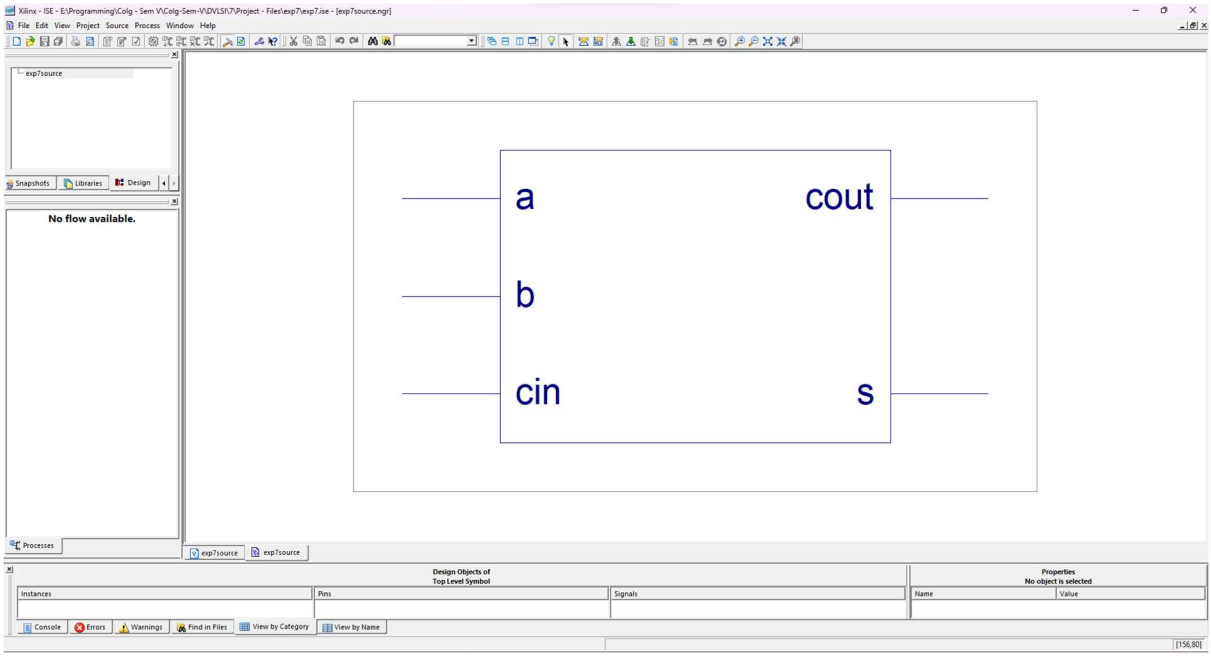
```
module verilo(a,b,cin, s,cout);
    input a,b,cin;
    output s,cout;
        assign s = a * b * cin;
        assign cout = (a&b)|(b&cin)|(a&cin);

endmodule
```



7. Next save the file and expand implement design on left most window. Double click Synthesize - XST (make sure no errrors)

8. Expand Synthesize column then click view RTL Schematic and make sure it matches with the image



9. Create new source, select verilog test fixture and name something different.

10. Copy paste the following part of code

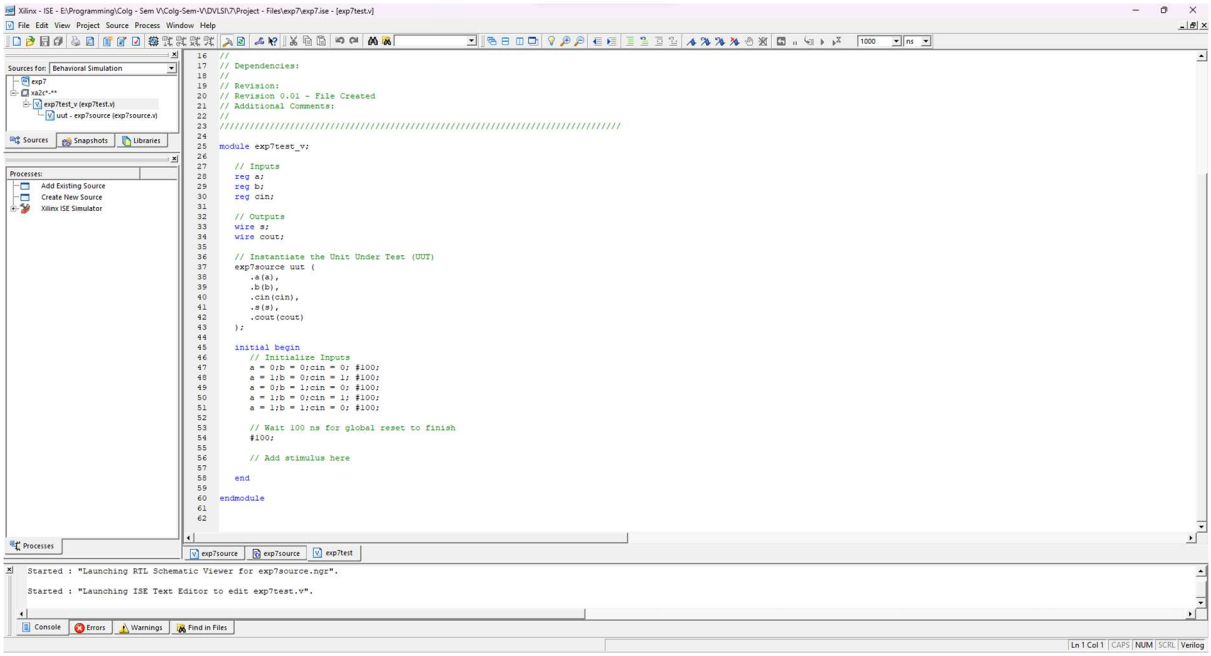
```
initial begin
        // Initialize Inputs
        a = 0;b = 0;cin = 0; #100;
        a = 1;b = 0;cin = 1; #100;
        a = 0;b = 1;cin = 0; #100;
        a = 1;b = 0;cin = 1; #100;
        a = 1;b = 1;cin = 0; #100;

        // Wait 100 ns for global reset to finish
```

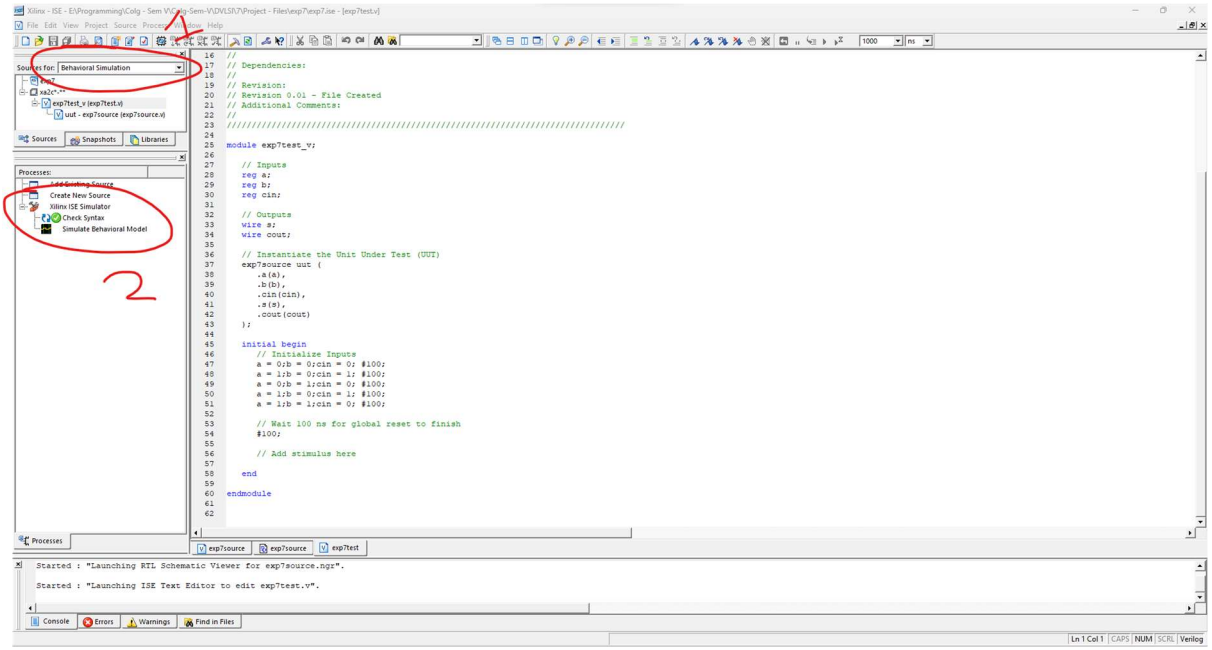
#100;

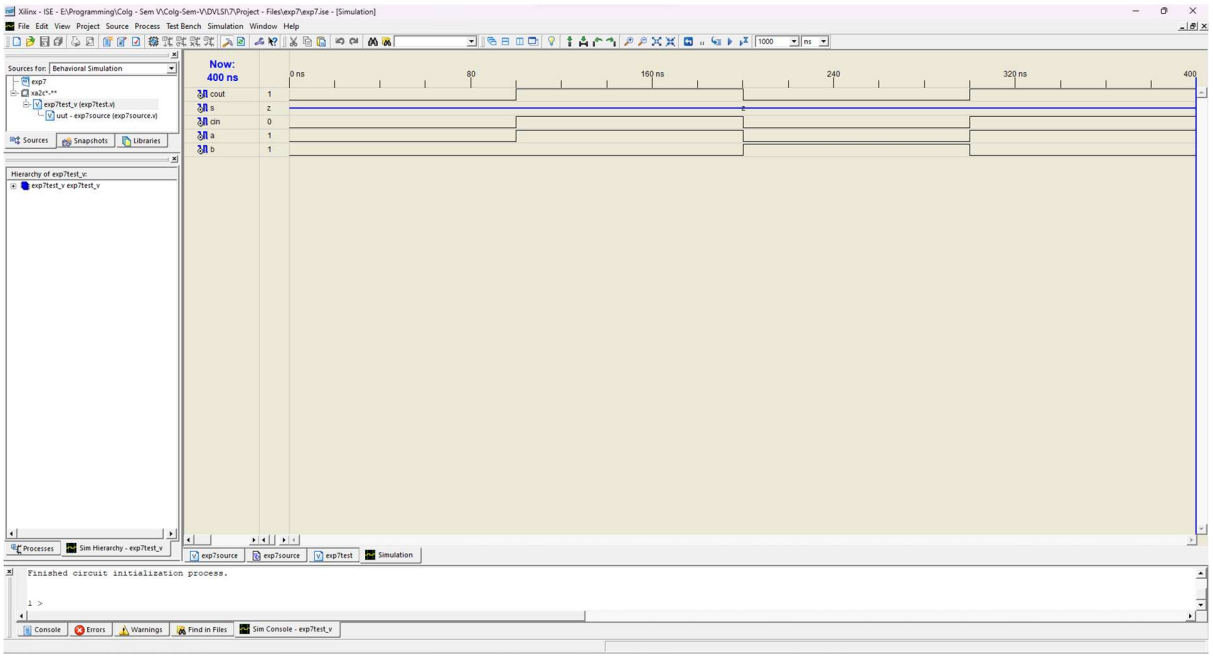
// Add stimulus here

end



11. Next on top left in sources for: select behavioral simulation. Below expand Simulator tab, check syntax, simulate behavioural model


Sources for: Behavioral Simulation
exp7test_v (exp7test.v)
uut - exp7source (exp7source.v)
Sources
Snapshots
Libraries
Processes:
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
2
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module exp7test_v;
// Inputs
reg a;
reg b;
reg cin;
// Outputs
wire s;
wire cout;
// Instantiate the Unit Under Test (UUT)
exp7source uut (
.a(a),
.b(b),
.cin(cin),
.s(s),
.cout(cout)
);
initial begin
// Initialize Inputs
a = 0;b = 0;cin = 0; #100;
a = 1;b = 0;cin = 1; #100;
a = 0;b = 1;cin = 0; #100;
a = 1;b = 0;cin = 1; #100;
a = 0;b = 1;cin = 0; #100;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here
end
endmodule
exp7source
exp7source
exp7test
Started : "Launching RTL Schematic Viewer for exp7source.ngr".
Started : "Launching ISE Text Editor to edit exp7test.v".
Console
Errors
Warnings
Find in Files
Ln 1 Col 1
CAPS
NUM
SCRL
Verilog


Now:
400 ns
0 ns
80
160 ns
240
320 ns
400
cout
s
cin
a
b
Hierarchy of exp7test_v:
exp7test_v exp7test_v
Processes
Sim Hierarchy - exp7test_v
exp7source
exp7source
exp7test
Simulation
Finished circuit initialization process.
Console
Errors
Warnings
Find in Files
Sim Console - exp7test_v