

CHAPTER 2

Materials and Technology¹

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2.1. Properties of single crystalline silicon

Single crystalline silicon has a number of remarkable mechanical properties. Being a semiconductor the chemical binding between the Si-atoms are covalent. Covalent binding potentials are strongly anisotropic, and they have a deep minimum. This is very much in contrast to metal binding potentials, and consequently, crystal dislocations are much more movable in metals than in semiconductor materials. One says that metals are ductile, and semiconductors are brittle.

Mechanical engineers often try to avoid the use of brittle material such as glass from very obvious reasons. But ductile materials are easily plastically deformed, meaning that these materials are subject to mechanical hysteresis.

Single crystalline silicon can be made perfectly - virtually without any defects. Being loaded, there are no dislocation lines that are able to move, and the introduction of a new dislocation line would immediately cause a crack into the material - silicon would break. At room temperature, single crystalline silicon can only be elastically deformed, there is no mechanical hysteresis.

This would not be so special if the yieldstrength of silicon would not be extremely high - it is of comparable strength as stainless steel. Thus silicon is a material of strength comparable to steel, but without any plastic deformability, no mechanical hysteresis. That fact makes silicon a material superior to any metal in many applications. In fig. 2.1.1. we show schematically stress-strain curves of steel and silicon.

¹ Based on: M. Elwenspoek, Lecture notes for the course Micromechanics, University if Twente, Enschede, the Netherlands.

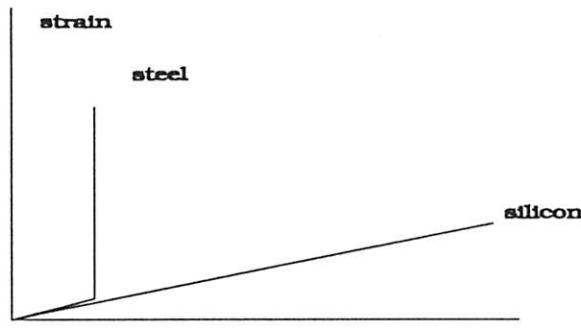


Fig. 2.1.1. Typical stress strain curves of metals and semiconductors

The elastic deformability is most impressive in microstructures. Fig. 2.1.2. shows a scanning electron microphotograph (SEM) of an etched silicon beam heavily loaded by a stylus inside a SEM [1]. If the load is released, the beam would return to its original shape.

In table 2.1.1. (from ref. [2]) we give a few figures of single crystalline silicon in comparison to other materials.



Fig. 2.1.2. (SEM) photograph of an etched silicon beam heavily loaded by a stylus force [1]

	Yield Strength (10^{10} dyne/cm 2)	Knoop Hardness (kg/mm 2)	Young's Modulus (10^{12} dyne/cm 2)	Density (gr/cm 3)	Thermal Conductivity (W/cm 2 °C)	Thermal Expansion ($10^{-6}/^\circ$ C)
*Diamond	53	7000	10.35	3.5	20	1.0
*SiC	21	2480	7.0	3.2	3.5	3.3
*TiC	20	2470	4.97	4.9	3.3	6.4
*Al ₂ O ₃	15.4	2100	5.3	4.0	0.5	5.4
*Si ₃ N ₄	14	3486	3.85	3.1	0.19	0.8
*Iron	12.6	400	1.96	7.8	0.803	12
SiO ₂ (fibers)	8.4	820	0.73	2.5	0.014	0.55
*Si	7.0	850	1.9	2.3	1.57	2.33
Steel (max. strength)	4.2	1500	2.1	7.9	0.97	12
W	4.0	485	4.1	19.3	1.78	4.5
Stainless Steel	2.1	660	2.0	7.9	0.329	17.3
Mo	2.1	275	3.43	10.3	1.38	5.0
Al	0.17	130	0.70	2.7	2.36	25

Table 2.1.1.

Similar properties has gallium arsenide (GaAs) [3], however the yield load is smaller by a factor of two in comparison to silicon. Still, this material is interesting enough for micromechanical applications.

Under certain conditions, we have to mention, plastic deformation of single crystalline silicon have been observed [4]. This observation, however has little practical impact on silicon micro mechanics.

According to Schweitz [1], polysilicon microstructures have similar mechanical properties (Young's modulus and yield strength) as single crystalline silicon. This is mainly due to the fact that dislocation lines in silicon are quite immobile at room temperature.

The crystal structure of silicon is of the diamond type with lattice constant $a = 5.43\text{\AA}$. The structure is like F.C.C. (face centred cubic) but with two atoms in the unit cell. Take an F.C.C. lattice, cornered at A, and put another atom at B a point 1/4 of the way along the main diagonal of the cube (fig.2.1.3.)

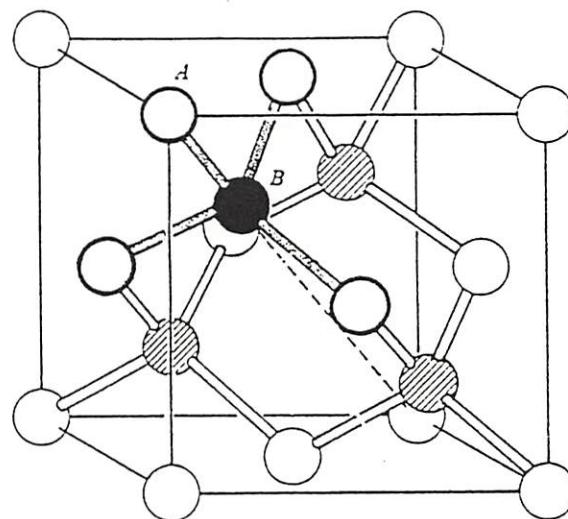


Fig.2.1.3. Unit cell of the diamond lattice (from [5])

Crystal planes are characterised by sets of three indices, the so-called Miller indices. They describe vectors normal to the crystal planes in question. E.g. in a simple cubic lattice, one finds atoms along the x,y and z-direction in a distance of an integer times the lattice constant a . The vectors \mathbf{a}_x and \mathbf{a}_y span a plane on which the vector \mathbf{a}_z is normal. This plane is referred to as (001). Similarly, the (011) direction is normal to the plane formed by the vectors \mathbf{a}_x and $(\mathbf{a}_y + \mathbf{a}_z)$. Finally, (111) is normal to the plane formed by the vectors $(\mathbf{a}_x + \mathbf{a}_z)$ and $(\mathbf{a}_y + \mathbf{a}_z)$. The Miller indices are the components of the unit cell vectors in the reciprocal lattice. We have enough with {100}, {110} and {111} for our purpose. {...} denotes a set of symmetrically equivalent planes, e.g. (100), (010) and (001) are all members of {100}. The (100), (110) and (111) planes are shown in fig. 2.1.4. More details can be found in standard textbooks on solid state physics (e.g. [5] and [6]).

Crystallographic directions are indicated by <...>.

Of great importance for anisotropic etching are the orientation of the relevant crystal planes with respect to particular directions. It is the (111)-plane which etches by far the slowest, and therefore one needs to know the angles the (111)-planes make with the wafer orientation if they are etched. For micromechanics, two wafer orientations are of importance: (100) and (110). (111) wafers cannot be micromachined using anisotropic etchants.

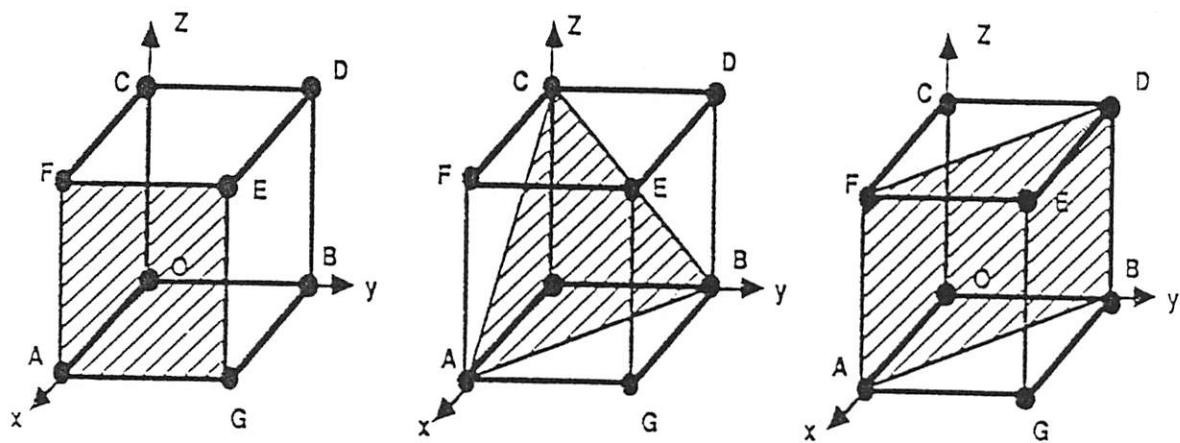


Fig. 2.1.4 The family of planes AFEG (100), ABC (111) and ABDF (110) in cubic lattices

2.2. Photolithography

In fig. 2.2.1.a we show a schematic of a mask for etching membranes of various size. The membranes have to be etched from the backside of the wafer as shown in fig. 2.2.1.b. Note the difference of the dimensions of the pattern on the mask and of the final result due to the inclined (111) faces.

We shall not describe here how such a mask can be generated. There are many mask generating systems on the market.

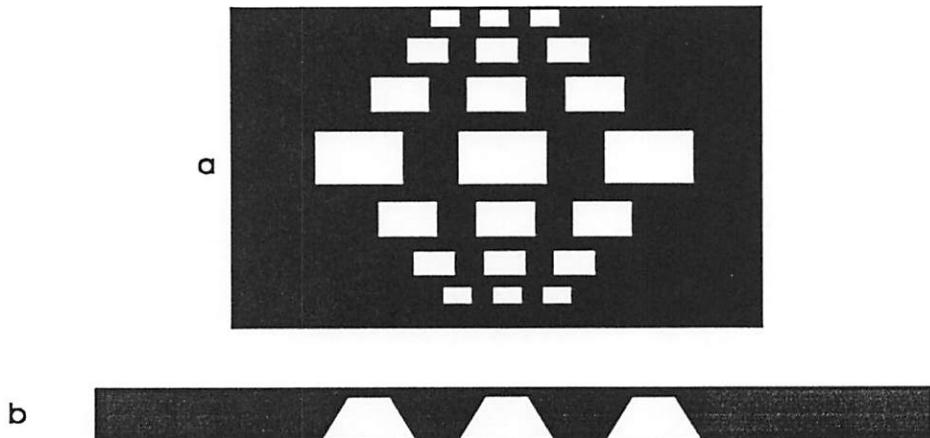


Fig. 2.2.1. (a) Mask for etching membranes. (b) lateral view of the etch result.

Let us assume that we want to etch the black regions as seen on the mask in fig. 2.2.1. in a (100) wafer. Let us start with a wafer we freshly got out of a box as delivered by the wafer manufacturer. We have to deposit a material that can serve as a mask for etching. The simplest way is to grow a thermal oxide in a tube oven. The growth rate of oxide is strongly dependent on the temperature. The rate controlling process seems to be the diffusion of oxide atoms or molecules through the growing layer of silicon dioxide.

The thickness of the oxide film required depends on a number of things. For the following etch step, one has to think of the etch rate of the oxide, which is not insignificant in KOH. This etch rate is typically such that a 300 µm wafer requires an oxide layer of 2 µm.

Next, one has to spin a photoresistive layer on the wafer. Some people prefer to use a primer first. Typically, one has to anneal the resist at 90 degree C for 10 minutes before spinning the other side of the wafer (if necessary) or before the illumination step. The annealing can be done on hot plates or in ovens. This step is usually called "prebake".

The next step is illumination of the resist. This very often requires alignment of the mask pattern with the flat of the wafer, or with patterns already existing on the wafer. Sometimes (in fact quite often) it is necessary to align the mask with patterns on the rear side of the wafer. This is rather convenient if one has a double sided maskaligner.

After illumination the wafers are developed, rinsed in water dry blown or dry spun, and annealed again, typically at 120 degree C, for 20 minutes. This process step is usually called "postbake". Higher temperature, or longer annealing time makes it difficult to remove the resist, and the resist tends to flow.

After post bake, the oxide can be stripped in an HF-solution. Also here the recipes are different; Some people use buffered HF ("BHF"), a mixture of 1 part 49% aqueous HF-solution and 7 parts of NH₄F. This solution does not attack silicon at all. High concentration aqueous solutions of HF, as used in other labs, seem to etch silicon slightly. The oxide stripping is done at room temperature, the etch rate of oxide in BHF is typically 6 µm/hour. Note that the resist does not like HF too much.

If the oxide stripping process has satisfactory results, the resist can be stripped now. This can be done in acetone (if the post bake was not too long or at a too high temperature), in fuming nitride acid or in an oxygen plasma.

Next, the wafer can be etched in an etchant, e.g. a potassium hydroxide (KOH) solution until the membranes have the desired thickness.

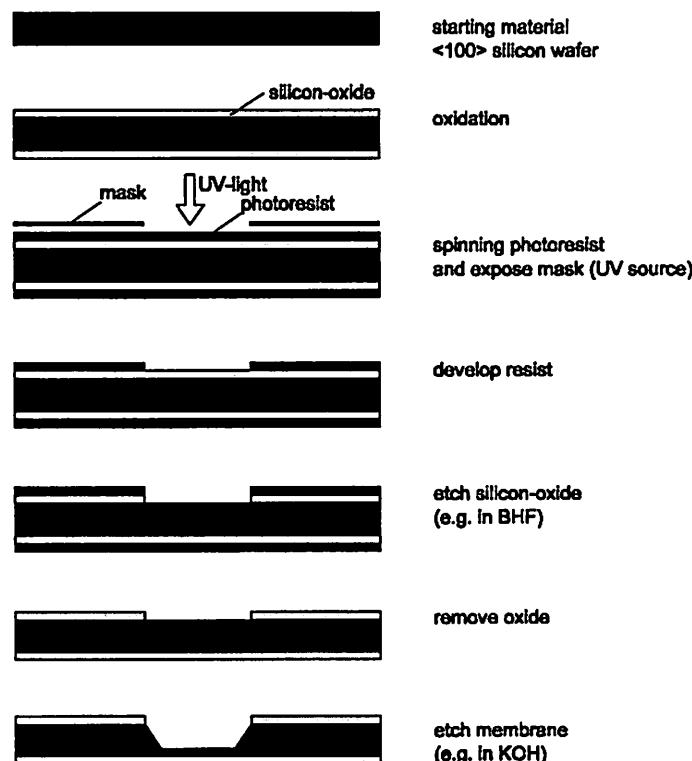


Fig. 2.2.2 Standard photolithography process

2.3. Etching of Si

2.3.1. Wet etching

The most recent and complete overview on the knowledge of anisotropic etching can be found in the paper of Seidel et al. [8].

There is a number of wet etchants that etch silicon anisotropic. The most important are alkali-hydroxides such as KOH and a mixture called EDP (ethylenediamine, pyrocatechol and water).

For the other etchants we refer to the literature:

- NaOH [8,9]
- CsOH [10]
- NH₄OH [11,12]
- Hydrazine [13]
- TMAH (tetramethyl ammonium Hydroxide, (CH₃)₄NOH) [14]

We shall concentrate on KOH since this is the most commonly used etchant. Hydrazine is extremely toxic, and its vapour is explosive, therefore it is avoided as far as possible. KOH has the disadvantage of being incompatible with IC-processes due to the potassium ions. EDP again is toxic, but to a lesser extend than hydrazine.

TMAH is non toxic and IC-compatible but there exist much fewer studies on this system than on e.g. KOH or EDP.

Except at very high concentration of KOH, the etched (100)-plane becomes rougher the longer one etches. This is thought to be due to the development of hydrogen bubbles, that hinder the transport of fresh solution to the silicon surface [15].

In the final choice of the etchant, a number of issues have to be considered, such as: ease of handling, toxicity, etch rate, topology of the etchground, IC-compatibility, etch stop, etch selectivity of other materials, mask material and thickness of the mask. The last three items will be treated in chapters II.5. and II.6.

KOH is the most common used etchant. It is much less dangerous as other etchants, easy to handle, readily available, and it etches fast. Note that KOH is fatal to the eyes. The greatest disadvantages are that KOH is IC-incompatible and that the selectivity to oxide is rather poor.

As compared with EDP, it has disadvantages regarding selectivity to oxide - EDP etches oxide slower than KOH by a factor of 100, practically, it doesn't attack oxide at all. Also the etch rate slows down at higher B⁺ - concentrations as compared with EDP.

In Fig. 2.3.1 we show lateral underetch rates as a function of orientation on <100>- and <110> wafers. For the experimental technique we refer to [8]. Note the deep minimum at the {111}-planes. Typical etch rates far away from the {111}-planes are of the order of 1 μm per minute. That means that etching through wafers is a time consuming process: To etch through a 300 μm thick wafer one needs five hours.

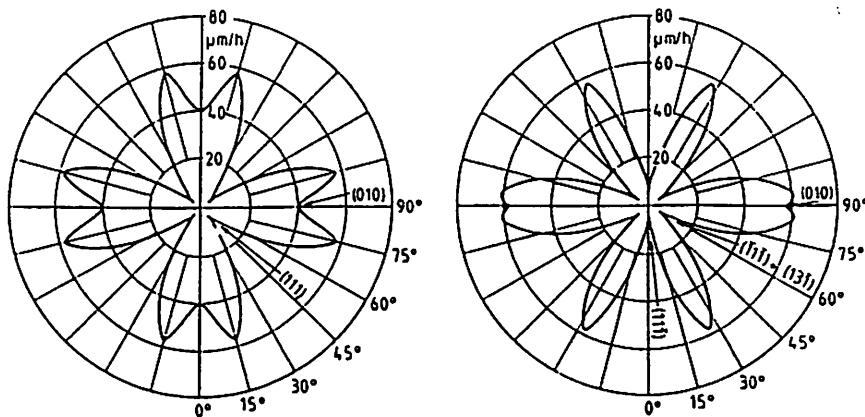


Fig. 2.3.1. Lateral underetch rates as a function of orientation. 50% KOH Solution, 78 degree C. a: <100>, b: <110> silicon wafers (from Seidel et al [8])

This fact illustrates that it is quite critical to etch thin structures without a mechanism that serves for a drastic slow down of the etch rate at a well defined etch depth. Often structures of a thickness of 10 - 20 μm are needed (this is the minimum thickness one can achieve without an etch stop mechanism), thus etching must be stopped after appr. 6 hours, 10 - 20 minutes before the structure one tries to obtain by etching, disappears.

In fig. 2.3.2. we show an Arrhenius plot of the etch rate in the <100> - and <110> direction using KOH. It is seen that the temperature dependence of the etch rate is quite large, and only slightly dependent on the orientation shown here. Included in this figure are etch rates with isopropyl alcohol added. It is seen that the activation energy is essentially unchanged, but the overall etch rate is reduced by adding isopropyl alcohol.

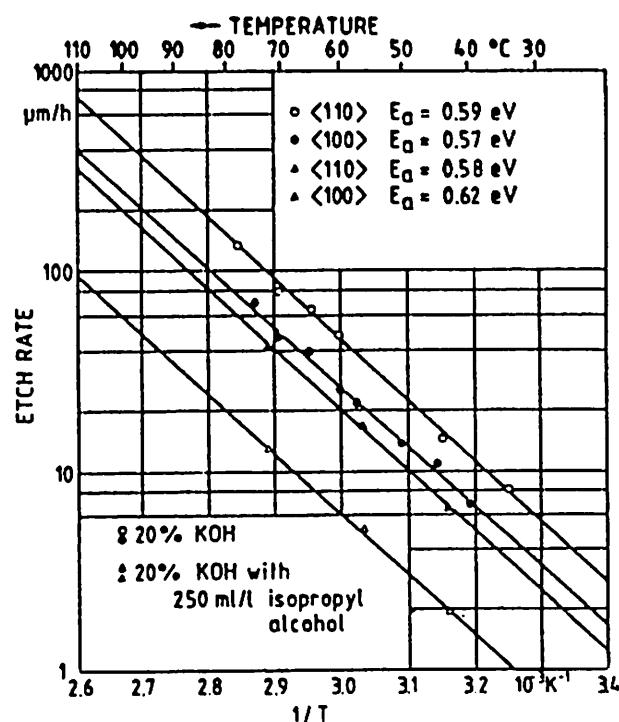


Fig. 2.3.2. Temperature dependence of Etch rates in 20% KOH solutions in <100> and <110> directions, with and without the addition of isopropyl alcohol (from Seidel et al. [8])

2.3.2. Dry etching

Dry etching technology has become a key part of integrated circuit manufacturing and is now indispensable in micromechanics. It uses gases to etch metals, dielectrics, and semiconductors whereas the alternative process, wet etching, uses liquids. The reasons for the prevalence of dry etching and its increasing importance in all stages of manufacture include lower chemical costs, less environmental impact, and ease of production-line automation.

The anisotropy, which can be obtained by dry etching methods, is not a result of the anisotropy of single crystals such as in anisotropic wet chemical etching. "Anisotropy" within the context of dry etching refers to the degree of under-etching the mask.

Wet chemical etching of a solid has the big advantage of being very selective and fast, but has usually no preferential direction, i.e., etching proceeds at the same rate in all directions. This leads to isotropic circular profiles, which undercut a mask and limit the density of circuit elements on a chip (fig. 2.3.3).

However in single-crystalline materials such as Si, it is possible to make use of the difference in wet chemical etch rates along different crystallographic directions and obtain highly anisotropic structures with high aspect ratios (height to width of lines) [2]. Dry etching on the other hand can result in anisotropic etch profiles in single crystalline as well as in poly crystalline or amorphous materials. In addition, under-etching (etch profile) can be controlled by varying the plasma chemistry (fig. 2.3.4(c)). Furthermore dry etching has the advantage over wet chemical etching that the adherence of the masking film to the substrate surface is not as critical as in wet chemical etching. Because of the acidic environments of most etchant solutions, photoresist can lose adhesion thereby altering patterning dimensions and preventing linewidth control.

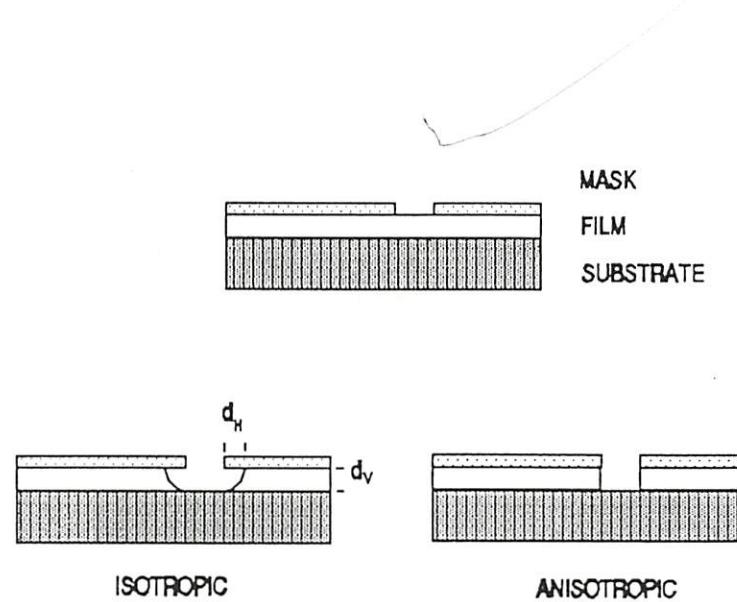
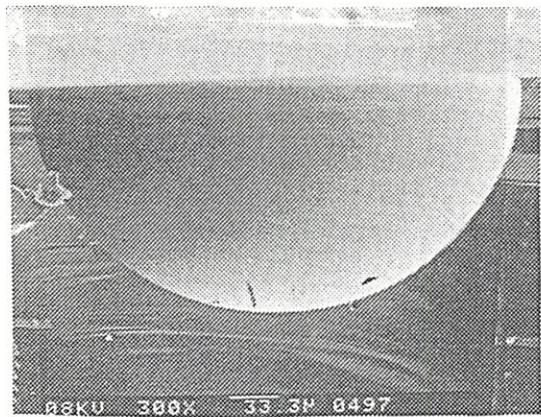
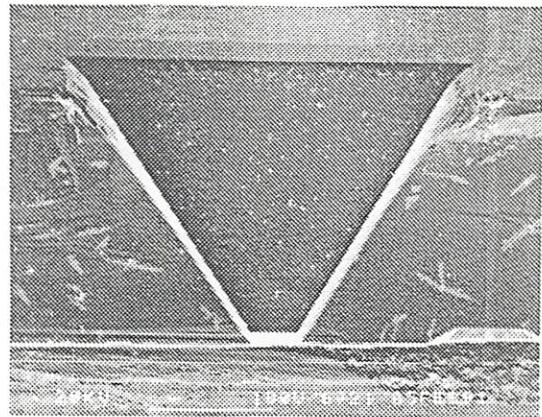


Fig. 2.3.3 Cross-section of an isotropic profile and anisotropic profile, etched with liquid or dry etching techniques. The thickness etched (d_V) equals the undercut (d_H) until etching reaches the film-substrate boundary. The anisotropic profile requires dry etching techniques, for example Reactive Ion Etching (RIE).



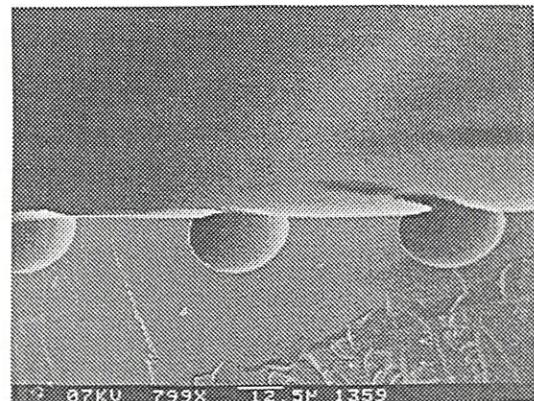
(a) Isotropic profile by wet chemical etching;
 $\text{HNO}_3/\text{HF}/\text{H}_2\text{O}$ -solution [3]



(b) Anisotropic profile by wet chemical etching;
EDP[2]



(c) Anisotropic profile by dry etching; RIE SF_6/O_2 [3]



(d) Isotropic profile by dry etching; RIE SF_6/N_2

Fig. 2.3.4 SEM photo's of trenches etched in single crystalline silicon by a chemical etchant and dry etching techniques.

Although in principle any etching process in which a solid surface is etched in a gaseous environment is a dry etching process, we are using the term "dry etching" in this paper as a synonym for plasma assisted-etching. Dry etching has evolved over the past 20 years from a novel method to ash organic materials in an O_2 -plasma to a method capable of transferring patterns with nanometre dimensions with extremely good control over size and etch profile (fig.2.3.5).

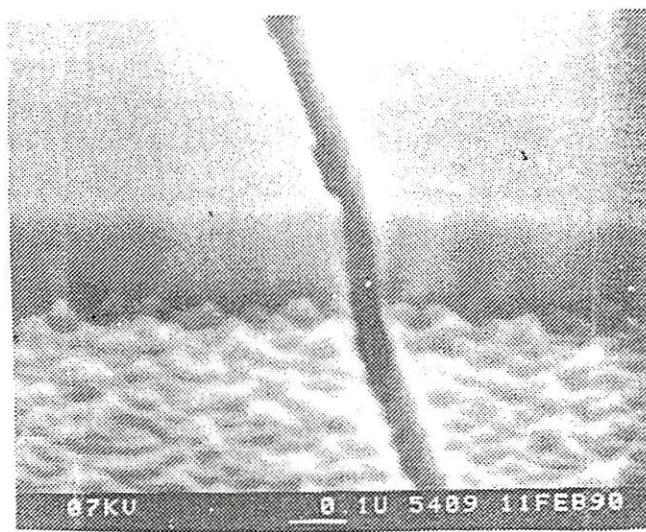


Fig. 2.3.5 Trench of less than 100 nm wide in a Nb film on top of a heavily doped Si substrate [4].

Figure 2.3.6 shows the relation between the various dry etching techniques. The plasma-assisted dry etching techniques can be broadly categorized into glow discharge techniques and ion beam techniques. In the glow discharge techniques the plasma is generated in the vacuum chamber where the substrate is located whereas in ion beam techniques the plasma is generated in a separate chamber from which ions are extracted and directed towards the substrate by a number of grids. In sputter/ion etching and ion beam milling or ion beam etching is only due to a physical effect, namely the momentum transfer between energetic Ar^+ -ions and the substrate surface [7]. In all the other methods indicated in fig.2.3.6 there is also some chemical reaction taking place. Plasma etching and reactive ion etching are the techniques most commonly used today in VLSI fabrication.

There are at least ten different dry etching techniques as seen in table 2.3.1. The easiest way to see the advantages and disadvantages of the various techniques is to classify them according to the mechanism being used to achieve etching [6]. There are three mechanisms: physical, chemical, and chemical-physical. Important considerations in selecting an etching technique are for instance the shape of the profile and the selectivity of the etching process. Selectivity refers to the difference in etch rate between the mask and the film to be etched. For instance, in plasma etching (at gas pressures in the 1 Torr range) the substrate sits on the grounded electrode [5]. At this relatively high gas pressure chemical effects dominate which means that the etch rates are usually higher and the selectivity is better than in ion beam etching which is performed in the 10^{-3} - 10^{-4} Torr range. In this lower pressure range it is usually easier to obtain anisotropic etching but physical effects like sloped edges of the mask, faceting, trenching, and redeposition can have unwanted effects.

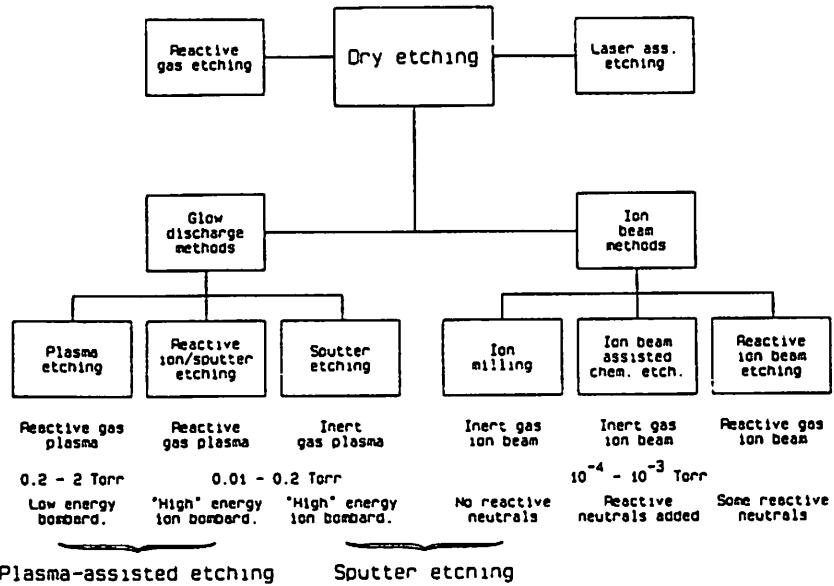


Fig. 2.3.6 The relationship between the various dry etching techniques [5].

Fig. 2.3.7 shows in a schematic way all the essential components of a dry etching system which consist of a vacuum chamber, a gas handling system to measure and control the flow of the reactant gases and pumping package to maintain the pressure required for a glow discharge (in the 1 - 1000 mTorr range). The rf-generator supplies the voltage for starting and maintaining the glow discharge. Fig. 2.3.7 furthermore gives some indication as to the large parameter space in dry etching. Many of these parameters (e.g. flow rate, pressure, power etc.) can independently be chosen for a particular experiment, whereas others (e.g. geometrical factors) are determined by the reactor used.

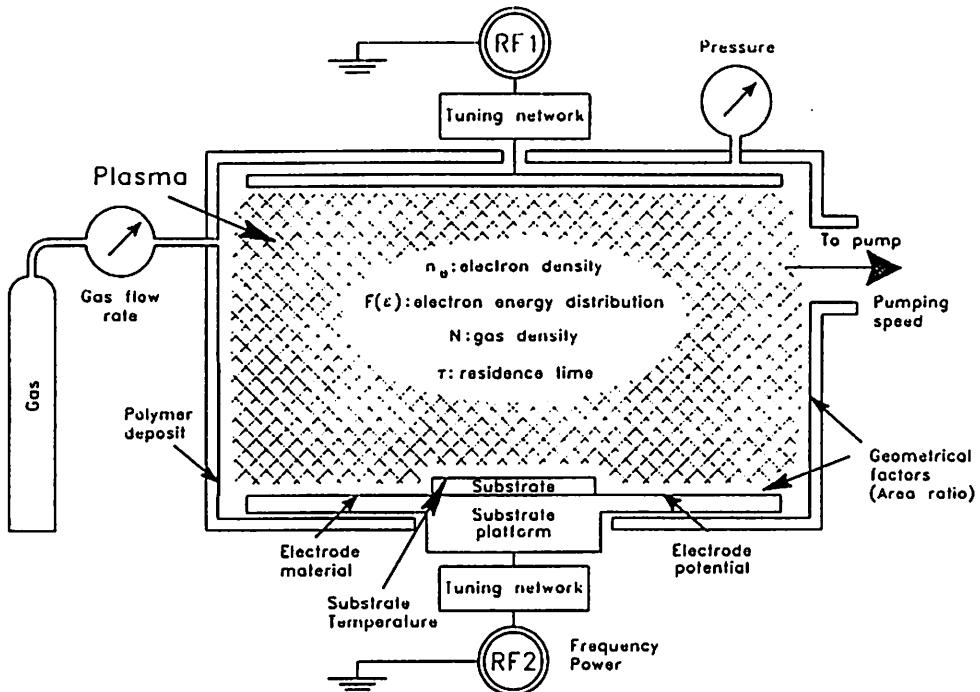


Fig. 2.3.7 Schematic cross-section through a parallel plate reactor showing experimental and fundamental plasma chemical parameters. Usually rf-voltage is applied either to the bottom electrode (in Reactive Ion Etching, RIE) or to the top electrode (in Plasma Etching, PE) [5]

2.4 Additional materials and deposition methods²

An huge number of materials are applied for micromechanical purposes, e.g. insulation layers, protection layers, masking materials, mechanically active layers, conducting layers, measurand-sensitive layers etc. These layers can be fabricated using a variety of processes, such as evaporation, sputtering, chemical vapour deposition, epitaxial growth, ion implantation, oxidation etc. etc. Below, a brief overview will be given for some commonly used deposition methods.

2.4.1. Chemical Vapour Deposition [16,17,18]

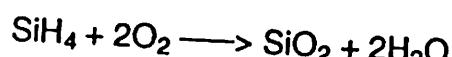
In semiconductor technology, dielectric films are deposited by Chemical Vapour Deposition for insulation and passivation of integrated circuits. It can be defined as a method in which the constituents of the vapour phase react to form a solid film on a substrate. The importance of chemical vapour deposition lies primarily in its versatility for depositing a very large variety of elements and compounds at relatively low temperatures in the form of both amorphous and polycrystalline layers having a high degree of perfection and purity. There are three commonly used deposition methods: atmospheric pressure chemical vapour deposition (referred to as CVD), low pressure chemical vapour deposition (LPCVD), and plasma-enhanced chemical vapor deposition (PECVD). Considerations in selecting a deposition process include (apart from availability of the equipment) the substrate temperature, the deposition rate, film thickness and uniformity, the electrical and mechanical properties and the chemical composition of the dielectric films.

Atmospheric Pressure Chemical vapour Deposition (CVD)

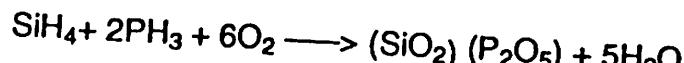
CVD is used for the preparation of silicate glasses: silicon dioxide, phosphosilicate glass (PSG) and borosilicate glass (BSG). The doped layers are used as a source for diffusion of dopants into silicon.

The chemical reactions are:

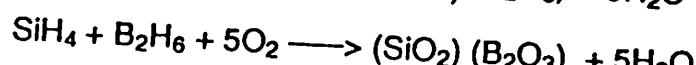
undoped SiO₂



PSG



BSG



Argon is used as a carrier gas. Figure 4.1 shows a typical construction for CVD. It is a simple vertical, single wafer process low temperature reactor.

² Based on: B. Kloeck, UETP-MEMS course Hands on MEMS

The deposition rate of the layers and thereby the homogeneity can be controlled by the temperature of the wafer ($300\text{-}425\text{ }^{\circ}\text{C}$) and/or the flow rate of the carrier gas. The concentration of phosphorous (P) or boron (B) in the deposited layer can be controlled by flow controllers. Although a good estimation of the concentration of the dopants can be given for the gas phase, it is very difficult to obtain from these values the correct concentration in the deposited layer. In order to obtain the correct values for the desired concentration in silicon after diffusion, experimental data are collected for a range of flow settings of the gases and temperatures, in order to establish calibration curves. These calibration curves are combined with computer simulations to obtain the required concentration of dopants and layer thickness.

The advantage of CVD silicon dioxide is its low deposition temperature, but it can not replace thermally grown oxide, because its electrical properties and its resistance to chemicals are inferior. For instance, the etch rate in buffered HF solutions is very high (4000 \AA/min.) which can lead to severe undercutting. This problem can be diminished by annealing at high temperature ($600\text{-}800\text{ }^{\circ}\text{C}$), however this anneal may not always be compatible with the process.

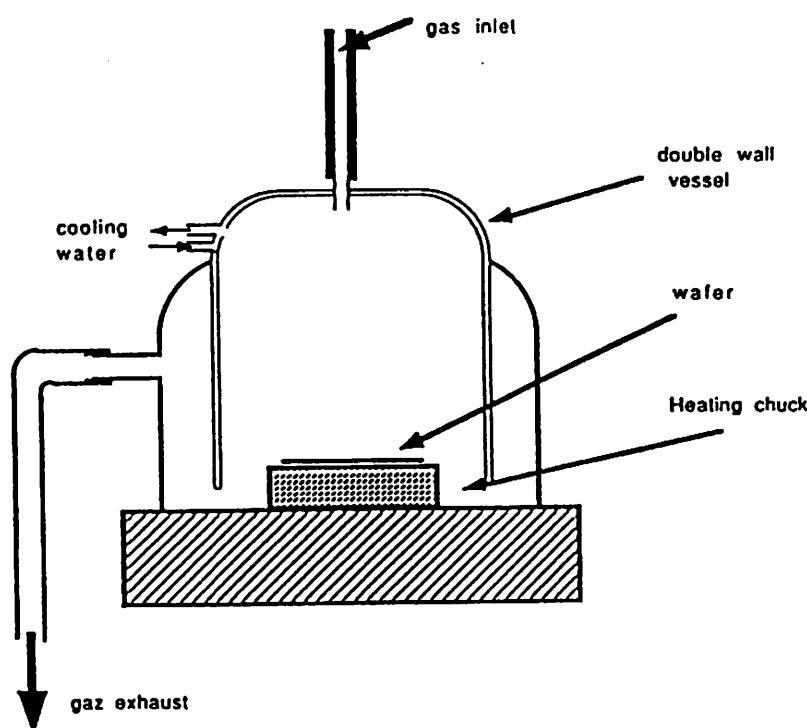


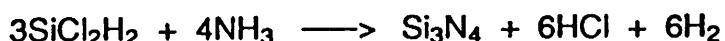
Fig 4.3 CVD reactor for glass deposition.

Low pressure chemical vapour deposition (LPCVD)

LPCVD is commonly used for the deposition of silicon nitride (Si_3N_4) and polysilicon (doped and undoped) thin films. The micro-actuator project includes nitride deposition only, and therefore this discussion will focus on Si_3N_4 . Silicon nitride can also be deposited with plasma-enhanced CVD, which will be discussed in the next section.

LPCVD nitride films have a high density (2.9 to 3.1 g/cm³). They can be used for passivating devices, because they are good barriers to the diffusion of water and sodium. The films also can be used as masks for the local oxidation of silicon (LOCOS), because silicon nitride oxidizes very slowly and prevents the underlying silicon from oxidizing. Finally the etch rate of LPCVD nitride in potassium hydroxide solutions is very low, and therefore the films are ideally suited as etching mask. Also the etch rate in buffered HF is very low, less than 10 Å/min.

In the LPCVD process, dichlorosilane and ammonia react at reduced pressure to deposit silicon nitride at temperatures between 700 and 850 °C. The reaction is:

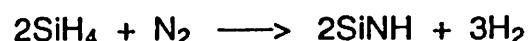
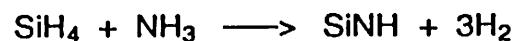


The deposition is controlled by temperature, pressure and reactant concentration. According to the reactant flow rates, the film can be stoichiometric, silicon rich or nitride rich, which has a great influence on the mechanical properties (stress) of the films.

Plasma-enhanced chemical vapour deposition (PECVD)

This section will again focus on the deposition of silicon nitride. PECVD deposited nitride films are not stoichiometric and have a lower density than LPCVD nitride (2.4 to 2.8 g/cm³). Because of the low deposition temperature (300 °C), they can be deposited over completely fabricated integrated circuits, including metallization, and serve as their final passivation.

In the plasma-assisted CVD process, silicon nitride is formed either by reacting silane and ammonia in an argon plasma, or by reacting silane in a nitrogen discharge. The reactions are:



The produced films depend strongly on deposition conditions. Films with very low stress can be prepared. The deposition rate generally increases with increasing temperature, power input and gas pressure. Large concentrations of hydrogen are contained in plasma-deposited films.

2.4.2. Metal Deposition [19,20]

Introduction

In IC technology, thin metal films are deposited for the formation of interconnections, ohmic contacts and rectifying metal-semiconductor contacts. In MEMS, the metal is also used for its mechanical properties and action. The deposition of metals is a physical process, and therefore almost any metal can be deposited as a thin film.

The deposition consists of three steps:

1. Transition from a condensed phase (solid or liquid) to the vapour phase
2. Transport of the vapours between the source and substrate
3. Condensation of vapours (and gases) followed by film nucleation and growth

Only Physical Vapour Deposition (PVD) will be discussed here, although other methods exist, such as CVD and galvanic deposition. PVD processes have the advantage that the three steps mentioned above can be controlled more or less independently. There are three physical vapour deposition processes, namely evaporation, ion plating and sputtering. The three methods are discussed briefly here, but the rest of the chapter is dedicated to evaporation, the method which will be used for the MEMS project.

In the evaporation process, vapours are produced from a material located in a source which is heated by direct resistance, radiation, eddy currents, electron beam, laser beam or arc discharge. The process is usually carried out in vacuum (typically 10^{-5} to 10^{-6} torr) so that the evaporated atoms undergo an essential collisionless line-of-sight transport prior to condensation on the substrate. The substrate is usually at ground potential (i.e., not biased).

In the ion-plating process, the material is vaporized in a manner similar to the evaporation process but it passes through a gaseous glow discharge on its way to the substrate, thus ionizing some of the vaporized atoms. The glow discharge is produced by biasing the substrate to a high negative potential (-2 to 5 kV) and admitting a gas, usually argon, into the chamber. Thus the substrate is bombarded by high-energy gas ions resulting in a better adhesion of the film and lower impurity content.

In the sputtering process positive gas ions (usually argon ions) produced in a glow discharge, bombard the target material (also called the cathode) dislodging groups of atoms which pass into the vapour phase and deposit onto the substrate. Sputtering is an inefficient way to induce a solid-to-vapour transition but it normally results in a better adhesion than evaporated layers because the surface is continuously cleaned by the ion bombardment.

Evaporation process and equipment

A schematic view of an evaporation apparatus is shown in Fig. 1. It consists of a chamber, vacuum pumps, vacuum gages, evaporation sources, substrate holders, a rate monitor and a process controller. Here some details are given about the Leybold system.

Vacuum Chamber: this is a bell jar of about 80 l with lead glass window to absorb X-rays. It is provided with a lift.

Vacuum Pumping System: primary rotary pump and a cryopump with autogenerator of liquid He (20 K) (cryosorption).

Substrate holder: rotating disk to provide homogeneity. Substrate heating (to improve adhesion) can be accomplished by radiant heaters with refractory wires.

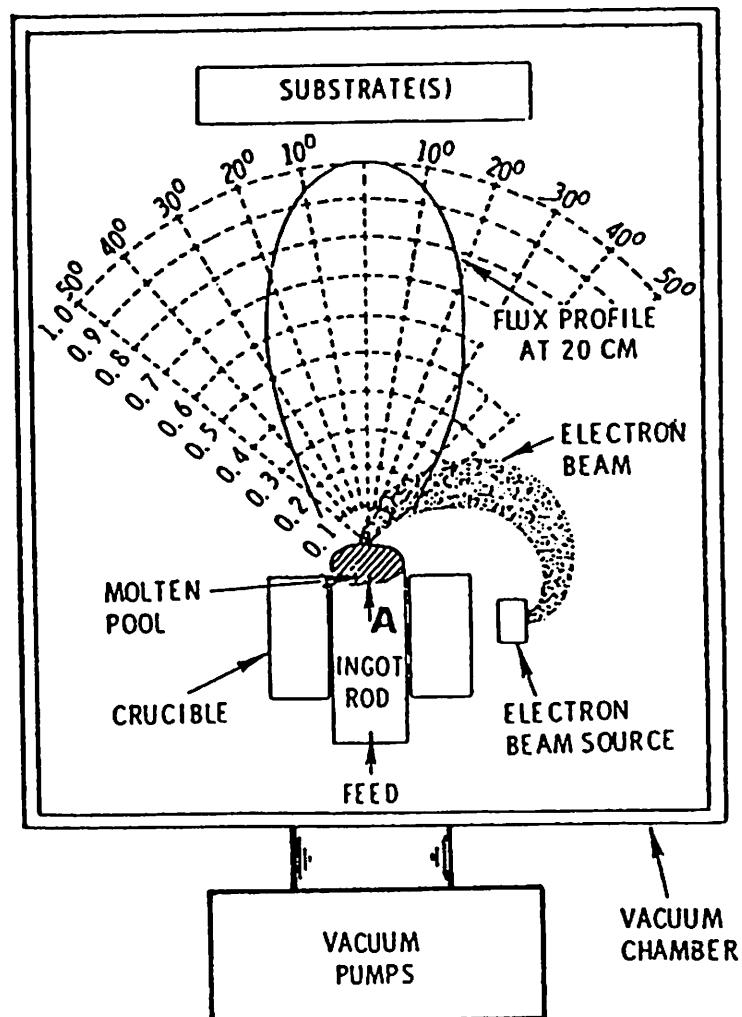


Fig. 1. Vacuum-evaporation process using electron beam heating.

Evaporation sources:

Resistance heated sources: wires or metal sheets. Problems with quantity, alloying, burn-through.

Electron beam heated sources: crucibles of oxides or metals. Can be cooled, but X-rays may distort the substrate surface.

Deposition rate monitor and process control:

Crystal oscillators: the crystal oscillator monitor uses the piezoelectric properties of quartz. During deposition, the same film thickness is deposited on the quartz as on the silicon wafers or other substrate. The resonance frequency induced by an a.c. field is inversely proportional to the crystal mass and thus to the layer thickness. In practice, the change in frequency of a crystal exposed to the vapour beam is compared to that of a reference crystal. Process control is performed by a microprocessor.

Cleaning of the substrate surface before deposition is possible by built-in glow-discharge in an argon atmosphere.

Properties of films after deposition

Microstructure: it is possible to deposit single crystal films on certain crystal planes of single crystal substrates (epitaxial growth), but in general the deposits are polycrystalline. In the case of films deposited by evaporation, the main variables are:

1. the nature of the substrate
2. the temperature of the substrate during deposition
3. the deposition rate
4. the layer thickness
5. the angle of incidence of the vapour beam
6. the pressure and nature of the ambient gas phase

Contrary to what might be expected intuitively, the deposition does not start out as a monolayer, but as three-dimensional nuclei which grow on favored sites on the substrate. A continuous film is achieved only after deposition of 10 Å (e.g. for Ni) to 1000 Å (for Au), both at 600 K. This explains the polycrystalline nature of thin films deposited on amorphous surfaces.

Residual Stress: Residual stress in deposits can be of two types. The first kind arises from the imperfections built in during growth (the so-called growth stress). An increase in deposition temperature produces a marked decrease in the magnitude of this stress. The second kind is due to the mismatch in the thermal expansion coefficients between the substrate and the deposited layer. A graded interface (i.e., producing the change in material over a finite distance instead of producing it abruptly at a sharp interface) decreases the thermal stress and results therefore in a better adhesion.

Adhesion layers: Apart from the various reasons for bad adhesion (dirty surfaces, residual stress), metals which do not form easily an oxide (i.e., noble metals) have generally bad adhesion on oxides (siliconoxide, glasses). This problem can be solved by depositing an intermediate layer of less noble metals like Ti or Cr. It is obvious that aluminum does not need such a layer.

2.5. Surface micro-machining

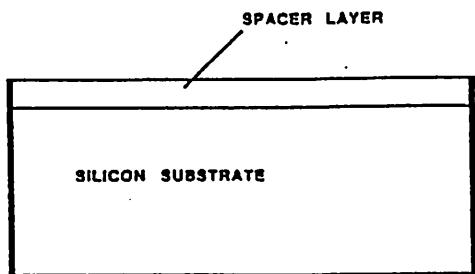
After Roger Howe's work on the surface micromachined resonating vapour sensor [21] an explosive development of surface micromachined sensors and (mainly) actuators started. A culmination of papers on surface micromachined electrostatic micromotors, grippers, accelerometers, pressure sensors, flow sensors, vacuum encapsulated resonating strain gauges, gears, x-y-stages, and other structures was observed at Transducers 1989 in Montreux, Switzerland, and in the time after this conference many groups started work in this field.

The great advantage of surface micromachining lies in the fact that one has much greater freedom in design of micro parts using surface micromachining than with "conventional" bulk micromachining as we have described in chapter II. The most important disadvantage of surface micromachining is the restriction to thin films. It must be said, however, that during the last one or two years more and more work is published on surface machining of thicker films, with the help of alternative ways for photolithography, so that surface micromachining using thicker structures becomes possible with the same precision as machining of thin films using conventional photolithography. The most developed alternative technology capable of surface micromachining is the so called LIGA process³. Originally synchrotron radiation was needed for the LIGA process but alternative, cheaper ways are being developed now for deep lithography.

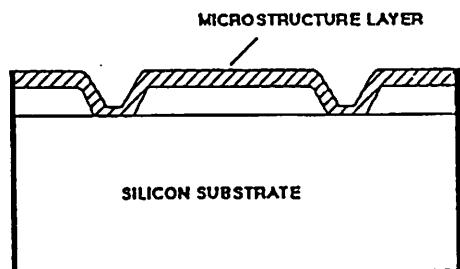
The basic idea of surface micromachining is illustrated in fig. 2.5.1. Successively, films of different material are deposited on a substrate, patterned and selectively etched. The most commonly used pair of materials for surface micromachining is silicon dioxide and poly silicon. The materials are etched in HF and KOH, respectively. For the growth of the thin films a good step coverage is important. This is achieved in LPCVD (Low Pressure Chemical Vapour Deposition) processes. Further a sacrificial layer is advantageous that is etched fast. Phosphorous doped silicon oxide (PSG) meets this requirement. It follows that besides the usual equipment for micromachining, LPCVD equipment for poly silicon and PSG is required.

³LIGA refers to the German "Lithographie, Galvanoformung, Abformung". In this process a thick resist layer (up to 1 mm thick) is illuminated by strong X-ray source (from synchrotron). After developing the resist one has structures with very high aspect ratios, into which metal is grown in an electroplating process. The resist is then removed and one has a metal mold that can be used to fabricate microstructures from plastics and other materials.

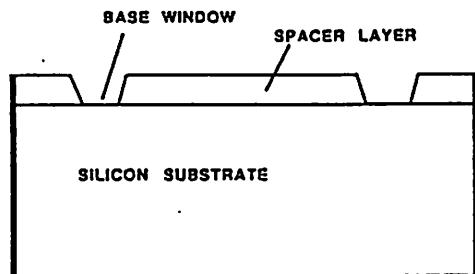
1. SPACER LAYER DEPOSITION



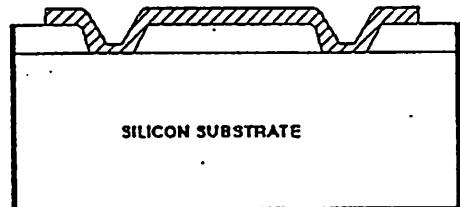
3. MICROSTRUCTURE LAYER DEPOSITION



2. BASE PATTERNING (MASK 1)



4. PATTERN MICROSTRUCTURE LAYER (MASK 2)



5. SELECTIVE ETCHING OF SPACER LAYER

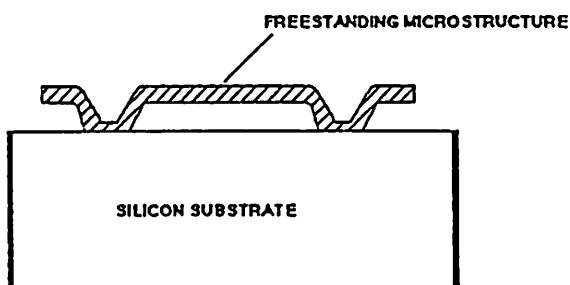


Fig. 2.5.1. Basic process scheme of surface micromachining

The material of which the structures are made are thin films, mainly poly silicon. The mechanical properties of thin films strongly depend on process parameters and thermal treatment. As grown the films are under a strong compressive stress, if released they buckle. Examples of buckled poly silicon structures are shown in fig. 2.5.2. [22]. The compressive stress disappears after annealing [23].

One has to distinguish between two kinds of stress that deform the released thin films. Compressive axial stress leads to buckling of the structures above a critical lateral size. Compressive and tensile stress is important e.g. for microbridges. Vertical stress gradients are visible in structures such as cantilever beams, beams that are clamped at one side. The stress gradients cause the beams to curl up or down, depending on the sign of the stress gradient. Stress gradients are invisible in microbridges. On the other hand, compressive axial stress is invisible in cantilever beams. Test structures that inform on both kinds of stress therefore must cover both types of residual stress.

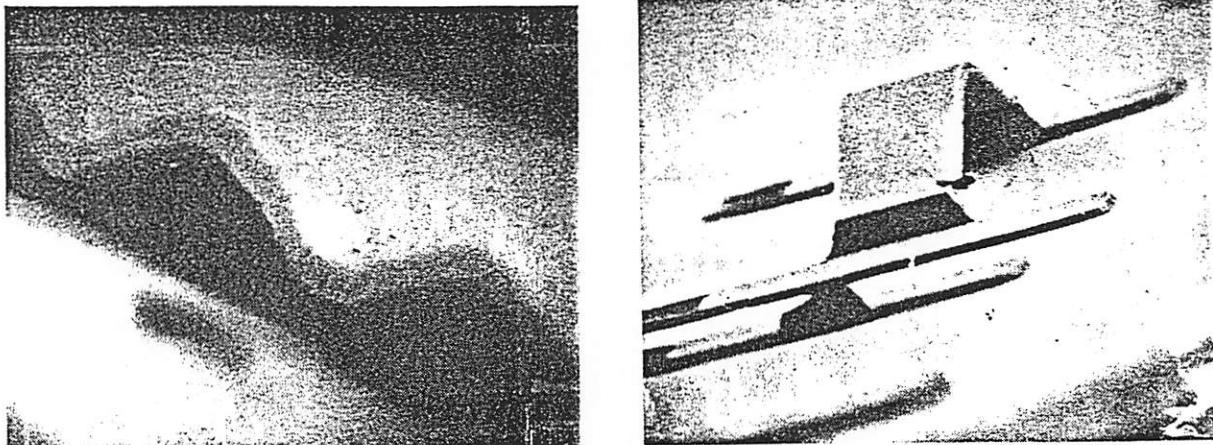


Fig. 2.5.2. Buckled poly silicon structures demonstrating compressive stress of not annealed thin films (from Howe, unpublished)

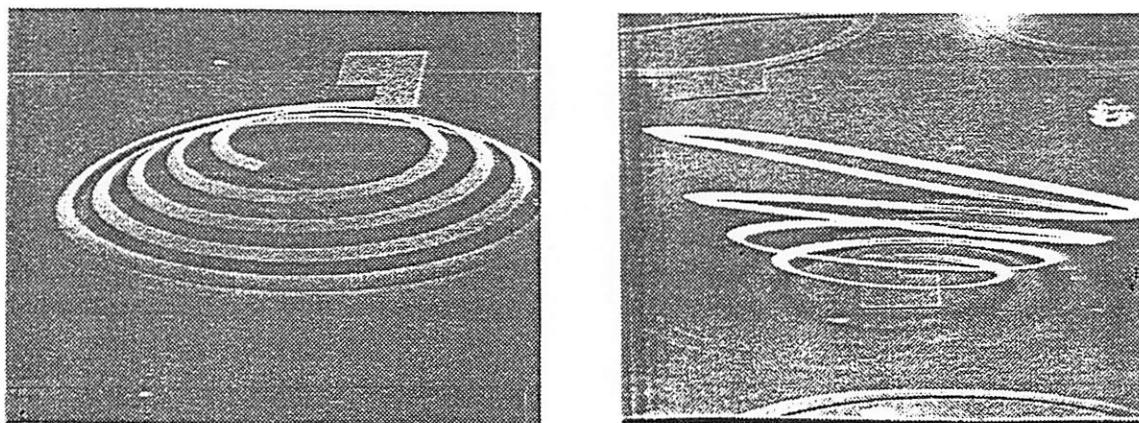


Fig. 2.5.3. Poly silicon spirals that, if released, deform under a vertical stress gradient (from Fan et al. [25])

A number of test structures have been designed to measure the stress in the thin films, many of which are based on buckling of beams. Under a given axial compressive stress, beams buckle if a certain critical length is exceeded [24], see fig. 2.5.2. In fig. 2.5..3. we give an example for a test structure sensitive to stress gradients.

Work of Guckel et al. revealed that it is possible to deposit poly silicon thin films under a tensile stress. This is accomplished if poly silicon is grown in an LPCVD-reactor at a rather low temperature, so that the film is amorphous or fine grained. [27].

Poly silicon has good mechanical properties. Although it is poly crystalline, and in principle can be plastically deformed more easily than single crystalline silicon, it appears that at least at room temperature poly crystalline silicon is comparable to single crystalline silicon regarding plasticity. Fracture strain has been measured by Tai and Muller [27]. Not annealed samples were found to be mechanically stronger than annealed ones. The fracture strain obtained was 1.7 % and 0.93 %, respectively. If Young's Modulus would be the same in both samples and equal to the bulk value (averaged over crystallographic orientations), this fracture strain corresponds to a fracture stress of $3.2 \times 10^9 \text{ N/m}^2$ and $1.8 \times 10^9 \text{ N/m}^2$. These values must be compared with $7 \times 10^9 \text{ N/m}^2$, which is the yield strength of single crystalline silicon.

A notorious problem in surface micromachining is sticktion of the thin films after underetching by wet chemical agents. There is a large amount of literature on this problem. It has been found that if the thin film structures come into contact with the substrate, they stick to it and there is no chance to get them free. Basically, it is the same phenomenon as waferbonding.

The mechanisms and the nature of the forces that attract the thin film to the substrate are controversial. In our opinion two different mechanisms play a key role [28]. The force that pulls the structure down to the surface probably comes from surface tension between the liquid in which the wafers are rinsed. When the liquid evaporates (during drying) a liquid film between the thin film and the substrate is bounded by a meniscus. The latter causes an attractive force between substrate and thin film. If the thin film structure is too weak, i.e. to thin, or too large, one finds an instability of the structure quite similar to the instability of charged plate capacitors. The structure collapses. By this collapse the thin film and the substrate approach each other so close that van der Waals forces and hydrogen bonds come into play. The latter two are thought to be responsible for the sticking force.

It follows that if one succeeds in avoiding the evaporation procedure the sticking problem is avoided. This is in fact the case. Guckel et al. [26] and Tilmans [29,30] demonstrated that it is possible to remove the rinsing liquid in a freeze drying procedure. The wafer is rinsed in a sequence of which the last rinse liquid has a high melting point and a high vapour pressure in the solid state. The wafer is cooled down below the melting point of this liquid without allowing the liquid to evaporate out of the micro structures. Then the liquid used in the last rinse step sublimates, and no sticktion occurs.

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