Review - The von Neumann Architecture (1/4)

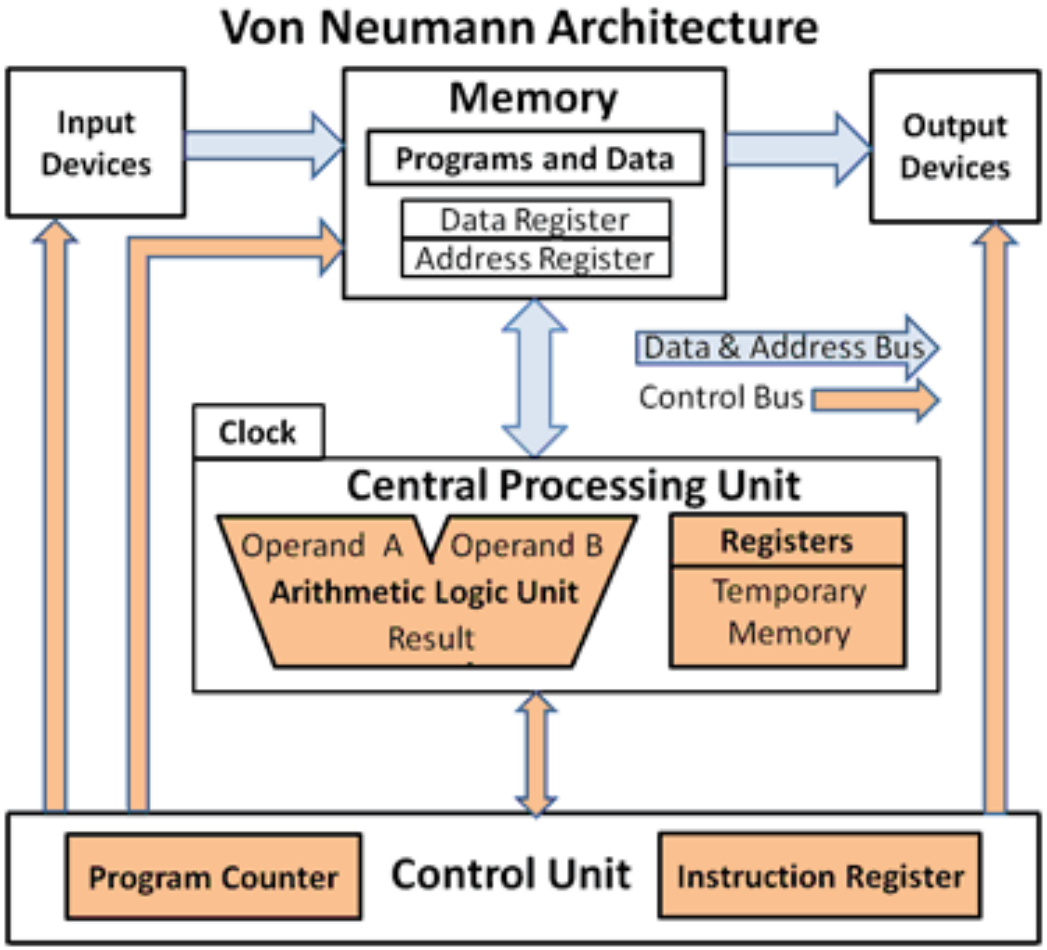


Image Source: https://www.mpoweruk.com/computer_architecture.htm

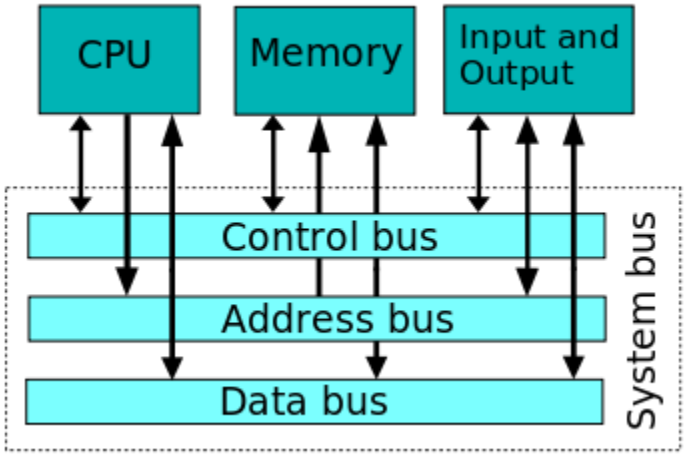
The von Neumann Architecture (2/4)

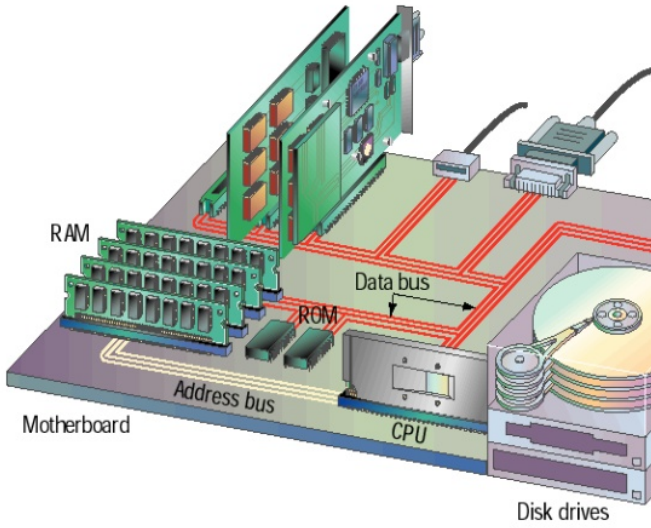
- The Central Processing Unit (CPU)
- The CPU consists of:
  - Control Unit
  - Arithmetic and Logical Unit (ALU)
  - Registers

- **Program Counter** – Address of the Next Instruction
- **Instruction Register** – Instruction currently being executed or decoded
- **Address Register** – Either stores the memory address from which data will be fetched, or the address to which data will be sent and stored
- **Accumulator (Register)** – short-term, intermediate storage of arithmetic and logic data computations

The von Neumann Architecture (3/4)

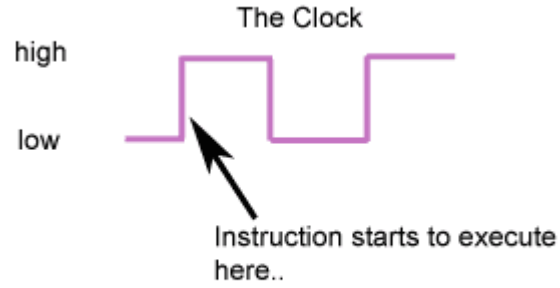
- System Bus
  - **Control Bus** – carries commands from the CPU and returns status signals from the devices
  - **Data Bus** – carries the actual data being processed
  - **Address Bus** – carries memory addresses from the processor to other components
- Memory (RAM)
- Input / Output Units

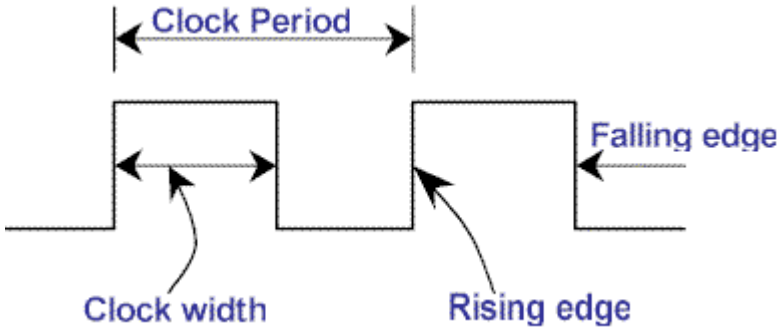




The von Neumann Architecture (4/4)

- Clock Cycle
  - A signal that oscillates between high and low - used to synchronise (coordinate) actions.
  - The number of cycles that a CPU uses per second is used to determine its speed.
    - This is measured in megahertz (MHz) and gigahertz (GHz)
  - The rate of the Fetch/Execute Cycle is determined by the computer's clock.





One Cycle per Clock Tick

- A computer with a 1 GHz clock has one billionth of a second—one nanosecond—between clock ticks to run the Fetch/Execute Cycle.
  - In that amount of time, light travels about one foot (~30 cm).
- Modern computers try to start an instruction on each clock tick.
- They pass off completing the instruction to other circuitry. This process is called **pipelining** and frees the fetch unit to start the next instruction before the last one is done.
  - It is not quite true that 1,000 instructions are executed in 1,000 ticks

Schematic Fetch/Execute Cycle (Pipelining)

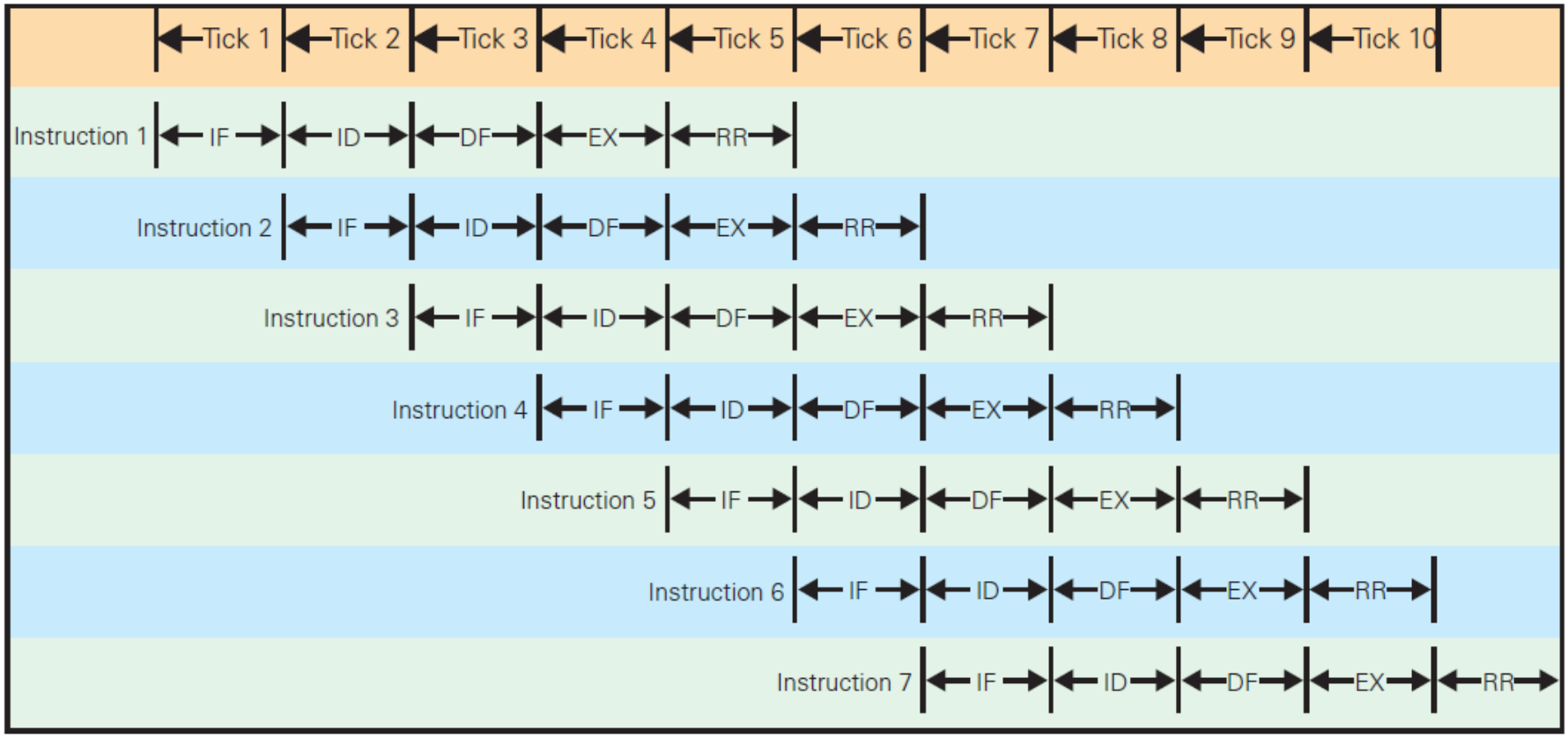
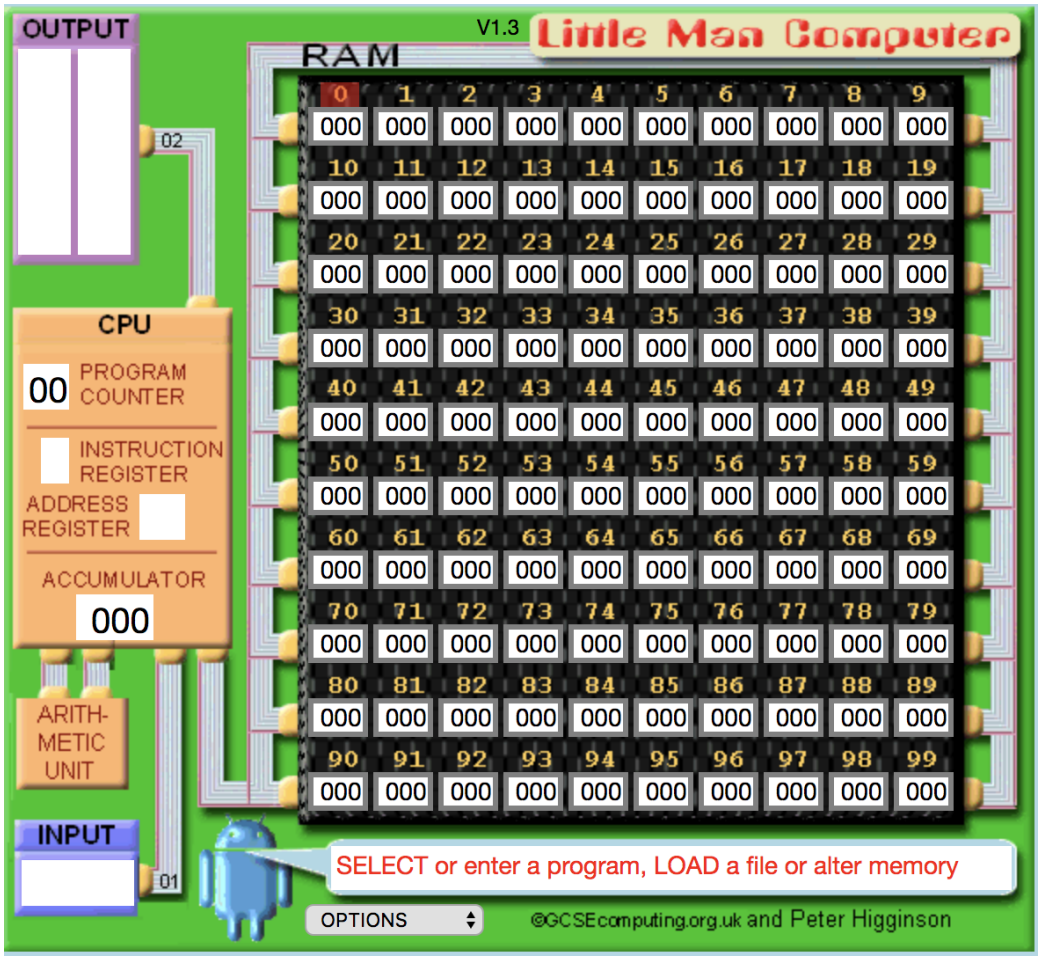


Figure 9.12 Schematic diagram of a pipelined Fetch/Execute Cycle. On each tick, the IF (Instruction Fetch) circuit starts a new instruction, and then passes it along to the ID (Instruction Decode) unit; the ID unit works on the instruction it receives, and when it finishes, it passes it along to the DF (Data Fetch) circuit, and so on. When the pipeline is filled, five instructions are in process at once, and one instruction is finished on each clock tick, making the computer appear to be running at one instruction per tick.

The von Neumann Architecture - Example



Demo:

http://peterhigginson.co.uk/LMC/