Lógica Digital (1001351)

Circuitos Sequenciais: Máquinas de Estados Finitos

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Modelo de *Mealy*

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	1	0	0	1	1	0	0

Figure 6.22 Sequences of input and output signals.

Máquina de Estados Finitos *(Mealy)*

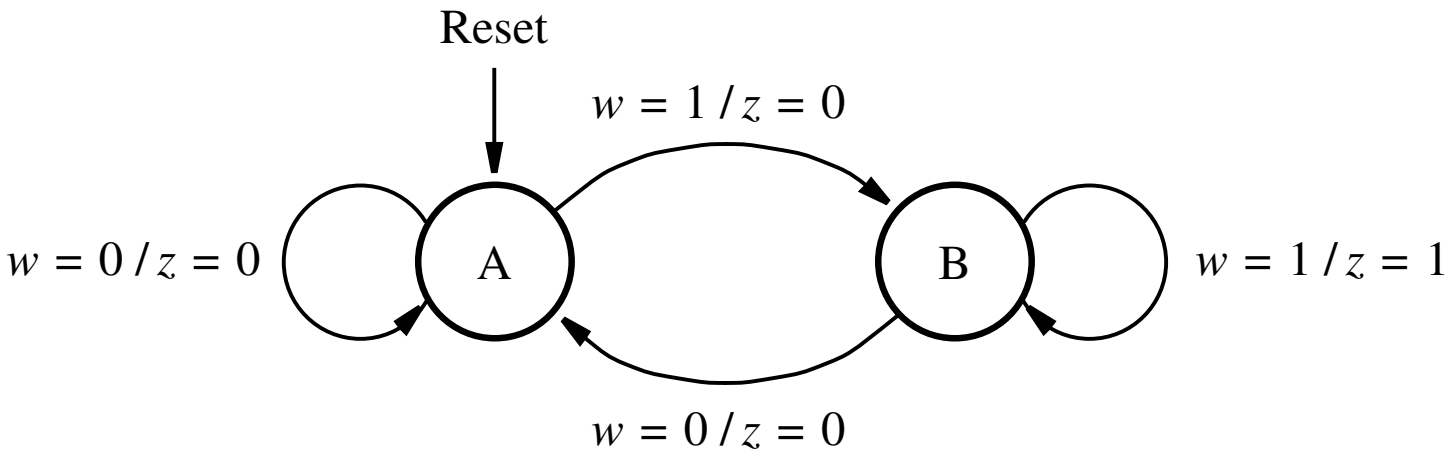


Figure 6.23 State diagram of an FSM that realizes the task in Figure 6.22.

Tabela de Estados

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

Figure 6.24 State table for the FSM in Figure 6.23.

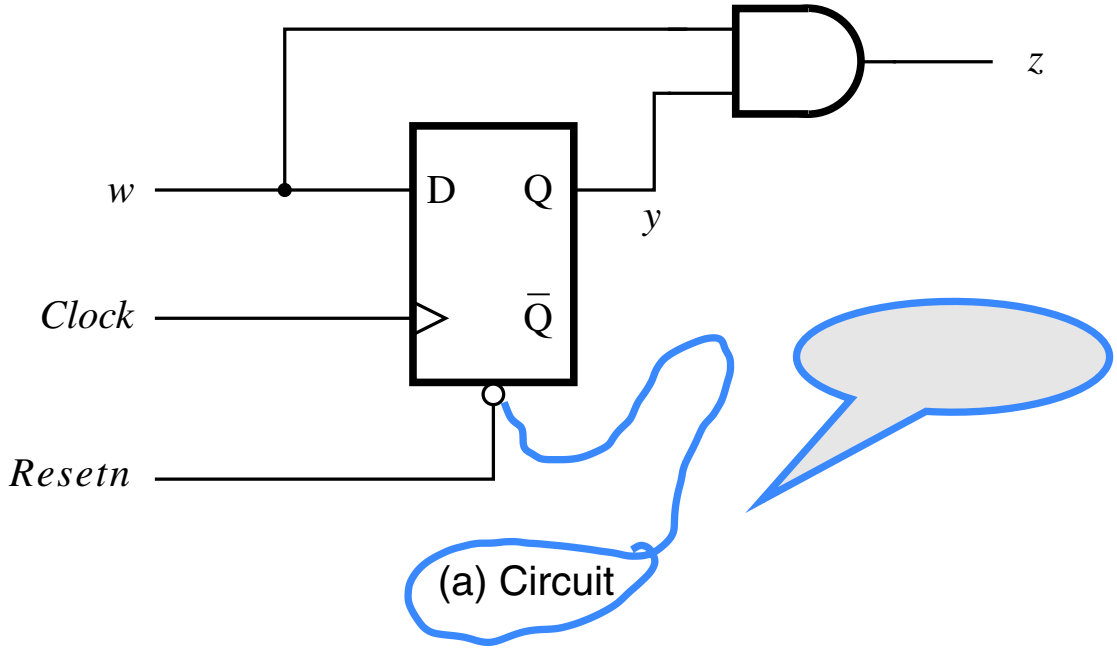
Tabela de Atribuição de Estados

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

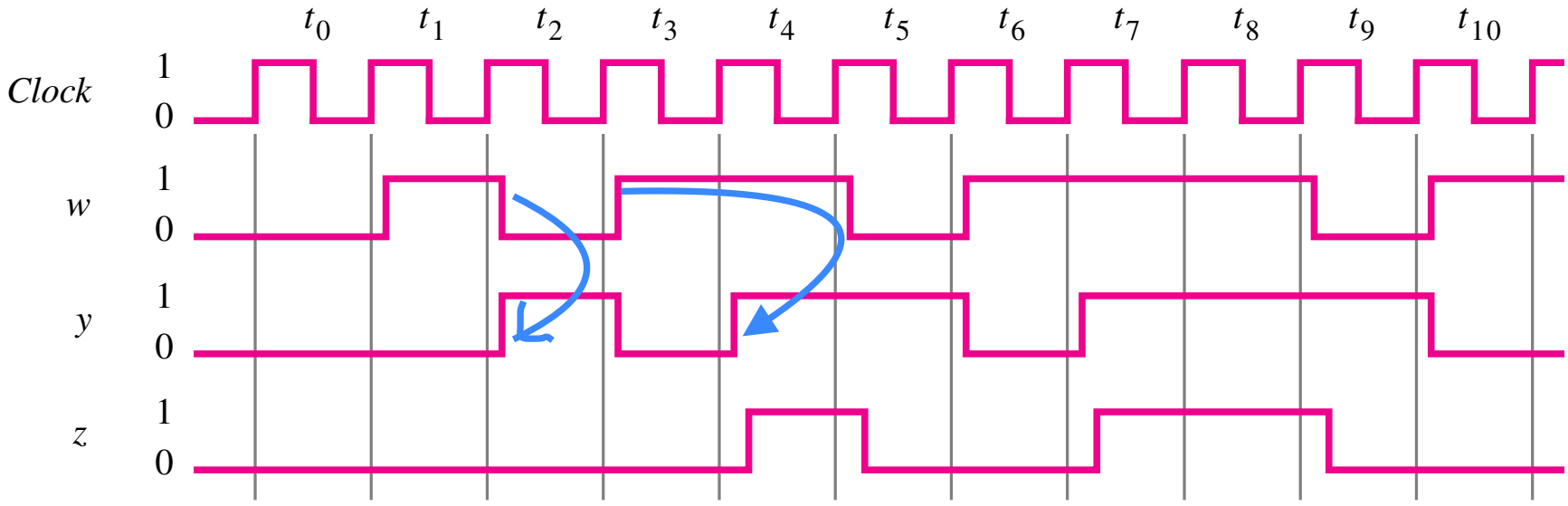
Figure 6.25 State-assigned table for the FSM in Figure 6.24.

$$Y = D = w$$
$$z = wy$$

Circuito Resultante e Simulação

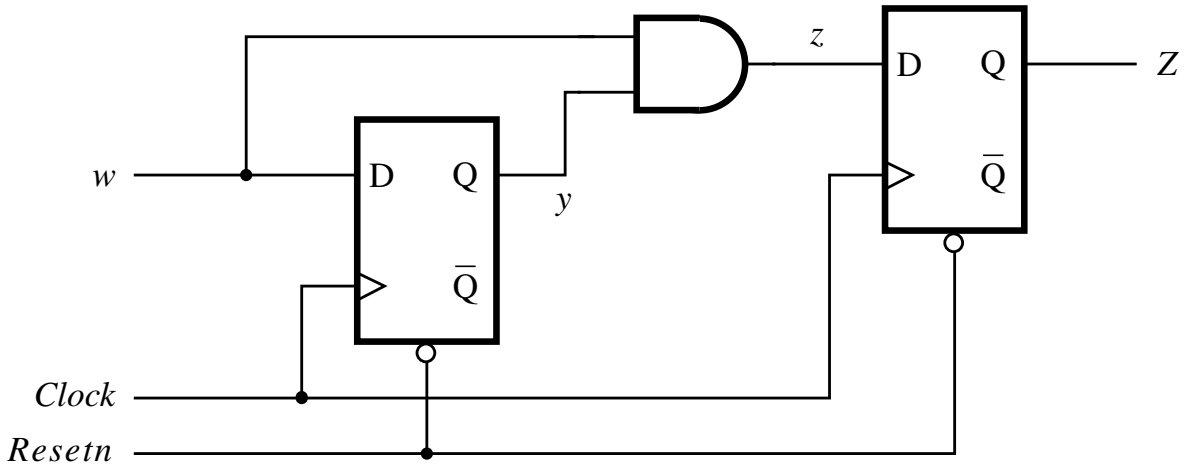


(a) Circuit

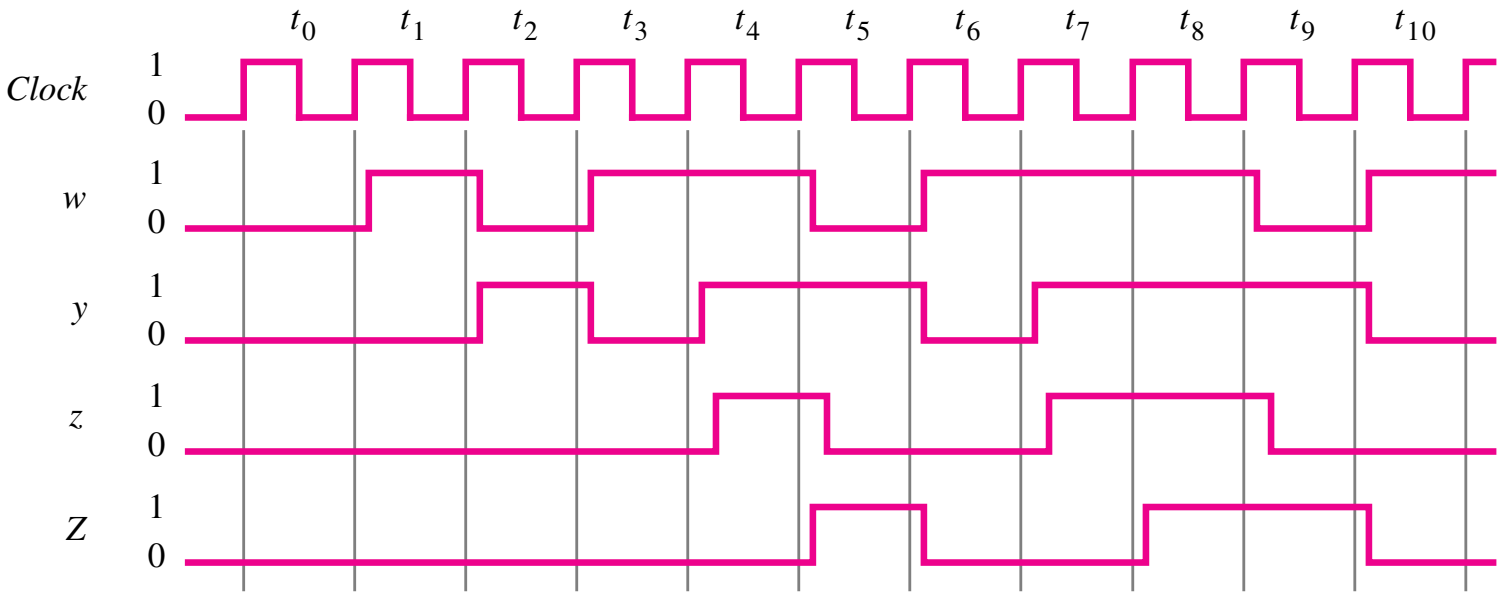


(b) Timing diagram

Circuito Resultante (melhorado) e Simulação



(a) Circuit



(b) Timing diagram

Máquina de Estados Finitos *(Mealy)*

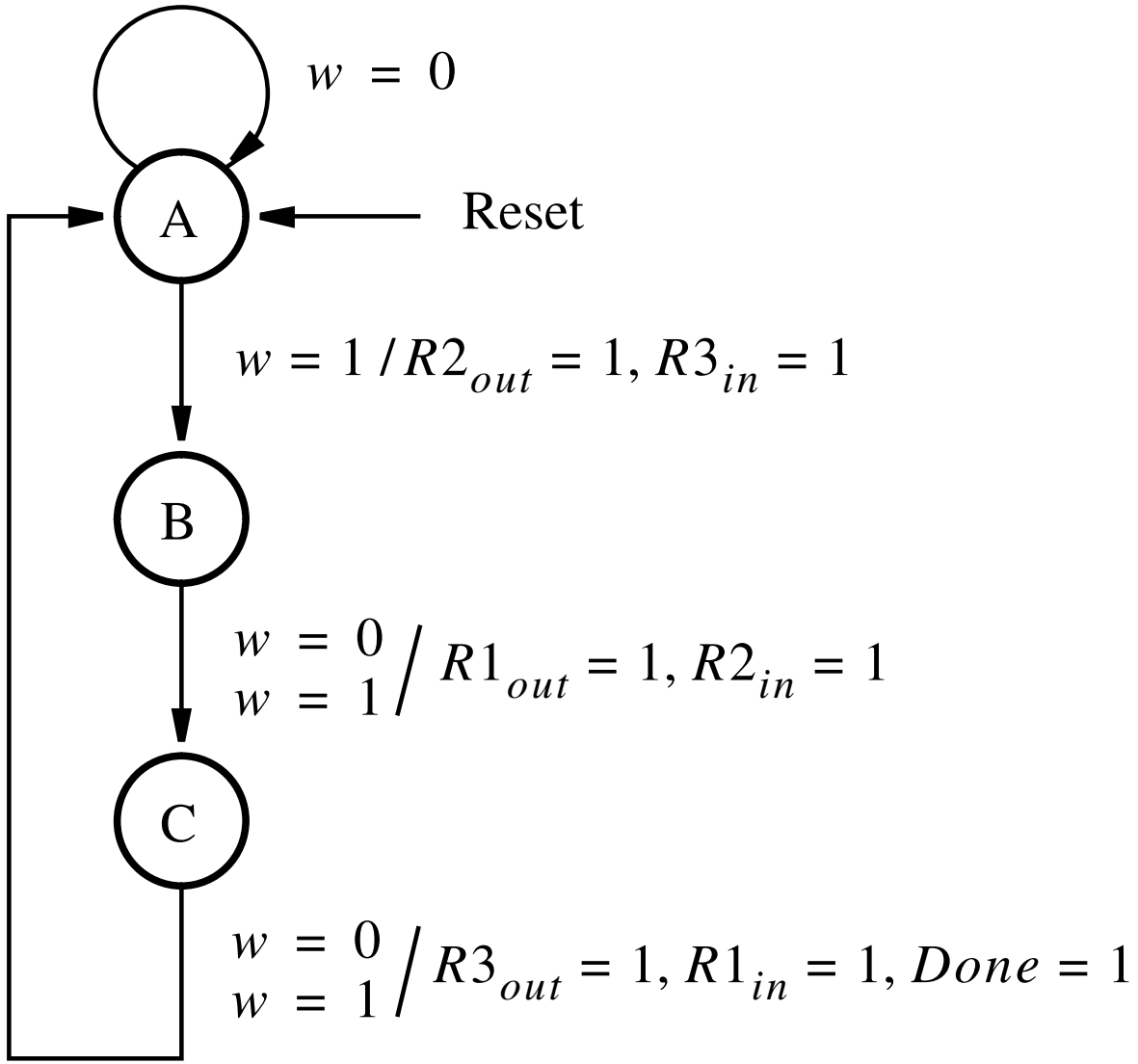


Figure 6.28 State diagram for Example 6.4.

Bibliografia

- Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009

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