

Lógica Digital (1001351)

Circuitos Sequenciais: Máquinas de Estados Finitos

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Atualizado em: 29 de maio de 2019



Troca de Valores entre Registradores

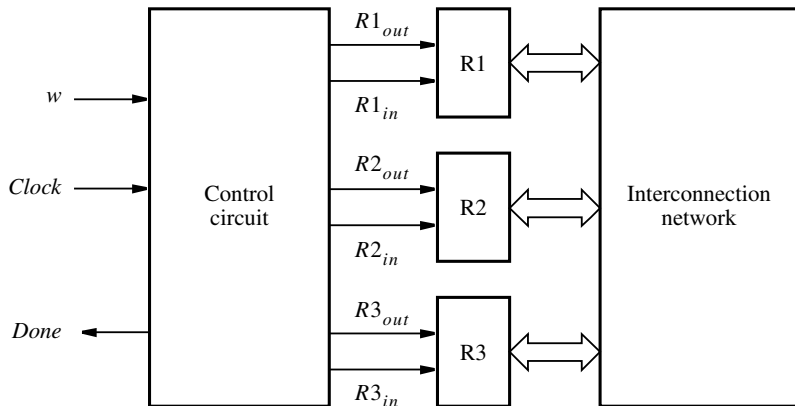


Figure 6.10 System for Example 6.1.

Máquina de Estados Finitos

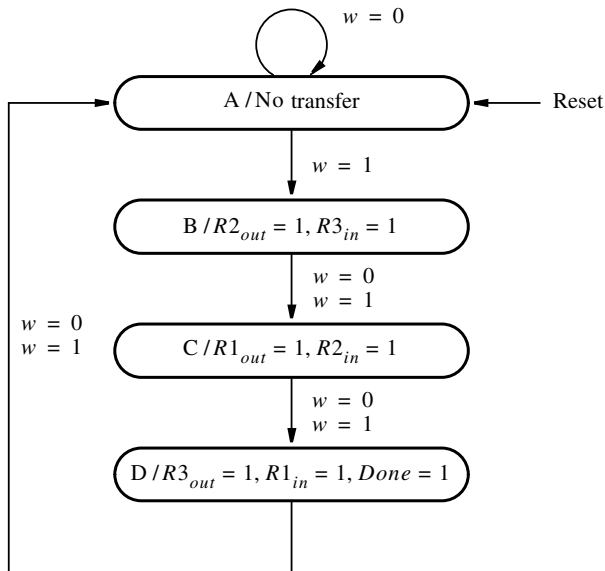


Figure 6.11 State diagram for Example 6.1.

Tabela de Estados

Present state	Next state		Outputs						
	$w = 0$	$w = 1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	<i>Done</i>
A	A	B	0	0	0	0	0	0	0
B	C	C	0	0	1	0	0	1	0
C	D	D	1	0	0	1	0	0	0
D	A	A	0	1	0	0	1	0	1

Figure 6.12 State table for Example 6.1.

Tabela de Atribuição de Estados

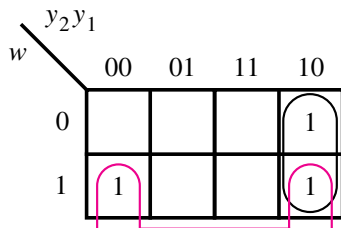
	Present state $y_2 y_1$	Next state		Outputs						
		$w = 0$	$w = 1$							
		$Y_2 Y_1$	$Y_2 Y_1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	$Done$
A	0 0	0 0	0 1	0	0	0	0	0	0	0
B	0 1	1 0	1 0	0	0	1	0	0	1	0
C	1 0	1 1	1 1	1	0	0	1	0	0	0
D	1 1	0 0	0 0	0	1	0	0	1	0	1

$$R1_{out} = R2_{in} = \bar{y}_1 y_2$$

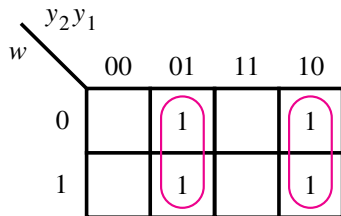
$$R1_{in} = R3_{out} = Done = y_1 y_2$$

$$R2_{out} = R3_{in} = y_1 \bar{y}_2$$

Expressões de próximo estado



$$Y_1 = w\bar{y}_1 + \bar{y}_1y_2$$



$$Y_2 = y_1\bar{y}_2 + \bar{y}_1y_2$$

Figure 6.14 Derivation of next-state expressions for Figure 6.13.

Circuito resultante

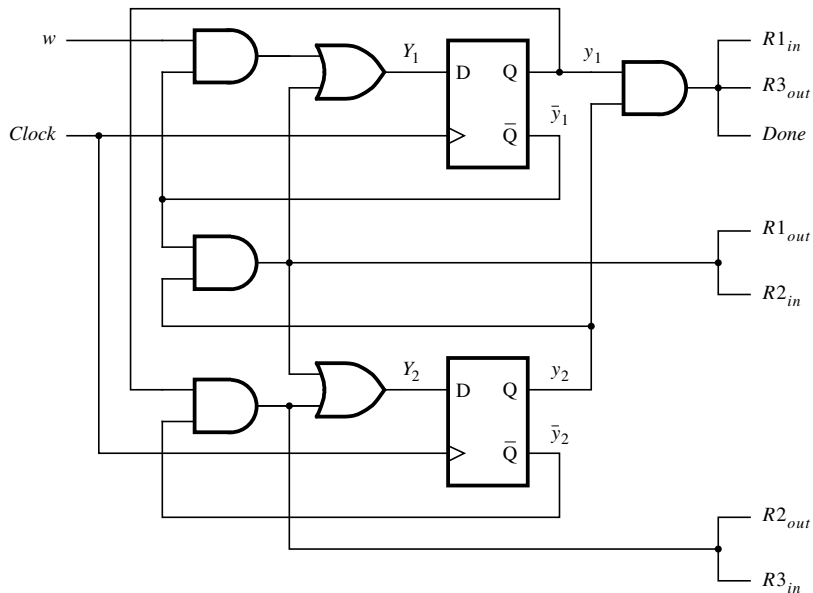
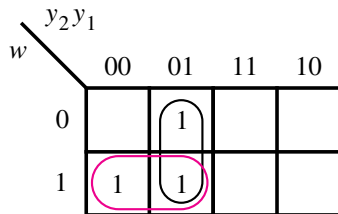


Tabela de Atribuição de Estados (alternativa)

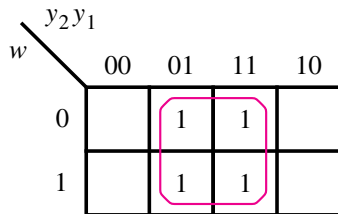
	Present state	Next state		Outputs						
		$w = 0$	$w = 1$							
	$y_2 y_1$	$Y_2 Y_1$	$Y_2 Y_1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	<i>Done</i>
A	0 0	0 0	0 1	0	0	0	0	0	0	0
B	0 1	1 1	1 1	0	0	1	0	0	1	0
C	1 1	1 0	1 0	1	0	0	1	0	0	0
D	1 0	0 0	0 0	0	1	0	0	1	0	1

Figure 6.18 Improved state assignment for the state table in Figure 6.12.

Expressões de próximo estado



$$Y_1 = w\bar{y}_2 + y_1\bar{y}_2$$



$$Y_2 = y_1$$

Figure 6.19 Derivation of next-state expressions for Figure 6.18.

One-hot encoding

	Present state $y_3y_2y_1$	Next state		Output z
		$w = 0$	$w = 1$	
		$Y_3Y_2Y_1$	$Y_3Y_2Y_1$	
A	0 0 1	0 0 1	0 1 0	0
B	0 1 0	0 0 1	1 0 0	0
C	1 0 0	0 0 1	1 0 0	1

Figure 6.20 One-hot state assignment for the state table in Figure 6.4.

$$Y_1 = \bar{w}$$

$$Y_2 = wy_1$$

$$Y_3 = w\bar{y}_1$$

$$z = y_3$$

One-hot encoding

	Present state	Next state		Outputs						
		$w = 0$	$w = 1$							
	$y_4 y_3 y_2 y_1$	$Y_4 Y_3 Y_2 Y_1$	$Y_4 Y_3 Y_2 Y_1$	$R1_{out}$	$R1_{in}$	$R2_{out}$	$R2_{in}$	$R3_{out}$	$R3_{in}$	$Done$
A	0 0 0 1	0 0 0 1	0 0 1 0	0	0	0	0	0	0	0
B	0 0 1 0	0 1 0 0	0 1 0 0	0	0	1	0	0	1	0
C	0 1 0 0	1 0 0 0	1 0 0 0	1	0	0	1	0	0	0
D	1 0 0 0	0 0 0 1	0 0 0 1	0	1	0	0	1	0	1

Figure 6.21 One-hot state assignment for the state table in Figure 6.12.

$$Y_1 = \overline{w}y_1 + y_4$$

$$Y_2 = wy_1$$

$$Y_3 = y_2$$

$$Y_4 = y_3$$

$$R1_{out} = R2_{in} = y_3$$

$$R1_{in} = R3_{out} = Done = y_4$$

$$R2_{out} = R3_{in} = y_2$$

Bibliografia

- ▶ Brown, S. & Vranesic, Z. - Fundamentals of Digital Logic with Verilog Design, 3rd Ed., Mc Graw Hill, 2009

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