FERMILAB SMART CAMAC CONTROLLER

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Abstract

A camac controller which can store list of function codes in RAM and then execute these codes without delay between cycles is described. The data is routed to a high speed parallel port that can be connected to either a Fastbus or VME based buffer memory. A readout speed increase of up to three times over present aquisition systems can be realized.

Introduction

The fixed target experiments at Fermilab have been steadily increasing their data aquisition rates to the point where the time required to read out Camac based electronics has become a serious bottleneck. Presently, the most common data aquisistion architecture consists of one or more groups of up to seven crates per group attached to Camac branch highways which terminate in interfaces to a DEC PDP11 or VAX computer. The transfer of data between the computer back plane and the branch highway invokes a high deadtime penalty. During block transfers, the fastest 16 bit transfers occur at approximately 2.5 uS per transfer with an initial set up time of 100uS even though the Camac standard allows transfers at a 1uS rate. The high speed readout possible with this controller will extend the useable service life of Fermilab's investment in Camac hardware. With the advent of newer high speed bus standards and substantial on line processing capability, a full speed Camac "spiggot" now has somewhere to send its data. On the high energy physics experiments being conducted here, buffering and processing of data is accomplished remote from Camac. Accordingly this module is optimized for high speed tranfers, although at much slower rates, data could be processed within the module.

Design Requirements

As the result of a series of meeetings between the Fermilab research division and prospective users of this device, a series of general specifications were devised:

I. It should be easy to use.

II. The controller should be operable as an auxillary in order to leave existing Camac hardware and software intact for debugging, calibration and testing.

III. Functionally it should execute all the standard block transfer modes; support some minimal LAM testing capability and perform write operations without deadtime between Camac cycles.

IV. A single width module is preferred.

A search for an existing device which would meet these requirements proved negative. There are various types of "smart controllers" commercially available but the emphasis in these modules is data processing rather than raw transfer speed. There are also at least two high speed transfer controllers designed and built by high energy physics experimenters to meet their specific readout requirements.[2,3] We decided to build a derivative of these special purpose devices that would fulfill our more general specifications. To effect ease of use, the computing department has provided software support in the form of a resident bebugger called Sccbug, a Camac function code list assembler called Calex[4], and a translation routine that will pick up and execute DOE standard Camac calls via RS-232.

Design Philosophy

We have divided execution of Camac routines into two catagories. The simplest operations can be executed without deadtime under control of the resident cycle generator. More complex routines are a concatenation of cycle generator "primitives" under the control of a standard microprocessor.

This we believe to be a good compromise between performance on typical readout lists and the amount of dedicated microcoding required to program the cycle generator. Another solution would have been to implement the cycle generator with a bit slice processor type of arrangement which would have been very fast for all possible list types, but difficult to program.

Operation

A block diagram of the controller is shown in Fig. 1. For Camac function codes 0-7, the primary data path is from the Camac read lines to the RS-485 16 bit wide output port. The list memory is loaded with function codes via RS-232 serial protocol from a host computer under the control of a resident microprocessor. Upon receipt of an external signal, the processor sets a bit in a control register which initiates arbitration for control of the Camac crate. When Grant from the next highest priority crate controller is received, list execution begins.

NOTE: The controller will stop execution of a list upon receipt of an ACL from an L2 controller. The ACL response is the only item where the controller is NON CAMAC STANDARD. Upon receipt of an ACL, the controller always completes the presently executing cycle. This means that a delay in releasing the dataway of up to 1.1 uS instead of the specified 800 nS can occur. The implication is that for reliable operation with an L2 controller, a serial Camac clock rate of 3.9 Mhz or less should be used.

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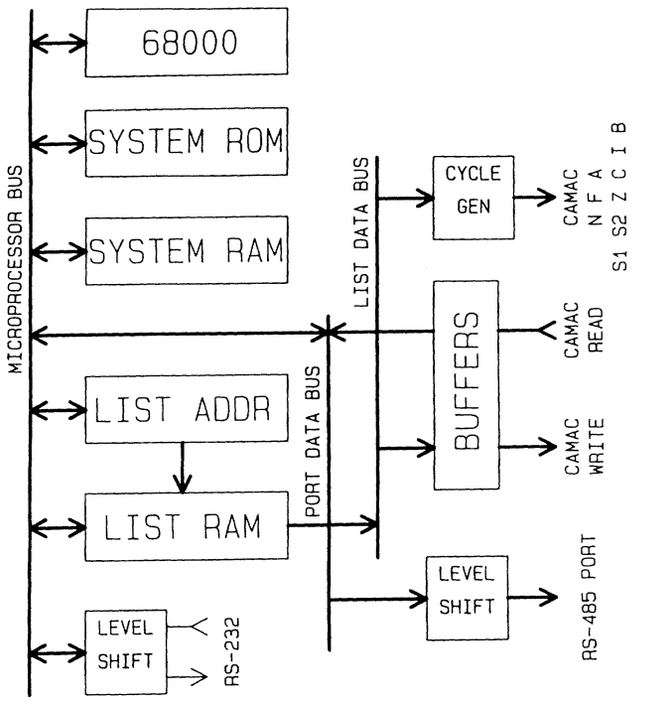
Figure 1
SCC Block Diagram



The repertory of cycle generator operations includes these types:

1. Execute single function code and increment to next list element;
2. repeat present function code until Q=1, then increment;
3. repeat present function code until Q=0, then increment. (This function sends no data);
4. repeat present function code until Q=0 ,then increment and include the first Q=0 transfer as valid;
5. perform a Camac write operation where the next list memory element contains write data rather than an op code. (Q mode block transfer paramaters are ignored during writes);
6. wait for specified LAM;

The LAM lines are brought into an encoder with no priority. If the specified LAM is present independent of the condition of other LAM's the next list element is executed.

7. set/Clear Camac Inhibit line;
8. perform Dataway Clear (Camac C);
9. perform Dataway Initialize (Camac Z);
10. halt list operation.

More complex readout algorithms are carried out under processor supervision. A library of the most commonly used sequences are defined as a portion of the 68000 assembly language macros that make up Calex and can be called when writing readout routines. For example, in the case of address scan, Calex loads the list memory with incrementing A's and F's and N's and specifies Q stop read mode. Once this list is set up the scan will run at full speed.

If the processor needs to examine Camac data, the cycle generator can be set to execute one function at a time. The data is stored in input latches which are strobed by the leading edge of the S1 signal. The processor can access this data as read only memory locations. The ouput port is a word wide write only location which allows the processor to attach extra information to the data stream between list operations or to send test data.

When operated as a primary, this controller has a "helper module"[5] resident in slot 25 of the crate which provides pull-up resistors for the appropriate dataway lines. Via the auxillary connector, the module decodes the N lines from the controller and fans them out to the dataway and routes the LAM lines from slot 25 back to the controller. When the controller is required to output its data to a Fastbus based buffer this module is also outfitted with level adapters to convert RS-485 TTL to differential ECL (unrelated to its Camac role which can be disabled in the case where the controller is an auxillary but the level conversion is neeeded). Only one level conversion is required for each ECL buffer used. The controllers are daisy chained via their RS-485 ports then the data port is level converted before going to the buffer.

List Data Structure

The list data word is 23 bits. (When the list word is write data, 24 bits are significant) 14 bits are used to specify Camac F (5 bits), Camac A (4 bits) and Camac N (5 bits). Two mode bits specify the block transfer type (case 1 through 4 above), 3 bits specify the operation type, 1 bit specifies cycle length. The state machine generates Camac cycles of 2 different lengths including a non-standard short cycle of 600 nS. 100 nSec can be added to the cycle lengths with a selector switch when the controller is installed as an auxillary as specified in the Camac standard. For 24 bit transfers, two words are sent out the data port; the first word containing only eight significant bits. The cyle time is independent of the number of bits per transfer. 1 bit specifies 16 or 24 bit transfers, 1 bit specifies whether X is expected and finally 1 bit specifies whether Q is expected. Table 1 shows this in detail.

The controller has a list memory 8K (1K = 1024) words deep and thus typically can store several complete readout sets. A front panel trigger port connector has as part of its pinout a trigger word five bits wide to be read by the processor as a vector to indicate which of these list sets is to be executed. It is expected that this trigger word will be fanned out to several controllers at once. In addition there is a daisy chained signal called permit which is used to sequence multiple controllers connected to one buffer memory. Since the trigger is fanned out simultaneously the relatively slow microprocessor controlled readout initialization is performed in parallel. Upon the receipt of a permit a controller can then begin readout with very little delay. The number of controllers connected to a given trigger fanout is not necessarily related to the number attatched to a given buffer. Fig. 2 shows a typical system interconnection.

Table 1.
Detail of List Memory Word

Bit #s	Function
00 - 19	parameter bits P00 - P19; the function depends on the operation code
20	significant only when word is write data
21 - 23	3-bit operation code
24 - 31	not used

INIT (operation code 0)

CLEAR (operation code 1)

INHIBIT (operation code 2) parameters are:
P0 1 sets I, 0 clears I

CAMAC (operation code 3) parameters are:

P19 - P15 Camac function (F) code --
00000 - 00111 (00-07) read
01000 - 01111 (08-15) control operation
10000 - 10111 (16-23) write
11000 - 11111 (24-31) control operation
For control operations, no data is transferred.

P14 - P10 Camac slot number (N) --
00000 (00) not used
00001 - 10111 (01-23) normal camac slots
11000 - 11001 (24-25) camac control stations
11010 - 11111 (26-31)
pseudo-slots normally not used

P09 - P06 Camac subaddress (A) - 0-15
P05 Camac cycle speed -- 0 normal cycle
1 fast cycle

P04 - P03 Camac block transfer mode --
00 (0) perform exactly one cycle
01 (1) repeat until Q=1
10 (2) repeat until Q=0, ignore data when Q=0
11 (3) repeat until Q=0, accept 1st data word when Q=0

P02 X Required -- if bit is 1
P01 Q Required -- if bit is 1
P00 Data word size --
0 Data read is 16 bits wide
1 Data read is 24 bits wide

WAITLAM (operation code 4) parameters are:

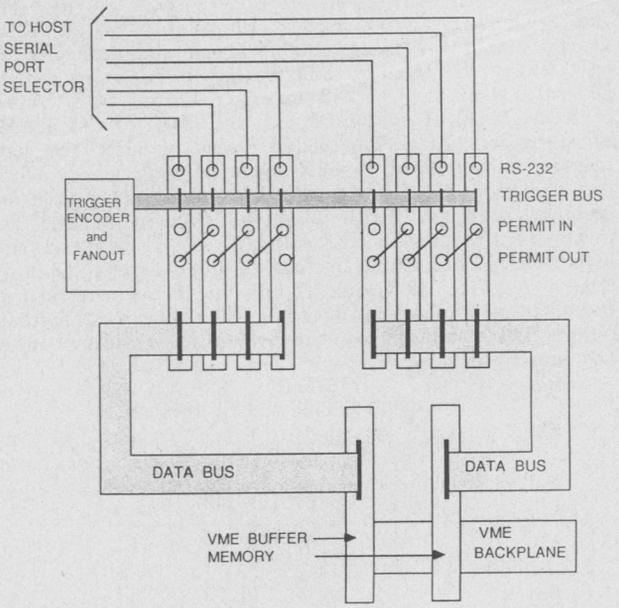
P10 - P14 Slot number from which a LAM is expected
operation codes 5 and 6 are not used.

ENDLIST (operation code 7)

Error Handling

Camac allows for only two error conditions: lack of an X response or lack of a Q response (meaningful only during non block transfer mode). These conditions halt list execution and are latched in an error register. There is also a time out flag which the processsor can set if list execution takes too long thus enabling the processor to halt list execution. List execution also stops if an ACL is sent from a primary controller. An ACL flag is set in a status register. The contents of the status and error registers are used by Calex for error archiving.

Figure 2
Typical System Interconnection



Processor system errors are flagged as bus errors and are of two types: access of non-existant memory locations or an attempt to access the contents of the list memory during list execution. The program counter contains the location of the bus error exception. If it flags a list memory location, the second error type occured.

Ancillary Features

Nine user definable control bits; three of I/O on the trigger port, and three each of input and ouput on the output port are available. An 8 position DIP switch which is used to define various parameters is provided. One position is used to indicate that a particular controller is the last in the chain. If this is set, it indicates to the controller an end of process signal needs to be sent to the buffer when it completes its readout. Two output strobes are available to distinguish between data and status information. A counter that records the number of port transfers can be read and cleared by the processor. This count can be included as status information. A rudimentary interval timer of 8 significant bits whose least count is 10uS is provided. Calex uses this for its watchdog timer routines.

Hardware Description

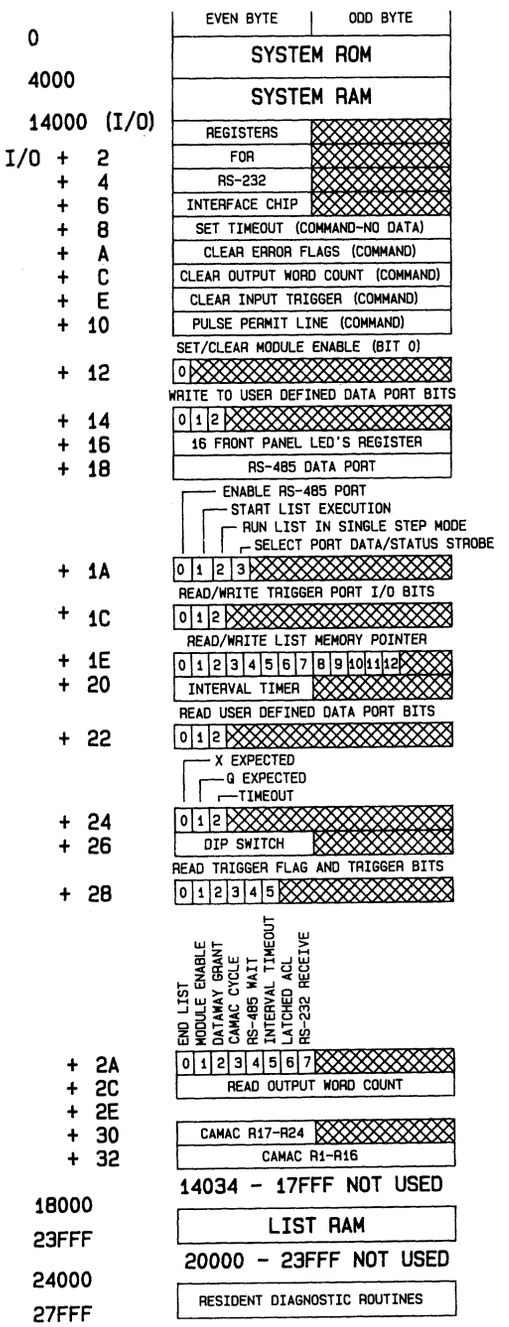
Mechanical

The controller is a single width Camac module. The front panel connectors include a ten pin ribbon connector for the trigger port, a 50 pin ribbon connector for the output port, lemo type connectors for Grant in, Grant out, Request, permit in, permit out, and a four pin lemo connector for the RS-232 serial port. In addition to the connectors, the front panel includes 16 status LED's and a system reset push button. On the rear is the Camac edge connector and the 40 pin ribbon Camac auxillary connector.

Microprocessor

The processor chosen is a Motorola/Signetics 68000 since good software and hardware support for this device is available here at Fermilab. The 10 MHz version executes with reasonable speed and multiples of this clock frequency are suitable for the cycle generator and the RS-232 interface chip. 32K bytes of ROM, 64K of system RAM and 24K of list RAM are provided. From the 68000 point of view the list memory is organized as 32K bytes of long words with the upper 8 bits set to 0. The the I/O space is memory mapped. Table 2 shows this in detail. To minimize the chip count, almost all of the control logic is implemented with fusable logic arrays. Sccbug and a portion of Calex reside in ROM and allow downloading and executing in RAM of S-record format object files produced by the assembler residing on a host computer.

TABLE 2.
MICROPROCESSOR MEMORY MAP

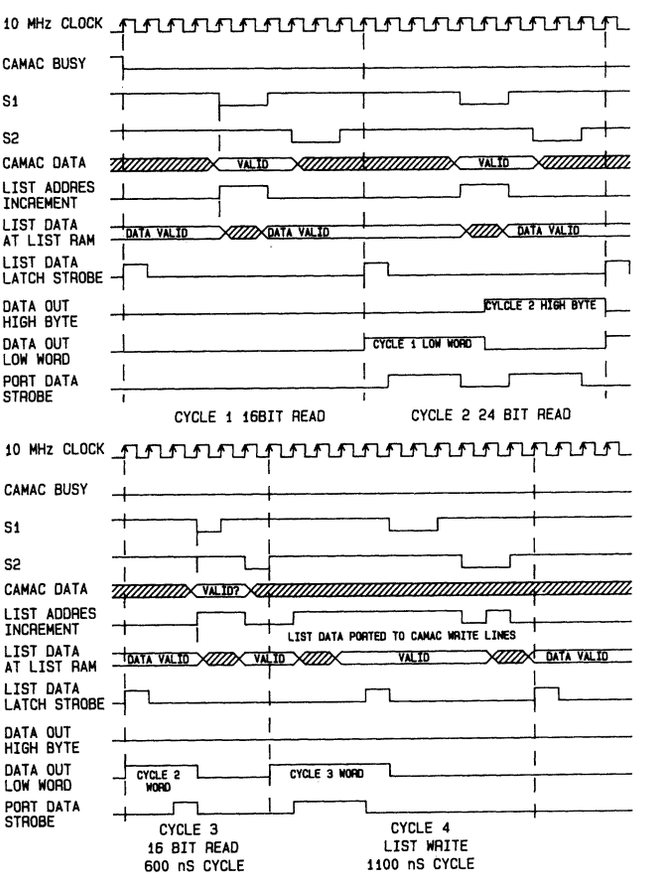


Cycle Generator

A single programmable logic sequencer chip (Signetics PLS168) generates the Camac dataway, output port and list memory timing pulses. A synchronous state machine properly implemented produces glitch free signals, a point of particular importance for a controller. The PLS168 contains 8 S-R flipflops on its output pins and 6 internal flipflops for use as state counters. 48 sets of combinatorial logic which inclide 12 input pin and 10 output feedback terms are available. The input clock is 10 MHz derived from a crystal oscillator assuring transitions on accurate 100 nSec intervals.

Recently, commercially available software for programming fusable logic has greatly facilitated state machine design. State diagrams are translated directly into data files compatible with fuse programming hardware. The design can also be simulated logically before programming. In our case ABEL(tm) software available from Data I/O corporation was used. The cycle generator can be modified by reprogramming the sequencer chip giving additional flexibilty. Waveforms of some some typical operations are shown in Fig. 3.

Figure 3
Data Transaction Timing



List Memory

The list memory is ported to three sets of data busses: the processor which loads the list data, the cycle generator which is controlled by list data and the Camac write lines when a list write is performed. The list memory to cycle generator path is buffered with a latch to store the present list data. Behind this latch the RAM can be incremented to the next address, both eliminating glitches due to RAM access

time and allowing Camac write data to be transmitted without being interpreted as a list instruction. A counter is attached to the address lines whose increment clock comes from the sequencer chip. Incrementing past top of list memory space rolls the address over to 0. The counter can be parrallel loaded from the processor so that list operation can start anywhere in list memory. Counter value readback is also provided.

I/O ports

The output data port is RS-485 three state differential TTL signal standard. Pinouts for the front panel connectors are given in Table 3. The first 18 signal pairs are designed to be compatible with a Fermilab designed VME based buffer memory. The remaining 5 pairs are user definable control and status lines under the control of the processor. These lines can be set and tested within Calex. At Camac data rates, RS-485 can transmit data over long lines. A cable length of 200' feet has been tested. The length of valid data is set by the the cycle generator to be as long as allowed by the type of transfer. 1uS transfers have longer data enables and data strobes than 600 nS transfers. If operations were limited to the 1uS rate, cable lengths of over 300' feet could be used.

Table 3
Pinout of Front Panel Connectors

A. Output Port

1- 32	Data bits 0-16
33- 34	Normal data strobe
35- 36	Status data strobe
37- 38	Wait input from buffer
39- 44	General purpose output bits 0-2
45- 50	General purpose input bits 0-2

B. Trigger Port

1 -	Ground
2 -	Trigger strobe
3 - 7	5 bit trigger word
8 - 10	User definable I/O lines

C. RS-232 Connector

1 -	Transmit
2 -	RS-232 high level to power port selector driver
3 -	Receive
4 -	Ground

The trigger port is single ended TTL. For very long trigger cables, ground backed ribbon cable is recommended. For this reason, pin 1 is connected to ground, since that is the connection to the shield. Line 2 is trigger strobe which when asserted both strobes the trigger word into the trigger latch and sets a flag which can be polled by the processor as a bit in the status register to determine when a trigger has occured. The "Trigwait" routine in Calex tests this line and reads the trigger lines and starts the execution of the specified list. Lines 3 through 7 are trigger data inputs and lines 8 through 10 are the user definable lines which are bidirectional open collector lines. Permit in and Permit out are active low single ended TTL level.

Alternate Uses

The controller with a terminal can be used as a stand alone Camac system. On the ROM are a series of diagnostic routines. One of these is a small routine that allows function codes to easily loaded from a local terminal into list memory. Data can be displayed or a repeat loop for hardware debugging can be specified. E-769 is using a controller as a dummy data generator to test the higher levels of their aquisition system.

Status

31 controllers have been built and tested. Comprehensive tests in a are under way at Fermilab experiment E-769. E-769 and E-653 are using the controllers for the the fixed target running period starting in June of this year. Results so far show the controller to function as expected. There is interest on the part of commercial vendors to produce this device. Software development is under way at this time and the first version of Calex is available. Software details are treated in a separate paper. A dedicated testing fixture which execises all the controller's data paths has also been built.

Acknowledgements

We wish to thank Richard Martin of Data I/O corporation for his help and patience in programming the sequencer.

References

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