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COUPLING CAMAC CRATE CONTROLLERS TYPE "A" TO THE PDP-11 UNIBUS

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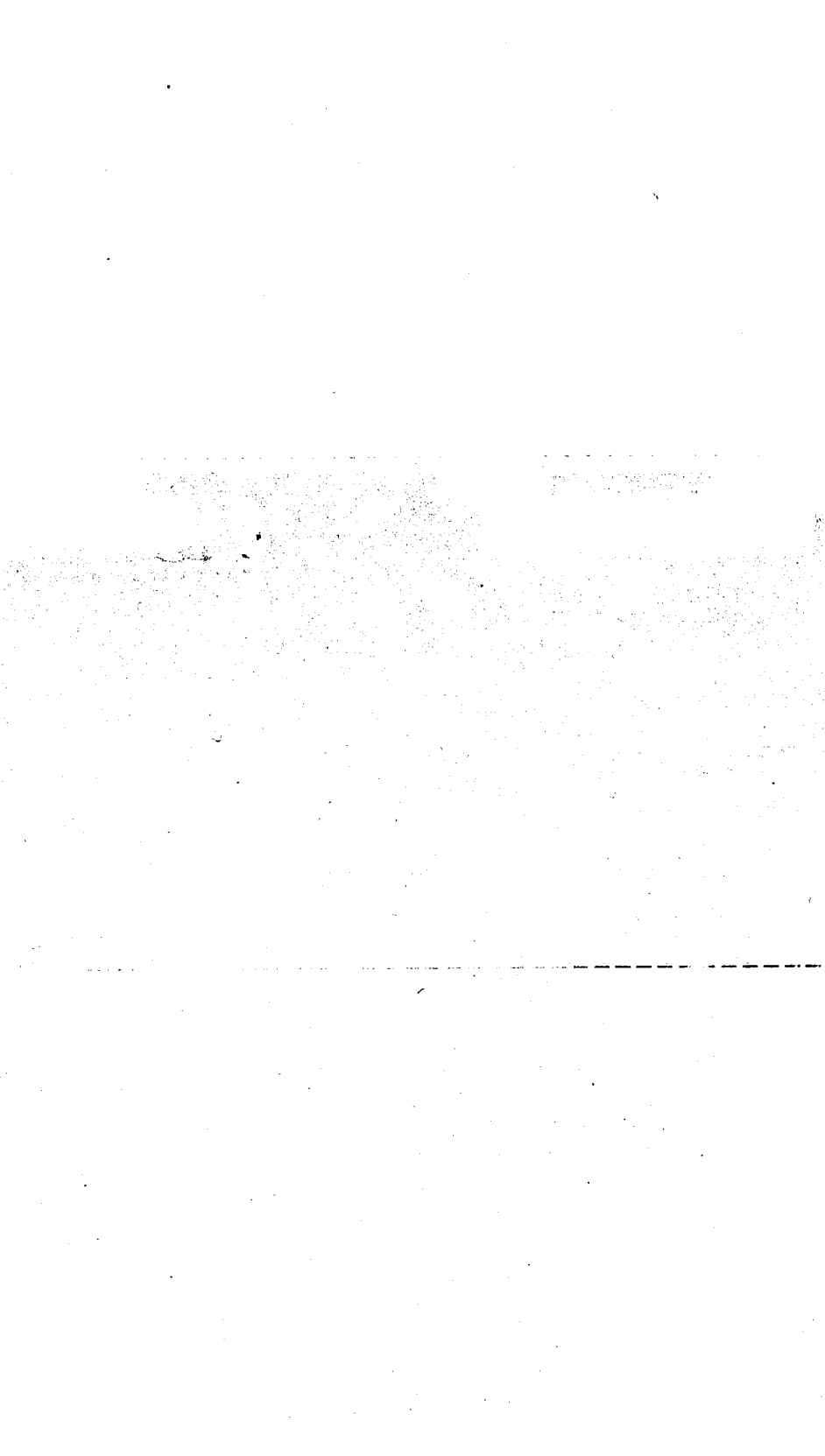
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ABSTRACT

Recently a new method has been proposed for connection of CAMAC to a PDP-11 computer, resulting in a very simple interface and simplified programming. Now such an interface is described in detail here. Some programming examples are also shown.

KEYWORDS

CONTENTS

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to the PDP-11 UNIBUS.

Introduction

CAMAC is a standardized modular instrumentation system originally intended for interfacing of nuclear physics experiments to computers. Data are sent in digital form from "modules" in a "crate" to a computer or vice versa via "crate dataway" and "branch highway". Up to 7 CAMAC crates can be connected in parallel to the branch highway, each of them using a standard interface called crate controller type "A". For connection of the CAMAC branch to a specific computer a specific interface, called branch driver, is needed.

This "double interfacing" (crate controller and branch driver) is necessary to get a highly standardized system, but might be too expensive for small CAMAC systems. To avoid this disadvantage it is possible to use special crate controllers, which interface directly to a specific computer. Fortunately this is not necessary if the computer is a PDP-11 (Digital Equipment Corp.). The input-output busline of this computer, the UNIBUS, is similar in structure to the CAMAC branch highway and uses similar signals. Many of the branch signals are compatible with corresponding UNIBUS signals, and the corresponding bus lines can be connected directly. In other words, crate controllers A can be connected directly to the UNIBUS [x]. Only for the incompatible signals

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[x]   To be correct, the UNIBUS transmitter drive capability is lower and the characteristic impedance of the UNIBUS is somewhat higher than that of the CAMAC branch. Nevertheless, up to 7 crate controllers "A" may be connected to the UNIBUS without troubles.

a branch interface is needed. In order to keep the number of incompatible signals low a special addressing method for the CAMAC modules has been proposed[1]. This method also simplifies programming, so that it might be of interest for large CAMAC systems, too.

        In the following first the description of the addressing scheme will be repeated briefly, and then details will be given on implementation and programming of the interface used.

1. Addressing

To address the CAMAC modules the following bit configuration has been proposed for the transition from the CAMAC branch[3] to the UNIBUS[2] .

CR 4, 2, 1	F 4	N 16, 8, 4, 2, 1	A 8, 4, 2, 1	F 2, 1, 8	CAMAC branch
2^{15} . .	2^{12}	. . 2^9 . .	2^6 . . 2^3	. . 2^0	UNIBUS

CR = crate address

N = module address

A = subaddress

F = function code

In addition, the read-write code line[4] F 16 must be connected to the in-out control line[2] Cl. The function code bits are treated as a "sub-subaddress" here. The "natural" sequence of the CAMAC address bits has been retained except for the F-bits. - F4 is active only for the non-standard and the reserved functions and, therefore, is not used very often. So it might be of advantage to take it

out of the UNIBUS address word and to replace it by an
additional crate address bit to gain more addressing space
for computer memory. The F4-line must then be driven
by a flipflop, which is loaded occasionally by an extra
instruction. - The UNIBUS address bit 2^0 must not be
a "1" except for byte instructions manipulating byte operands
at odd addresses. CAMAC uses only complete data words,
not bytes. To circumvent this difficulty we drive the
F8-line by the UNIBUS 2^0-address line. F8=1 means command
functions which do not transmit data. So we need not
worry about data bytes or words.

Concerning the 3 or 4 most significant address bits,
there is still some freedom left for the user. They can be
used e.g. to define up to 7 CAMAC crate addresses
(one branch). In this case a one-of-eight decoder will serve
to select the addressed crate. Per crate 4K word addresses
are needed on the UNIBUS, if F4 is driven directly by the
2^{12} bus line. So this one-step addressing scheme can only
be used for small CAMAC systems with not too much
computer memory. It might be of advantage in small de-
dicated systems with fixed configuration, because the interface
between CAMAC and UNIBUS is inexpensive and programming
is as easy as with devices connected directly to the UNIBUS. - It
should be mentioned here that a CAMAC crate does not use
all of the 4K addresses allocated to it. There are always some
gaps which can be used for other devices. For example,
the crate controller type A does not recognize commands
addressed to N(31). Inside such a gap of 64 consecutive
word addresses the addresses of the PDP-11 processor
registers and of the standard peripherals will be situated,
if the crate uses the word addresses from 28K to 32K.

For large systems and those, which are expected to grow large or must be software compatible with them, it is recommended to use a crate address register, which will drive the decoded crate address lines BCR, and which has to be loaded at the beginning of every input-output routine. In this register also the seldom -used F4-bit can be incorporated as well as several branch address bits. Then the binary configuration 1110 of the 4 most significant UNIBUS address bits would mean "CAMAC addressed". Of course, the 2048 word addresses belonging to this configuration must not be used for memory addresses. If in the beginning only one crate is used, the hardware does not need a detector for 1110. Nevertheless, the software should use already these addresses to be compatible for later expansion.

2. Interface implementation

Many of the PDP-11 UNIBUS-signals have equivalent counterparts on the CAMAC branch and need no interface at all. Only those lines which are not compatible must be connected via an interface. Of these the most important are SSYN and BTB. On the UNIBUS the leading edge of the response signal SSYN (slave synchronisation) signals the end of the transfer cycle, whereas on the CAMAC branch the same is done by the trailing edge of BTB (branch timing signal B). When SSYN arrives the processor strobes the data and then drops the address lines, but CAMAC needs the address till the end of BTB (or at least of strobe S2).

We can overcome this problem by storing the address bits and the status of the control line C1 in a register till the end of BTB, or by changing the processor

timing. The first solution is somewhat expensive but straight/forward and, therefore, will not be discussed here. It might be of advantage if digital repeaters are necessary to drive a long CAMAC branch. But for the normal case we prefer the more economical second solution, which has the sole disadvantage that a small change in the processor is necessary.
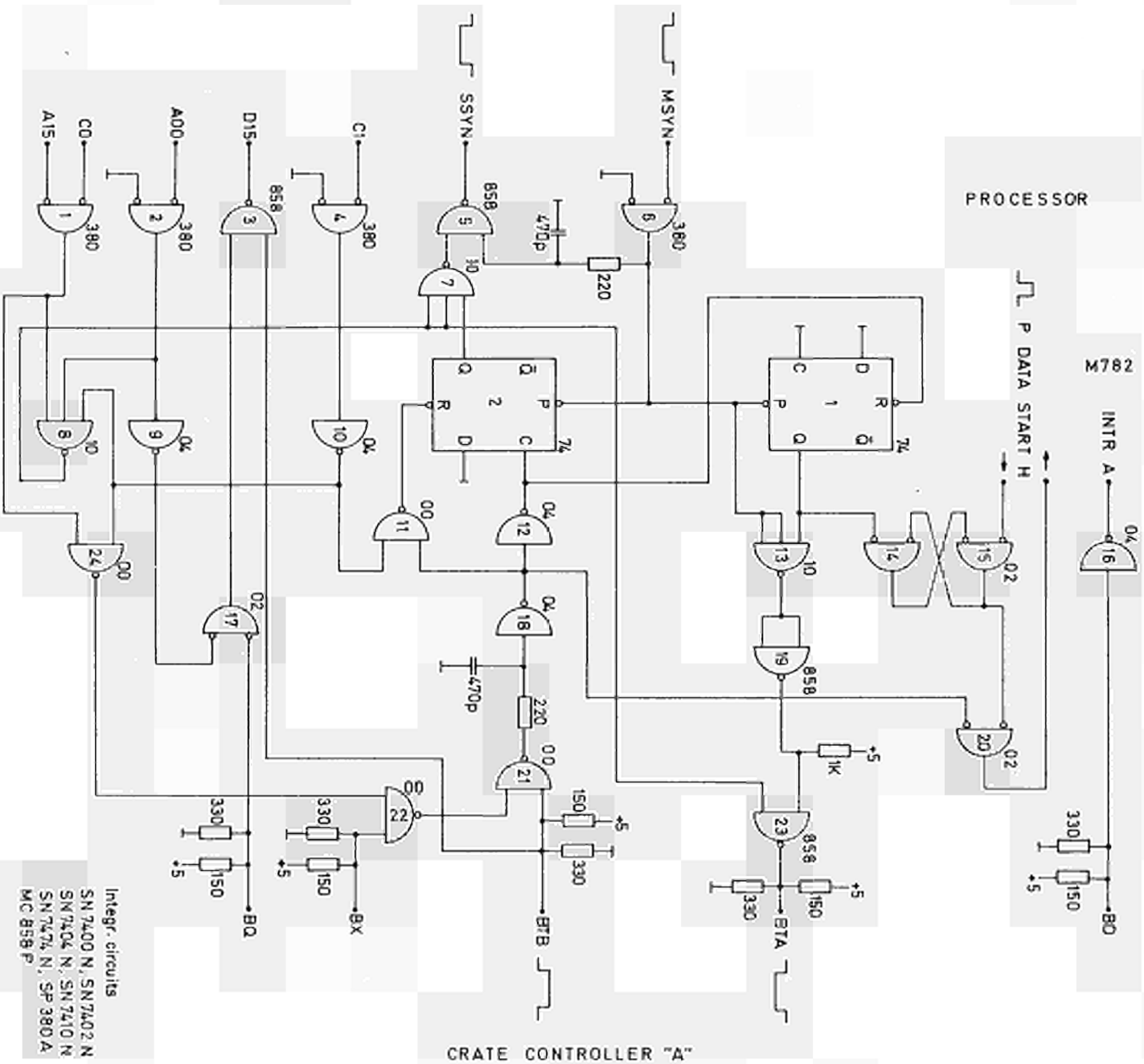
This solution is presented now in the description of the minimum PDP-11 to CAMAC interface. This interface is only for one CAMAC crate and a computer with not more than 16K of memory. More crates or more computer memory can be used when a crate address decoder and extra BTB inputs will be added. For a large CAMAC system the crate address decoder must be replaced by a crate address register, which can be preloaded with the decoded crate addresses. - In addition it is assumed that our CAMAC system contains only modules with 16 or less data bits. Then no interfacing is required for the unused upper 8 bits of the 24-bit CAMAC data word. The lower 16 bits can be connected directly to the corresponding UNIBUS data lines.

3.   The minimum PDP-11 CAMAC interface

The main task of this interface is to accommodate the UNIBUS timing to the CAMAC branch timing. This is done by flipflops 1 and 2 (fig.). When MSYN is asserted BTA is asserted, too, via gates 13, 19, and 23. When the crate controller responds with BTB, BTA is extinguished by resetting flipflop 1. If a DATO cycle is executed, which can be sensed via gate 4 on the UNIBUS C1 line, flipflop 2 is clocked to zero at the end of BTB and then asserts SSYN.

This means that the addressed CAMAC unit has taken the data. The processor removes MSYN, which brings both flipflops to their rest state (= preset). If a DATI cycle is executed, flipflop 2 is loaded to zero at the beginning of BTB, asserting again SSYN. This occurs approximately at the time of CAMAC strobe S1 and stimulates the processor to strobe in the data. At the same time an internal processor pulse P DATA START H is generated, which will clear MSYN and somewhat later also the address and control lines. As the latter cannot be tolerated by CAMAC before strobe S2, it is necessary to delay this processor pulse appropriately. For this purpose the wire connection for this pulse has to be cut and the combination of gates 14, 15, and 20 must be inserted. Gates 14 and 15 form a flipflop, which will store the pulse till gate 20 is opened at the end of BTB. (This occurs only for CAMAC-DATIs. In all other cases gates 15 and 20 will work as simple inverters, giving only a negligible delay).

The interface has also some other features. In CAMAC systems where the response line BX is already implemented, the corresponding signal can be used to gate BTB in such a way, that SSYN is suppressed if the addressed module fails to respond (time-out). When A00 is asserted (CAMAC control function), BQ is gated via gates 17 and 3 onto the data line D15. So it is possible to test LAM (Look at Me) in the normal way the PDP-11 performs a test. Unfortunately this is not possible for "Test Status", as this CAMAC function has been standardized somewhat illogically with F16="1". The Branch Demand signal BD is inverted by inverter 16 so that it can be used to trigger an interrupt via an M782 Interrupt Control Module.

Minimum PDP-11/CAMAC Interface (1crate)

UNIBUS

PROCESSOR

M782

CRATE CONTROLLER "A"

Integr. circuits
SN 7400 N, SN 7402 N
SN 7404 N, SN 7410 N
SN 7474 N, SP 380 A
MC 858 P

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Some extra gating is required, using gates 1, 5, 7, 8, 23, and 24, because the PDP-11/20 behaves also not completely logical. When a DATO bus cycle is needed, the machine will perform first a DATIP bus cycle, which is unnecessary and in our case can cause errors [x]. So we must suppress this DATIP bus cycle on the CAMAC branch and generate an extra SSYN on the UNIBUS, if the condition (CAMAC addressed). (DATIP). (CAMAC control function) = "1" is fulfilled. In the simplest case: "CAMAC addressed" = "A15 asserted". As the DATIP bus cycle must not be suppressed for normal CAMAC read operations, there are still some difficulties left. A write-only register will not respond to the unwanted DATIP read operation, which precedes the write. To avoid a time-out error the response signal BX must be generated artificially for each DATIP (gates 24, 22). In those CAMAC modules, which are able to execute both F(2) and F(18) at the same subaddress, the register will be cleared unintentionally if F(18) is executed. Avoiding this by means of special circuitry in the interface will cause other difficulties. So it is advisable to avoid such CAMAC modules in connection with the PDP-11/20.

4. Interrupt facilities

The CAMAC interface would be of almost no value without the possibility of program interrupts by L-requests (Look at Me). The L signals are available at the rear connector of crate

[x] According to DEC the other models of the PDP-11 family will not show this extra DATIP.

controller A and can be brought from there to a corresponding number of PDP11 interrupt modules type M782. (As the L signals will be gated off by the busy signal of each dataway cycle, they must be staticised by flipflops to avoid multiple interrupts[x]). This method will lead to a very fast interrupt handling but is quite expensive. For "slow" interrupts it is possible to make a graded-L search by program. Up to 16 module L signals can be "ored" together to cause a common BD (Branch Demand) signal. BD will trigger the L-search routine via an M782 interrupt module. To avoid multiple interrupting by busy gating of the L-signal the branch demand signal BD must be disabled till the L has been found and cleared [x]. Follows an example of such a search routine.

x) This is not necessary if all CAMAC modules in the system conform with the new recommendation of EUR 4100 (72) to maintain each L-signal continuously except during an operation that will cancel it.

```
; GRADED-L SEARCH 22.3.72

            • = 0
            GL = 167400
            LOCAL = .+0
            LOCAH = LOCAL+1
            PIR16 = .+32. ; PIR15=.+30. ,PIR14=.+28. ,....,PIR1=.+2.
            INX = PIR16-OUTA-4
            DISABD = 167521


            • = .+42

    GLS:    CLRB @#DISABD        ; DISABLE BRANCH DEMAND
            MOV @#GL,LOCAL       ; READ GRADED-L PATTERN INTO MEMORY
            BMI OUTB             ; BRANCH IF HIGHEST PRIORITY IS SET
            MOV %0,-(%6)         ; SAVE REGISTERS ON STACK
            MOV %1,-(%6)         ;
            CLR %1              ; PREPARE SHIFT COUNTER
            MOVB LOCAH,%0        ; LOAD R0 WITH HIGH BYTE OF L-PATTERN
            BNE SHIFT            ; BRANCH IF AT LEAST ONE BIT IS SET
            MOV #-8.,%1          ; BUT LOAD -8 INTO R1 IF NONE SET
            MOVB LOCAL,%0        ; LOAD R0 WITH LOW BYTE OF L-PATTERN
            BMI OUTA             ; BRANCH IF HIGHEST PRIORITY
                                 ; OF LOW BYTE IS SET
    SHIFT:  DEC %1              ; R1 COUNTS NUMBER OF SHIFTS (REVERSE)
            ASLB %0             ; SHIFT LOOP SEARCHES FOR L-BIT
            BPL SHIFT           ; BRANCH BACK IF NOT FOUND
    OUTA:   ASL %1              ; MULTIPLY COUNT BY 2 FOR WORD ADDRESS
            ADD %7,%1           ; MAKE ROUTINE POSITION INDEPENDENT
            MOV INX(%1),%7      ; LOAD PC WITH ROUTINE ADDRESS
    OUTB:   MOV PIR16,%7        ; LOAD PC WITH HIGHEST PRIORITY
                                 ; ROUTINE ADDRESS
```

When the interrupting CAMAC module has been identified
it is eventually necessary to search further for the
interrupting subaddress. To have an example for such a
routine we assume that the CAMAC module has several
independent registers, which can be loaded from external
data sources. The contents of these registers shall be
totalized in separate but adjacent memory locations. - At
the end of the routine the processor registers 0 and 1
have to be restored from the stack.

```
; INTERRUPT ROUTINE IR15 15.3.72

            CAF02 = 000004    ; CAMAC F-CODE 2 (READ AND CLEAR)
            CATLAM = 163001   ; CAMAC REGISTER N=12 TEST LAM
            ENABD = 167525    ; ENABLE BRANCH DEMAND
            INX1 = LOC-M-2

IR15:       MOV #CATLAM,%1    ; LOAD R1 WITH CAMAC ADDRESS + F-CODE
            JSR %7,SSR        ; GO TO SUBADDRESS-SEARCHROUTINE
            BIS #CAF02,%1     ; INSERT NEW F-CODE IN ADDRESS FOUND
M:          ADD %7,%0         ; MAKE ROUTINE POSITION INDEPENDENT
            ADD (%1),INX1(%0);  TRANSFER & ADD CONTENTS
                              ; OF INTERRUPTING ADDRESS
            CLRB @#ENABD      ; ENABLE BRANCH DEMAND
                              ; FOR FURTHER INTERRUPTS
            MOV (%6)+,%1      ; RESTORE REGISTERS
            MOV (%6)+,%0      ; FROM STACK
            RTI               ; RETURN TO MAIN PROGRAM
LOC:


; SUBADDRESS-SEARCHROUTINE 22.3.72

            DISABD= 167521
            .= 0

SSR:        MOV #8.,%0        ; LOAD R0 WITH SUBADDRESS-INCREMENT
            BR TEST
LOOP:       ADD %0,%1         ; INCREMENT SUBADDRESS
TEST:       TSTB @%1          ; TEST LOOK-AT-ME
            BPL LOOP          ; BRANCH BACK IF NOT FOUND
            MOV %1,%0         ; LOAD R0 WITH INTERRUPTING ADDRESS
            BIC #177607,%0    ; ISOLATE SUBADDRESS FOUND
            ASR %0            ; AND ADJUST IT AS A
            ASR %0            ; NORMAL WORD ADDRESS
            BIC #10007,%1     ; CLEAR CAMAC FUNCTION CODE
            RTS %7            ; RETURN TO INTERRUPT ROUTINE
```

These examples show clearly the ease of programming
with the proposed addressing scheme. On the other hand
it is evident that a hardware Graded -L   search unit
(LAM-grader) would be 20 to 50 times faster than the
programmed Graded-L search. Thus a LAM-grader
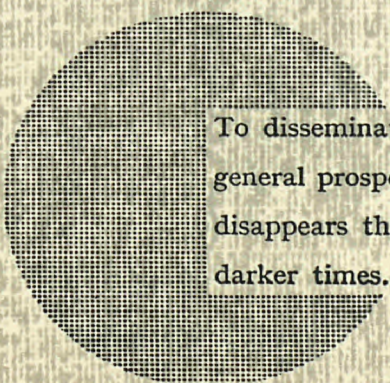(for 24 bits) would be a considerable improvement.

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1.   Direct Connection of CAMAC Crate Controllers
        Type "A" to the PDP-11 UNIBUS.
        by W. Stüber, CAMAC bulletin 4, 1972.

2.   PDP-11 handbook, Digital Equipment Corp.

3.   CAMAC: Organisation of Multi-Crate Systems,
        EUR 4600e.

4.   CAMAC: A Modular Instrumentation System
        for Data Handling, EUR 4100e.

To disseminate knowledge is to disseminate prosperity — I mean general prosperity and not individual riches — and with prosperity disappears the greater part of the evil which is our heritage from darker times.

Alfred Nobel

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