

Atomic Energy of Canada Limited

A REVIEW OF THE CAMAC CONCEPT

by

R. L'ARCHEVEQUE and G. YAN

Chalk River, Ontario

March 1971

AECL-3806

A REVIEW OF THE CAMAC CONCEPT

by

R. L'Archevêque and G. Yan

Electronics Branch

Chalk River Nuclear Laboratories

Chalk River, Ontario

March, 1971

AECL-3806

A REVIEW OF THE CAMAC CONCEPT

by

R. L'Archevêque and G. Yan

ABSTRACT

CAMAC, which is a modular instrumentation system developed under the auspices of the ESONE Committee, is reviewed from the viewpoint of general electronic packaging concepts and described in a format that is readily available to AECL personnel. Its envisaged advantages are evaluated within the framework of present and projected electronic technology for instrument and system applications. The computer independence of CAMAC at the crate level has far reaching implications and is discussed in detail. The viability of the CAMAC Branch as a generalized system approach is also considered.

Chalk River Nuclear Laboratories
Chalk River, Ontario
March, 1971

AECL-3806

Une évaluation du concept CAMAC

par

R. L'Archevêque et G. Yan

Résumé

CAMAC, système d'instrumentation modulaire développée sous les auspices du Comité ESONE, est passé en revue du point de vue des concepts généraux de l'emballage électronique et il est décrit sous une forme facilement accessible pour le personnel de l'EACL. Ses avantages envisagés sont évalués dans le cadre de la technologie électronique présente et future pour des applications d'instruments et de systèmes. L'indépendance de CAMAC vis-à-vis des ordinateurs, au niveau du contenant, a des implications de longue portée et elle fait l'objet d'une discussion détaillée. La viabilité de la Section CAMAC comme système généralisé est également considérée.

L'Energie Atomique du Canada, Limitée
Laboratoires Nucléaires de Chalk River
Chalk River, Ontario

AECL-3806

TABLE OF CONTENTS

	<u>Page</u>
LIST OF FIGURES	
FOREWORD - CAMAC and the General Electronic Packaging Problem	1
1. INTRODUCTION	5
1.1 A Brief Historical Note	5
1.2 The CAMAC Concept	6
2. THE CAMAC SYSTEM	7
2.1 The CAMAC Crate	7
2.2 The CAMAC Multi-Crate Branch	18
3. THE CAMAC SYSTEM IN THE AECL CONTEXT: CONCEPT AND IMPLEMENTATION	30
3.1 CAMAC Crate Usage	31
3.2 CAMAC Multi-Crate Branch Usage	33
3.3 Possible Choices Open To AECL	34
4. CONCLUSIONS	35
5. REFERENCES	36
6. BIBLIOGRAPHY	39

LIST OF FIGURES

	<u>Page</u>
Fig. 1 - Universality of Electronic Packaging Problem	2
Fig. 2 - Schematic Diagram of (a) CAMAC crate and (b) CAMAC multi-crate branch	8
Fig. 3 - Orthographic projection of a CAMAC crate	9
Fig. 4(a) - Pin Allocation at normal station as viewed from rear of crate (adapted from EUR 4100e)	10
Fig. 4(b) - Pin Allocation at control station as viewed from rear of crate (adapted from EUR 4100e)	11
Fig. 5 - Front and side views of a single-width plug-in module	13
Fig. 6 - A summary of Dataway command and control signals (adapted from EUR 4100e)	17
Fig. 7 - Timing of a Dataway operation (Fig. 9, EUR 4100e)	19
Fig. 8 - A possible CAMAC branch arrangement (Fig. 2, ref. 8)	21
Fig. 9 - The CAMAC branch and Dataway Command structures	22
Fig. 10 - A summary of branch highway signal lines (from Table I, ref. 8)	24
Fig. 11 - Sequence of Command Mode Operation (Table III, Ref. 8)	26
Fig. 12 - Sequence of Graded-L Operation (Table IV, ref. 8)	27
Fig. 13 - Timing of Branch Read Operations (Fig. 3, ref. 8)	28
Fig. 14 - Timing of Branch Write Operations (Fig. 4, ref. 8)	29

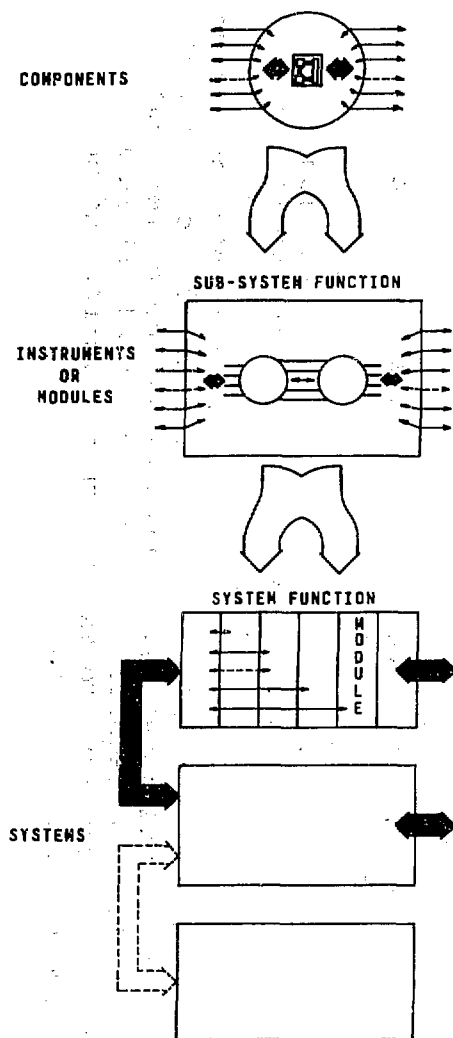
FOREWORD

CAMAC and the General Electronic Packaging Problem

Packaging constitutes today one of the major obstacles to the full realization of modern electronics capabilities^{1,2,3,4}. Present technologies are seriously limited by the inadequacies of packaging approaches at all levels, i.e. components, instruments and systems.

In fact, the problem of packaging is fundamental in electronics and can never be resolved absolutely or permanently as long as technologies continue to evolve or to be replaced by better ones. To be viable, packaging concepts must be adapted closely to current technologies at all levels in order to permit a harmonious combination of all parts in an efficient and economical manner. Due to the rapid changes that have taken place in electronics over the last decade⁵, the field of packaging has been very dynamic and is still in turmoil.

Figure 1 illustrates the universality of the packaging problem in electronics. The figure is grossly oversimplified but it can serve to demonstrate the current capabilities of modern electronics and some corresponding packaging problems. The technical and economic advantages offered by integrated circuits have been described elsewhere⁵ and need not be repeated here. It is therefore assumed in Fig. 1 that the first level of packaging is the monolithic integrated circuit and a complex MSI or LSI chip is referred to as a component. It should be noted, however, that the starting point is rather irrelevant to the argument since any significant change in the technology at a given level causes a relative shift at other levels without affecting the overall pattern. To illustrate this fact it is sufficient to remember that the functional complexity of an MSI or an LSI component is equivalent to what would have been found in a complete instrument or a system only a few years ago. Regardless of the functional complexity of the new components, designers find good reasons for interconnecting more than one into modules or instruments and for combining these units into systems. Consequently, no matter what is the starting technology, the three levels shown in Fig. 1 will continue to exist with the corresponding interconnection problems.



TECHNOLOGY	CURRENT LEVEL OF TECHNOLOGY	ULTIMATE LIMIT
ANY MONOLITHIC TECHNOLOGY	<ul style="list-style-type: none"> - MSI AND LSI - MANY COMPLEX FUNCTIONS SAY 100 TO 1000 GATES - 4 TO 5 LAYERS OF INTERNAL CONNECTIONS - 40 OR MORE EXTERNAL CONNECTIONS 	THE OPTIMUM PARTITIONING
ANY HYBRID TECHNOLOGY	<ul style="list-style-type: none"> - PRINTED CIRCUIT BOARDS (14 TO 15 LAYERS OF INTERNAL CONNECTIONS) - THICK FILM (13 TO 15 LAYERS) - THIN FILM (2 TO 5 LAYERS) 	DEPENDS ON OUR ABILITY TO CONNECT RELIABLY AND ECONOMICALLY MANY ELEMENTS WITHIN A UNIT AND TO INTERCONNECT MANY
	<ul style="list-style-type: none"> - DATAWAY - DAISY CHAIN - NIM - CAMAC - VARIOUS COMPUTER AND HARDWARE SYSTEMS 	UNITS TO FORM THE NEXT LEVEL

FIG.1 UNIVERSALITY OF ELECTRONIC PACKAGING PROBLEM

It should be realized, of course, that Fig. 1 is concerned only with the "interconnection" aspect of the general packaging problem and does not take into consideration many other functions of packages such as protection from the environment, heat dissipation, etc. These various other aspects however would not affect the present argument.

It can be seen from Fig. 1 that at all three levels, i.e. components, instruments and systems, two categories of connections must exist: the internal connections between elements in a package and the external connections to the outside world. The maximum practical number of both types of connections impose serious design limitations at all three levels. Ideal partitioning would permit optimum trade-off between internal and external connections at all levels. At the component level, for instance, as the chip functional complexity is increased, the number of external connections may decrease within certain limits but the number of internal connections increases. A similar situation exists with complete instruments and systems.

For the present arguments, a "module" or an "instrument" is defined as a combination of two or more "components" into a unit capable of performing a sub-system function and having adequate means of communicating with the outside world. Similarly, a system is a combination of two or more "modules" performing a system function and providing adequate means of communicating with the outside world.

From these considerations, both NIM and CAMAC approaches would fall into the same general category, both having "modules" that can be combined into "systems". However, there are some important differences between the two schemes.

The NIM approach did not simplify system interconnection problems between modules within a crate except in a very limited way with the power and ground distribution. The few provisions for signal bus lines on the back connector in NIM modules were so restrictive that they offered no help at the system level. In fact, the greatest contribution of the NIM approach to system design has been more mechanical than electrical in that it simplified the building of standard modules and their assembly into crates. The designer still had to devise

some way of interconnecting modules through cables and of communicating with the outside world through similar means. It is also found that NIM modules become inefficient (i.e. empty space with large front and back panels loaded with connectors and switches) as soon as a high level of circuit integration is used. This is an indication that the scheme was conceived for the first generation integrated circuits or even for discrete component designs and becomes "inter-connection limited" when applied to MSI or LSI circuits.

The CAMAC approach offers similar mechanical advantages to NIM but goes one step further in providing a highly sophisticated method of interconnecting modules within a crate. CAMAC still does not ease the problem of communicating with the outside world. In fact, such an approach can only be justified practically and economically if the very complex crate internal connection method is fully exploited. In order to meet this requirement, modules must be built with high density packaging techniques using complex integrated circuits. It also means that front panels must be shrunk to the minimum width, thus eliminating most switches and old time displays whenever possible and imposing serious restrictions on the size of connectors and cables to the outside world. The real significance of the efficiency argument can be illustrated with reference to a digital multiplexer unit being designed in the Electronics Branch. This unit will permit the SUCCESS I computer system to communicate with up to 128 groups of 12 input data lines and as many output ones. If current packaging methods were used to build modules with first generation integrated circuits, at least six CAMAC crates would be required for a complete multiplexer unit. The system would become so expensive that building it in CAMAC crates would be out of the question. On the other hand, if the full capability of the crate internal connection scheme were utilized and multifunction single-width modules could be assembled, less than one fifth of a crate would be sufficient for a complete multiplexer unit. It can be seen that the cost of the crate internal connections and associated hardware would then become negligible. In practice, however, more modules would be needed since communication with the outside world would require over 700 contacts per module if the minimum number were used. The system designer is obviously back to the familiar internal/external connection trade-off.

In the light of these considerations, it is possible to evaluate the CAMAC approach in a meaningful context.

1. INTRODUCTION

Recently, the CAMAC system has aroused the strong interest of people involved with nuclear instrumentation in American laboratories. Active research and development work on the CAMAC modular system have been going on for a few years in most of the nuclear establishments in Europe and the United Kingdom. While up until now Atomic Energy of Canada Limited has not undertaken any program to develop or to utilize the CAMAC scheme, the Electronics Branch at CRNL has kept in close contact with the principal laboratories involved in developing the system. As the number of AECL employees interested as users or designers of CAMAC is expected to grow, a need for a concise report on the current status of the system has become urgent. The objectives of this report are as follows: (a) to summarize and to discuss the important features of CAMAC in a format that is easily accessible to AECL personnel, and (b) to evaluate the potentialities and limitations of CAMAC in the light of AECL requirements.

1.1 A Brief Historical Note

CAMAC is the result of collaborative efforts of European laboratories, under the ESONE (European Standards Organizations on Nuclear Equipment) committee, in defining a modular system for electronic instrumentation. Originally called IANUS⁶, CAMAC is a palindrome, signifying the dual role of CAMAC units that must look into the direction of both the computer and the experimenter. Apart from this, the word CAMAC does not appear to have any other meaning.

CAMAC is organized in two levels of sophistication - the "crate" level and the "multi-crate branch" level. The description and specification of a CAMAC crate was published in March 1969⁷ while a preliminary draft on the organization of multi-crate CAMAC systems was issued in September, 1970⁸.

In March 1970, the USAEC NIM (Nuclear Instrument Module) Committee, except for a few minor changes, formally endorsed the CAMAC system as contained in EUR 4100e⁹. This endorsement does not imply the outright acceptance of future ESONE recommendations by the NIM Committee. A close working liaison, however, has been established between ESONE and NIM.

The CERN and Harwell laboratories have developed a comprehensive series of CAMAC hardware (see Bibliography). However, in the process of building multi-crate systems, these laboratories have developed different styles of crate and system controllers, manual controllers, interfaces and command modules¹⁰. In the United States, modules have been designed to CAMAC specification and are being used by Stanford Linear Accelerator Centre, National Argonne Laboratories, Yale and Lawrence Radiation Laboratories¹¹. In England, CAMAC modules are commercially manufactured by Nuclear Enterprises Ltd. and by the Dynatron Division of EKO Electronics, Ltd. There are indications that European subsidiaries of American computer and instrumentation manufacturers like Digital Equipment Corp. (DEC), Hewlett-Packard and Data General are prepared to offer standard CAMAC interfaces*.

1.2 The CAMAC Concept

CAMAC is basically a modular instrumentation scheme aimed at facilitating the assembly of data gathering and processing systems from standard building blocks. The idea behind the CAMAC system was the establishment of interfacing standards with the intention of alleviating incompatibility problems between computers and peripherals. Attendant with system standardization are potential availability of economically mass-produced units, interchangeability of units between different laboratories and more efficient use of equipment funds. An attractive feature of CAMAC, at this stage, may well be its claim to be "computer independent". If this claim were realized a computer-based system could be designed using CAMAC without reference to a computer except in the design of a specific interface. The overall efficiency of such a system is uncertain. However, the CAMAC approach can also be considered on its own merits quite independently of the presence of any computer, i.e. "the use of a computer is entirely optional and no part of this (CAMAC crate) specification depends upon its presence in the system"¹².

*DEC has indicated that it will build couplers for PDP-11 or PDP-15 computers on special order.

In considering the CAMAC system then, the issues at hand are whether the purported advantages of system standardization and computer independence are fully realizable or not. As the claim that CAMAC is computer independent has far reaching implications in the design of future instrumentation systems, this aspect will be dealt with in greater detail after a description of the CAMAC system is given.

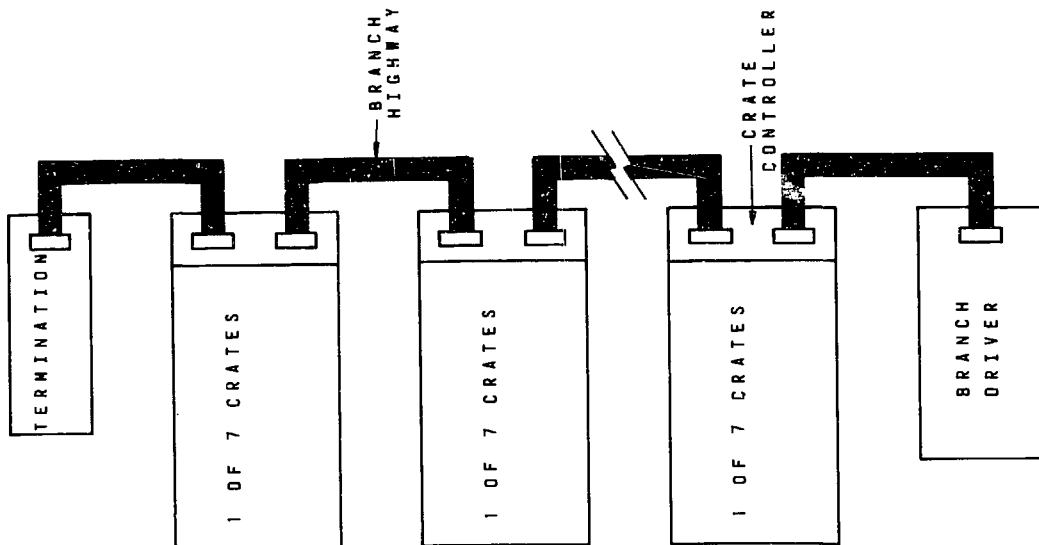
2. THE CAMAC SYSTEM

As mentioned, the CAMAC system is organized in "crates" and in "multi-crate branches". Figure 2 shows a schematic diagram of a CAMAC crate and a multi-crate branch. These two parts of CAMAC are described separately in the subsequent sections.

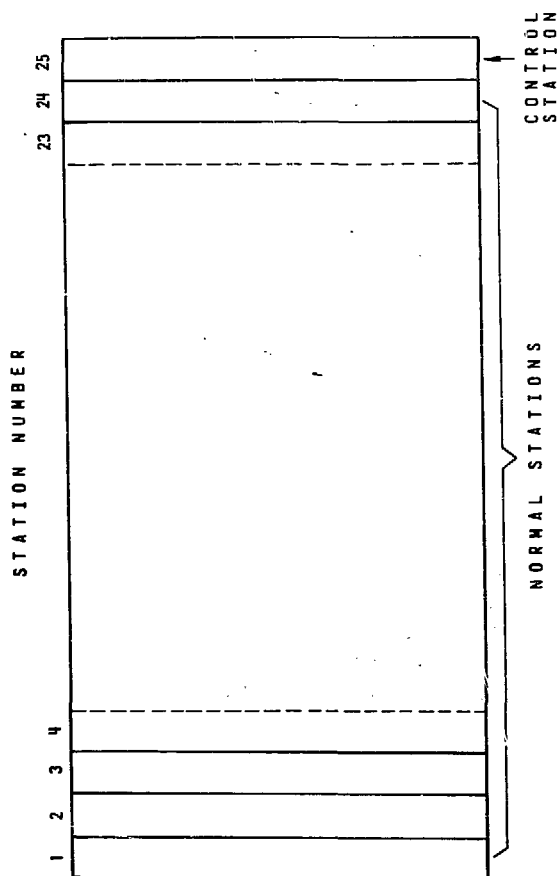
2.1 The CAMAC Crate

The following is a brief summary of the specification of a CAMAC crate together with explanatory comments. Since the crate specification may change as a result of feedback from users^{13,14}, the most up-to-date official reports should be consulted for future revisions.

Figure 3 shows the diagram of a CAMAC crate. Each crate contains 25 separate double-layer 43-pin (86-pin total) plug-in sockets. Each socket position is called a "station" in a crate. Viewed from the front, the stations are numbered from left to right starting with "normal stations" 1 to 24 and ending with station 25, which is the "control station". The stations are interconnected by an 86-line "Dataway". The Dataway consists mainly of bus-lines linking corresponding pins at all normal stations and, in certain cases, the control station. In addition, individual look-at-me and address lines connect each normal station to the control station. Digital data, control signals and power are all conveyed by the Dataway according to a set of rules to be described later. The pin allocation of a normal and a control station are given in Figs. 4a and 4b, respectively. A "crate controller" is needed to link the control station to the normal station bus lines. It must therefore be plugged into the control station and must have access to a normal station. When circuit complexity requires it, the "crate controller" may occupy more than

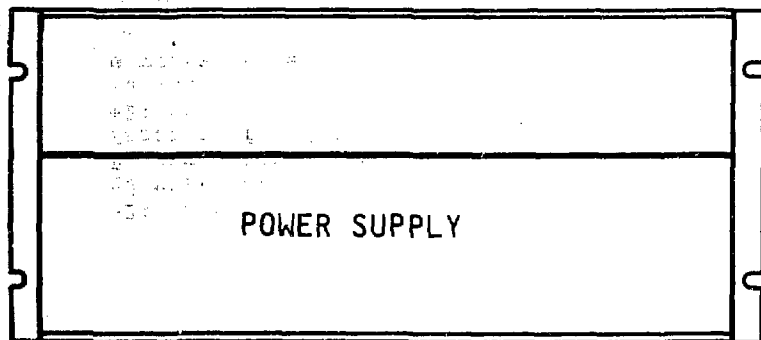


(b)

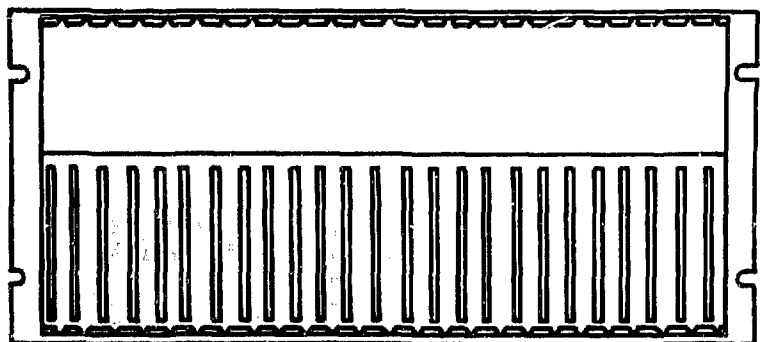


(a) FRONT VIEW

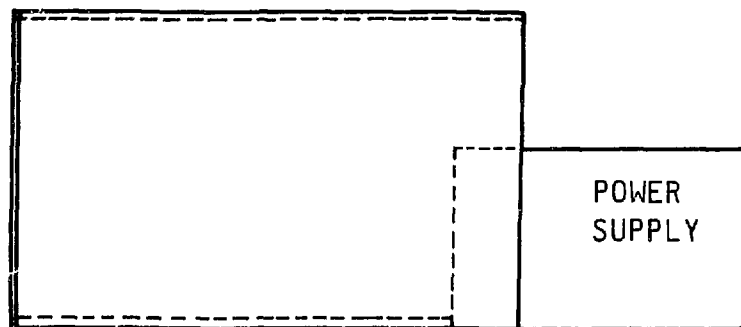
FIG. 2 SCHEMATIC DIAGRAM OF (a) CAMAC CRATE AND (b) CAMAC MULTI-CRATE BRANCH



REAR VIEW



FRONT VIEW



SIDE VIEW

FIG. 3 ORTHOGRAPHIC PROJECTION OF A CAMAC CRATE

Function			Pin No.	Designation		Pin No.	Function		
Busy	-	Bus Line	2	B	P1	1	Individual Patch Point		
Function	"	"	4	F16	P2	3	"	"	"
"	"	"	6	F8	P3	5	"	"	"
"	"	"	8	F4	P4	7	"	"	"
"	"	"	10	F2	P5	9	"	"	"
"	"	"	12	F1	X	11	Bus Line - Reserved		
Sub-Address	-	"	14	A8	I	13	"	"	with Patch Point- Inhibit
"	"	"	16	A4	C	15	"	"	" - Clear
"	"	"	18	A2	N	17	Individual Lines { - Station Number		
"	"	"	20	A1	L	19	with Patch Points { - Look-at-Me		
Initialise	"	"	22	Z	S1	21	Bus Line - Strobe 1		
Response	"	"	24	Q	S2	23	Bus Line - Strobe 2		
			26	W23	W24	25	24 Write Bus Lines		
			28	W21	W22	27			
			30	W19	W20	29			
			32	W17	W18	31			
			34	W15	W16	33			
			36	W13	W14	35			
			38	W11	W12	37			
			40	W9	W10	39			
			42	W7	W8	41			
			44	W5	W6	43			
			46	W3	W4	45			
			48	W1	W2	47			
			50	R23	R24	49	24 Read Bus Lines		
			52	R21	R22	51			
			54	R19	R20	53			
			56	R17	R18	55			
			58	R15	R16	57			
			60	R13	R14	59			
			62	R11	R12	61			
			64	R9	R10	63			
			66	R7	R8	65			
			68	R5	R6	67			
			70	R3	R4	69			
			72	R1	R2	71			
-24 volts D.C.			74	-24	-12	73	Reserved for -12 volts D.C.		
-6 volts D.C.			76	-6	+200	75	Reserved for +200 volts D.C.		
Reserved for 117 volts A.C. Neutral			78	ACN	ACL	77	Reserved 117 volts A.C. Live		
Reserved for Clean Earth			80	E	Y1	79	Reserved		
+24 volts D.C.			82	+24	+12	81	Reserved for +12 volts D.C.		
+6 volts D.C.			84	+6	Y2	83	Reserved		
0 volts (Power Return)			86	0	0	85	0 volts (Power return)		

FIG. 4A PIN ALLOCATION AT NORMAL STATION AS VIEWED FROM REAR OF CRATE (ADAPTED FROM EUR 4100e)

Function	Pin No.	Designation	Pin No.	Function
Busy.	2	B	P1	Individual Patch Point
Function	4	F16	P2	" " "
"	6	F8	P3	" " "
"	8	F4	P4	" " "
"	10	F2	P5	" " "
"	12	F1	X	Bus Line -Reserved
Sub-address	14	A8	I	" " with Patch Point-Inhibit
"	16	A4	C	" " " " " - Clear
"	18	A2	P6	Individual Patch Point
"	20	A1	P7	" " "
Initialise	22	Z	S1	Bus Line -Strobe 1
Response	24	Q	S2	Bus Line -Strobe 2
	26	N24	L24	
	28	N23	L23	
	30	N22	L22	
	32	N21	L21	
	34	N20	L20	
	36	N19	L19	
	38	N18	L18	
	40	N17	L17	
	42	N16	L16	
	44	N15	L15	
	46	N14	L14	
	48	N13	L13	
	50	N12	L12	
	52	N11	L11	
	54	N10	L10	
	56	N9	L9	
	58	N8	L8	
	60	N7	L7	
	62	N6	L6	
	64	N5	L5	
	66	N4	L4	
	68	N3	L3	
	70	N2	L2	
	72	N1	L1	
	74	-24	-12	Reserved for -12 volts D.C.
	76	-6	+200	Reserved for +200 volts D.C.
	78	ACN	ACL	Reserved for 117 volts A.C. live
	80	E	Y1	Reserved
	82	+24	+12	Reserved for +12 volts D.C.
	84	+6	Y2	Reserved
	86	0	0	0 volts (Power Return)
<u>24 Individual Station Lines</u>				<u>24 Individual Look-at-Me Lines</u>
-24 volts D.C.				
-6 volts D.C.				
Reserved for 117 volts A.C. Neutral				
Reserved for Clean Earth				
+24 volts D.C.				
+6 volts D.C.				
0 volts (Power Return)				

FIG. 4B PIN ALLOCATION AT CONTROL STATION AS VIEWED FROM REAR OF CRATE (ADAPTED FROM EUR 4100e)

two stations, e.g. triple-width units. It may become a very complex module since it has to supervise all operations on the Dataway and may provide the interfacing between a CAMAC crate and a computer or other external digital processor. Other modules may occupy any of the remaining normal stations. In principle, CAMAC has been designed so that "... a crate and plug-in units can be connected to an on-line digital computer by means of a plug-in unit which adapts the specific computer standards to the Dataway standards"¹². Furthermore, "The Dataway and plug-in units are kept as simple as possible. Any system complexity is introduced between the Dataway and the computer"¹². Thus, the characteristics of a computer must never be reflected beyond the crate controller which serves as an interface between two systems that may have to obey considerably different functional rules.

The dimensions of a typical single-width plug-in unit is shown in Fig. 5. It should be obvious from Fig. 5 that high-density packaging techniques consistent with microelectronic practices are required. Of course, a CAMAC module can occupy more than one normal station, depending upon the unit's complexity.

At least two plug-in units are involved in a typical Dataway operation. One acts as a "controller" and the other as a controlled "module". If only two modules are involved, the controller must occupy the control station. As every normal station is linked to the control station by individual lines, there is no restriction on the number of normal stations and hence modules, that can be simultaneously addressed by the controller. When a plug-in unit that occupies a normal station acts as a controller, it can only address a controlled module via the crate controller. Thus a three-way conversation is established between the controller, the crate controller and the controlled module during a Dataway operation.

During a Dataway operation, the controller issues a command consisting of: a Station Number N (24 individual lines), Sub-address A8, A4, A2, A1 (4 bus-lines), and Function F16, F8, F4, F2, F1 (5 bus-lines). The Station Number identifies the module to be addressed; the Sub-address selects a specific section in a module, e.g. a register within the module, and the function

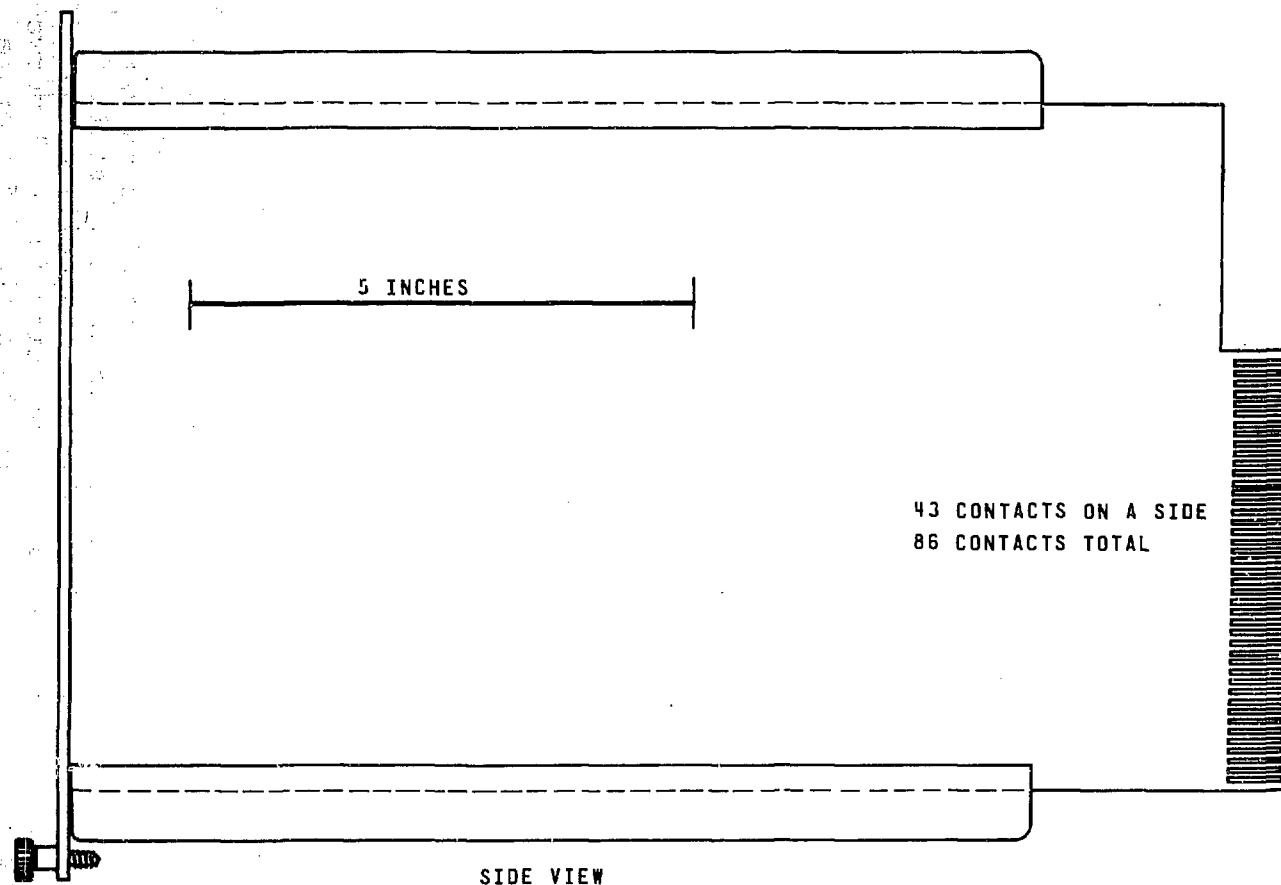
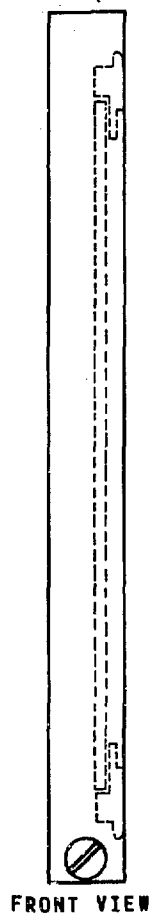


FIG. 5 FRONT AND SIDE VIEWS OF A SINGLE-WIDTH PLUG-IN MODULE

specifies the operation to be performed. The Busy (B) signal, which prevents any other operation on the Dataway, must always accompany a command. There are 32 possible function codes of which 16 have been specified and are mandatory. Full decoding of the function codes in the module is not always necessary, i.e. a module does not require the full five F bits to recognize a command. While some hardware may be saved by this scheme, the gain is often outweighed by the danger of confusion created in a large system. A revision was suggested by the NIM committee wherein full decoding is to be done at all addressed modules¹³.

The term "data" is used to describe all information carried by the parallel highway. Independent Read and Write bus-lines are provided for the bi-directional transfer of data between a controller and a controlled module. Thus a total of 48 data lines are used and the maximum word length during a transfer is 24 bits. The Read lines typically serve a few data receivers (e.g. a controller) and many data sources while the Write lines typically serve a few data sources (e.g. a controller) and many data receivers.

During a Dataway operation, the controller that issues a command must also generate two sequential strobes S1 and S2 on separate bus-lines. Data Transfer or command operation can occur only in response to these strobes. The timing of each Dataway operation is controlled by S1 and S2. The first strobe S1 is used for actions which do not alter the status of the Dataway lines, e.g. read or write operations. Any other action which may alter the status of the Dataway lines must be initiated by strobe S2, e.g. clear write lines. While not stated explicitly in the CAMAC specification, the usages of S1 and S2 suggest that they generally occur in pairs and in sequence. An exception to this rule is during the issuance of an initialize or clear command where the generation of S2 is mandatory while S1 is optional. However, this point is still not fully resolved¹⁵. The CAMAC crate specification does not specify whether or not the time interval between S1 and S2 is a free parameter in the design of a crate controller. Nevertheless, the overall system philosophy and the timing diagram (Fig. 9, EUR 4100e⁷) seem to indicate that the time interval is fixed (300 nsec).

The status of a particular module is conveyed by signals on the Look-at-me L (24 individual lines, one for each normal station), Busy B (1 bus-line) and Response Q (1 bus-line) . Like the N lines, the individual L lines are linked to separate pins at the control station. When no Dataway operation is in progress, any plug-in unit may generate an L signal to indicate that it requires attention. When the Dataway is busy, i.e. a B signal is present, each unit that generates an L signal must gate it off the Dataway; an L signal cannot be initiated when a B signal is present. An undesirable consequence of this arrangement is that no priority interrupt can be raised during a string of operations. This was also recognized by the NIM Committee; an ESONE working group is presently studying this problem¹⁶. If more than one L signal is present in the Dataway, the controller must assign priorities. One design scheme, suggested by ESONE, is to do a sequential search of L sources starting from sub-address 0. For a computer-based system, such a scheme could become unsatisfactorily slow as each station could have up to 16 sub-addresses.

The Busy signal (B) has been mentioned in several situations. The primary function of B is to lock out other operations of a system that can compete for access to the Dataway during a Dataway command or common control operation. The common controls are described later. When B is present, all command and data signals in the Dataway must remain constant with the exception of those data signals which are modified in response to strobe S2. The B signal must be present whenever an N signal is present. Since the B signal may be continuously maintained over more than one Dataway operation, the situation wherein other modules are indefinitely barred from using the Dataway is a possibility, unless adequate precautions are taken.

The Response (Q) signal is used by a module during a Dataway operation to indicate the status of its selected feature. For example, during a read or write operation, the Q signal signifying that the module is ready, must reach a steady-state before S1 is initiated. (It is interesting to note that the Q signal is absent from the diagram on the timing of a Dataway Operation (Fig. 9, EUR 4100e)). The Q signal must remain constant during the entire read or write operation unless the

data source is changed at S2. However, the Q signal may change at any time during all other control commands.

There are three Common Controls that operate on all modules. These controls are Initialize Z (1 bus-line), Inhibit I (1 bus-line with patch points), and Clear C (1 bus-line with patch-points). The Z signal has absolute priority over all other signals or controls. All registers, whether data or control, are set to pre-defined states and all L signals are reset and disabled, where possible, by the Z signal. The unit that generates a Z signal must always cause S2 and B to be generated. As a protection against spurious noise on the Z line, modules that accept Z should gate it with S2. The presence of the I signal inhibits activity in any module selected by the designer. This signal must either not change when B is present, or have rise or fall times not less than 200 nsec. The C signal clears all registers or bistables connected to it. The designer has complete freedom in his use of the C signal. One rule that must be adhered to is that units which generate C must also cause S2 and B to be generated. Modules that accept C should gate it with S2.

The different Dataway commands and controls are summarized in Fig. 6.

The signal and timing standards that are mandatory for Dataway operation, patch pins in the Dataway connector, and auxiliary connectors on the front panel or at the rear panel above the Dataway are described in detail in EUR 4100e; only the salient features are summarized here. It should be noted that the signal and timing standards are not mandatory within units themselves.

The logic signal levels have been defined to agree with those of current-sinking logic devices (e.g. TTL and DTL integrated circuits). Instead of using positive logic, which is the accepted standard for TTL and DTL logic, negative logic (logic "0" is high) is adopted for the reason that an OR configuration is immediately achieved by connecting together the open collector at the outputs of standard logic elements. An OR configuration is essential if more than one unit is to be connected to the bus-lines in the Dataway. Each

Title	Designation	Pins	Use at Module	Direction of Information Transfer	
				Module	Crate Controller
<u>Command</u>					
Station Number	N	1	Selects the module (Individual line from control station).	←	←
Sub-Address	A1,2,4,8.	4	Selects a section of the module.	←	←
Function	F1,2,4,8,16.	5	Defines the function to be performed in the module.	←	←
<u>Timing</u>					
Strobe 1.	S1	1	Controls first phase of operation (Dataway signals must not change).	←	←
Strobe 2.	S2	1	Controls second phase (Dataway signals may change).	←	←
<u>Data</u>					
Write	W1 - W24	24	Bring information to the module.	←	←
Read	R1 - R24	24	Take information from the module.	→	→
<u>Status</u>					
Look-at-me	L	1	Indicates request for service (Individual Line to control station).	→	→
Response	Q	1	Indicates status of feature selected by command.	→	→
Busy	B	1	Indicates that a Dataway Operation is in progress.	←	←
<u>Common Controls</u>					
Initialise	Z	1	Operate on all features connected to them, no command required. Sets module to a defined state. (Accompanied by S2 and B)	←	←
Inhibit	I	1	Disables features for duration of signal.	←	←
Clear	C	1	Clears registers. (Accompanied by S2 and B)	←	←

FIG. 6 A SUMMARY OF DATAWAY COMMAND AND CONTROL SIGNALS (ADAPTED FROM EUR 4100e)

line must also be provided with a pull-up resistor to restore the line to the "0" state in the absence of an applied "1" signal. The pull-up current sources for all bus-lines are to be located in the crate controller. The pull-up for the N and L signals are located in the generator and the receiver of these signals, respectively.

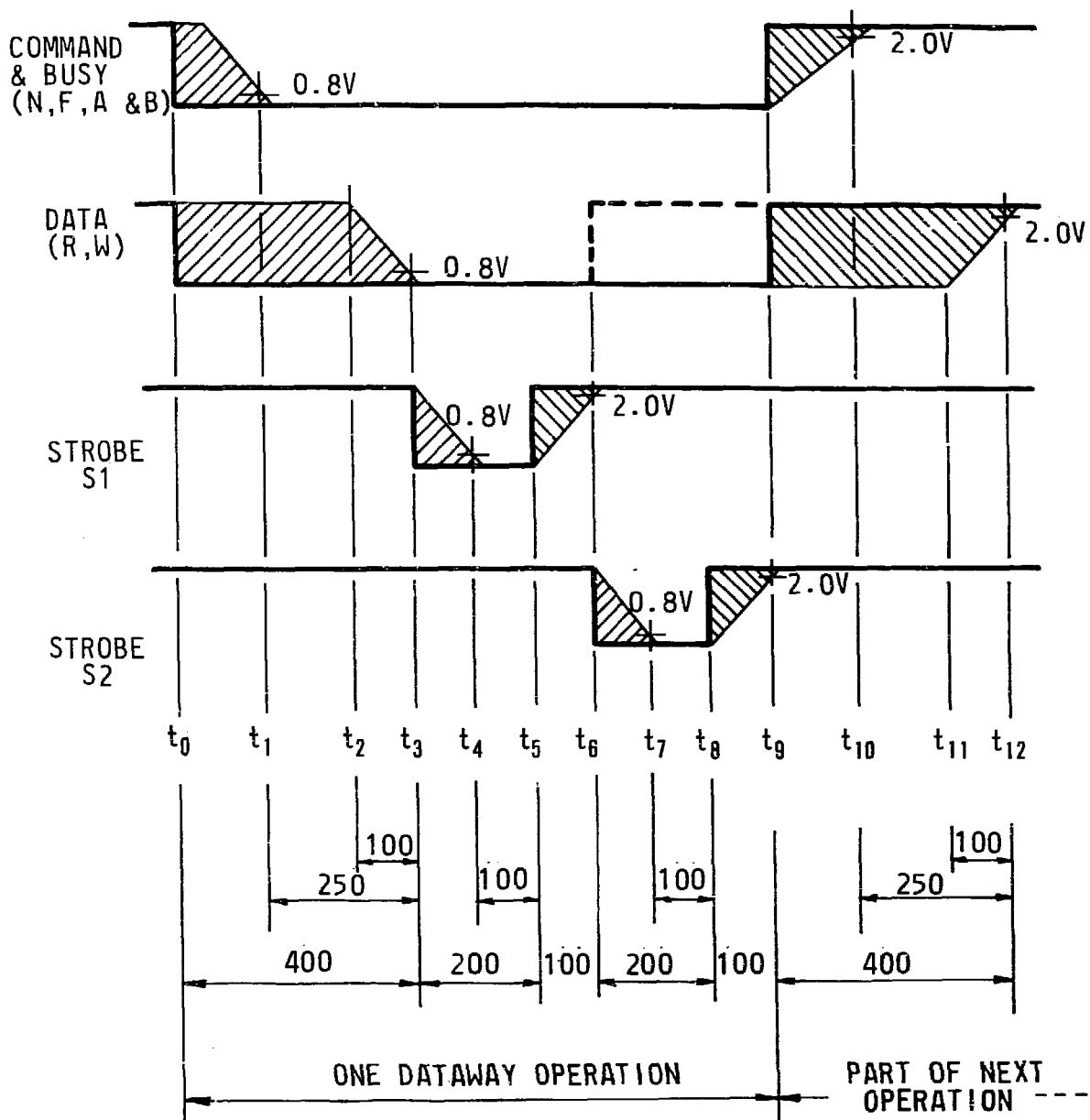
Figure 7 shows the timing sequence of one Dataway operation. The shaded areas indicate the permitted variation of each signal between an ideal square wave and a signal which satisfies the +0.8 V or +2.0 V threshold condition. The Busy and Command signals need not occur in synchronism provided they are within the tolerance limits shown. It can be seen from Fig. 7 that in the worst case, modules must recognize and accept a command within 150 nsec after its generation and must be able to perform the requested operation in response to strobe S1 which may be as narrow as 100 nsec. In other words, if elements with logic delays of 30 nsec were used, no more than 5 logical steps could be cascaded within a module in preparation for a command. In practice this requirement may impose the need for parallel design or for the use of high speed elements.

The mandatory supply voltages are ± 6 Vdc, ± 24 Vdc with maximum current loads of 2A and 1A in a single-width unit and 25A and 6A in a crate, respectively. As a provision for compatibility with NIM modules, ± 12 Vdc and 117 Vac supplies are also available. There is still some controversy over the choice of ± 6 Vdc vis-à-vis ± 5.2 Vdc¹³, but the ESONE committee appears to be satisfied with ± 6 Vdc¹⁶. The user is free to specify the use and locations of remote sensing wires for voltage regulations.

2.2 The CAMAC Multi-Crate Branch

The specifications of the CAMAC multi-crate branch, or simply called "branch", is as yet not finalized. The following summary is based on the Preliminary Issue of the ESONE Committee that is intended for publication as EUR 4600e⁸.

The CAMAC branch consists of up to 7 crates and a "branch driver". All crate controllers and the branch driver are connected to a 132-line "branch highway" by means of standard "highway ports", i.e.



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

FIG. 7 TIMING OF A DATAWAY OPERATION (Fig.9, EUR4100e)

connectors. Each crate controller must have two identical internally-linked ports in order to allow the crates to be connected in a chain configuration as shown in Fig. 2. Another possible configuration of a CAMAC multi-crate branch is as shown in Fig. 8, where the branch driver is not situated at one end of the branch highway. The branch highway lines should be twisted-pair cables, or equivalent, with a characteristic impedance preferably 100Ω but more than 70Ω . All signal lines must be terminated at least at one end of the branch highway; all return lines are grounded at this point. Preferably, the branch highway should be terminated at both ends to minimize line reflections. Appropriate pull-up current sources must be provided at one end of the branch highway in order to be able to restore the lines to the "0" state.

The three modes of operation of the branch are the "Command mode", the "Graded-L mode", and the "Branch Demand". In the command mode, which is the basic one, the branch driver issues a command, consisting of a crate address BCRu ($u = 1, 2, 3, \dots, 7$) (7 individual lines), a crate normal station number BNu ($u = 1, 2, 4, 8, 16$) (5 bus-lines), a station sub-address BAu ($u = 1, 2, 4, 8$) (4 bus-lines), and a function BFu ($u = 1, 2, 4, 8, 16$) (5 bus-lines). Note that apart from BCRu and BNu, the branch command has the same structure as a Dataway command. Upon recognizing a branch command, the addressed crate controller generates a corresponding Dataway command. The CAMAC branch and Dataway command structures are shown in Fig. 9. A branch driver can simultaneously address up to 7 crates. During Read operations data is generated in a module and flows sequentially to the Dataway, the crate controller, to the branch highway and then to the branch driver. During Write operations, the direction of flow is reversed. It should be noted that while the Dataway contains 24 Read and 24 Write bus-lines, the branch highway contains 24 bus-lines that serve for both read and write functions (BRWu ($u = 1, 2, 3, \dots, 24$)). Furthermore a normal station address N is transmitted along the branch highway as a 5-bit code (BNu). As only 23 codes are required to completely specify the normal stations, the remaining 9 codes have been given different assignments (see Table II, ref. 8).

The Graded-L mode (BG) (1 bus-line) is a demand handling signal generated by the branch driver. In this mode, the branch driver addresses all the on-line crates (by the BCR lines) and requests a composite 24-bit data word representing the status of Look-at-me conditions within the branch. The L signals in each crate are graded (processed by the crate controller or by special Look-at-me graders connected to the crate controller) and then presented to any BRW lines. The OR combination of all the Graded-L signals from all crates form the 24-bit Graded-L word on the BRW lines which is then read by the branch driver.

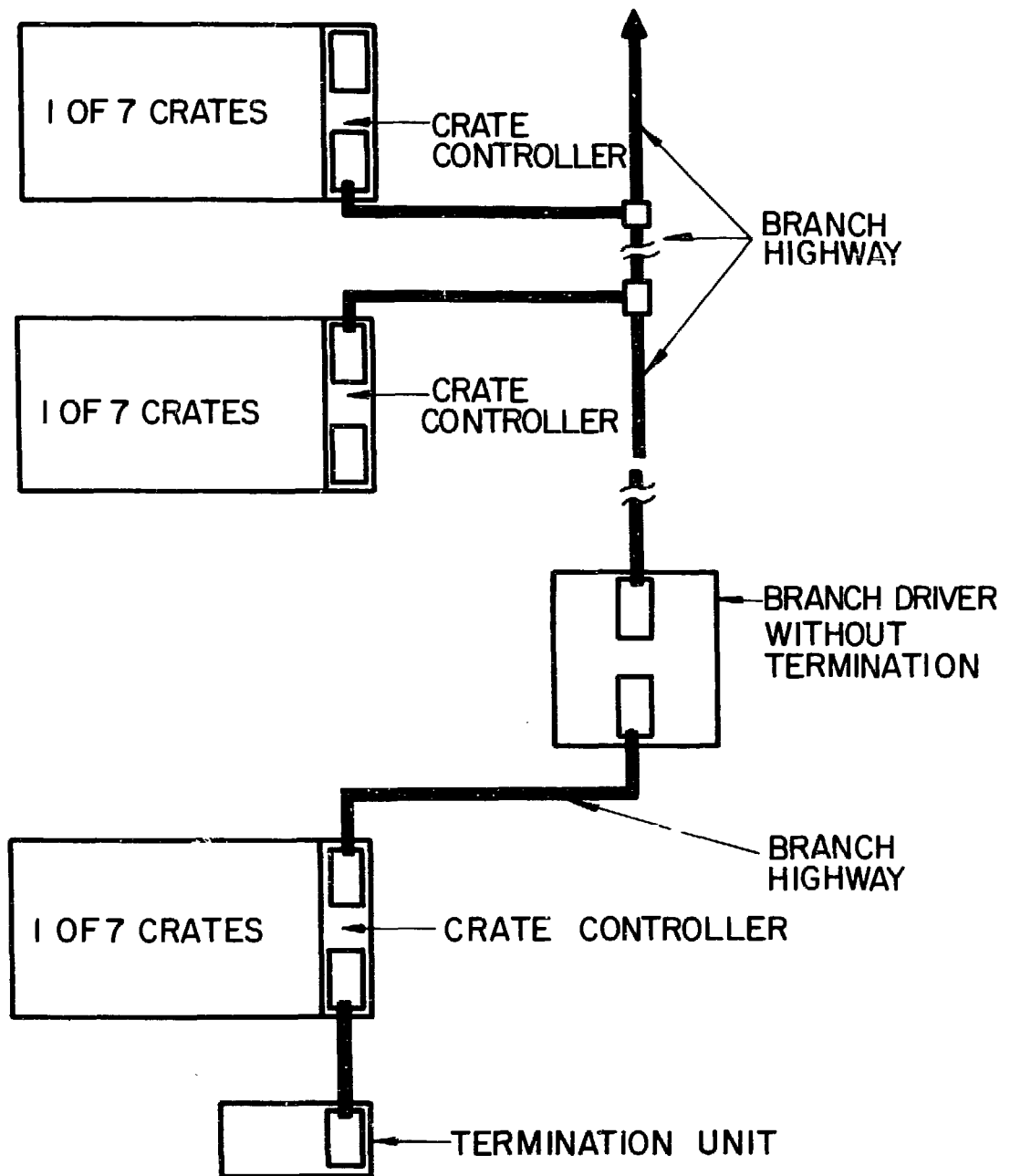


FIG.8. A POSSIBLE CAMAC BRANCH ARRANGEMENT
(FIG.2, REF.8)

(a) Branch command (BC) issued by branch driver.

BCRu	BN	BA	BF
1 of 7 indiv. lines	5-bits	4-bits	5-bits

Crate controller decodes branch command and issues
a corresponding Dataway command.

(b) Dataway command (DC) issued by addressed crate controller.

Nu	A	F
1 of 32 N codes	4-bits same as BC	5-bits same as BC

FIGURE 9 - THE CAMAC BRANCH AND DATAWAY COMMAND STRUCTURES

The Branch Demand BD (1 bus-line) signal is generated by any crate controller signifying that it needs attention. The presence of a BD signal, which may be the result of any logical combination of Look-at-me signals on the Dataway, merely informs the branch driver that one or more crates require attention, without actually having the branch driver identify the crate(s) or perform any operation(s). The crate controller can issue BD at any time independently of the branch timing signals.

The Status BQ (1 bus-line) signal is generated by the crate controller. The BQ signal is the OR combination of Q signals of the addressed crates. An on-line un-addressed crate controller and an off-line crate controller must maintain BQ = 0. When a crate controller is on-line and addressed, it shall respond by setting BQ = 1 only when the Q signal from the addressed module within its crate is recognized to be "1".

There is only one branch common control signal. This is the Branch Initialize BZ (1 bus-line) and it is generated by the branch driver. The BZ signal has absolute priority over all branch signals; it does not make use of the normal branch timing signals. As a protection against short-duration noise, the issuance of BZ = 1 must be maintained for at least 10 μ sec. Furthermore, no Graded-L or Command mode operation must be generated during the following 5 μ sec period.

Upon recognizing a BZ signal whose duration is greater than $3 \pm 1 \mu$ sec, a crate controller must initiate the Dataway initialize (Z), Busy (B) and Strobe (S2) signals as described in Sec. 2.1.

A summary of signal lines at branch highway ports is given in Fig. 10.

The timing of all command mode and Graded-L mode operations is controlled by the branch driver generated signal Timing A BTA (1 bus-line) and by the crate controller(s) generated signal(s) Timing B BTBu, $u = 1, 2, 3, \dots, 7$ (7 individual lines). All off-line or absent crates must maintain BTBu = 0. Each on-line but unaddressed crate must have BTBu = 1. The branch driver maintains BTA = 0 until such time when it puts a command or Graded-L request on the branch highway, in which case BTA = 1. BTA = 1 is maintained until the branch driver has accepted the relevant BRW or BQ signals. Each addressed crate controller sets BTBu = 0 when it has

TITLE		DESIGNATION	GENERATED BY	SIGNAL LINES	USE
COMMAND	CRATE ADDRESS	BCR1 - BCR7	BRANCH DRIVER	7	EACH LINE ADDRESSES ONE CRATE IN THE BRANCH
	STATION NUMBER	BN1,2,4,8,16	" "	5	BINARY CODED STATION NUMBER
	SUB-ADDRESS	BA1,2,4,8	" "	4	AS ON DATAWAY A LINES
	FUNCTION	BF1,2,4,8,16	" "	5	AS ON DATAWAY F LINES
DATA	READ/WRITE	BRW1 - BRW24	BRANCH DRIVER (W) OR CRATE CONTROLLER (R, GL)	24	FOR READ DATA, WRITE DATA, AND GRADED-L
STATUS	RESPONSE	BQ	CRATE CONTROLLER	1	AS ON DATAWAY Q LINE
TIMING	TIMING A	BTA	BRANCH DRIVER	1	INDICATES PRESENCE OF COMMAND, ETC.
	TIMING B	BTB1 - BTB7	CRATE CONTROLLER	7	EACH LINE INDICATES PRESENCE OF DATA, ETC., FROM ONE CRATE CONTROLLER
DEMAND HANDLING	BRANCH DEMAND	BD	CRATE CONTROLLER	1	INDICATES PRESENCE OF DEMAND
	GRADED-L REQUEST	BG	BRANCH DRIVER	1	REQUESTS 'GRADED-L' OPERATION
COMMON CONTROLS	INITIALISE	BZ	BRANCH DRIVER	1	AS ON DATAWAY Z LINE
SPARE	RESERVED	BX1 - BX9	-	9	FOR FUTURE REQUIREMENTS

FIG. 10 A SUMMARY OF BRANCH HIGHWAY SIGNAL LINES (from Table 1, ref.8)

initiated a Dataway operation and established Read-data on branch highway or Write-data on Dataway, or established Graded-L information on branch highway. Thus, the branch operates in a "shake hand" mode.

The timing of a branch operation is adjusted for delays as the delays encountered by the BTA and BTB_i signals are always taken into account. There may exist differential delays (skews) between BTA and the individual 15 bits of branch command and 24 bits of Write-data received at the crate controller. Similarly, there may be skews between BTB and the individual 24 bits of Read-data and 1 bit of BQ signal received at the branch driver. To compensate for the possible skews, the branch driver must introduce an appropriate delay before generating BTA = 1, and must also delay its internal action in response to BTB = 0.

Each branch operation is divided into four "phases" as defined in Figs. 11, 12, 13 and 14. The description of the four phases are given as follows:¹⁷

"During Phase 1 the branch driver presents at its port either a command (together with Write-data if required by the command) or a Graded-L Request and crate address. After a delay which compensates for signal skew it generates BTA = 1 to start the next phase.

During Phase 2 each addressed crate controller responds to BTA = 1 either by initiating the Dataway operation required by the command and presenting any resulting Read-data and Q response at its port, or by presenting Graded-L information. It then generates BTB_i = 0 (BTB_i in this report) on its individual BTB line. The branch driver starts the next phase when it has received BTB_i = 0 from all addressed crate controllers.

During Phase 3 the branch driver introduces a delay to compensate for signal skew and then accepts the Read-data and Q response or Graded-L information. It generates BTA = 0 to start the next phase.

During Phase 4 each addressed crate controller responds to BTA = 0 either by completing the Dataway operation and removing any Read-data and Q response which it has been presenting at its port, or by removing the Graded-L information. It then generates BTB_i = 1 on its individual BTB line.

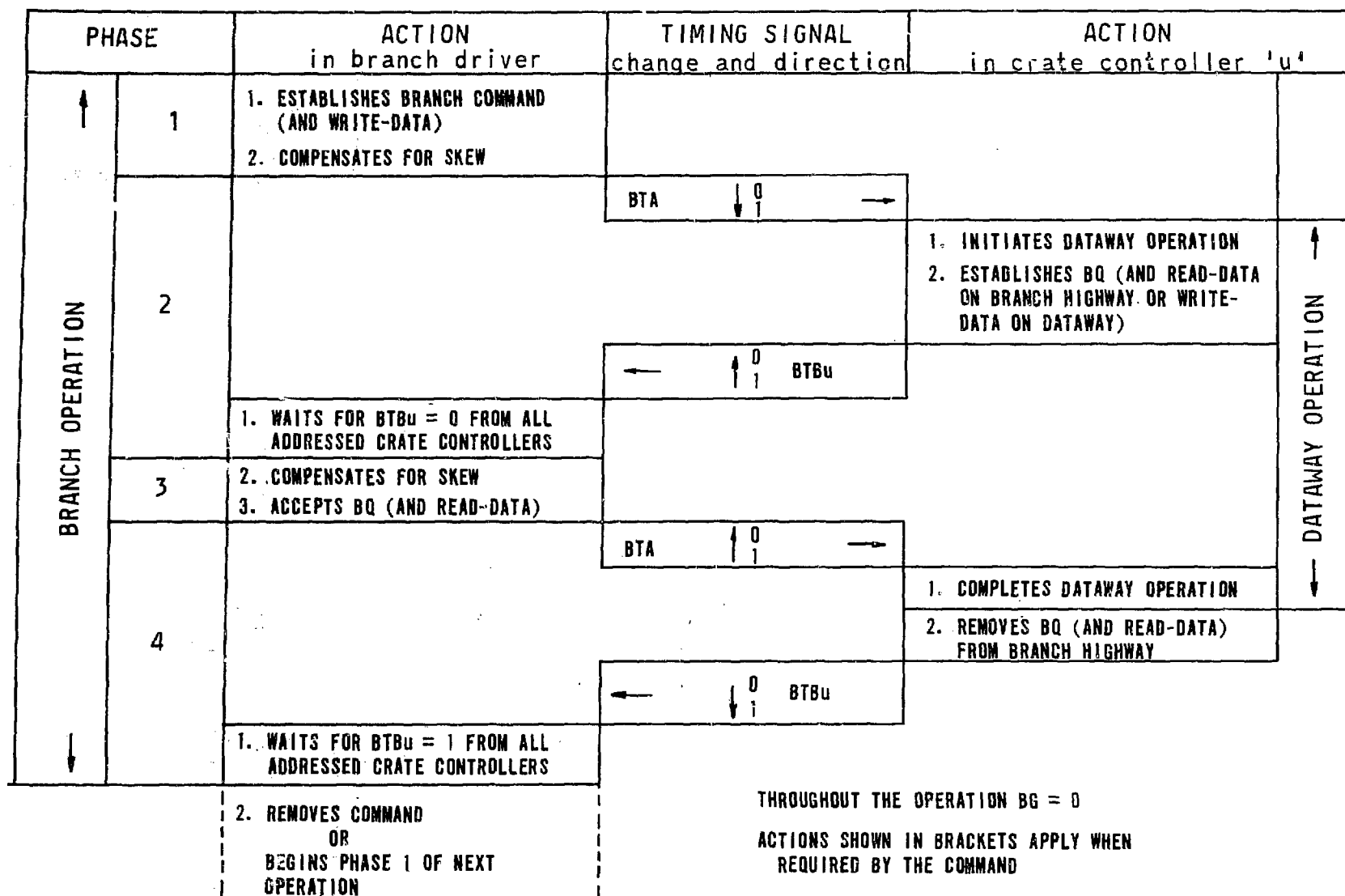


FIG. 11 SEQUENCE OF COMMAND MODE OPERATION (Table III, ref.8)

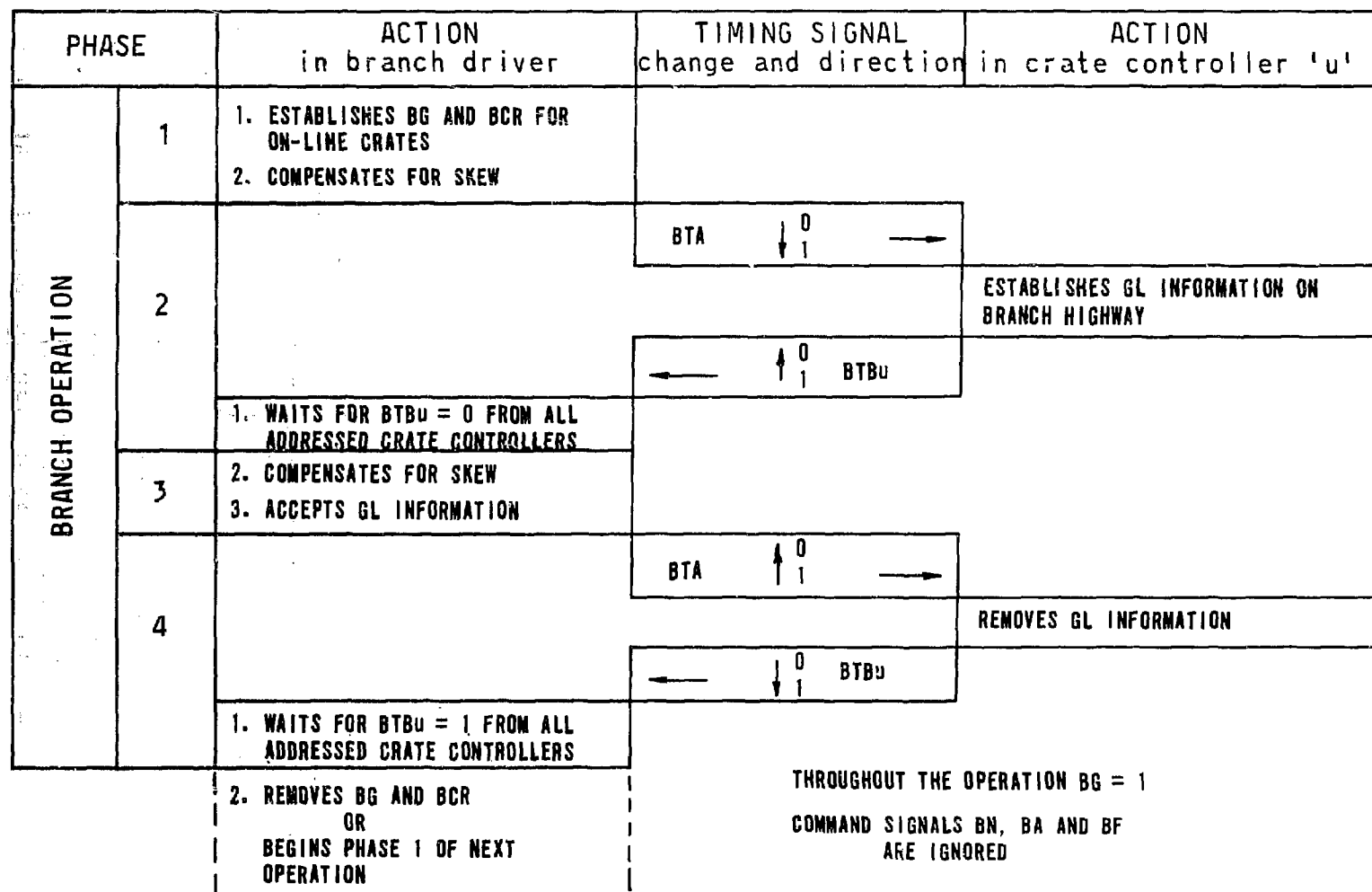


FIG. 12 SEQUENCE OF GRADED-L OPERATION (Table IV, ref.8)

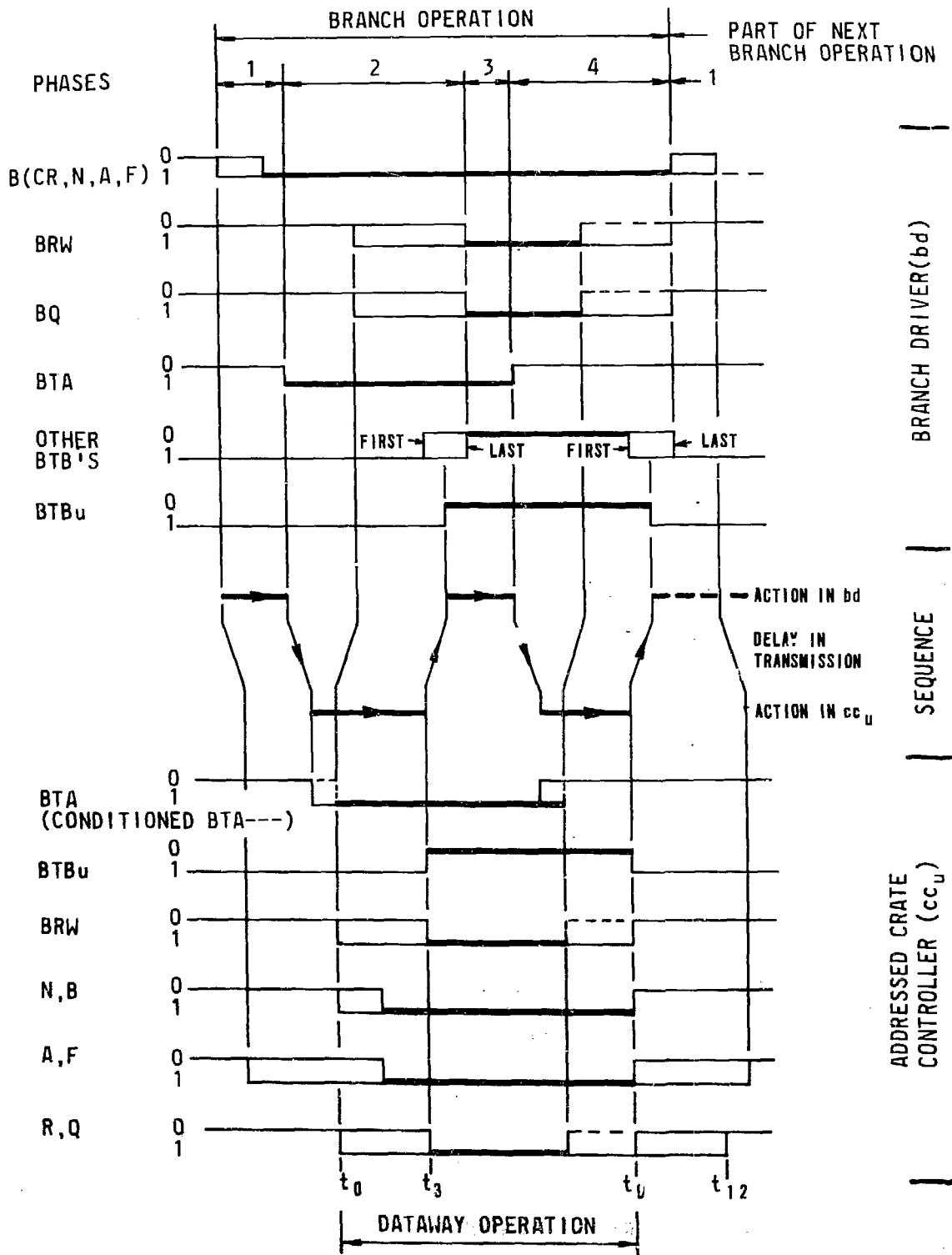


FIG. 13 TIMING OF BRANCH READ OPERATION (Fig.3,ref.8)

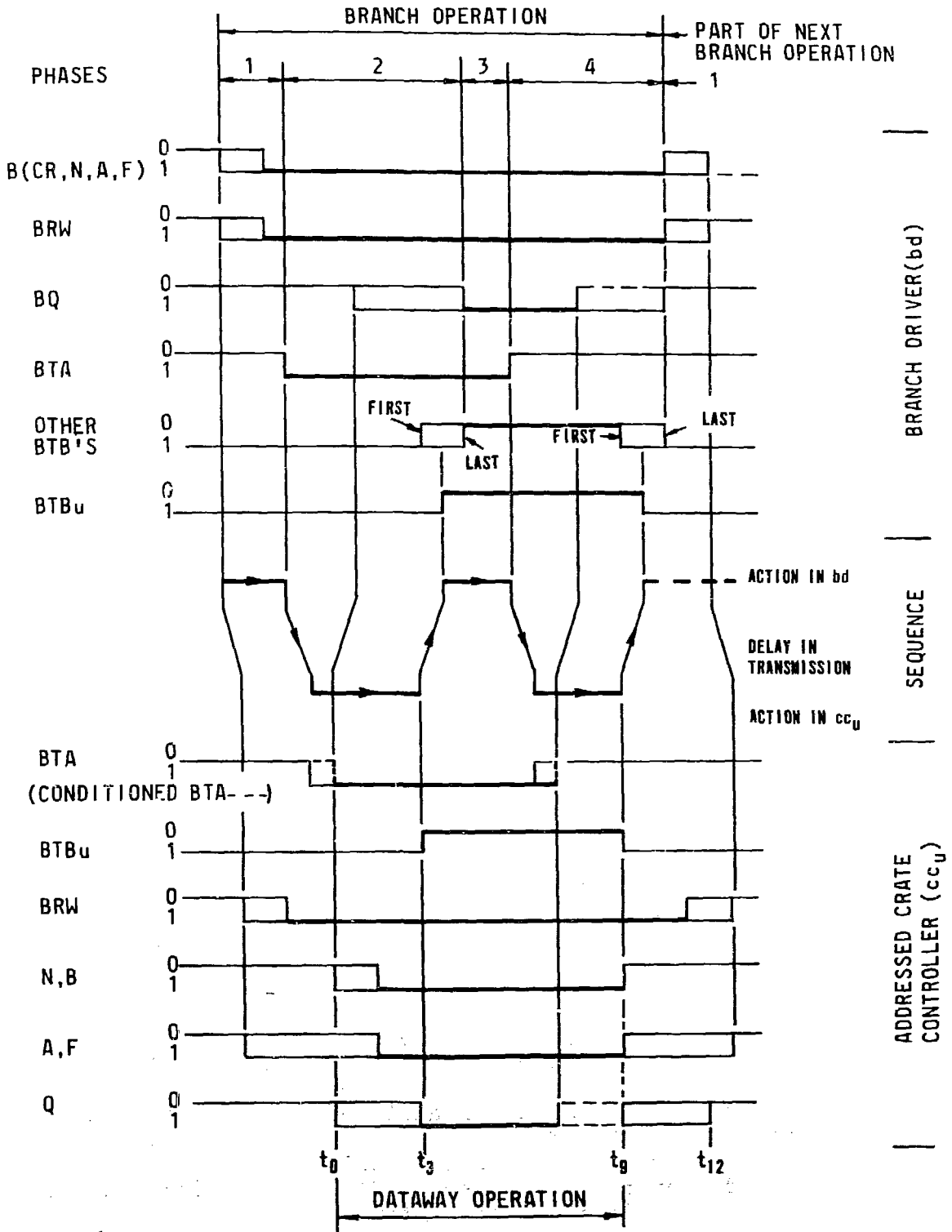


FIG. 14 TIMING OF BRANCH WRITE OPERATION (Fig.4,ref.8)

The branch driver ends Phase 4 when it has received $BTB_i = 1$ from all addressed crate controllers, and is then free to begin another branch operation, either immediately (in which case new command, Write-data, or Graded-L Request signals are set up) or later (in which case the existing signals may be removed)."

3. THE CAMAC SYSTEM IN THE AECL CONTEXT: CONCEPT AND IMPLEMENTATION

After pointing out the endorsement of CAMAC by NIM, of which AECL is a member, and following a summary of the system's specification, it is worthwhile defining the possible attitudes that AECL can adopt with regard to CAMAC.

As in any engineering study, a careful scrutiny of CAMAC requires an examination of two interrelated but distinct aspects: the validity of the approach in terms of general instrumentation and system design concepts and the practical implications to both designers and users. The former aspect will be discussed first.

To recapitulate, the principle underlying the CAMAC approach is the establishment of interfacing standards with the aim to alleviate incompatibility problems between computers and peripherals and to facilitate the assembly of hardware systems from standard building blocks. A very important feature of these interfacing standards is that their specification is entirely independent of any given computer, i.e. CAMAC is "computer independent". There is no doubt that, from an engineering viewpoint, standardization is always attractive for it can allow more efficient information exchange, better documentation and, in certain cases, economic gains as a result of mass production. To the user, standardization could also lead to easier training of personnel, simpler fault diagnosis and maintenance, reduced down-time due to availability of interchangeable units and wider choice of compatible units from different manufacturers. To the designer, standardization means the elimination of many chores normally associated with each design and allows him to concentrate on more creative work. These advantages of CAMAC will be more readily achieved if it finds wide enough support. There are indications that most nuclear laboratories subscribe in principle to the CAMAC concept and that the wider use of CAMAC-specified nuclear instruments is a distinct possibility in the near

future. While CAMAC "is not restricted to nuclear instrumentation"¹⁸, it was conceived in nuclear laboratories and many modules will either be designed particularly for, or by, nuclear laboratories. Since nuclear instrumentation represents but one sector of the general field of electronic applications, it cannot be assumed that the impact of CAMAC in other sectors, e.g. computers, industrial controls, etc., will necessarily follow the trend of the nuclear field. It should be remembered that large manufacturers of systems and computers have traditionally tended to adopt their own standards.

The claim that CAMAC is "computer independent" requires closer attention. To say that CAMAC is "computer independent" would naturally lead to the questions: (a) "What is a computer?", (b) "In what way(s) is CAMAC independent of a computer?". The contextual use of "computer" in the CAMAC specification suggests a digital computer with the basic organization containing input-output units, a memory unit, a processing or arithmetic unit and a control unit. These units obey a set of prescribed rules peculiar to the computer.

To better answer question (b) CAMAC is discussed again separately in the crate and in the multi-crate branch levels. From the discussions, some insight in possible ways of applying CAMAC may be gained.

3.1 CAMAC Crate Usage

A CAMAC crate can be used with or without a computer. In the absence of a computer, the crate controller is entirely responsible for supervising every Dataway operation. Examples of computer independent controllers are manual controllers for checking individual modules, controllers that can accept and read from a limited number of modules, and programmed controllers that contain some control programs. Generally, these controllers can only perform specific tasks and are of limited use as general purpose units. Nevertheless, the merits of such controllers should not be overlooked for they can be economical and perfectly adequate in performing specialized functions. In order to have a general purpose crate controller, it must contain features usually found in small computers¹⁹. In that sense, to say that CAMAC is "computer independent" is a moot point. Certainly, a computer is an optional adjunct to CAMAC if a CAMAC crate, by itself, operates very much like a small computer. Conceivably, a computer could even be connected to the crate as one of the peripherals. In the present state of our technology, the overall efficiency of such an arrangement is suspect and most likely would be low.

In a computer-based system, i.e. one in which a computer plays an important part, the implications of CAMAC's computer independence are far reaching. The characteristics of the computer must not be reflected in the Data-way or in any of the modules. The interfacing is done between the crate controller and the computer. Should it ever occur that the CAMAC crate is to be used with another computer, one merely has to redesign another interfacing unit and the entire CAMAC crate can be transferred to the other system.

The design of this interfacing unit involves the intimate matching of two parts of a system that obey different sets of rules. Three possible choices are open to the designer: (i) CAMAC rules predominate, (ii) computer rules predominate, or (iii) a compromise between computer and CAMAC rules is established. If CAMAC rules predominate, the interface can be relatively simple and any conflict between the two parts of the system is resolved at the expense of the computer efficiency. This case falls essentially under the non-computer based system category. On the other hand, if the computer predominates and its efficiency is not to be compromised, the concept of computer independence is no longer valid since the crate design must necessarily reflect some of the features of the computer in case of conflicts. Consequently, the only case in which true computer independence could be accomplished is the one in which a happy combination of computer and CAMAC rules could be attained. Ideally, both the computer and the CAMAC crate would communicate via an interface with optimum efficiency. The complexity of the interface would then be directly related to the degree of mismatch between the two sets of rules. However, it may not always be possible for practical and economical reasons to eliminate within the interface all the incompatibilities. The designer is obviously faced with the task of matching two sets of analogous rules that most likely were developed independently while concurrently ensuring that they retain their self-consistency. He must keep in mind the possible restrictions imposed by his design on programmers and users. He must also realize that the cost of CAMAC's generality is an increase in complexity either in hardware or in software or both. Above all, he should ensure that the approach does not compromise the overall system efficiency.

3.2 CAMAC Multi-Crate Branch Usage

As seen in Section 2.2, the branch driver is to the branch highway operations what the crate controller is to the crate Dataway operations. The branch driver, however, is as yet not well defined. Specification of a general purpose Type A crate controller has been published⁶ but no detailed description of a branch driver is available yet.

In principle, a CAMAC branch can be used either in a non-computer system or in a computer-based system. A "non-computer" type branch driver must necessarily contain highly complex circuitry in order to supervise the execution of the various tasks associated with the normal operation of a complete branch, i.e. timing sequences, command functions, demand handling and servicing of a large number of units. The cost of developing, building and testing such a driver, which in fact functionally resembles a computer, would probably be more expensive than buying a field-proven computer. It seems unlikely that non-computer-based CAMAC branches using a number of crates will become practical in the near future.

Computer-based CAMAC branch systems can certainly be designed*. In this case, it may be possible to build a relatively simple branch driver and to depend on the computer to perform the more complex functions. However, due to the universality of the CAMAC approach, a heavy burden would be imposed on the computer in taking care of all branch operations, e.g. BTA and BTB timing, graded-L identification and servicing, and extra restrictions would be placed on programming sequences due to the fact that CAMAC functional rules must be obeyed. Such a system would be difficult to program, would be inefficient and would probably be slow.

A compromise between the two extreme cases mentioned is to have the branch driver function as a sophisticated controller interfaced to a computer. Such a branch driver would have the capability to perform certain specific tasks independently of the computer. The computer would simply initiate these tasks. Since a branch can include as many as 161 modules and a total of 7 crate controllers, the branch driver would have to perform extremely complex functions. Certain tasks, however, could still be directly under the control of the computer.

*DEC has issued a preliminary description of a branch driver that interfaces with their PDP-15 computer.

All the instances described so far are theoretically feasible. In practice, however, it is very difficult to maintain complete universality in such a large system and to avoid building-in special features. It is questionable, then, whether the CAMAC branch approach would still be advantageous. In order to maintain generality at all levels, the designer would have to incorporate more complexity in a CAMAC system than would otherwise be required for a special purpose system. It would result in a more expensive and probably less efficient system to the user. Of course it could be argued that due to CAMAC's modularity, a large system could be assembled from standard building blocks for specific applications, or that a system could be modified readily to meet different requirements. However, one should not underestimate the effort required to develop a sufficiently powerful and general scheme that would permit changing module functions or locations without involving significant alterations in corresponding programs. The designer and the user may still have to pay a high price for features that would be unnecessary in a custom designed system. Experience with Large Scale Integration (LSI), for instance, has shown that the higher the complexity, the stronger the incentive for custom design and the smaller the quantities required. The analogy with the use of CAMAC in large systems may be of some relevance. The solution may not be in total standardization and modularity up to the system level but rather in the improved ability to custom design and build with rapid turnaround time as is being done in LSI. At this stage it is not clear whether the CAMAC Branch Highway will ever make a real contribution as a viable approach to system design. Many difficulties still have to be resolved^{13, 14, 20}.

3.3 Possible Choices Open to AECL

Three practical roles that AECL can adopt with regard to CAMAC are as follows: as an Interested Observer, as a Passive Participant or as an Active Participant. Our activities over the past few years can be described as that of an Interested Observer. We kept abreast with the most recent developments on CAMAC through publications issued by European and U.K. Nuclear Laboratories and by personal contacts. Recently it was felt that due to ESONE's increased experience with CAMAC and NIM's formal involvement, the time was appropriate for us to assume the role of a Passive Participant. The primary objective was to improve our understanding of CAMAC's implications by performing a thorough study of the concept taking into

account the specific requirements of AECL. This report summarizes some of our results. In order to acquire some working experience with CAMAC as an Active Participant, a Data Multiplexer Unit is being designed, by the Electronics Branch, as part of the SUCCESS I Engineering Package. Wider utilization of CAMAC units would presumably follow as our favourable experience with CAMAC system grows. Whether or not CAMAC will significantly influence the future development of instruments and systems at AECL is still uncertain. At this stage, it seems likely that commercial CAMAC modules will be used in the relatively near future. In considering the question, we must look into commercially available systems, while bearing in mind our own experiences in system design in order to define our present and future requirements.

4. CONCLUSIONS

The CAMAC approach is based on a concept of standardization of modular units aimed at lessening incompatibility problems currently faced by designers and users when combining computers, peripheral units and various instruments into systems. A distinct advantage of using a CAMAC crate is the elimination of one level (as defined in the Foreword) of mechanical and cabling designs otherwise necessary in every new system. To exploit the full potential of CAMAC's Dataway, high density microelectric packaging techniques are essential. The commercial availability of standard modules should be realized as soon as CAMAC gains a wider acceptance in Nuclear establishments throughout the world. The future importance of CAMAC outside the nuclear field is still uncertain.

One possible danger of standardization would be that in order to conform with completely general standards, systems may become more complex than would really be needed to perform the intended tasks; this would counteract the cost advantage of buying standard units. To guarantee interchangeability and compatibility with the highly sophisticated Dataway may require more complex and costly hardware in modules which otherwise could be relatively simple. Furthermore, computer operation of a CAMAC crate is likely to result in more cumbersome and lengthier programming sequences. The confusing claim that CAMAC is "computer independent", at the crate level, should be interpreted to mean that CAMAC is a self-contained system which has its own set of functional rules specified independently of any computer. These rules are sufficient to define most functions usually found in small digital computers.

Specifications for the CAMAC multi-crate branch are not finalized. It appears at this stage that the usefulness of CAMAC branches as a general system approach may be debatable. The absolute universality of the branch together with the large system size it implies, may have reached the point where the attendant increase in complexity to maintain standardization at all levels would render the branch unsatisfactory for specific applications. In practice, CAMAC branches would probably be used in relatively large systems where specific requirements are more likely to influence the design, possibly creating incompatibilities with the general operation of the Branch Highway.

In spite of any opinion one might have at this stage, it remains that the viability of the CAMAC approach for modular instruments and systems will be decided in the next few years as a result of the considerable effort presently going on in most nuclear laboratories. The CAMAC rules that have been developed are not always perfectly clear and still require interpretation. To be truly useful, the approach must evolve, through experience, a new, simplified set of rules that will be easier for both designers and users to follow. If in order to keep its generality, the scheme must be complex and vague, it defeats its own purpose. It can only be hoped that, faced with practical applications, the CAMAC approach will not have to degenerate such as to become unnecessarily restrictive.

5. REFERENCES*

1. Proceedings of the Technical Program, National Electronic Packaging and Production Conference, New York, Industrial and Scientific Conf. Management, Inc., Chicago (June 1970).
2. "The Outlook for Electronic Packaging, a 5-Year Forecast", page 173. Electronic Packaging and Production, M.S. Kiver (May 1967).

*ESONE Committee documents available from Secretary, C.C.R., EURATOM, Ispra, Italy.

NIM Committee documents available from Chairman, AEC Committee on NIM, Wash., U.S.A.

CERN-NP CAMAC Leaflets available from Mr. J. Halon, CERN-NP, Geneva, Switzerland.

3. J.J. Staller, "The Packaging Revolution - Part 1: Form and Function Interact", page 72, Electronics, McGraw-Hill (18 October, 1965).
4. J.J. Staller and G. Sideris, "The Packaging Revolution, Part 2: Design and Manufacturing Overlap", page 75, ibid (1 November, 1965).
5. R. L'Archevêque, "The Changing Field of Electronics: A Report on Integrated Circuits and Related Technologies", AECL-3852 (December, 1969).
6. "ESONE System of Nuclear Electronics", EUR 1831e JNRC EURATOM Ispra, Brussels.
7. "CAMAC, A Modular Instrumentation System for Data Handling", EUR 4100e, ESONE Committee EURATOM (March 1969).
8. "CAMAC, Organization of Multi-Crate Systems". Preliminary Issue to be published as EUR 4600e, ESONE Committee EURATOM (September 1970).
9. "Statement of the NIM Committee regarding CAMAC", adopted by NIM, USAEC on March 10, 1970.
10. R.S. Larsen, "Report on ESONE-CAMAC Dataway Working Group Meeting of May 20-22, 1970, London". SLAC, Stanford University, California (June 1970).
11. D.A. Mack, "CAMAC, A Standard for Digital Data Handling", UCRL-20034 Preprint, LRL, University of California, Berkeley (July 1970).
12. "CAMAC, A Modular Instrumentation System for Data Handling", page 2, EUR 4100e (March 1969).
13. "Preliminary Draft Proposals for Discussion - for Revision of CAMAC Specifications", NIM Committee, USAEC (29 September, 1970).
14. "AEC Committee on Nuclear Instrument Modules, Minutes of Meeting held November 4, 1970", (16 November, 1970).
15. Ibid, page A-1.
16. Ibid, page 2.
17. "CAMAC, Organization of Multi-crate Systems", Preliminary Issue to be published as EUR 4600e, page 8, ESONE Committee (September 1970).

18. "CAMAC, A Modular Instrumentation System for Data Handling", page 1, EUR 4100e (March 1969).
19. L.D. Ward, G.S.L. Mitchell and J.M. Richards, "A Programmed Controller in the CAMAC System", AERE-R6334, Harwell (1970).
20. I.N. Hooton, "Further Thoughts on CAMAC Commands", Software Working Group, ESONE Committee, EURATOM (14 August, 1970).

6. BIBLIOGRAPHY

1. A. Lewis, "A Small Computer used as a Multi-Channel Analyzer", AERE-R5844, Harwell (1968).
2. I.N. Hooton, R.C.M. Barnes, "A Standardized Data Highway for On-Line Computer Applications", AERE-R5866, Harwell (1968).
3. R.C.M. Barnes, I.N. Hooton, "The CAMAC System of Modular Instrumentation", Harwell (1969).
4. G.C. Best, I.N. Hooton, "A CAMAC Multi-User System", AERE-R6082, Harwell (1969).
5. R.C.M. Barnes, I.N. Hooton, J.M. Richards, "Data Transfers and Demand Handling in Multicrate CAMAC Systems", AERE-R6214, Harwell (1969).
6. A. Lewis, "Guidelines for a CAMAC Programming Language", AERE-R6266, Harwell (1969).
7. A. Lewis, "Coupling CAMAC to Computers", AERE-R6407, Harwell (1970).
8. H. Bisby, "ESONE Committee Paper, The IANUS System", Harwell.
9. F. Kirsten, "Foreign Trip Report", LRL, Berkeley, California, (8 June, 1970).
10. CERN-NP CAMAC Note 0-01, Review 1 (March 1969).
11. CERN-NP CAMAC Note 1-00, CAMAC CERN-NP Options (December 1968).
12. CERN-NP CAMAC Note 2-00, Crate Controller (January 1969).
13. CERN-NP CAMAC Note 3-00, Executive Controller (January 1969).
14. CERN-NP CAMAC Note 4-00, Display Controller (February 1969).
15. CERN-NP CAMAC Note 5-00, Octal-Decimal Display (February 1969).
16. CERN-NP CAMAC Note 6-00, Print Controller (February 1969).
17. CERN-NP CAMAC Note 7-00, Print Terminal (March 1969).
18. CERN-NP CAMAC Note 8-00, Pattern Unit A (January 1969).

19. CERN-NP CAMAC Note 9-00, Parameter Unit A
(January 1969).
20. CERN-NP CAMAC Note 10-00, Transfer Selector
(November 1969).
21. CERN-NP CAMAC Note 11-00, Miniscaler (February 1969).
22. CERN-NP CAMAC Note 12-00, Binary Display (May 1969).
23. CERN-NP CAMAC Note 13-00, Binary to Decimal Converter
(April 1969).
24. CERN-NP CAMAC Note 14-00, Digest of CERN NP CAMAC
External Control Logic (May 1969).
25. CERN-NP CAMAC Note 15-00, Preset Scaler (May 1969).
26. CERN-NP CAMAC Note 16-00, Microscaler (February 1970).
27. CERN-NP CAMAC Note 18-00, Crate Controller
(January 1970).
28. CERN-NP CAMAC Note 21-00, Systems Controller 1
(January 1970).



**Additional copies of this document
may be obtained from
Scientific Document Distribution Office
Atomic Energy of Canada Limited
Chalk River, Ontario, Canada**

Price - \$1.00 per copy

716-71