REPORT ON
FOUR WEEKS OF INTERNSHIP
carried out at

CoreEL Technologies

Submitted To

NMAM INSTITUTE OF TECHNOLOGY, NITTE
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In partial fulfillment of the requirements for the award of the

Degree of Bachelor of Engineering
in
Electronics and Communication Engineering
by

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Under the guidance of
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CERTIFICATE

This is to certify that the "Internship report" submitted by ***Mr. Bhuvanesh S K*** *bearing USN* ***4NM16EC026*** *of* ***VIII*** *semester B.E., a bonafide student of* ***NMAM Institute of Technology****, Nitte, has undergone four weeks of internship at* ***CoreEL Technologies*** *during June 2019 fulfilling the partial requirements for the award of degree of Bachelor of Engineering in Electronic and Communication Engineering at* ***NMAM Institute of Technology****, Nitte.*

Name and Signature of Mentor **Signature of HOD**

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Certificate of Training & Internship

This is to certify that

Bhuvanesh S K

of

NMAM Institute of Technology

has successfully completed the Internship Program on

Designing with FPGA

held from 3rd June to 3rd July, 2019 at

Sandeepani School of Embedded System Design, Bangalore,

Training Division of CoreEL Technologies (I) Pvt Ltd

Sadiya

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Director – Sales
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CoreEL Technologies

Authorized Training Provider (ATP)

XILINX

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Abstract

The Internship started with brushing up basic concepts of Embedded Systems, Hardware Development languages, different computer architectures, basic concepts related to Field Programmable Gate Arrays (FPGAs), ASICs etc were covered. Different problems and it's solution in verilog HDL was discussed. Introduction Xilinx Vivado Toolkit. Implementation of basic memory cells and switches like FIFOs (First in, First out), RAM (Random Access Memory), Cross Switches were discussed. Then Design and Functional verification of RISC Processor was assigned as the project. The project aims at developing a 16-bit RISC Processor based on Load/Store architecture using FPGA. The system consists of Register Bank, Decoder and Arithmetic and Logic Unit to perform the required operations such as reading/writting, fetching,loading, executing and decoding. The architecture is implemented in Verilog HDL and is realised on Xilinx Zedboard. In Further works custom assembler written in python used to generates input/output coe files, which are fed to Block RAM for testing.

Chapter 1

Introduction to the Industry

CoreEL Technologies is a Customer Application Specific Product and Solutions (CASPS) company offering innovative solutions, ranging across Intellectual Property (IP) cores, Design and Development, System Design and Prototype Development, Next-Gen Digital products, Integrated solutions, Low Volume Manufacturing, System Upgrades and Obsolescence management, EDA tools, COTS products, Semiconductor solutions and Technology Training. It is a leading developer of advanced electronic system level products and solutions to three primary markets – Aerospace and Defence, Digital Media Broadcast and Universities and Institutions of higher learning. Company has deep domain knowledge and expertise in the field of Semiconductors, Embedded Systems, Field Programmable Gate Arrays (FPGA), Radio Frequency (RF) and other forms of Digital systems in the rapidly advancing Electronics sphere.

Sandeepani is the training division of CoreEL Technologies. It is a Technical Finishing School with a focus on VLSI Design and Verification, FPGA Design and Embedded System Design. Sandeepani has trained on advanced topics of HDL Coding, Advanced Verification, Embedded Design and Signal Integrity across various domains as a Xilinx Authorized Training Partner(ATP).

Chapter 2

Description of Training

Training started with basic concepts of Embedded Systems, Hardware Development languages, different computer architectures, basic concepts related to FPGAs, ASICs etc were covered. Different problems and it's solution in verilog HDL was discussed. Introduction Xilinx Vivado Toolkit. Implementation of basic memory cells and switches like FIFOs, RAM, Cross Switches were discussed.

FIFO is a special type of buffer. FIFO stands for first in first out and means that the data written into the buffer first comes out of it first. Crossbar Switches are collection of many switches which are arranged in matrix form. It contains multiple inputs and outputs lines which form a crossed pattern of interconnecting lines between which a connection may be established by closing a switch. The designed one has 4 input/output stream of 13 bit, where 8 bit corresponded to data, 2 bit to address of destination and 2 bit address of time slots.

After completion of these modules, Design and Functional verification of RISC Processor was assigned. The objective of this project was to study, design, and validate a 16-bit RISC processor based on simple LOAD/STORE architecture. It covers the study of simple LOAD/STORE architecture design and investigation on how the processor executes its instruction.

Chapter 3

Project Undertaken

3.1 Introduction

The project undertaken during the period of internship was ***"Design and Functional Verification of RISC Processor"*** in which 16 bit RISC processor had to be designed. RISC stands for Reduced Introduction Set Computer. RISC is a microprocessor architecture which runs using a pipelining arcitechture to improve the performance of a processor. In RISC, the instruction set contains simple and basic instructions from which more complex instruction can be produced.

The scope of work in this project covers the design of a 16-bit RISC processor with implementation of 4-stage that can execute two main types of instruction set architecture which are data processing and single data transfer.The project was designed using Verilog HDL and synthesize using Xilinx Vivado Tool.

3.2 Block Diagram and working

The Processor has 24-bit instruction words and 16 x 16 Data memory. Every instruction is completed in eight cycles. An external clock is used as the timing mechanism for the control and datapath units. A synchronous reset is used as an input. The output of the processor is a 16-bit data along with a 1-bit Carry/Borrow signal and a 'done' signal of 1-bit is made high at the end of every instruction.

3.2.1 Block Diagram Description

The three main elements present in the RISC processor are ALU, Register Bank and Decoder as shown in Figure 3.1. Reset is used to reset all the registers and ports. The system requires 8 clock cycles to complete one instruction. Each instruction has 5 machine cycles (INIT,Instruction Fetch and Decode, Execution, Write Back).

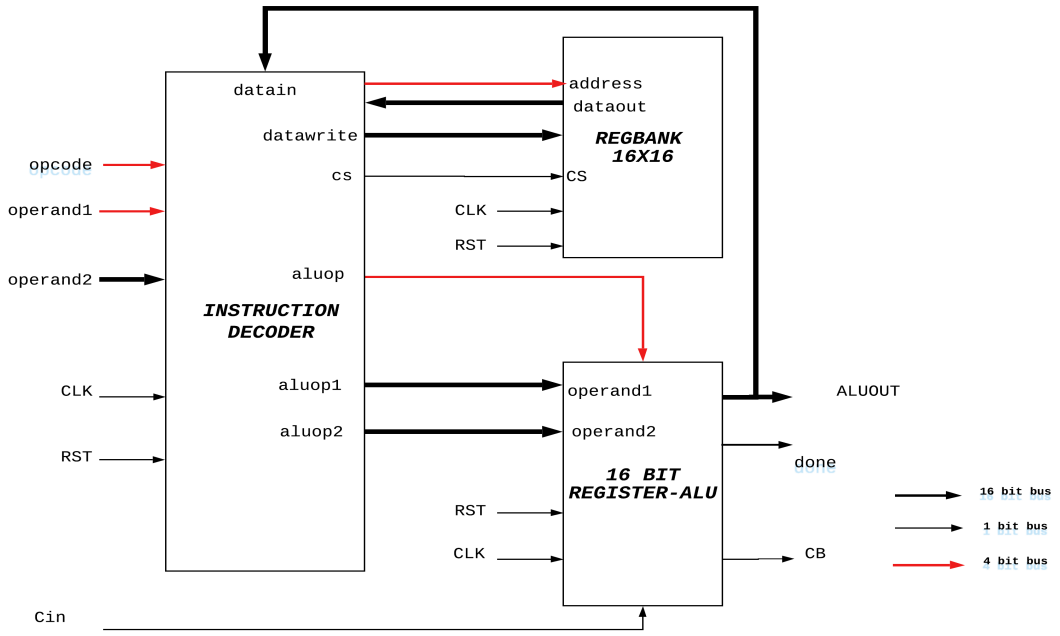

Figure 3.1: Block diagram

Table 3.1: Signal Description of Block Diagram

Signal Name	Desrciption
Opcode	4 bit size, specifying the operation performed by ALU on given operands
Operand1	4 bit size,consisting the address of location where the first operand stored in memory
Operand2	16 bit immediate data/ 4 bit source memory address
CLK	Processor clock
CIN	Carry in for ALU, used for arithmetic operations
RST	Reset (when RST is high then register ALU and instruction decoder will reset)
ALUOUT	16 bit data output from ALU
CB	1-bit carry/borrow out from ALU
done	1-bit instruction to acknowledge the end of every writeback to the memory.

3.2.1.1 Instruction Decoder

Instruction decoder is an Finite State Machine (FSM), which has 5 states. If RST signal is asserted the instruction decoder will enter into initial state. After it's de-assertion, for every positive edge of clock the state will change from init to fetch, decode, execute and then to load. Figure 3.2 shows state diagram of instruction decoder.

INIT: RST signal is asserted the instruction decoder will enter into initial state. After

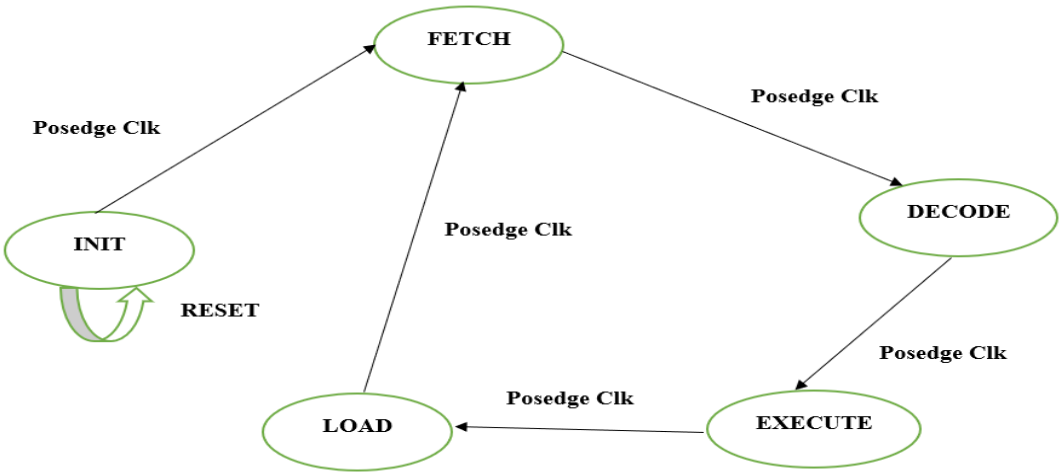

Figure 3.2: State Diagram of Instruction Decoder

it's deassertion, for every positive edge of clock the state will change from init to fetch, decode, execute and then to load.

FETCH: In this cycle Fetch control signal becomes low, Decode control signal becomes high and other control signals (Execute and Load) are low. OPCODE bits are loaded into ALUOPERATION, OPERAND1 bits are loaded into ADDRESS and OPERAND2 bits are loaded into ALUOPR2. $R/\bar{W}$ and CS signals are high while WB signal is low.

DECODE: In this cycle Decode control signal becomes low, Execute control signal becomes high and other control signals (Fetch and Load) are low. 16-bit data comes from the memory (DATAOUT) are loaded into ALUOPR1. $R/\bar{W}$, CS and WB signals are low.

EXECUTE: In this cycle Execute control signal becomes low, Load control signal becomes high and other control signals (Fetch and Decode) are low. 16-bit data comes from the memory (DATAOUT) are loaded into ALUOPR1. CS and WB signals are high, $R/\bar{W}$ signal is low. In this cycle ALU performes operation depending upon ALUOPERATION on 16-bit data 0PR1 and OPR2 and output of the operation is available on ALUOP and CB. ALUOP is applied to DATAIN of the memory through multiplexer.

LOAD: In this cycle Load control signal becomes low, Fetch control signal becomes high and other control signals (Decode and Execute) are low. CS , WB and $R/\bar{W}$ signals are low. Data available on DATAIN is loaded into the memory depending upon the ADDRESS.

3.2.1.2 Arithmetic & Logic Unit

This unit is 16-bit ALU register used for performing basic Arithmetic and Logical operations.The output of the ALU is registered which 16 bit wide. The output of a ALU consists of result obtained from the operation performed on operands from the input, Carry/Borrow and a done signal to indicate end of instruction.

Table 3.2: Signal Description of Arithmetic and Logical Unit

Signal Name	Desrciption
ALUOP	4 bit size, specifying the operation performed by ALU on given operands
ALUOP1	16 bit data
ALUOP2	16 bit data
CLK	System clock
CIN	Carry in for ALU, used for arithmetic operations
RST	Reset (when RST is high then register ALU will reset)
ALUOUT	16 bit data output from ALU
CB	1-bit carry/borrow out from ALU
done	1-bit instruction to acknowledge the end of every writeback to the memory.

3.2.1.3 Register Bank

It has width of 16-bit and depth of 16 locations. It is a single port memory which is used to provide 16-bit data and to store 16-bit result of the ALU.
Write operation: CS control signal is high and $R/\bar{W}$ control signal is low, the data available at the DATAIN is loaded into memory as per the address given on posedge of clock signal.
Read Operation:CS and $R/\bar{W}$ control signals are high, the data available at the specified address location into the memory is fetched at posedge of clock signal and it is available at the DATAOUT port.

3.3 Hardware and Software Description

3.3.1 Xilinx Zedboard

Xilinx Zedboard (IC Part No. XC7Z020clg484-1) is used as a development board in this project. Zedboard is a Zynq Evaluation and low-cost Development board for the Xilinx Zynq-7000 all programmable SoC (AP SoC). The key features of this SoC involves 4 GB SD Card, 256 MB Quad-SPI Flash, 512 MB DDR3, Onboard USB-JTAG Programming and Dual-Core ARM Cortex -A9.

Table 3.3: Signal Description of Register Bank

Signal Name	Desrciption
ADDRESS	It provides the address where the data is stored or fetched.
DATAIN	Input data is available at this input signals.
Chip Select(CS)	Chip select , it is used to select the memory
CLK	Processor clock, provides clock signal to the memory
CIN	Carry in for ALU, used for arithmetic operations
$R/\bar{W}$	It is a control signal for read and write operation
DATAOUT	Data fetched from the memory is available at this signal

3.3.2 Xilinx Vivado

Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for System on a Chip Development and high-level synthesis. Vivado enables developers to synthesize their designs, perform timing analysis, examine RTL diagrams (shown in Figure 3.4), simulate a design's reaction to different stimuli, and configure the target device with the programmer. Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips.

3.4 Outputs and Functional Verification

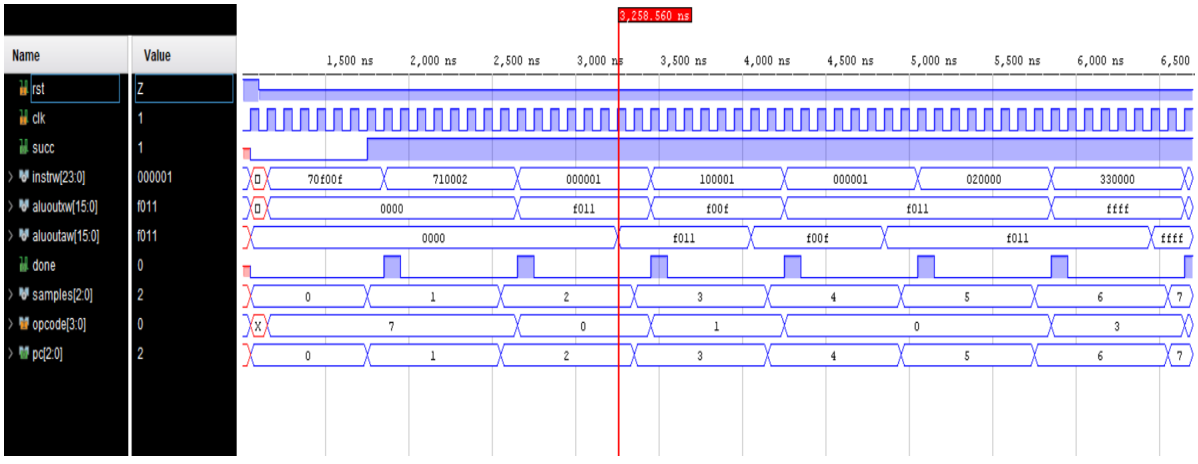

Figure 3.3: Simulation waveforms for the testbench

In order to test the design on hardware, the concept of Block RAM(BRAM) is used. The BRAMs are populated using Xilinx coeffiecient files.The input instructions and the corresponding ALU outputs are written into BRAMs.

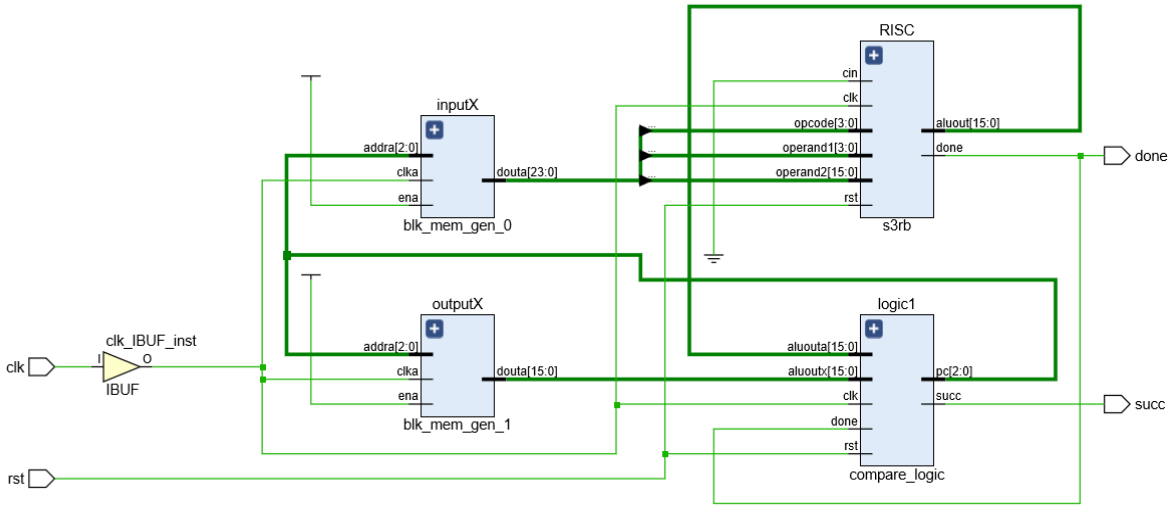

Figure 3.4: RISC RTL Schematic Diagram

During verification, the inputs to RISC Processor are fed from input Block RAM and the corresponding outputs are compared with expected outputs from output Block RAM. When the expected output matches the actual output, an active high 'Success' signal is given to an output port which in hardware is connected to a LED along with done signal of the RISC processor.

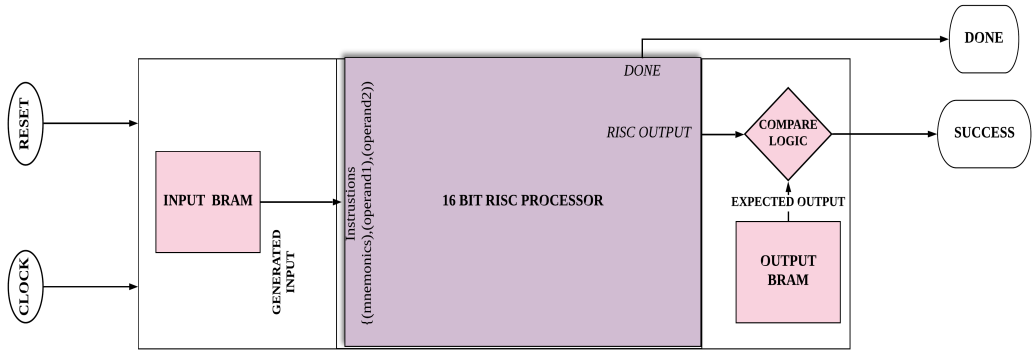

Figure 3.5: Block Diagram of RISC Testbench Module

3.5 Custom Assembler in python

In order to automate the process of producing input and output COE files, an assembler and assembly interpreter was written in Python. The assembler generates the input COE from an assembly program and the expected ALU outputs are generated by the interpreter which generates the ALU outputs by emulating the processor operations.

Chapter 4

Conclusion

The Internship started with training on Embedded Systems, Hardware Development languages, different computer architectures, basic concepts related to FPGAs, ASICs etc were covered. Different problems and it's solution in verilog HDL was discussed. Introduction Xilinx Vivado Toolkit. Implementation of basic memory cells and switches like FIFOs, ROM, RAM, Cross Switches were discussed. Concluded with Project and verifying it's functionality and submitting the results to the company.

RISC Processor module submitted based on simple LOAD/STORE architecture was designed using Vivado software and is implemented on Zedboard. The designed RISC processor basically involves 3 major blocks ALU, Decoder and Register Bank. These design blocks were tested. Overall the system worked as expected and the outputs obtained from the FPGA (Zedboard) were compared with the simulation results and theortical values. The RISC processor was developed using Vivado Software. The Hardware Description Language code developed and designed using Verilog is converted to Register Tranfer Langauge by Vivado and synthesized. The synthesized code generates a bitstream which is implemented and loaded to the FPGA. Testing of this done by comparing the obtained value from FPGA with groundtruth value. Groundtruth value generated from RISC Processor model in python. Along with it Custom assembler integrated to the system and results are verified.

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