



V853&V853S

Datasheet

Revision 1.1

March 23, 2022

Revision History

Revision	Date	Author	Description
1.0	March 9, 2022	AWA1896	Initial Version
1.1	March 23, 2022	AWA1896	<ol style="list-style-type: none">1. Update NPU specification in section 1.1.1 , section 1.3.3, and figure 1-42. Update V853/V853S application diagram in section 1.23. Update bit[26:24] of CSIC register (offset: 0x0008) in section 6.1.6.34. Add SPI1 base address in section 10.3.5



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About This Document

Purpose and Scope

This document describes the features, logical structures, functions, operating modes, and related registers of each module about V853/V853S. This document also describes interface timings and related parameters, pins, pin usages, performance parameters, and package dimension of V853/V853S in detail.



The document defines two devices: V853 and V853S. Throughout this document, the devices are referred to as V853/V853S when material being presented applies to all of them. Unless other stated, V853 and V853S contents are consistent.

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Reset Value Conventions

In the register definition tables:

If other column value in the row of a bit or multiple bits is “/”, this bit of these multiple bits are unused.

If the default value of a bit or multiple bits is “UDF”, this default value is undefined.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

Acronyms and Abbreviations

The following table contains acronyms and abbreviations used in this document.

ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
AWB	Automatic White Balance
BROM	Boot ROM
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FEL	Fireware Exchange Launch
FIFO	First In First Out
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface

HiSPI	High-Speed Serial Pixel Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
KEYADC	Analog to Digital Converter for Key
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OSD	On-Screen Display
OTP	One Time Programmable
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Synchronous Dynamic Random Access Memory

SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TFBGA	Thin Fine Ball Grid Array
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface



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1 Product Description

1.1 Overview

V853/V853S is a new generation of high-performance and low-power processor SoC targeted for the field of intelligent vision. It can be widely used in intellectually upgraded industries such as intelligent door lock, intelligent attendance and access control, webcam, tachograph, and intelligent desk lamp.

V853/V853S integrates the single Cortex-A7 core and RISC-V core. It is also designed with a new generation of high-performance ISP image processor and Allwinner Smart video engine with maximum 5M@25fps H.265/H.264 encoding and 5M@25fps H.264 decoding to achieve professional picture effect. It has built-in NPU with maximum 1T computing power and supports INT8/INT16 hybrid operation and typical network models such as TensorFlow/MXNet/PyTorch/Caffe. V853/V853S has advanced 22nm technics to support product miniaturization design. It also supports various special video input and output interfaces such as 1*4-lane MIPI/DVP/MIPI-DSI/RGB to meet the needs of all AI visual products. V853 supports 16-bit DDR3/DDR3L to meet the requirements of various products on high bandwidth. In addition, Allwinner provides the stable and easy-to-use matching reference design for Linux SDK and software and hardware to assist clients in the rapid mass production of products.

1.1.1 Device Difference

The V853/V853S is configured with different sets of features in different devices. The feature differences across different devices are shown in the following table. For detail pins, see the [**V853/V853S_PINOUT.xls**](#).

Table 1-1 Device Feature Differences

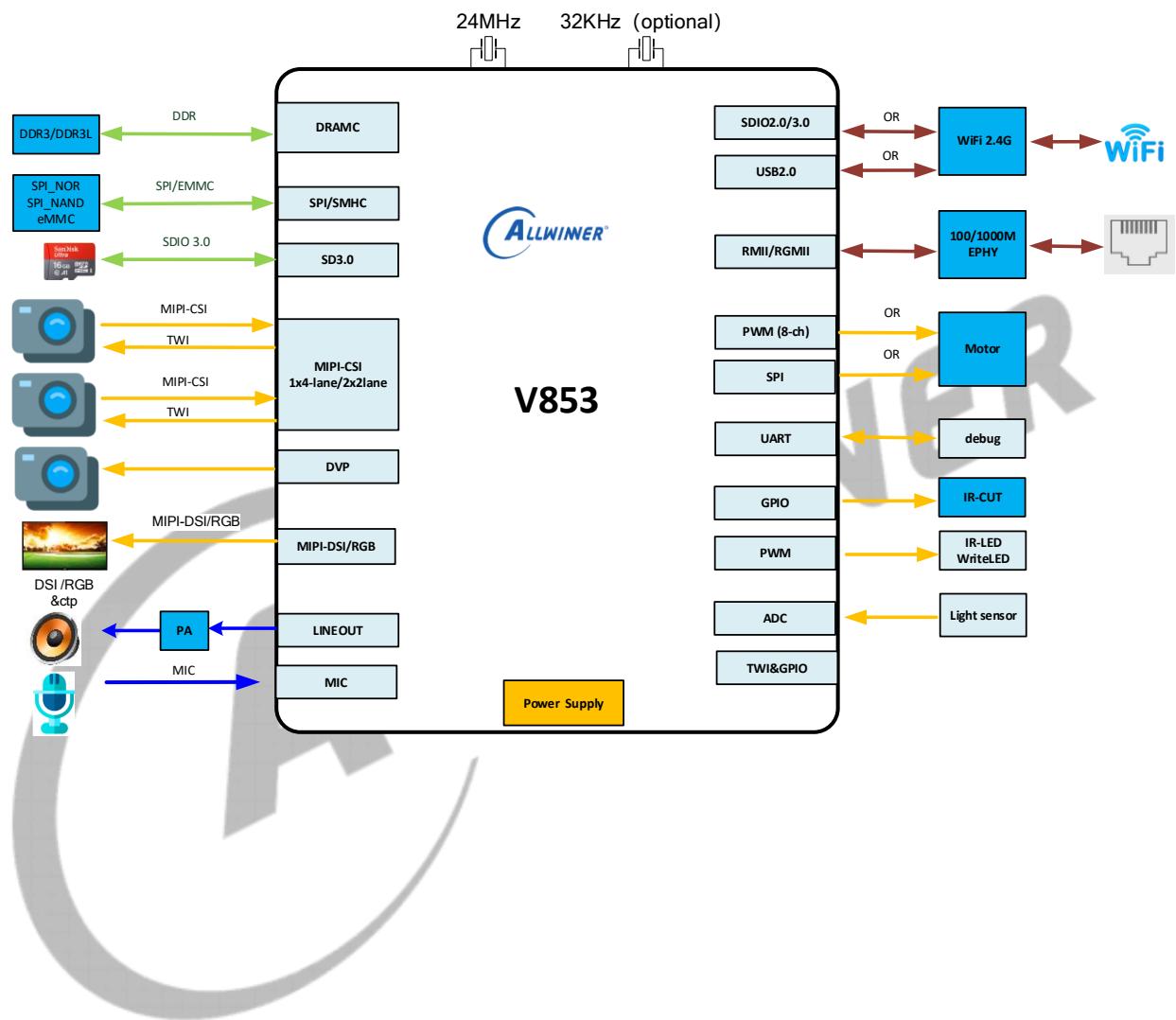
Contents	V853	V853S
NPU	1 Tops	0.8 Tops
SDRAM	External 1GB DDR3/DDR3L	SIP 128MB DDR3L

1.2 Application Scenarios

1.2.1 V853 AI Vision Solution

The following figure shows the application scenarios of V853.

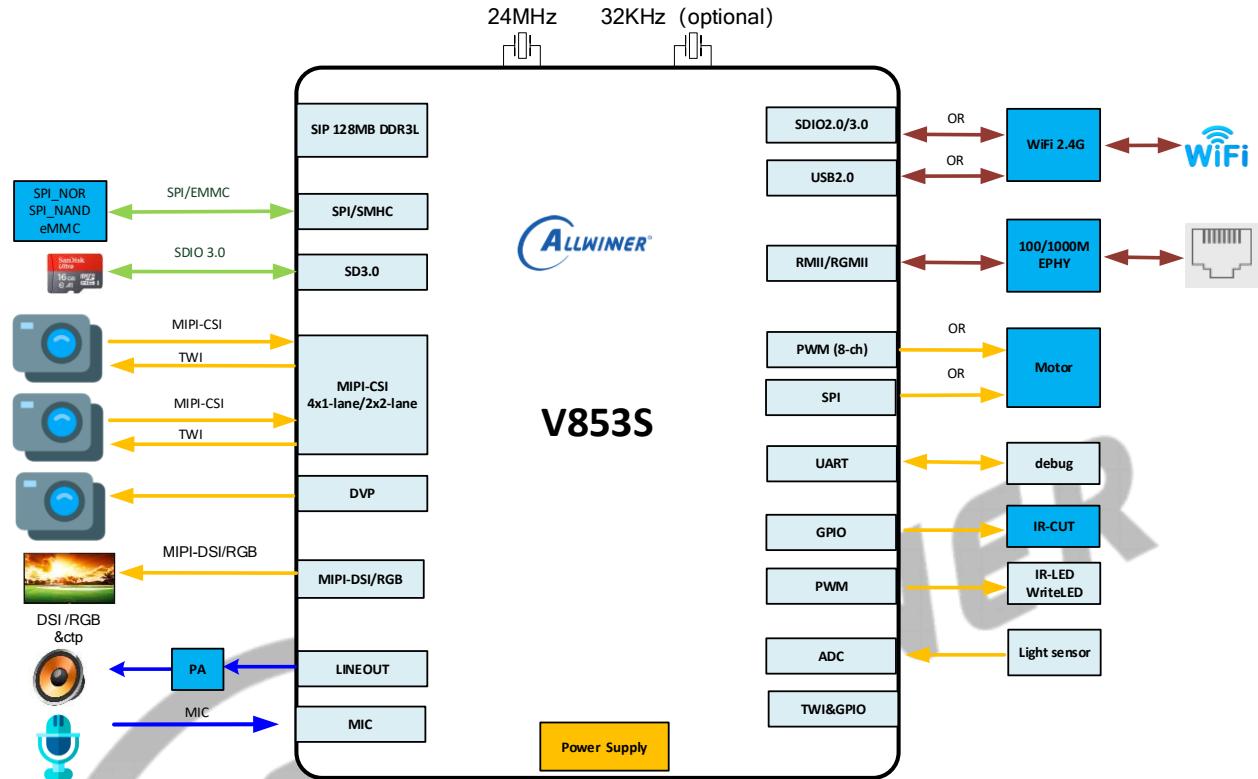
Figure 1-1 V853 AI Vision Solution



1.2.2 V853S AI Vision Solution

The following figure shows the application scenarios of V853S.

Figure 1-2 V853S AI Vision Solution



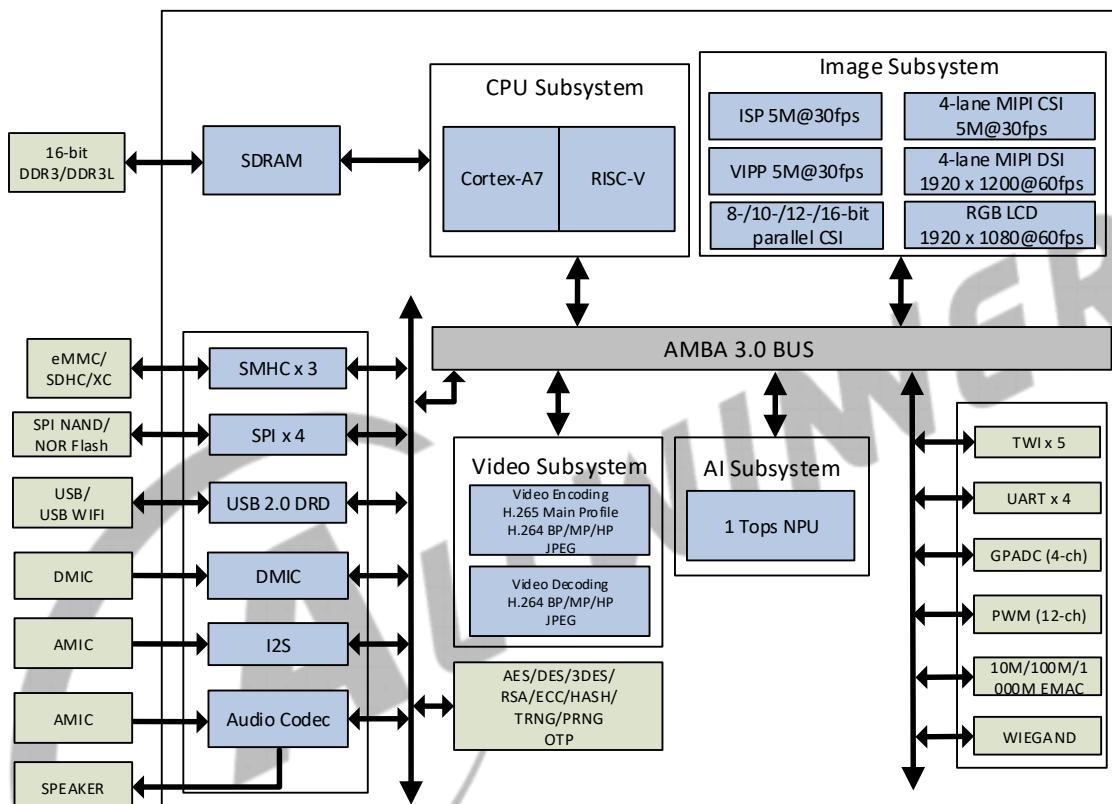
1.3 Architecture

1.3.1 Block Diagram

1.3.1.1 V853

The following figure shows the logic block diagram of the V853.

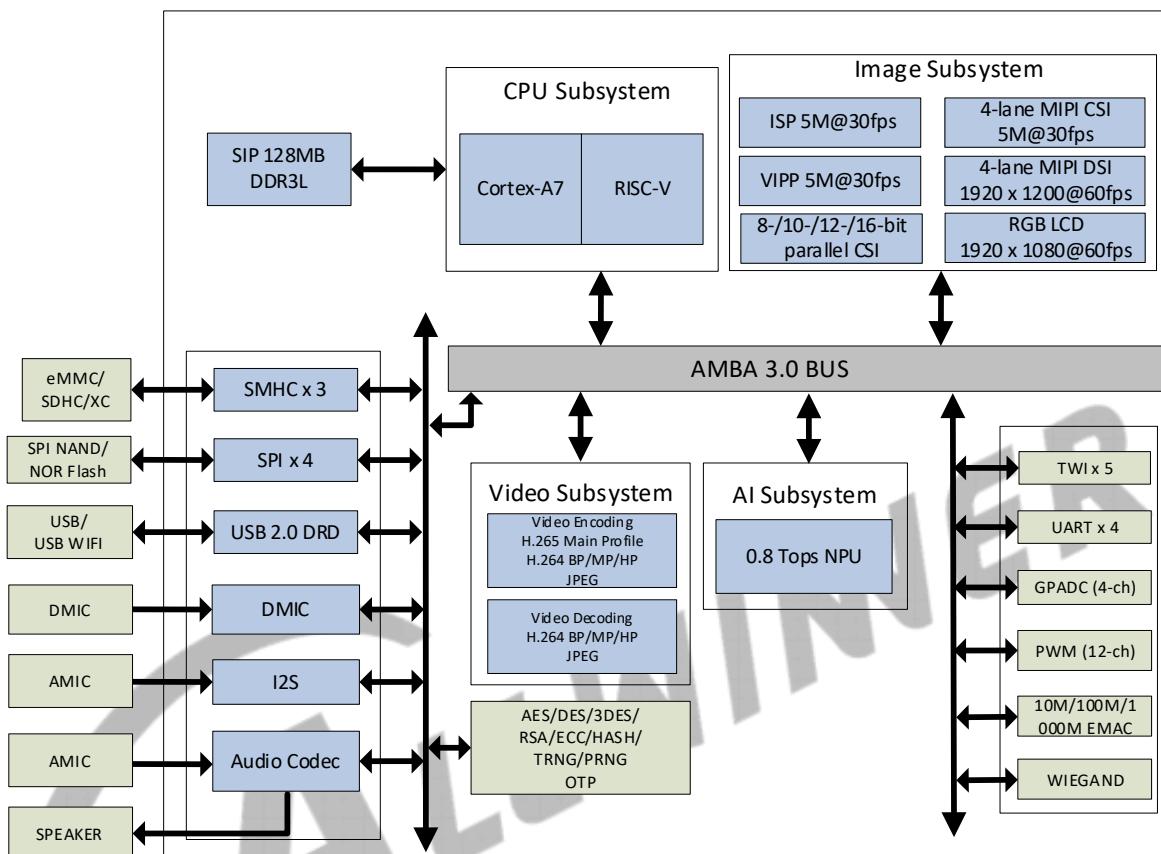
Figure 1-3 V853 Logic Block Diagram



1.3.1.2 V853S

The following figure shows the logic block diagram of the V853S.

Figure 1-4 V853S Logic Block Diagram



1.3.2 CPU Architecture

- Cortex-A7 CPU core, supporting 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache
- RISC-V core, supporting 16 KB I-cache and 16 KB D-cache

1.3.3 NPU Architecture

- Maximum performance up to 1 Tops for V853 and 0.8 Tops for V853S
- Embedded 128KB internal buffer
- Supports deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, and so on

1.3.4 Video Encoding/Decoding Performance

- H.264 BP/MP/HP encoding
- H.265 MP encoding

- H.264/H.265 supports I/P frame type
- MJPEG/JPEG baseline encoding
- H.264/JPEG decoding
- Maximum resolution for H.264/H.265 decoding is 16 megapixels (4096x4096)
- A maximum of eight ROIs
- CBR, VBR and FIXEDQP modes
- JPEG encoder supports 1080p@60fps@400MHz
- H.264/H.265 encoder supports 3840x2160@20fps@400MHz
- H.264/H.265 multi-stream real-time encoding capability: 5M@25fps + 720p@25fps

1.3.5 Video Output

1.3.5.1 MIPI DSI

- Compliance with MIPI DSI V1.02 and MIPI DPHY V1.2
- Supports 4-lane MIPI DSI, up to 1920 x 1200@60fps
- Supports normal mode and burst mode
- Up to 1.0 Gbps/Lane

1.3.5.2 TCONLCD

- i8080 interface, up to 800 x 480@60fps
- Serial RGB interface, up to 800 x 480@60fps
- RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- supports BT656 interface

1.3.6 Video Input

1.3.6.1 ISP

- Supports 1 individual image signal processor(ISP), with maximum resolution of 3072 x 3072 (online mode)
- Maximum frame rate of 5M@30fps
- Supports offline mode

- Supports WDR spilt, 2F-WDR line-based stitch, dynamic range compression (DRC), tone mapping, digital gain, gamma correction, defect pixel correction (DPC), cross talk correction (CTC), and chromatic aberration correction (CAC)
- Supports 2D/3D noise reduction, bayer interpolation, sharpen, white balance, and color enhancement
- Adjustable 3A funtions: automatic white balance (AWB), automatic exposure (AE), and automatic focus (AF)
- Supports anti-flick detection statistics, and histogram statistics
- Supports graphics mirror and flip

1.3.6.2 VIPP

- Four VIPP YUV422 or YUV420 outputs
- Maximum resolution of 3072x3072
- Each VIPP has one sub-VIPP in online mode
- Each VIPP has maximum four sub-VIPPs for time division multiplexing in offline mode
- Functions for each Sub-VIPP
 - Crop
 - 1 to 1/16 scaling for height and width
 - 16 ORLs

1.3.6.3 Parallel CSI

- Supports 8/10/12/16-bit width
- Supports BT.656, BT.601, BT.1120 interface
- Maximum pixel clock for parallel to 148.5MHz
- Supports ITU-R BT.656 up to 4*720P@30fps
- Supports ITU-R BT.1120 up to 4*1080P@30fps

1.3.6.4 MIPI CSI

- Supports one 4-lane MIPI CSI input or two 2-lane MIPI CSI inputs
- Compliant with MIPI CSI2 V1.1 and MIPI DPHY V1.1
- Up to 1.2 Gbps/Lane
- maximum video capture resolution for serial interface up to 5M@30fps

1.3.7 Audio Subsystem

1.3.7.1 Audio Codec

- One audio digital-to-analog converter (DAC) channels
 - Supports 16-bit and 20-bit sample resolution
 - 8 kHz to 192 kHz DAC sample rate
 - 95 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- Two audio analog-to-digital converter (ADC) channels
 - Supports 16-bit and 20-bit sample resolution
 - 8 kHz to 48 kHz ADC sample rate
 - 95 ± 3 dB SNR@A-weight, -80 ± 3 dB THD+N
- Two audio inputs:
 - Two differential microphone inputs: MICIN1P/N, MICIN2P/N
- One audio output:
 - One differential lineout output (LINEOUTP/LINEOUTN)
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA

1.3.7.2 I2S

- Two I2S/PCM external interfaces (I2S0, I2S1) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
 - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
 - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
 - Programmable FIFO thresholds
 - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
 - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)

- Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA Slave interface
- Supports multiple application scenarios
 - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
 - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
 - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

1.3.7.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

1.3.8 External Peripherals

- Five TWI interfaces
- Four UART interfaces
- Four SPI interfaces
- Eight GPIO interfaces
- Four channels general purpose analog-to-digital converter(GPADC)
- One PWM controller(12-ch)

1.3.9 Security System

1.3.9.1 Crypto Engine (CE)

- Supports symmetrical algorithm for encryption and decryption: AES, DES, 3DES
 - Supports ECB, CBC, CTS, CFB, OFB, CBC-MAC, GCM mode for AES
 - Supports 128/192/256-bit key for AES
 - Supports ECB, CBC, CTR, CBC-MAC mode for DES
- Supports hash algorithm for tamper proofing: MD5, SHA, HMAC
 - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
 - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
 - Supports multi-package mode for HMAC/SHA1/SHA224/SHA256/SHA384/SHA512
 - Supports hardware padding

- Supports public key algorithm: RSA, ECC
 - RSA supports 512/1024/2048/3072/4096-bit width
 - ECC supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG with 15-bit seed
- Supports 256-bit hardware TRNG
- Supports secure and non-secure interfaces respectively, each world issues task request through its own interface
- Supports byte-aligned address for all configurations

1.3.9.2 Security ID (SID)

- Supports 2048 bit eFuse
- Backs up eFuse information by using SID_SRAM
- Burning the key to the SID
- Reading the key use status in the SID
- Loading the key to the CE

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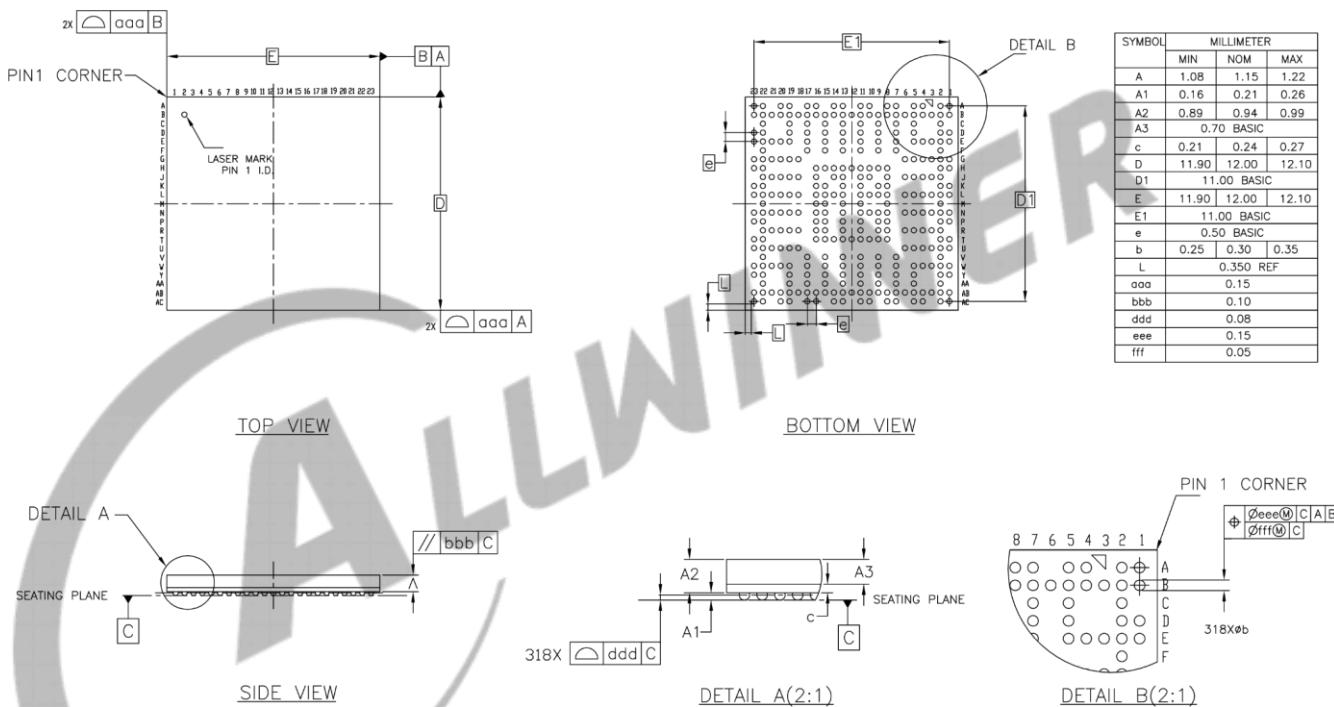
2 Hardware

2.1 Package and Pinout

2.1.1 Package

The V853/V853S uses the LFBGA package, it has 318 pins, its body size is 12 mm x 12 mm, and its ball pitch is 0.50 mm. The following figure shows the top, the bottom, and the side views of the V853/V853S package dimension.

Figure 2-1 V853/V853S Package Dimension



2.1.2 Pin Quantity

The following table lists the pin quantity of the V853.

Table 2-1 V853 Pin Quantity

Pin Type	Quantity
I/O	199
Power	24
GND	81
DDR Power	5
NC	9
Total	318

The following table lists the pin quantity of the V853S.

Table 2-2 V853S Pin Quantity

Pin Type	Quantity
I/O	145
Power	24
GND	135
DDR Power	5
NC	9
Total	318

2.2 Pin Description

For details about pin description of the V853/V853S, see the *V853/V853S_PINOUT.sls*.

2.3 Electrical Characteristics

2.3.1 Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

2.3.2 Absolute Maximum Ratings

The device will be damaged if the stresses are beyond the absolute maximum ratings. The following table specifies the absolute maximum ratings.



CAUTION

Stresses beyond those listed under Table 2-3 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device in these or any other conditions beyond the values in the Section 2.3.4 *Recommended Operating Conditions* is not implied. Exposure to the absolute maximum rated conditions for extended periods may affect the device reliability.

Table 2-3 Absolute Maximum Ratings

Symbol	Parameter	Min ⁽¹⁾	Max ⁽¹⁾	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-PA	Digital GPIO A Power	-0.3	3.96	V
VCC-PC	Digital GPIO C Power	-0.3	3.96	V
VCC-PD	Digital GPIO D Power	-0.3	3.96	V
VCC-PE	Digital GPIO E Power	-0.3	3.96	V
VCC18-PF	1.8V Digital GPIO F Power	-0.3	2.16	V
VCC33-PF	3.3V Digital GPIO F Power	-0.3	3.96	V

Symbol	Parameter		Min ⁽¹⁾	Max ⁽¹⁾	Unit
VCC-PG	Digital GPIO G Power		-0.3	3.96	V
VCC-PI	Digital GPIO I Power		-0.3	3.96	V
VCC-IO	Power Supply for 3.3 V Digital Part		-0.3	3.96	V
VCC-RTC	Power Supply for RTC		-0.3	2.16	V
VCC-PLL	Power Supply for System PLL		-0.3	2.16	V
VCC-LDOA	Internal LDOA Output Voltage for Analog Device and IO		-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM IO and DDR3/DDR3L		-0.3	2.16	V
VCC18-MCSI	MIPI CSI Power		-0.3	2.16	V
VCC18-MDSI	MIPI DSI Power		-0.3	2.16	V
VCC-EFUSE	Power Supply for EFUSE Program Mode		-0.3	2.16	V
VCC33_USB	USB Analog Power		-0.3	3.96	V
VDD09_USB	USB Digital Power		-0.3	1.08	V
VDD33	Power Supply for 3.3V Analog Part		-0.3	3.96	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
VDD-SYS	Power Supply for System		-0.3	1.08	V
T _{STG}	Storage Temperature		-40	150	°C
T _j	Working Junction Temperature		-40	125	°C
V _{ESD}	Electrostatic Discharge ⁽²⁾	Human Body Model(HBM) ⁽³⁾	-2000	2000	V
		Charged Device Model(CDM) ⁽⁴⁾	-500	500	V
I _{Latch-up}	Latch-up I-test performance current-pulse injection on each IO pin ⁽⁵⁾		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin ⁽⁶⁾		Pass		

- (1) The min/max voltages of power rails are guaranteed by design, not tested in production.
- (2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.
- (3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
- (4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.
- (5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.
- (6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

2.3.3 Thermal Resistance Parameters

The following table shows thermal resistance parameters. The following thermal resistance characteristics is based on JEDEC JESD51 standard, because the actual system design could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.



NOTE

Test condition: four-layer board (2s2p), natural convection, no air flow.

Table 2-4 V853 Thermal Resistance Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	-	32.45	-	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	-	10.85	-	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	-	10.83	-	°C/W

Table 2-5 V853S Thermal Resistance Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	-	29.12	-	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	-	11.08	-	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	-	11.15	-	°C/W

2.3.4 Recommended Operating Conditions

The following table describes the operating conditions of the V853/V853S.


NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 2-6 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	70	°C
Tj	Junction Temperature Range	-40	-	115 ⁽¹⁾	°C
AVCC	Power Supply for Analog Part	1.77	1.8	1.83	V
VCC-IO	Power Supply for 3.3V Digital Part	2.97	3.3	3.63	V
VCC-PA	Power Supply for Port A 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PC	Power Supply for Port C 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PD	Power Supply for Port D 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PE	Power Supply for Port E 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC18-PF	Power Supply for Port F 1.8V voltage	1.62	1.8	1.98	V
VCC33-PF	Power Supply for Port F 3.3V voltage	2.97	3.3	3.63	V

Symbol	Parameter	Min	Typ	Max	Unit
VCC-PG	Power Supply for Port G 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PI	Power Supply for Port I 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-RTC	Power Supply for RTC	1.62	1.8	1.98	V
VCC18-MCSI	MIPi CSI Power	1.62	1.8	1.98	V
VCC18-MDSI	MIPi DSI Power	1.62	1.8	1.98	V
VCC-DRAM	Power Supply for DDR3 IO Domain	1.425	1.5	1.575	V
	Power Supply for DDR3L IO Domain	1.28	1.35	1.45	V
VCC33-USB	3.3V Power Supply for USB	2.97	3.3	3.63	V
VDD33	Power Supply for 3.3V Analog Part	2.97	3.3	3.63	V
VDD09-USB	0.9V Power Supply for USB	0.81	0.9	0.99	V
VDD-SYS	Power Supply for System	0.81	0.9	1	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power	1.7	1.8	1.95	V

- (1) The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 2-6.

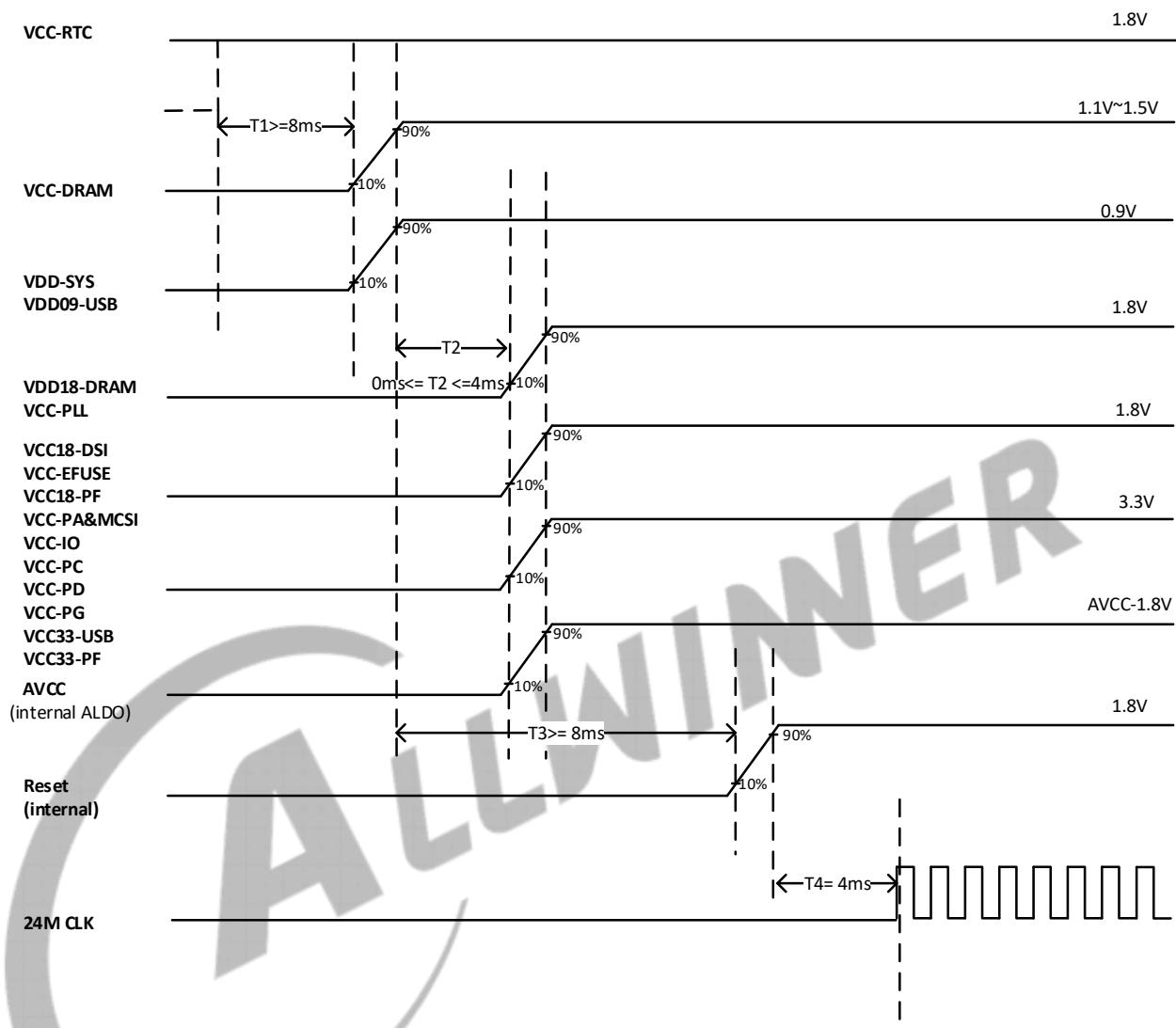
2.3.5 Power-On and Power-Off Sequences

The following figure shows an example of the sequence for V853/V853S device.

The description of the power-on sequence for V853/V853S is as follows:

- VCC-RTC must be ramped no later than other power rails.
- RESET rail starts to ramp after VDD-SYS is stable with a minimum delay of 8 ms.
- 24MHz clock starts oscillating 4 ms after the RESET signal is released.

Figure 2-2 V853/V853S Power on Sequence



During power-off, all powers start to ramp down at the same time, and the ramp rate of each power rail is generated by the load on the power.

2.3.6 DC Electrical Parameters

The following table summarizes the DC electrical characteristics of the V853/V853S.

Table 2-7 DC Electrical Characteristics

(VCC-IO/VCC-PA/VCC-PC/VCC-PD/VCC-PE/VCC-PF/VCC-PG/VCC-PI)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	PI1 to PI4	3.76	4.7	5.64	kΩ
		PC1 to PC10,	12	15	18	kΩ

Symbol	Parameter		Min	Typ	Max	Unit
		PF3				
		PG0 to PG5	26	33	40	kΩ
		Other GPIOs	80	100	120	kΩ
R _{PD}	Input Pull-down Resistance	PI1 to PI4	3.76	4.7	5.64	kΩ
		PC1 to PC10, PF3	12	15	18	kΩ
		PG0 to PG5	26	33	40	kΩ
		Other GPIOs	80	100	120	kΩ
I _{IH}	High-Level Input Current	-			10	uA
I _{IL}	Low-Level Input Current	-	-		10	uA
V _{OH}	High-Level Output Voltage	VCC-IO - 0.2	-		VCC-IO	V
V _{OL}	Low-Level Output Voltage	0	-		0.2	V
I _{OZ}	Tri-State Output Leakage Current	-10	-		10	uA
C _{IN}	Input Capacitance	-	-		5	pF
C _{OUT}	Output Capacitance	-	-		5	pF

2.3.7 SDRAM I/O DC Electrical Parameters

The DDR I/O pads support DDR3/DDR3L operational modes. The SDRAM Controller(DRAMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DRAMC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3F DDR3 JEDEC standard release July,2012
- DDR3L SDRAM compliant to JESD79-3-1A DDR3L JEDEC standard release January,2013

Table 2-8 DC Input Logic Level

Characteristics	Symbol	Min	Max	Unit
DC input logic high	V _{IH(DC)}	V _{ref} +20	-	mV
DC input logic low	V _{IL(DC)}	-	V _{ref} -20	mV

Table 2-9 DDR3/DDR3L mode, DC Input Conditions

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Reference Voltage	V _{ref}	V _{DQQ}	30.1%	31.1%	32.1%	Please refer to Note 1 and 2
On-die termination(ODT) programmable resistances	R _{TT}	ohm	-	open, 120, 60	-	Please refer to Note 3

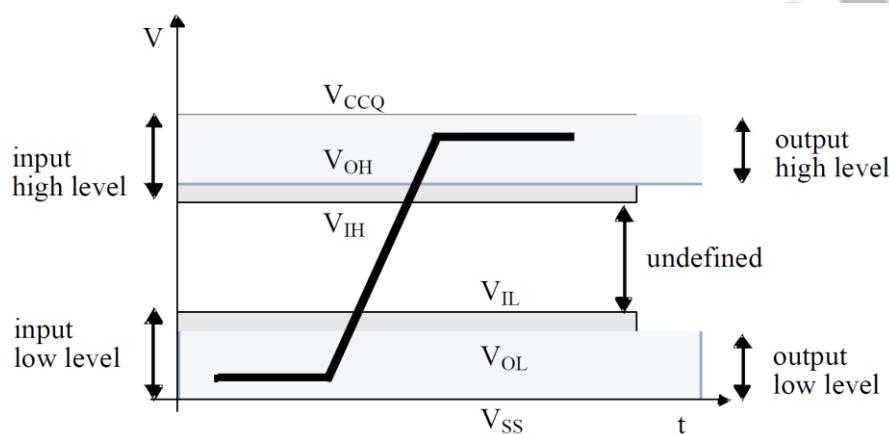
**NOTE**

- If the external Vref to the receivers is enabled, Vref is expected to be set to a nominal value of $(VDDQ/2) * RxAtten$ (RxAttenuation for DDR3/DDR3L is 0.623) through a voltage divider in order to track VDDQ level. It can be adjusted in the system to margin the input DQ signals, although this margin does not necessarily represent the eye height since a change in Vref also changes the input receiver common mode, altering receiver performance.
- Externally supplied Vref is not recommended. Internal Vref generation through local Vref generation at each receiver is preferred.
- For DDR3, ODT is a Thevenin resistance to $VDDQ/2$.

2.3.8 SDIO Electrical Parameters

The SDIO electrical parameters are related to the different supply voltage.

Figure 2-3 SDIO Voltage Waveform



The following table shows 3.3V SDIO electrical parameters.

Table 2-10 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7	-	3.6	V
V_{OH}	Output high-level voltage	$0.75 * V_{CCQ}$	-	-	V
V_{OL}	Output low-level voltage	-	-	$0.125 * V_{CCQ}$	V
V_{IH}	Input high-level voltage	$0.625 * V_{CCQ}$	-	$V_{CCQ} + 0.3$	V
V_{IL}	Input low-level voltage	$V_{SS} - 0.3$	-	$0.25 * V_{CCQ}$	V

The following table shows 1.8V SDIO electrical parameters.

Table 2-11 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V _{CCQ}	I/O voltage	1.7	-	1.95	V
V _{OH}	Output HIGH voltage	V _{CCQ} - 0.45	-	-	V
V _{OL}	Output LOW voltage	-	-	0.45	V
V _{IH}	Input HIGH voltage	0.625 * V _{CCQ} ⁽¹⁾	-	V _{CCQ} + 0.3	V
V _{IL}	Input LOW voltage	V _{SS} - 0.3	-	0.35 * V _{CCQ} ⁽²⁾	V

 **NOTE**
0.7 * VDD for MMC4.3 or lower. 0.3 * VDD for MMC4.3 or lower.

2.3.9 GPADC Electrical Characteristics

The GPADC contains a 4-ch analog-to-digital (ADC) converter. The GPADC is a type of the successive approximation register (SAR) converter.

Table 2-12 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Quantizing Error	-	8	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

2.3.10 Audio Codec Electrical Parameters

The following table shows audio codec electrical parameters.

Test Conditions:

VDD-SYS = 0.9V , AVCC= 1.8V , Ta= 25°C , 1kHz sinusoid signal, DAC fs = 48 KHz, ADC fs = 16 KHz, input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 2-13 Audio Codec Electrical Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTLP/N or LINEOUTRP/N (48 KHz)					
	Full-scale	0dBFS 1kHz	-	1.1	-	Vrms
	SNR(A-weighted)	0data	-	97	-	dB
	THD+N	0dBFS 1kHz	-	-88	-	dB

Symbol	Parameter	Test Conditions	Mi n	Typ	Max	Unit
	Crosstalk	R_0dB_L_Odata 1kHz L_0dB_R_Odata 1kHz	-	-	-	dB
ADC Path	MIC via ADC (16 KHz)					
	Output Level	MICP=3.3Vpp/2,MICN=3.3Vpp/2,1kHz,0dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	97	-	dB
	THD+N		-	-88	-	dB
	Output Level	MICP=1.695Vpp/2,MICN=1.695Vpp/2,1kHz,6dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	96	-	dB
	THD+N		-	-90	-	dB
	Output Level	MICP=0.788Vpp/2,MICN=0.788Vpp/2,1kHz,12dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	94	-	dB
	THD+N		-	-85	-	dB
	Output Level	MICP=0.392Vpp/2,MICN=0.392Vpp/2,1kHz,18dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	92	-	dB
	THD+N		-	-83	-	dB
	Output Level	MICP=0.197Vpp/2,MICN=0.197Vpp/2,1kHz,24dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	88	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=0.101Vpp/2,MICN=0.101Vpp/2,1kHz,30dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	83	-	dB
	THD+N		-	-74	-	dB
	Output Level	MICP=0.053Vpp/2,MICN=0.053Vpp/2,1kHz,36dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	76	-	dB
	THD+N		-	-68	-	dB
MBIAS	Current	-	-	2.0	-	mA
	Voltage	-	1.8	2.0	2.55	V
	Noise	20Hz--20kHz	-	2.5	-	uV

2.3.11 High Speed External Clock Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator.

Table 2-14 High-speed 24 MHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency		24		MHz
	Crystal frequency stability and tolerance at 25 °C ⁽¹⁾	-50			ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance ⁽²⁾	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of V853/V853S. It is recommended to select 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for the Wi-Fi chip, the crystal uses the recommended specification or the specified model for the Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 2-15 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

The frequency stability mainly requires that the total load capacitance (C_L) is constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1 , C_2 , and C_{shunt} .

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excepts the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize the output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details about the resonator characteristics.

2.4 PCB Design Recommendations

For details about PCB design recommendations, see the *V853/V853S Hardware Design User Guide*.

2.5 Interface Timings

2.5.1 SDRAM Interface Timing

2.5.1.1 DDR3/DDR3L Parameters

The following figure shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 2-16.

Figure 2-4 DDR3/DDR3L Command and Address Timing

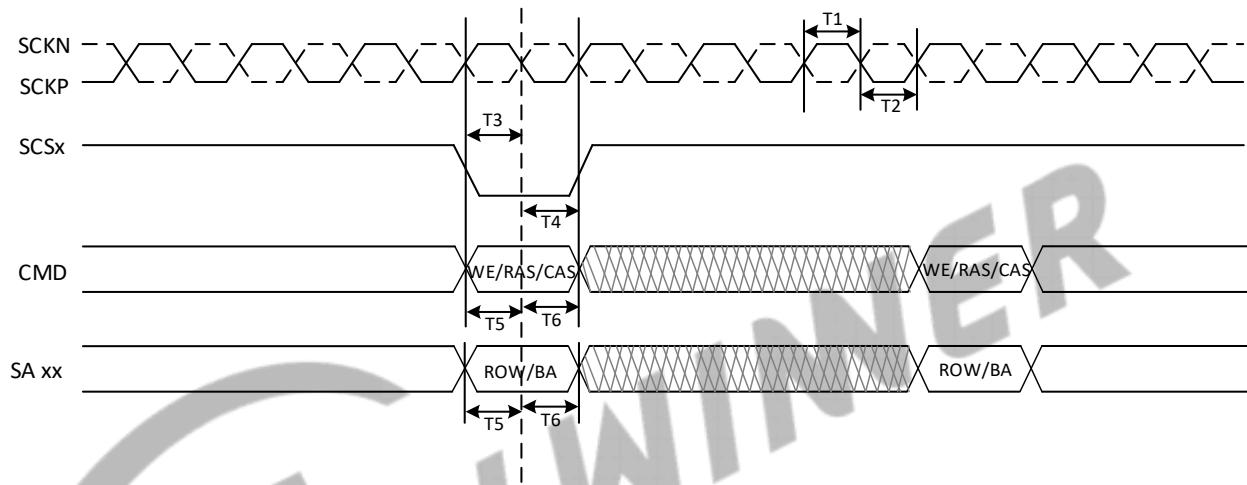


Table 2-16 DDR3/DDR3L Timing Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T1	Clock high-level width	t_{CH}	0.47	-	0.53	tck
T2	Clock low-level width	t_{CL}	0.47	-	0.53	tck
T3	CS setup time	t_{IS}	170	295	-	ps
T4	CS hold time	t_{IH}	120	245	-	ps
T5	Command and Address setup time to Clock edge	t_{IS}	170	295	-	ps
T6	Command and Address hold time to Clock edge	t_{IH}	120	245	-	ps

T1 and T2 are in reference to Vref level.

T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

The following figure shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 2-17.

Figure 2-5 DDR3/DDR3L Write Cycle

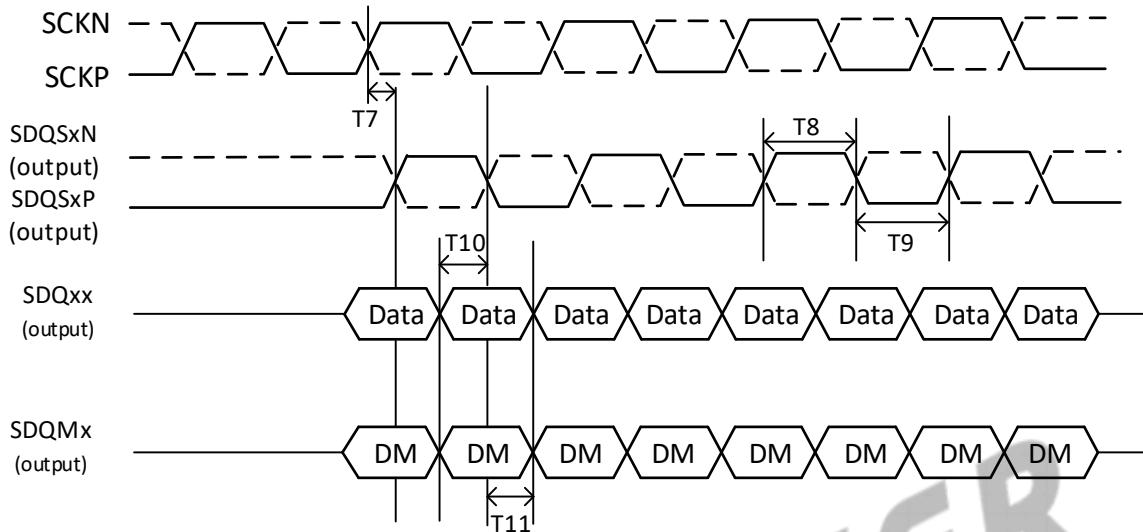


Table 2-17 DDR3/DDR3L Write Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQS high level width	t_{DQSH}	0.45	-	0.55	t_{CK}
T9	SDQS low level width	t_{DQSL}	0.45	-	0.55	t_{CK}
T10	Data setup time to SDQS	t_{DS}	10	145	-	ps
T11	Data hold time to SDQS	t_{DH}	45	180	-	ps

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.

T7,T8, and T9 are in reference to Vref level.

T10 and T11 are in reference to $V_{ih}(ac) / V_{il}(ac)$ levels. (AC150/DC100).

The following figure shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 2-9.

Figure 2-6 DDR3/DDR3L Read Cycle

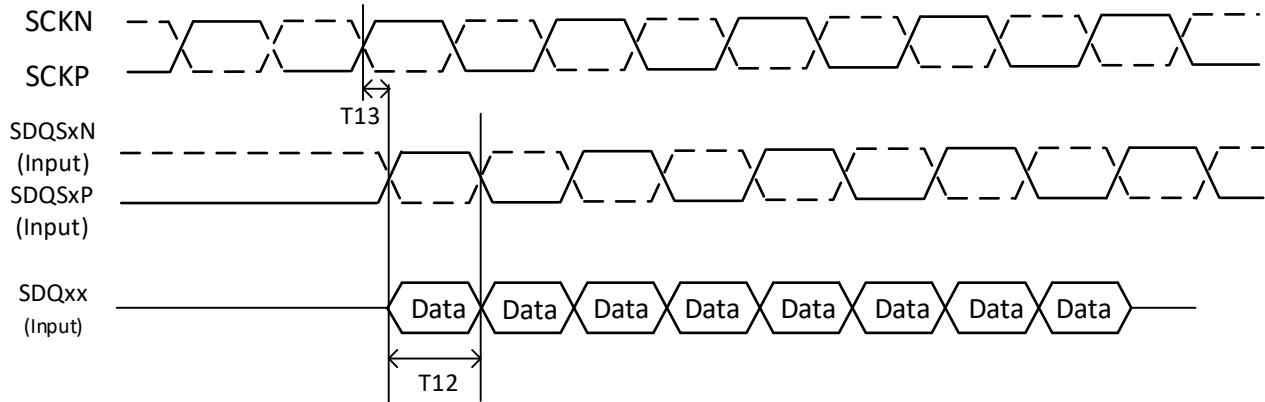


Table 2-18 DDR3/DDR3L Read Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz		Unit
			Min	Max	
T12	Read Data valid width	t_{Data}	200	-	ps
T13	SDQS rising edge to SCK rising edge	t_{DQSCK}	-225	225	ps

T12 and T13 are in reference to V_{ref} level.

2.5.2 SMHC Interface Timing

2.5.2.1 HS-SDR/HS-DDR Mode



NOTE

IO volatage is 1.8V or 3.3V.

Figure 2-7 SMHC HS-SDR Mode Output Timing Diagram

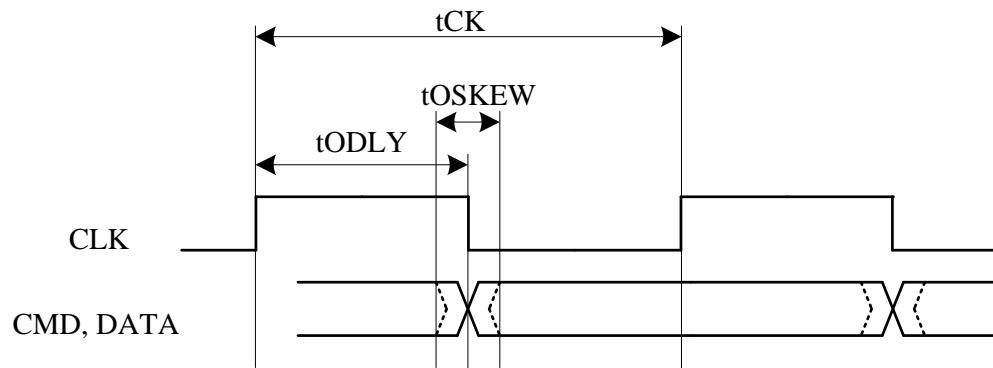


Figure 2-8 SMHC HS-DDR Mode Output Timing Diagram

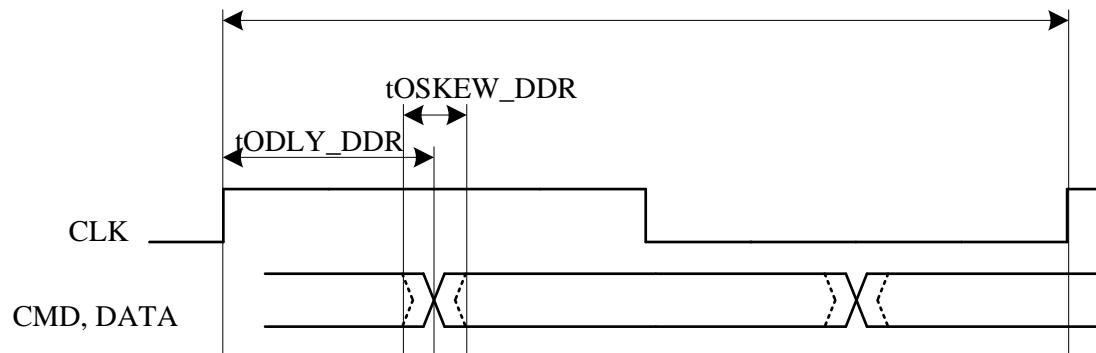


Table 2-19 SMHC HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	t_{CK}	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	t_{ODLY}	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	t_{ODLY_DDR}	-	0.25	0.25	UI	
Data output delay skew time	t_{OSKEW}	-	-		ns	

NOTE
Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.
The GPIO's driver strength level is 2 for test.

Figure 2-9 SMHC HS-SDR Mode Input Timing Diagram

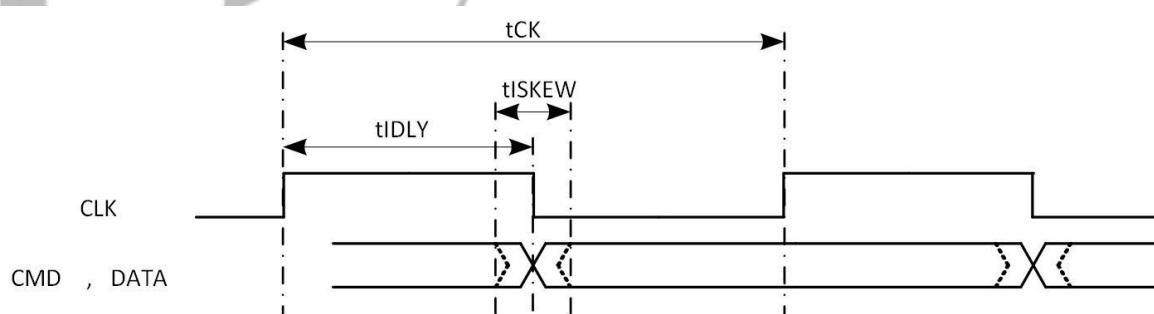


Figure 2-10 SMHC HS-DDR Mode Input Timing Diagram

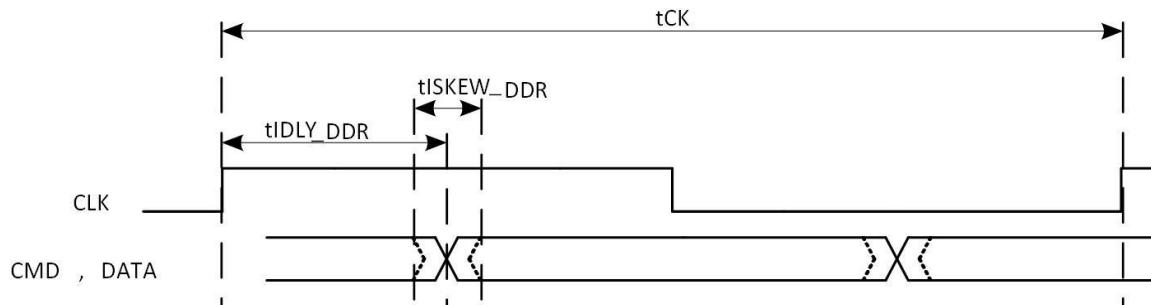


Table 2-20 SMHC HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	-	ns	
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	-	ns	
Data input skew time in SDR mode	tISKEW	-	-	-	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	-	ns	
NOTE The GPIO's driver strength level is 2 for test.						

2.5.2.2 HS200 Mode

Figure 2-11 SMHC HS200 Mode Output Timing Diagram

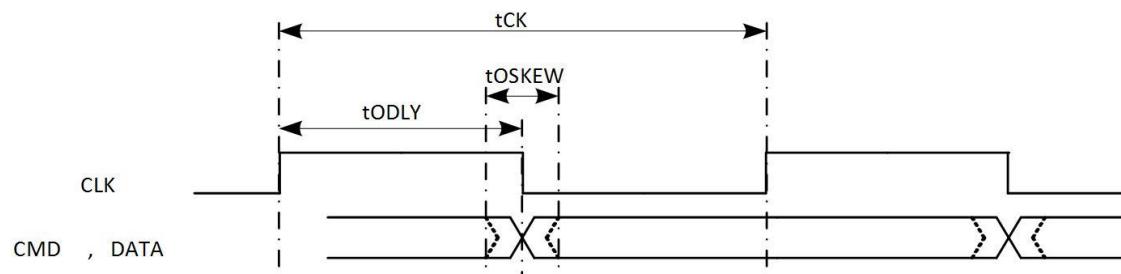


Table 2-21 SMHC HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-		ns	

NOTE
Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.
The GPIO's driver strength level is 3 for test.

Figure 2-12 SMHC HS200 Mode Input Timing Diagram

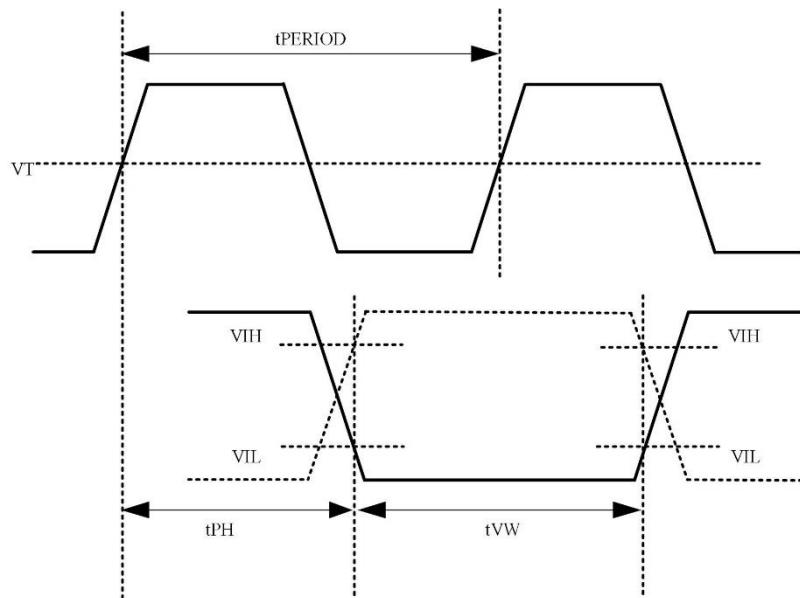


Table 2-22 SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350 ^[3]	-	1550 ^[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
NOTE (1): Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.						
NOTE (2): The GPIO's driver strength level is 3 for test.						
NOTE (3): Temperature variation: -20°C.						
NOTE (4): Temperature variation: 90°C.						

2.5.2.3 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 2-13 SMHC HS400 Mode Data Output Timing Diagram

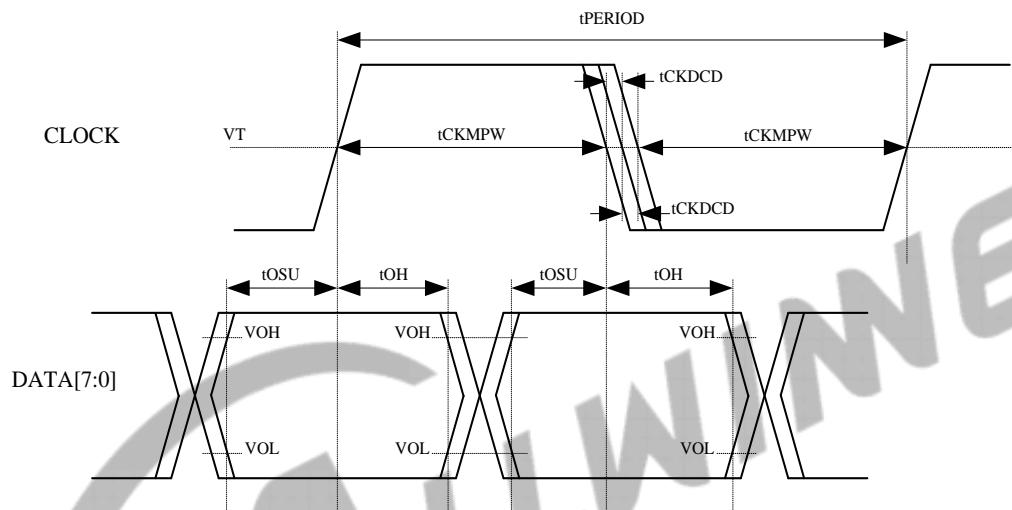


Table 2-23 SMHC HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	V/ns	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
 NOTE						
Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. The GPIO's driver strength level is 3 for test.						

Figure 2-14 SMHC HS400 Mode Data Input Timing Diagram

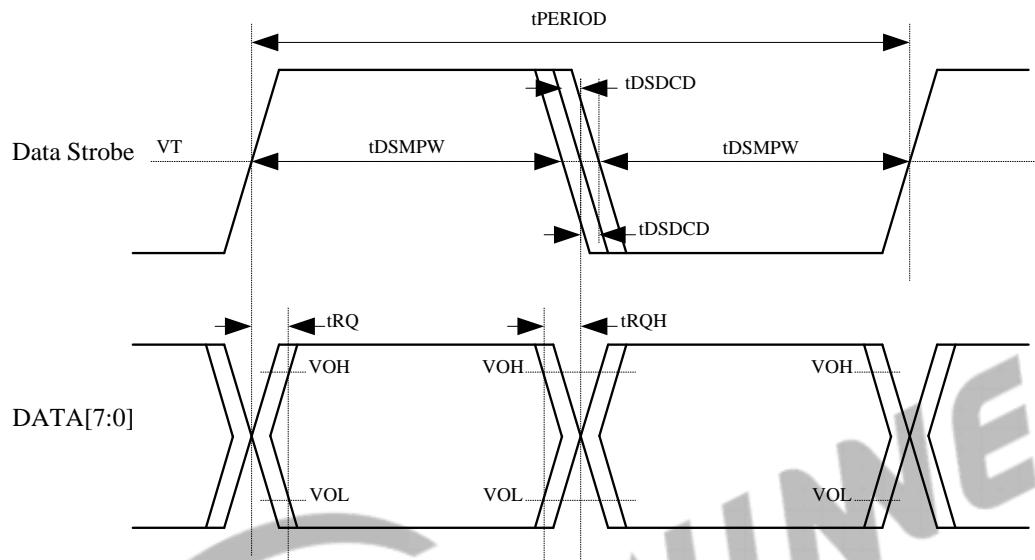


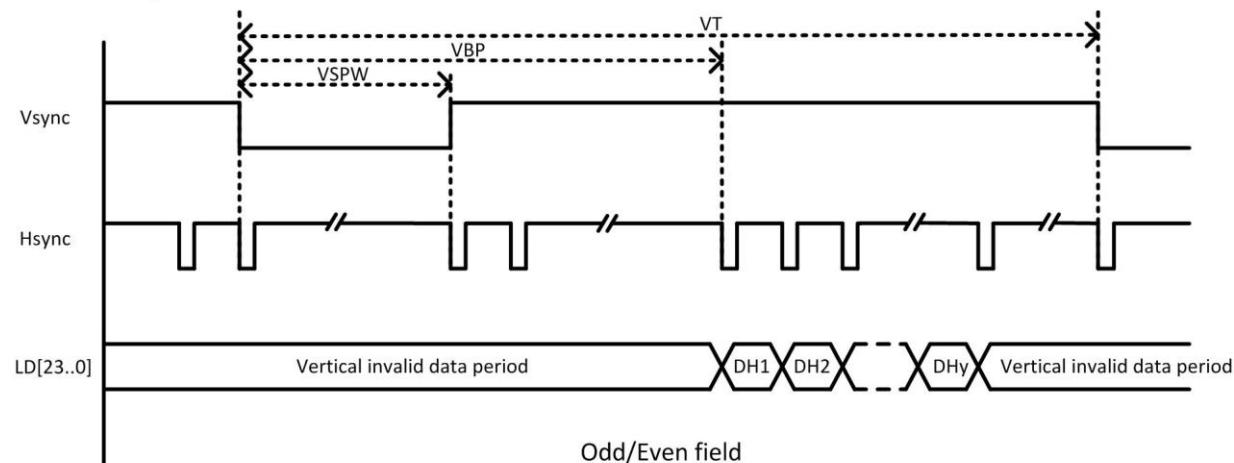
Table 2-24 SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
 NOTE						
Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. The GPIO's driver strength level is 3 for test.						

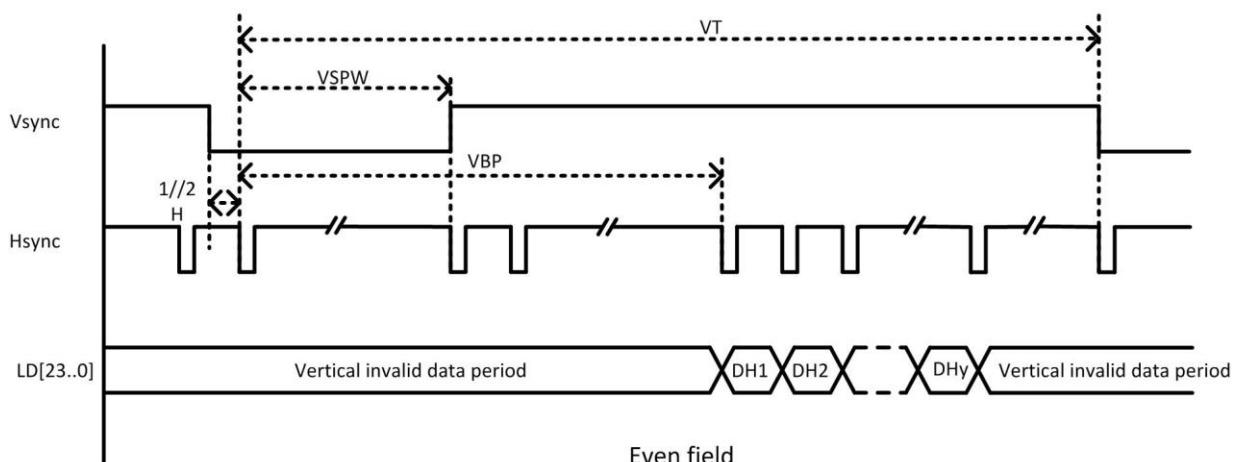
2.5.3 LCD Interface Timing

Figure 2-15 HV_IF Interface Vertical Timing

Vertical Timing



Odd/Even field



Even field



Figure 2-16 HV Interface Horizontal Timing

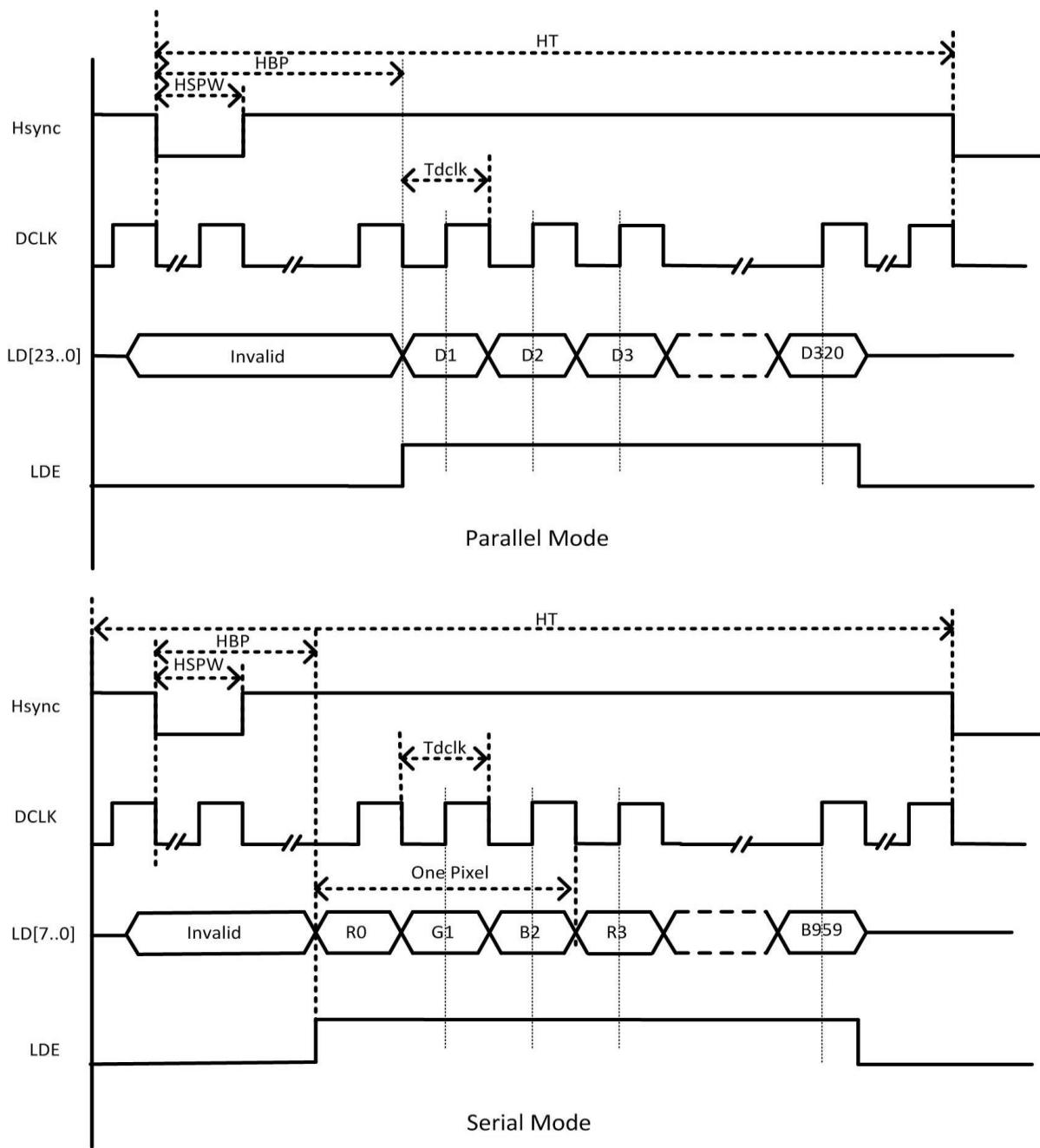


Table 2-25 HV Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
 NOTE					
Vsync: Vertical sync, indicates one new frame					
Hsync: Horizontal sync, indicates one new scan line					
DCLK: Dot clock, pixel data are sync by this clock					
LDE: LCD data enable					
LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel					

2.5.4 CSI Interface Timing

Figure 2-17 CSI Interface Timing

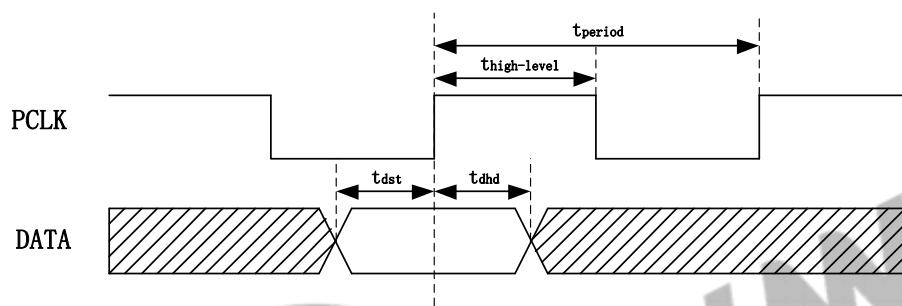


Table 2-26 CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.7	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	150	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{ddh}	0.6	-	-	ns

2.5.5 EMAC Interface Timing

2.5.5.1 RGMII

Figure 2-18 RGMII Transmit Timing

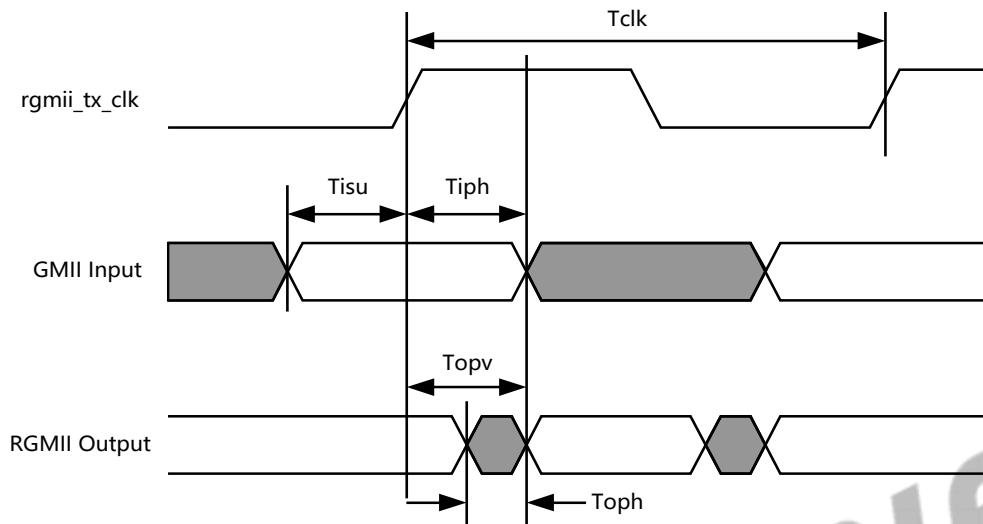


Table 2-27 RGMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_tx_clk clock period	Tclk	8	-	DC	ns
RGMII/TBI input set up prior to rgmii_tx_clk	Tisu	2.8	-	-	ns
RGMII/TBI input data hold after rgmii_tx_clk	Tiph	0.1	-	-	ns
RGMII output data valid after rgmii_tx_clk	Topv	-	-	0.85	ns
RGMII output data hold after rgmii_tx_clk	Toph	0	-	-	ns

Figure 2-19 RGMII Receive Timing

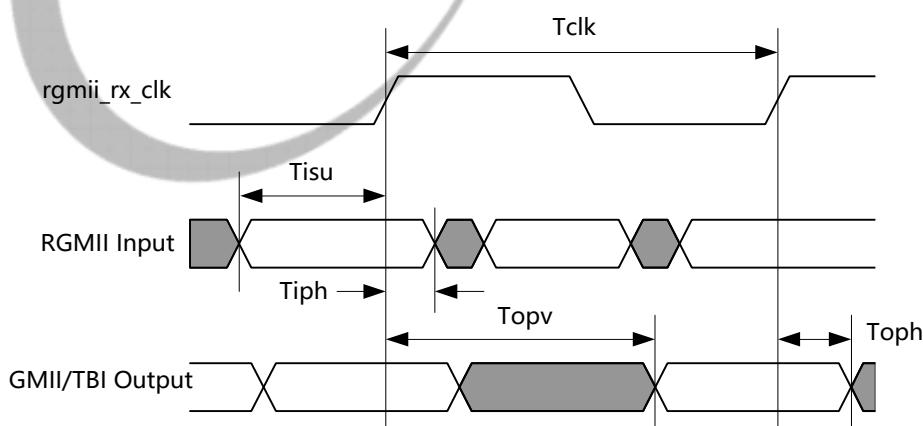


Table 2-28 RGMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_rx_clk clock period	Tclk	8	-	DC	ns
RGMII input set up prior to rgmii_rx_clk	Tisu	2.6	-	-	ns

RGMII input data hold after rgmii_rx_clk	Tiph	0.8	-	-	ns
GMII/TBI input data valid after rgmii_rx_clk	Topv	-	-	5.2	ns
GMII output data hold after rgmii_rx_clk	Toph	0.1	-	-	ns
TBI output data hold after rgmii_rx_clk		0.5			

2.5.5.2 RMII

Figure 2-20 RMII Transmit Timing

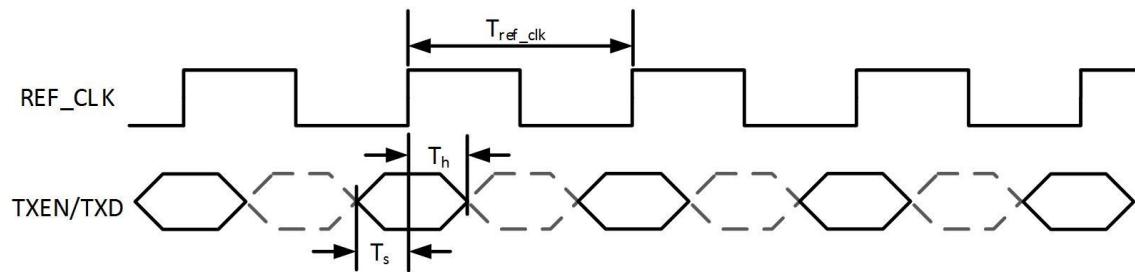


Table 2-29 RMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock Period	T_{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	T_s	4	-	T_h	TXD/TXEN to REF_CLK hold time

Figure 2-21 Receive Timing

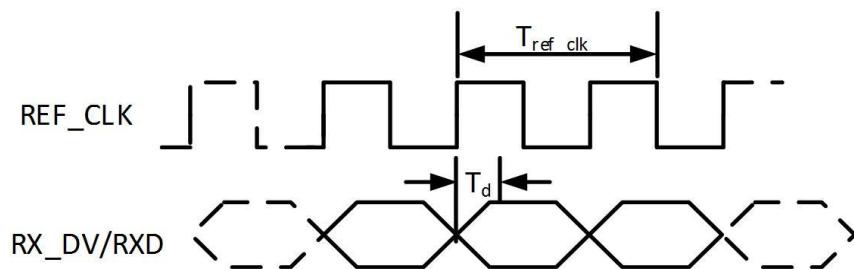


Table 2-30 RMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock Period	T_{ref_clk}	-	20	-	ns
REF_CLK rising edge to RX_DV/RXD	T_d	-	10	12	ns

2.5.6 I2S/PCM Interface Timing

Figure 2-22 I2S/PCM in Master Mode Timing

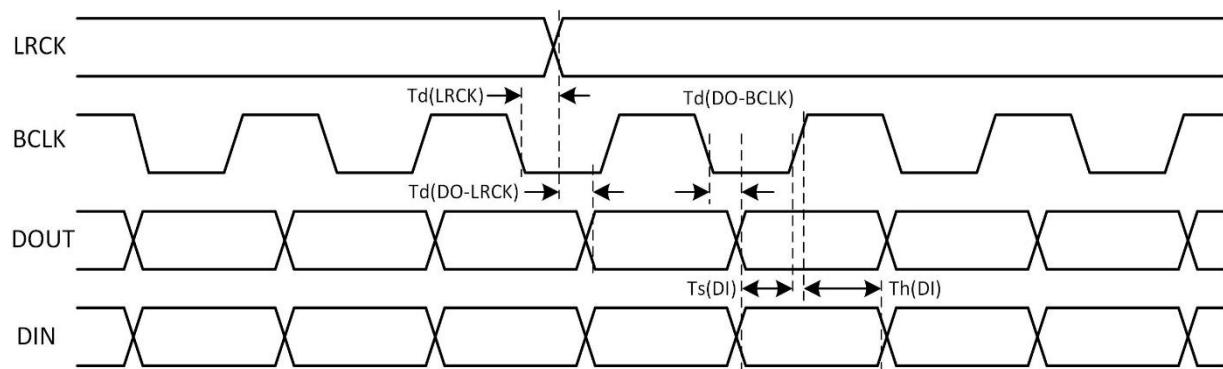


Table 2-31 I2S/PCM in Master Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Delay	$T_d(LRCK)$	-	-	10	ns
LRCK to DOUT Delay(For Ljf)	$T_d(DO-LRCK)$	-	-	10	ns
BCLK to DOUT Delay	$T_d(DO-BCLK)$	-	-	10	ns
DIN Setup	$T_s(DI)$	4	-	-	ns
DIN Hold	$T_h(DI)$	4	-	-	ns
BCLK Rise Time	T_r	-	-	8	ns
BCLK Fall Time	T_f	-	-	8	ns

Figure 2-23 I2S/PCM in Slave Mode Timing

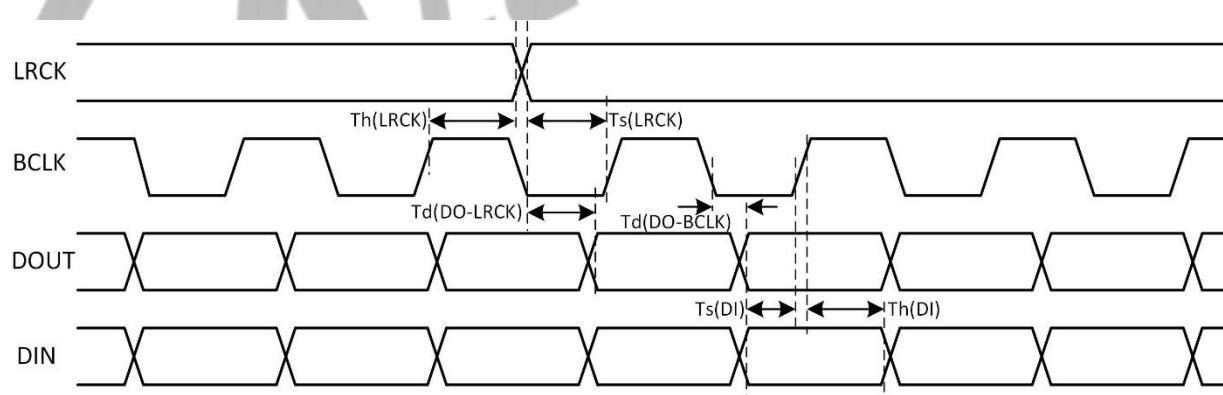


Table 2-32 I2S/PCM in Slave Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Setup	$T_s(LRCK)$	4	-	-	ns
LRCK Hold	$T_h(LRCK)$	4	-	-	ns
LRCK to DOUT Delay(For Ljf)	$T_d(DO-LRCK)$	-	-	10	ns
BCLK to DOUT Delay	$T_d(DO-BCLK)$	-	-	10	ns
DIN Setup	$T_s(DI)$	4	-	-	ns
DIN Hold	$T_h(DI)$	4	-	-	ns
BCLK Rise Time	T_r	-	-	4	ns

Parameter	Symbol	Min	Typ	Max	Unit
BCLK Fall Time	T_f	-	-	4	ns

2.5.7 DMIC Interface Timing

Figure 2-24 DMIC Timing

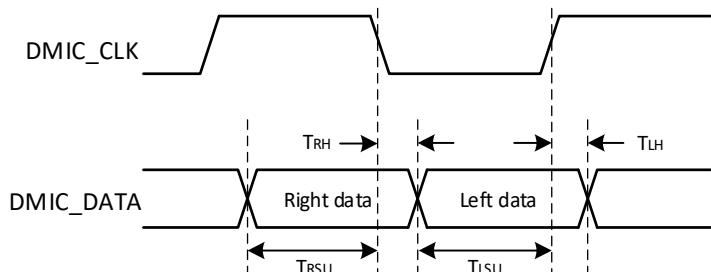


Table 2-33 DMIC Timing Constants

PARAMETER		MIN	MAX	UNITS
TRSU	DMIC_DATA(Right) setup time to falling DMIC_CLK edge	15		ns
TRH	DMIC_DATA(Right) hold time from falling DMIC_CLK edge	0		ns
TLSU	DMIC_DATA(Left) setup time to rising DMIC_CLK edge	15		ns
TLH	DMIC_DATA(Left) hold time from rising DMIC_CLK edge	0		ns

2.5.8 SPI Interface Timing

Figure 2-25 SPI MOSI Timing

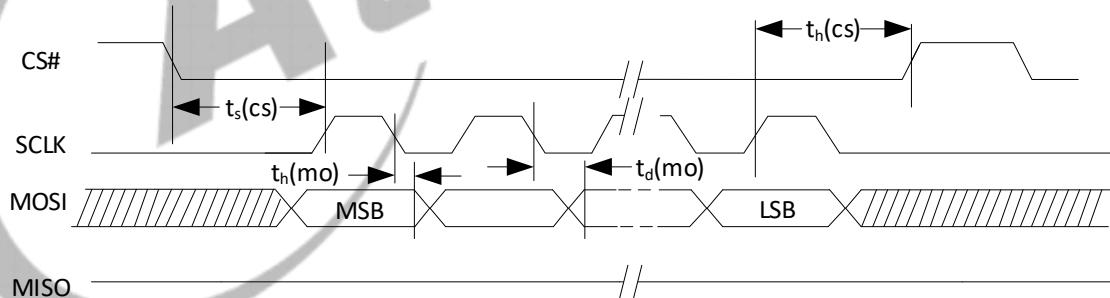


Figure 2-26 SPI MISO Timing

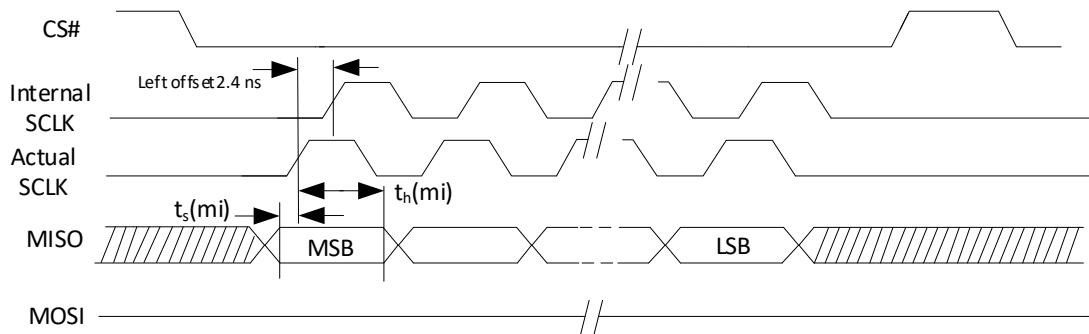


Table 2-34 SPI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CS# Active Setup Time	$t_s(cs)$	-	$2T^{(1)}$	-	ns
CS# Active Hold Time	$t_h(cs)$	-	$2T^{(1)}$	-	ns
Data output delay time	$t_d(mo)$	-	$T^{(1)}/2-3$	-	ns
Data output hold time	$t_h(mo)$	-	$T^{(1)}/2-3$	-	ns
Data In Setup Time	$t_s(mi)$	0.2	-	-	ns
Data In Hold Time	$t_h(mi)$	0.2	-	-	ns



NOTE

T is the cycle of clock.

2.5.9 UART Interface Timing

Figure 2-27 UART RX Timing

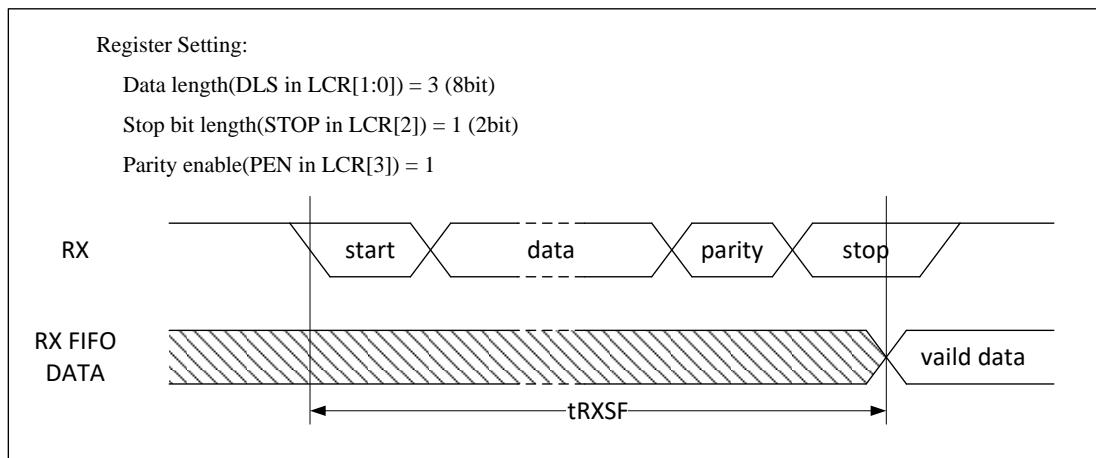


Figure 2-28 UART nCTS Timing

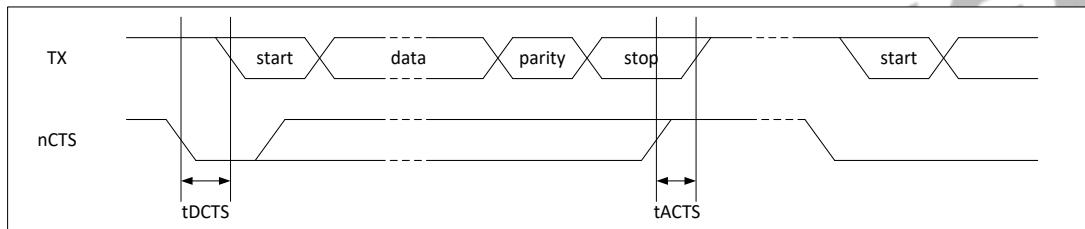


Figure 2-29 UART nRTS Timing

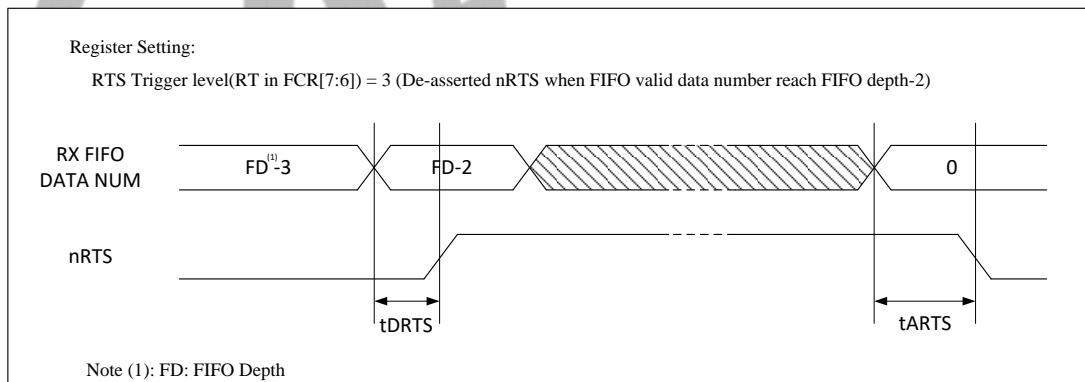


Table 2-35 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP ⁽¹⁾	-	11× BRP	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP ⁽¹⁾ /4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP	ns
Delay time of asserted nRTS	tARTS	-	-	BRP	ns

Parameter	Symbol	Min	Typ	Max	Unit
NOTE BRP: Baud-Rate Period.					

2.5.10 TWI Interface Timing

Figure 2-30 TWI Timing

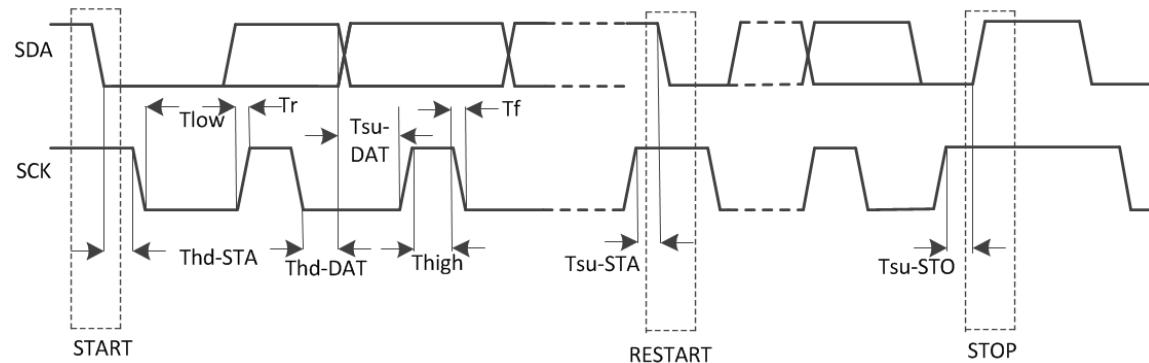


Table 2-36 TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in start	Tsu-STA	4.7	-	0.6	-	us
Hold time in start	Thd-STA	4.0	-	0.6	-	us
Setup time in data	Tsu-DAT	250	-	100	-	ns
Hold time in data	Thd-DAT	5.0	-	-	-	ns
Setup time in stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

2.5.11 MIPI DSI Interface Timing

Figure 2-31 MIPI DSI Timing Diagram

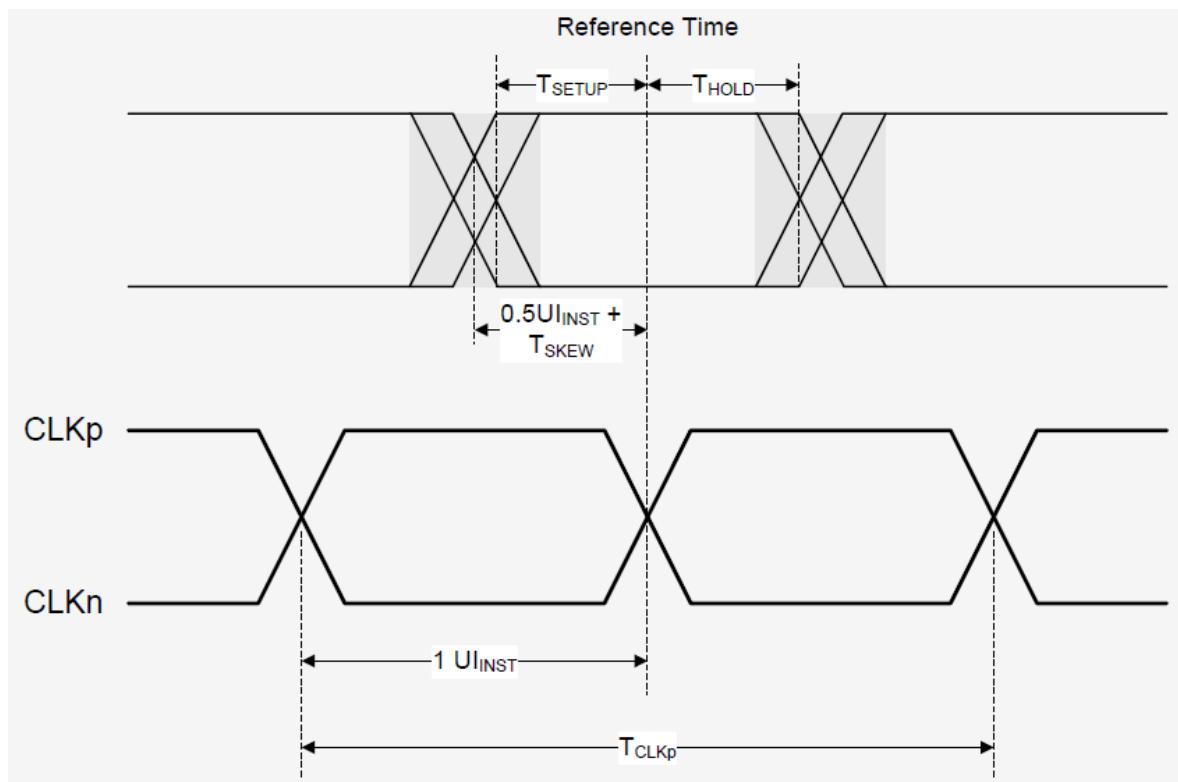


Table 2-37 MIPI DSI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Data to Clock Skew	T _{skew}	-0.15	-	0.15	UI _{INST}
Data to Clock Setup Time	T _{setup}	0.15	-	-	UI _{INST}
Clock to Data Hold Time	T _{hold}	0.15	-	-	UI _{INST}

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3 System

3.1 Memory mapping

Module	RISCV Address	Size (Bytes)
BROM & SRAM		
N-BROM	0x0000 0000—0x0000 DFFF	56KB
SRAM C	0x0002 0000---0x0004 0FFF	132K (Using ISP SRAM)
VE_SYS		
VE	0x01C0 E000---0x01C0 FFFF	8K
SP0		
GPIO	0x0200 0000---0x0200 07FF	2K
PWM	0x0200 0C00---0x0200 0FFF	1K
CCMU	0x0200 1000---0x0200 1FFF	4K
GPADC	0x0200 9000---0x0200 93FF	1K
THS	0x0200 9400---0x0200 97FF	1K
IOMMU	0x0201 0000---0x0201 FFFF	64K
WIREGAND	0x0202 0000---0x0202 03FF	1K
Audio_Codec	0x0203 0000---0x0203 0FFF	4K
DMIC	0x0203 1000---0x0203 13FF	1K
I2S0	0x0203 2000---0x0203 2FFF	4K
I2S1	0x0203 3000---0x0203 3FFF	4K
TIMER	0x0205 0000---0x0205 0FFF	4K
SP1		
UART0	0x0250 0000---0x0250 03FF	1K
UART1	0x0250 0400---0x0250 07FF	1K
UART2	0x0250 0800---0x0250 0BFF	1K
UART3	0x0250 0C00---0x0250 0FFF	1K
TWI0	0x0250 2000---0x0250 23FF	1K
TWI1	0x0250 2400---0x0250 27FF	1K
TWI2	0x0250 2800---0x0250 2BFF	1K
TWI3	0x0250 2C00---0x0250 2FFF	1K
TWI4	0x0250 3000---0x0250 33FF	1K
SH0		
SYSCTRL	0x0300 0000---0x0300 0FFF	4K
DMAC	0x0300 2000---0x0300 2FFF	4K
CPUX_MSGBOX	0x0300 3000---0x0300 3FFF	4K
SPINLOCK	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 6FFF	4K
HSTIMER	0x0300 8000---0x0300 8FFF	4K
DCU	0x0301 0000---0x0301 FFFF	64K (Only external AHB access)
CPU_GIC	0x0302 0000---0x0302 FFFF	64K

Module	RISCV Address	Size (Bytes)
CE_NS	0x0304 0000---0x0304 07FF	2K
NPU	0x0305 0000---0x0305 0FFF	4K
MSI+MEMC	0x0310 2000---0x0330 1FFF	2M
SH2		
SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
SPI0	0x0402 5000---0x0402 5FFF	4K
SPI1	0x0402 6000---0x0402 6FFF	4K
SPI2	0x0402 7000---0x0402 7FFF	4K
SPI3	0x0402 8000---0x0402 8FFF	4K
USBO	0x0410 0000---0x041F FFFF	1M
EMAC	0x0450 0000---0x0450 FFFF	64K
VIDEO_OUT_SYS		
DE	0x0500 0000---0x053F FFFF	4M
G2D	0x0541 0000---0x0544 FFFF	256K
DSI0	0x0545 0000---0x0545 1FFF	8K
DISPLAY_TOP	0x0546 0000---0x0546 0FFF	4K
TCON_LCDO	0x0546 1000---0x0546 1FFF	4K
VIDEO_IN_SYS		
CSI	0x0580 0000---0x058F FFFF	1M
ISP	0x0590 0000---0x05CF FFFF	4M
RISCV_SYS		
RISCV_CFG	0x0601 0000---0x0601 0FFF	4K
RISCV_WDG	0x0601 2000---0x0601 2FFF	4K
RISCV_TIMESTAMP	0x0601 4000---0x0601 4FFF	4K
RISCV_TIMER	0x0601 5000---0x0601 53FF	1K
RISCV_MSGBOX1	0x0602 0000---0x0602 0FFF	4K (only RISC CPU access)
APBS0		
R_CPUFCFG	0x0700 0400---0x0700 0BFF	2K
R_PPU	0x0700 1000---0x0700 13FF	1K
R_SPC	0x0700 2000---0x0700 23FF	1K
R_PRCM	0x0701 0000---0x0701 FFFF	64K
R_TWD	0x0702 0800 – 0x0702 0BFF	1K
AHBS		
RTC	0x0709 0000---0x0709 03FF	1K
CPUX Related		
CPU_SYS_CFG	0x0810 0000---0x0810 03FF	1K
TIMESTAMP_STA	0x0811 0000---0x08011 0FFF	4K
TIMESTAMP_CTRL	0x0812 0000---0x0812 0FFF	4K
IDC	0x0813 0000---0x0813 0FFF	4K
CO_CPUX_CFG	0x0901 0000---0x0901 03FF	1K

Module	RISCV Address	Size (Bytes)
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K
RISC CPU Interrupts (Only RISC CPU access)		
RISCV_CLINT	0x3000 0000---0x3000 FFFF	
RISCV_CLIC	0x3080 0000---0x3080 4FFF	
RESERVE	0x3080 5000---0x3FFF FFFF	
DRAM Space		
DRAM SPACE	0x4000 0000---0xBFFF FFFF	2G



3.2 CPUX Configuration

3.2.1 Overview

The CPUX Configuration(CPUX_CFG) module is used to configure CLUSTER0 control, including power on, reset, cache, debug, and check the status of CPU. It will be used when you want to disable/enable the CPU, cluster switch, CPU status check, and debug, etc.

The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as GIC-400, JTAG.

The CPUX configuration includes the following features:

- CPU reset system: CORE reset, debug circuit reset and other reset function
- CPU related control: interface control, CP15 control, power on and power down control
- CPU status check: idle status, SMP status, interrupt status and so on
- CPU debug related register for control and status

3.2.2 CPUX Power Block Diagram

Figure 3-1 CPUX Power Domain Diagram

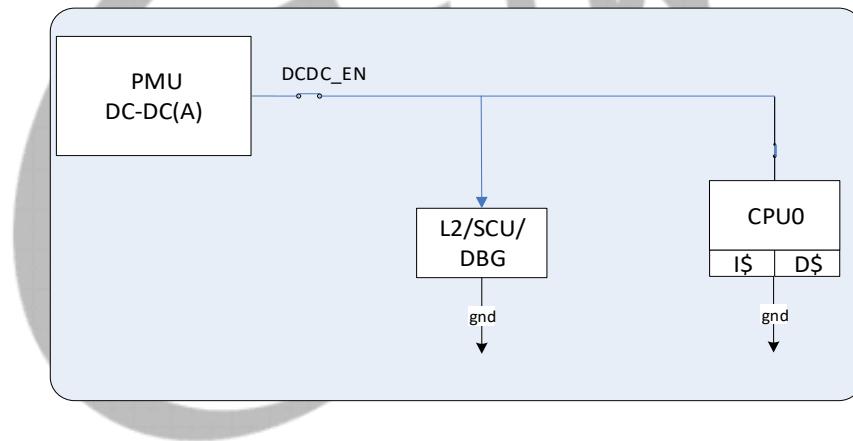


Figure 3-1 above lists the power domain of CLUSTER in default. All power switch of CPU core are default to power on. All CPU pwron_rst is de-asserted, core reset of CPU0 is de-asserted, core reset of CPU1 is asserted.

Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

CPU_SUBSYS_CTRL belongs to system power domain. The power domains of CPU related module are as follows.

Table 3-1 Power Attributes

Power Domain	Modules	Description
Cluster0	Cluster0/C0_CPUX_CFG/C0_MBIST	Cluster0 circuit, C0_CPUX_CFG module and CPU reset/power(mbist)

Power Domain	Modules	Description
System	Timestamp/GIC/CPU_SUBSYS_CTRL/Clock	Provide system source of CPU sub-system

3.2.3 Operations and Functional Descriptions

3.2.3.1 Signal Description

For the detail of CPUX signal, please refer to **ARM Cortex-A7 TRM**.

3.2.3.2 L2 Idle Mode

When the L2 of Cluster needs to enter WFI mode, firstly make sure the CPU0/1 of Cluster enter WFI mode, which can be checked through the bit[17:16] of **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing 1 to the bit0 of **Cluster Control Register1**, and then check whether L2 enters idle status by checking whether the **STANDBYWFL2** is high. Remember to set the **ACINACTM** to low when exiting the L2 idle mode.

3.2.3.3 CPUX Reset System

The CPUX reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset < power-on Reset < H_Reset**. The description of all reset signal in CPUX Reset System is as follows.

Table 3-2 Reset Signal Description

Reset signal	Description
CORE_RST	This is the primary reset signal which resets the corresponding core logic that includes NEON and VFP, Debug, ETM, breakpoint and watchpoint logic. This maps to a warm reset that covers reset of the processor logic.
PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. This maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Reset all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/CO_CPUX_CFG.
CPU_SUBSYS_RST	Including CO_H_RST/GIC-400/CPU_SUBSYS_CTRL.

3.2.3.4 Operation Principle

The CPU-related operation needs proper configuration of CPUCFG related register, as well as related system control resource including BUS, clock , reset and power control.

3.2.4 Programming Guidelines

For CPU core and cluster operation,please see *V853/V853S_CPU_AP_Note.pdf*.

3.2.5 Cluster Configuration Register List

Module Name	Base Address	Comments
C0_CPUX_CFG	0x09010000	Cluster0 CPUX configuration register

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1
C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
CACHE_CFG_REG	0x0024	Cache Configuration Register
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	L2 Status Register
DBG_REG0	0x00C0	Cluster 0 Debug Control Register0
DBG_REG1	0x00C4	Cluster 0 Debug Control Register1

3.2.6 Cluster Configuration Register Description

3.2.6.1 0x0000 Cluster 0 Reset Control Register (Default Value:0x13FF_0101)

Offset:0x0000			Register Name:C0_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: Assert 1: De-Assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal for test 0: Assert 1: De-Assert

Offset:0x0000			Register Name:C0_RST_CTRL
Bit	Read/Write	Default/Hex	Description
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: Assert 1: De-Assert
23:20	R/W	0xF	ETM_RST Cluster ETM Reset Assert 0: Assert 1: De-Assert
19:16	R/W	0xF	DBG_RST Cluster Debug Reset Assert 0: Assert 1: De-Assert
15:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: Assert 1: De-Assert.
7:1	/	/	/
0	R/W	0x1	CORE_RESET Core Reset Cluster CPU0 Reset Assert 0: Assert 1: De-Assert

3.2.6.2 0x0010 Cluster 0 Control Register0 (Default Value:0x8000_0000)

Offset:0x0010			Register Name:C0_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus: 0: Barriers are broadcast onto system bus, this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus. This is compatible with an AXI3 interconnect.
30	R/W	0x0	BROADCAST_INNER Enable broadcasting of Inner Shareable transactions: 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.

Offset:0x0010			Register Name:C0_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	BROADCAST_OUTER Enable broadcasting of outer shareable transactions: 0: Outer Shareable transactions are not broadcasted externally. 0: Outer Shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches: 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:24	/	/	/
23:12	/	/	/
11:8	R/W	0x0	CP15S_DISABLE Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset: 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3:1	/	/	/
0	R/W	0x0	L1_RST_DISABLE L1 Cache Reset Disable Disable automatic Cluster CPU0 L1 cache invalidate at reset: 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.2.6.3 0x0014 Cluster 0 Control Register1 (Default Value:0x0000_0000)

Offset:0x0014			Register Name:C0_CTRL_REG1
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	CRM_SEL_EN CRM Auto Select Slow Frequency En 0: Disable auto select 1 : Enable auto select

Offset:0x0014			Register Name:C0_CTRL_REG1
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepting requests. 0: Snoop interface is active 1: Snoop interface is inactive

3.2.6.4 0x0018 Cluster 0 Control Register2 (Default Value:0x0000_0010)

Offset:0x0018			Register Name:C0_CTRL_REG2
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake up from WFE state This bit must remain HIGH for at least one clock cycle to be visible by the cores.
23:21	/	/	/
20	R/W	0x0	EXM_CLR Clear the status of interface EXM_CLR
19:0	R/W	0x10	Reserved

3.2.6.5 0x0024 Cache Configuration Register (Default Value:0x0018_001A)

Offset: 0x0024			Register Name: CACHE_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:19	R/W	0x3	EMA_L2D L2 Cache SRAM EMA Control Port
18:17	R/W	0x0	EMAW_L2D L2 Cache SRAM EMAW Control Port
16	R/W	0x0	EMAS_L2D L2 Cache SRAM EMAS Control Port
15:12	/	/	/
11:8	R/W	0x0	DVS FARADAY SRAM Delay Signal
7	R/W	0x0	DVSE FARADAY SRAM Delay Enable Signal
6	R/W	0x0	STOV STOV

Offset: 0x0024			Register Name: CACHE_CFG_REG
Bit	Read/Write	Default/Hex	Description
5:3	R/W	0x3	EMA Cache SRAM EMA Control Port
2:1	R/W	0x1	EMAW Cache SRAM EMAW Control Port
0	R/W	0x0	EMAS Cache SRAM EMAS Control Port

3.2.6.6 0x0080 Cluster 0 CPU Status Register (Default Value:0x000E_0000)

Offset:0x0080			Register Name:C0_CPU_STATUS
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R	0x0	SMP_AMP AMP Mode or SMP Mode CPU0 is in Symmetric Multiprocessing mode or Asymmetric Multiprocessing mode. 0: AMP mode 1: SMP mode
23:17	/	/	/
16	R	0xE	STANDBYWFI WFI Standby Mode Indicates if Cluster CPU0 is in WFI standby mode. 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:9	/	/	/
8	R	0x0	STANDBYWFE WFE Standby Mode Indicates if Cluster CPU0 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFI2 L2 WFI Standby Mode Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

3.2.6.7 0x0084 L2 Status Register (Default Value:0x0000_0000)

Offset:0x0084			Register Name:L2_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R	0x0	EVENTO Event Output This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8:0	/	/	/

3.2.6.8 0x00C0 Cluster 0 Debug Control Register0 (Default Value:0x0000_000F)

Offset:0x00C0			Register Name:DBG_REG0
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	EX_RST_REQ External Restart Requests DBGRESTART
7:4	/	/	/
3:0	R/W	0xF	C_DBGPWDUP Cluster Powered Up 0: Core is powered down 1: Core is powered up

3.2.6.9 0x00C4 Cluster 0 Debug Control Register1 (Default Value:0x0000_0000)

Offset:0x00C4			Register Name:DBG_REG1
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	DBGRESTARTED Handshake for DBGRESTART DBGRESTARTED
11:5	/	/	/
4	R	0x0	C_DBGNOPWRDWN No power down request. Debugger has requested that processor is not powered down. Debug no power down
3:1	/	/	/

Offset:0x00C4			Register Name:DBG_REG1
Bit	Read/Write	Default/Hex	Description
0	R	0x0	C_DBGPWRUPREQ Power Up Request Debug power up request 0: Do not request that the core is powered up 1: Request that the core is powered up

3.2.7 CPU Subsystem Control Register List

Module Name	Base Address	Comments
CPU_SUBSYS_CTRL	0x08100000	CPU subsystem control

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GIC_JTAG_RST_CTRL	0x000C	GIC and Jtag reset control Register
C0_INT_EN	0x0010	CLUSTER_0 Interrupt Enable Register
IRQ_FIQ_STATUS	0x0014	GIC IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2
DBG_STATE	0x001C	Debug State Register

3.2.8 CPU Subsystem Control Register Description

3.2.8.1 0x0000 General Control Register0 (Default Value:0x0000_0000)

Offset:0x0000			Register Name:GENER_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	C0_corepll_SEL Cluster 0 Corepll Select Register width state: 0: CCU clock; 1: DISP PLL clock.
1	R/W	0x0	IDC_CLK_EN IDC clock enable 0: Disable IDC clock; 1: Enable IDC clock.
0	R/W	0x0	GIC_CFGSDISABLE Disables write access to some secure GIC registers.

3.2.8.2 0x000C GIC and Jtag reset control Register (Default Value:0x0000_0F07)

Offset:0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EXM_CLR Clear the status of interface for debug EXM_CLR
15:12	/	/	/
11	R/W	0x1	CS_RST CoreSight Reset 0: Assert 1: De-assert.
10	R/W	0x1	DAP_RST DAP Reset 0: Assert 1: De-assert.
9	R/W	0x1	PORTRST JTAG PORTRST 0: assert 1: de-assert.
8	R/W	0x1	TRST JTAG TRST 0: Assert 1: De-assert.
7:3	/	/	/
2	R/W	0x1	Reserved
1	R/W	0x1	IDC_RST Interrupt Delay Controller Reset 0: Assert 1: de-assert.
0	R/W	0x1	GIC_RST GIC_RESET_CPU_REG 0: Assert 1: De-assert.

3.2.8.3 0x0010 CLUSTER_0 Interrupt Enable Register (Default Value:0x0000_FFFF)

Offset:0x0010			Register Name:C0_INT_EN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFFFF	C0_GIC_EN Interrupt Enable Control Register Mask IRQ_OUT/FIRQ_OUT to system domain.

3.2.8.4 0x0014 GIC IRQ/FIQ Status Register (Default Value:0x0000_FFFF)

Offset:0x0014			Register Name: IRQ_FIQ_STATUS
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	FIQ_OUT FIQ interrupt FIQ_OUT[15:0]
15:0	R/W	0xFFFF	IRQ_OUT IRQ interrupt IRQ_OUT[15:0]

3.2.8.5 0x0018 General Control Register2 (Default Value:0x0000_0000)

Offset:0x0018			Register Name:GENER_CTRL_REG2
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CDBGSTACK Debug Reset ACK.
15:2	/	/	/
0	R/W	0x0	C0_TSCLKCHANGE Cluster 0 Time Stamp change bit.

3.3 RISC System

3.3.1 Overview

The RISC system includes RISC IP core and related peripheral devices (RISC_CFG, RISC_TIMESTAMP, Watchdog, PSENSOR, BROM, and so on), which are interconnected by BUS Matrix.

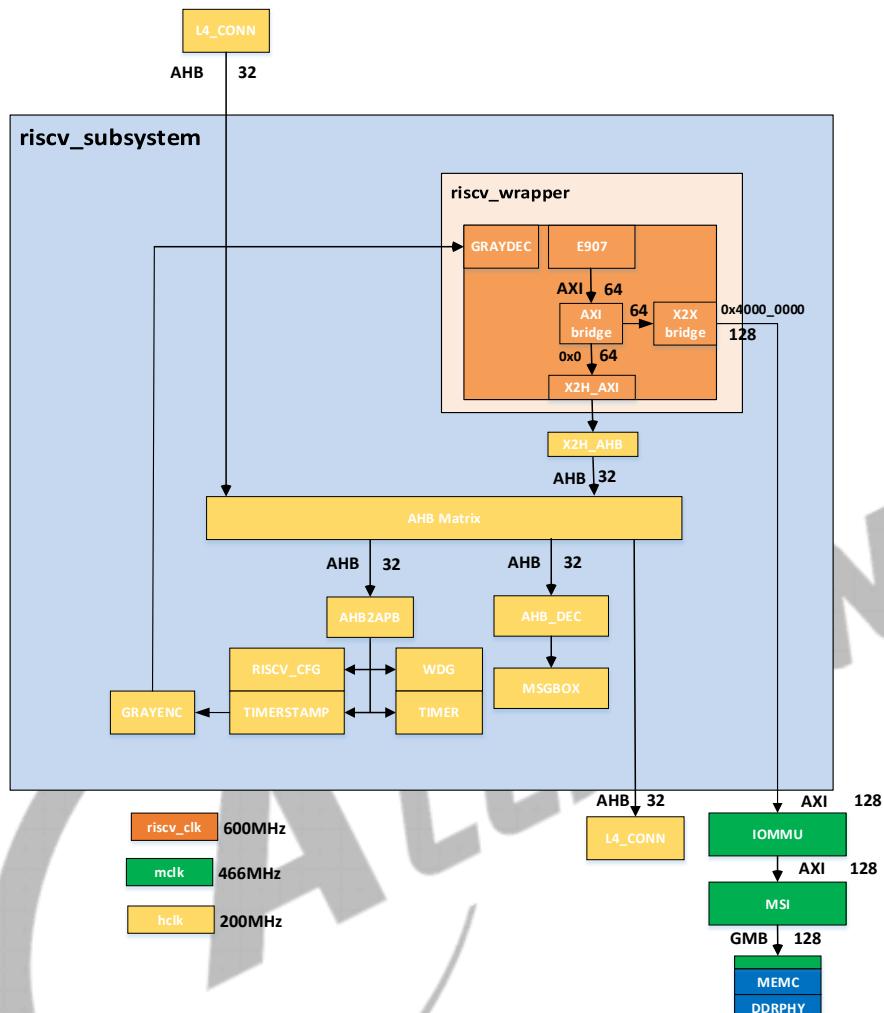
The RISC system has the following features:

- RISC 64GCV instruction architecture
- configurable base address via software
- combined with PPU module, supporting standby in low-power mode and wake-up through external interrupts
- separate timestamp supports timing immediately after reset is released
- separate watchdog supports preventing system from malfunctioning
- separate message box supports communicating with other modules
- supports separate PMU check module

3.3.2 Block Diagram

The following figure shows the block diagram of RISC system.

Figure 3-2 RISCV System Block Diagram



3.3.3 Register List

Module Name	Base Address	Comments
RISCV_CFG	0x0601_0000	

Register Name	Offset	Description
RF1P_CFG_REG	0x0010	RF1P Configuration Register
TS_TMODE_SEL_REG	0x0040	Timestamp Test Mode Select Register
RISCV_STA_ADD_REG	0x0204	RISCV Start Address Register
RISCV_WAKEUP_EN_REG	0x0220	RISCV Wakeup Enable Register
RISCV_WAKEUP_MASK0_REG	0x0224	RISCV Wakeup Mask0 Register
RISCV_WAKEUP_MASK1_REG	0x0228	RISCV Wakeup Mask1 Register

Register Name	Offset	Description
RISCV_WAKEUP_MASK2_REG	0x022C	RISCV Wakeup Mask2 Register
RISCV_WAKEUP_MASK3_REG	0x0230	RISCV Wakeup Mask3 Register
RISCV_WAKEUP_MASK4_REG	0x0234	RISCV Wakeup Mask4 Register
RISCV_WORK_MODE_REG	0x0248	RISCV Work Mode Register
RISCV_AXI_PMU_CTRL	0x0304	RISCV AXI PMU Control Register
RISCV_AXI_PMU_PRD	0x0308	RISCV AXI PMU Period Register
RISCV_AXI_PMU_LAT_RD	0x030C	RISCV AXI PMU Read Latency Register
RISCV_AXI_PMU_LAT_WR	0x0310	RISCV AXI PMU Write Latency Register
RISCV_AXI_PMU_REQ_RD	0x0314	RISCV AXI PMU Read Request Register
RISCV_AXI_PMU_REQ_WR	0x0318	RISCV AXI PMU Write Request Register
RISCV_AXI_PMU_BW_RD	0x031C	RISCV AXI PMU Read Bandwidth Register
RISCV_AXI_PMU_BW_WR	0x0320	RISCV AXI PMU Write Bandwidth Register

3.3.4 Register Description

3.3.4.1 0x0010 RF1P Configuration Register (Default Value: 0x0000_0013)

Offset:0x0010			Register Name: RF1P_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x13	RF1P_CFG. RF1P Configuration.

3.3.4.2 0x0040 Timestamp Test Mode Select Register (Default Value: 0x0000_0000)

Offset:0x0040			Register Name: TS_TMODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	RISCV_TS_TEST_MODE_EN. RISCV Timestamp Test Mode Enable. 0: Normal Mode 1:Test Mode
0	/	/	/

3.3.4.3 0x0204 RISCV Start Address Register (Default Value: 0x0000_0000)

this register is the running PC address after RISCV releases reset. Before releasing reset, this register should be configured. This register does support dynamic configuration.

Offset:0x0204			Register Name: RISCV_STA_ADD0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	STA_ADD. Start Address. The bit0 is fixed as 0 and can not be written.

3.3.4.4 0x0220 RISCV Wakeup Enable Register (Default Value: 0x0000_0000)

Offset:0x0220			Register Name: RISCV_WAKEUP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WP_EN. Wakeup Enable.

3.3.4.5 0x0224 RISCV Wakeup Mask0 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x0224			Register Name: RISCV_WAKEUP_MASK0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK0. Wakeup Mask0.

3.3.4.6 0x0228 RISCV Wakeup Mask1 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x0228			Register Name: RISCV_WAKEUP_MASK1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK1. Wakeup Mask1.

3.3.4.7 0x022C RISCV Wakeup Mask2 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x022C			Register Name: RISCV_WAKEUP_MASK2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK2. Wakeup Mask2.

3.3.4.8 0x00230 RISCV Wakeup Mask3 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x00230			Register Name: RISCV_WAKEUP_MASK3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK3. Wakeup Mask3.

3.3.4.9 0x0234 RISCV Wakeup Mask4 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x0234			Register Name: RISCV_WAKEUP_MASK4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK4. Wakeup Mask4.

3.3.4.10 0x0248 RISCV Work Mode Register (Default Value: 0x0000_000B)

Offset: 0x0248			Register Name: RISCV_WORK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset: 0x0248			Register Name: RISCV_WORK_MODE_REG
Bit	Read/Write	Default/Hex	Description
3	R	0x1	<p>LOCKUP_STA. Lockup Status. 0: Not Lockup 1: Lockup Note: if CPU has a lockup, CPU will stop accessing data and fetching, and clear the pipeline. Reset processor unit and debug unit to unlock.</p>
2	R	0x0	<p>DM_STA. Debug Mode Status. 0: Normal Mode 1: Debug Mode</p>
1:0	R	0x3	<p>LP_STA. Low Power Status. 00: Low Power Mode 01: Reserved 10: Reserved 11: Normal Mode Reserved</p>

3.3.4.11 0x0304 RISCV AXI PMU Control Register (Default Value: 0x0000_0000)

Offset:0x0304			Register Name: RISCV_AXI_PMU_CTRL
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	WC	0x0	<p>PMU_CLR. PMU Clear. 0 No operation. 1 PMU cleared.</p>
0	R/W	0x0	<p>PMU_EN. PMU Enable. 0 PMU disabled. 1 PMU Enabled.</p>

3.3.4.12 0x0308 RISCV AXI PMU Period Register (Default Value: 0x0000_0000)

Offset:0x0308			Register Name: RISCV_AXI_PMU_PRD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>PRD. Period. Suggest that the field is in units of 1 us (1 ms).</p>

3.3.4.13 0x030C RISCV AXI PMU Read Latency Register (Default Value: 0x0000_0000)

Offset:0x030C			Register Name: RISCV_AXI_PMU_LAT_RD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD_LAT. Read Latency. Monitor the total latency of read-channel durning period

3.3.4.14 0x0310 RISCV AXI PMU Write Latency Register (Default Value: 0x0000_0000)

Offset:0x0310			Register Name: RISCV_AXI_PMU_LAT_WR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	WR_LAT. Write Latency. Monitor the total latency of read-channel durning period

3.3.4.15 0x0314 RISCV AXI PMU Read Request Register (Default Value: 0x0000_0000)

Offset:0x0314			Register Name: RISCV_AXI_PMU_REQ_RD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD_REQ. Read Request. Monitor the total command numbers of read-channel durning period

3.3.4.16 0x0318 RISCV AXI PMU Write Request Register (Default Value: 0x0000_0000)

Offset:0x0318			Register Name: RISCV_AXI_PMU_REQ_WR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	WR_REQ. Write Request. Monitor the total latency of write-channel durning period

3.3.4.17 0x031C RISCV AXI PMU Read Bandwidth Register (Default Value: 0x0000_0000)

Offset:0x031C			Register Name: RISCV_AXI_PMU_BW_RD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD_BW. Read Bandwidth. Monitor the total data (KB) of read-channel durning period

3.3.4.18 0x0320 RISCV AXI PMU Write Bandwidth Register (Default Value: 0x0000_0000)

Offset:0x0320			Register Name: RISCV_AXI_PMU_BW_WR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	WR_BW. Write Bandwidth. Monitor the total data (KB) of write-channel durning period



3.4 Clock Controller Unit (CCU)

3.4.1 Overview

The clock controller unit (CCU) controls the PLL configurations and most of the clock generation, division, distribution, synchronization, and gating. The input signals of the CCU include the external clock for the reference frequency (24 MHz). The outputs from the CCU are mostly clocks to other blocks in the system.

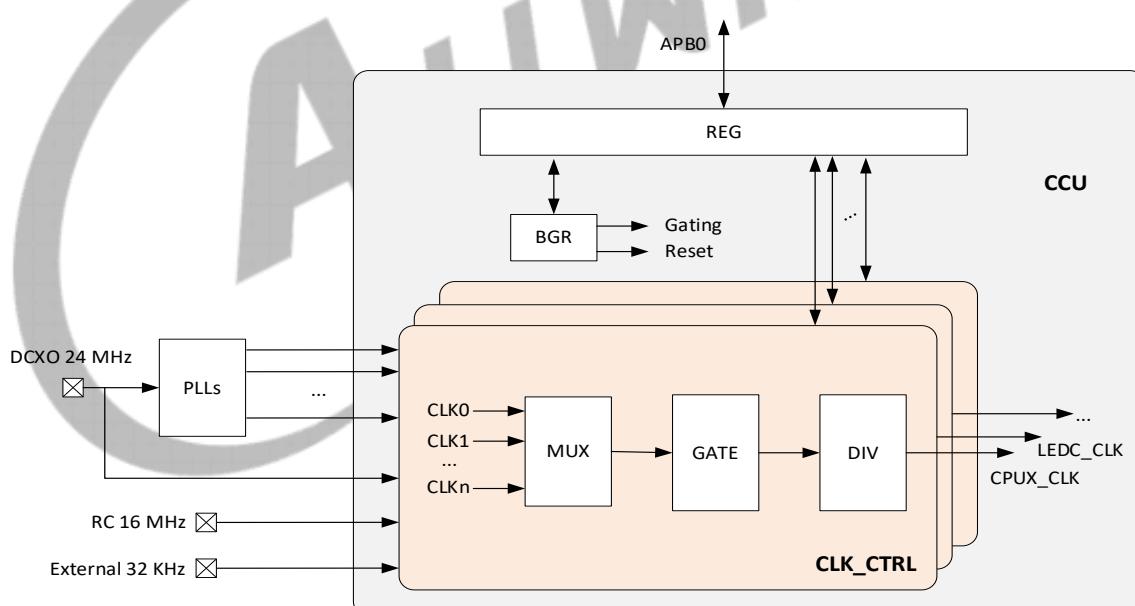
The CCU includes the following features:

- Bus Source and Divisions
- Clock Output Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset

3.4.2 Block Diagram

The following figure shows the functional block diagram of the CCU.

Figure 3-3 CCU Block Diagram



3.4.3 Functional Description

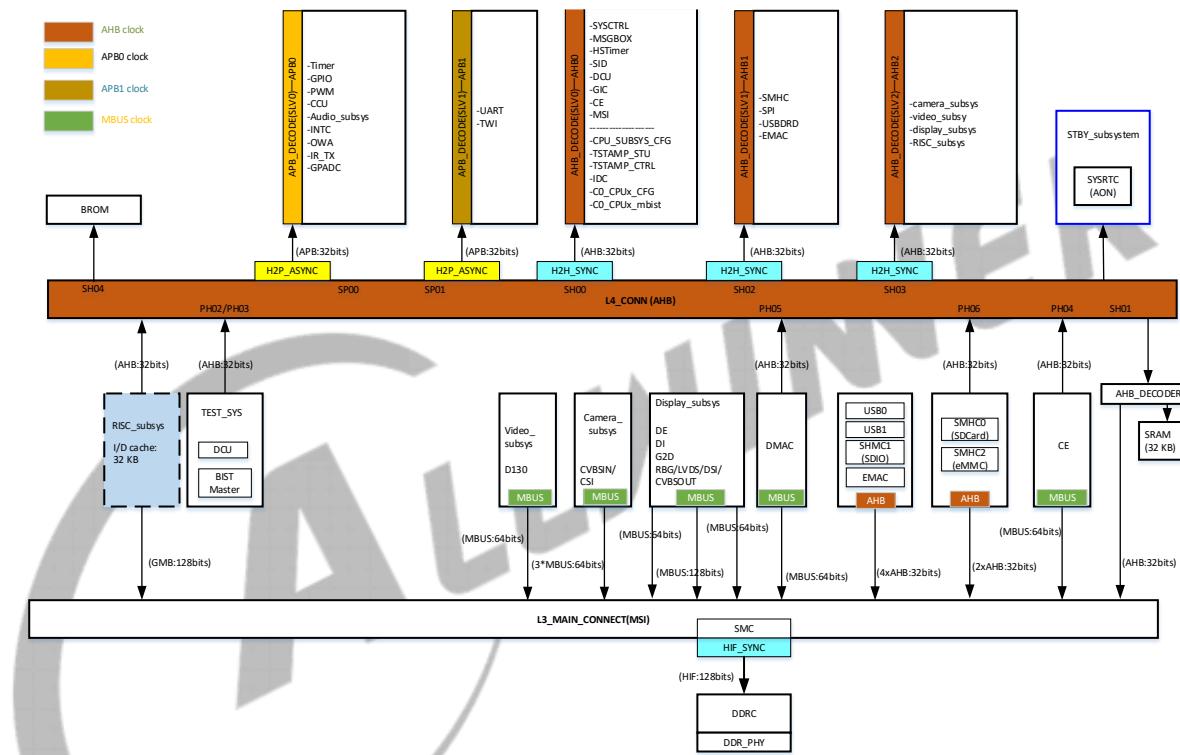
3.4.3.1 System Bus Tree

The system buses include advanced high-performance buses (AHBs), advanced peripheral buses (APBs), and MBUS.

All devices mounted at the bus should use the related bus clocks, and the gating signals for the bus are from the CCU module.

The following figure shows the diagram of the System Bus Tree.

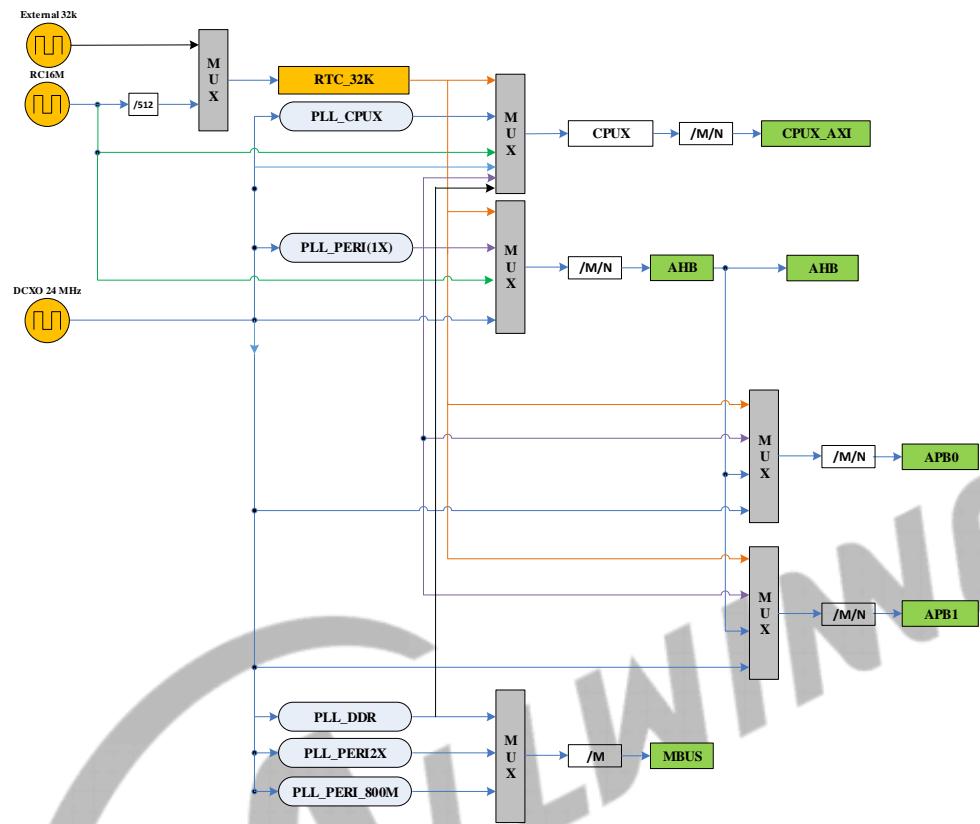
Figure 3-4 System Bus Tree



3.4.3.2 Bus Clock Generation

The following figure describes module clock generation.

Figure 3-5 Bus Clock Generation



3.4.3.3 PLL Distribution

The following figure shows the block diagram of the PLL distribution.

Figure 3-6 PLL Distribution

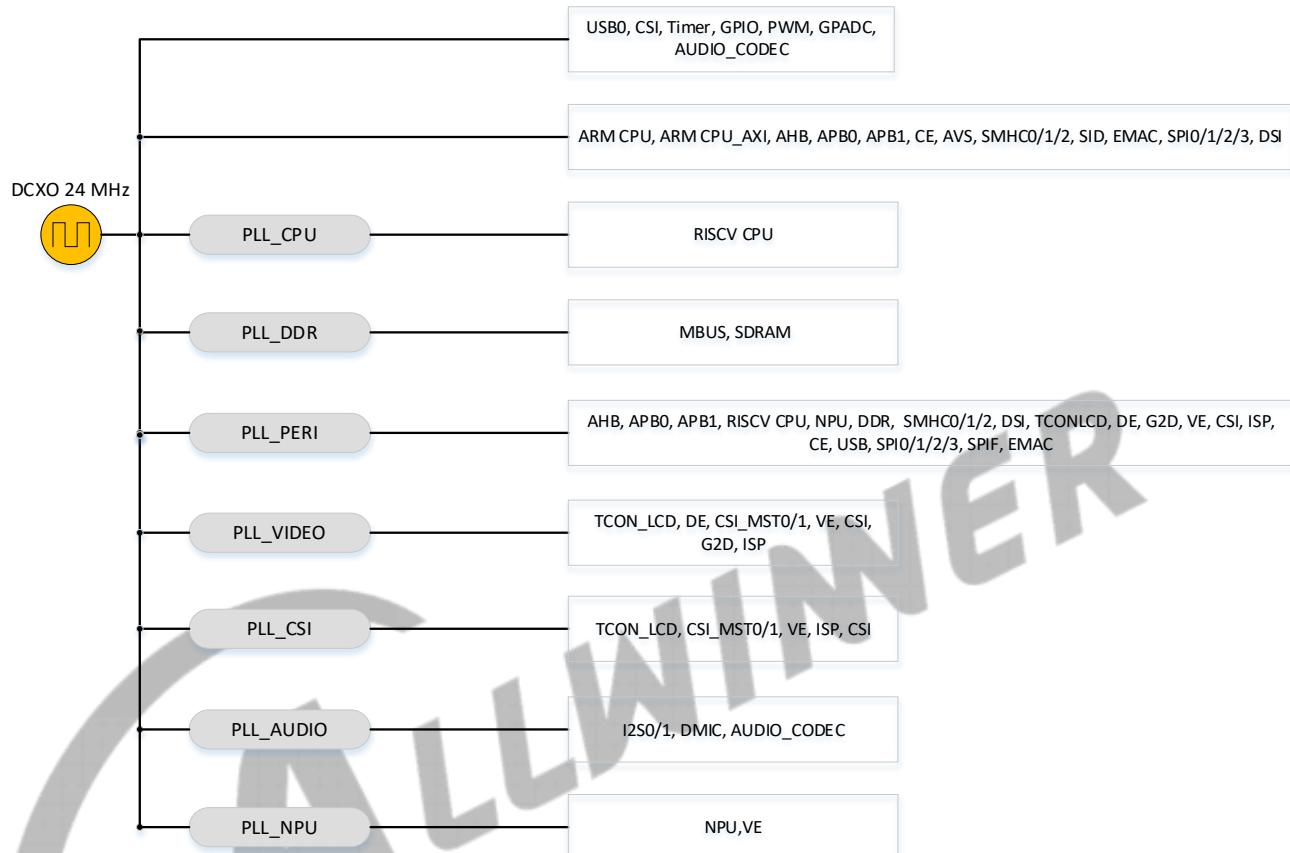


Table 3-3 PLL Typical Application

PLL Type	Application Module	Notes
PLL_CPU	RISCV CPU	Support DVFS
PLL_DDR	MBUS, SDRAM	Support spread spectrum No support linear FM
PLL_PERI	AHB, APB0, APB1, RISCV CPU, NPU, DDR, SMHCO/1/2, DSI, TCONLCD, DE, G2D, VE, CSI, ISP, CE, USB, SPI0-3, SPIF, EMAC	No support dynamic FM
PLL_VIDEO	TCONLCD, DE, CSI_MST0/1, VE, CSI, G2D, ISP	No support DVFS
PLL_CSI	TCON_LCD, CSI_MST0/1, VE, ISP, CSI	No support DVFS
PLL_AUDIO	I2S0/1, DMIC, AUDIO_CODEC	No support DVFS
PLL_NPU	NPU, VE	No support DVFS

3.4.3.4 PLL Features

The following table shows the PLL features.

Table 3-4 PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Default Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Lock Time
PLL_CPU	288 MHz to 3.0 GHz (24*N)	288 MHz to 1.8 GHz	408 MHz	No	Yes	No	< 200 ps	1.5 ms
PLL_AUDIO	80 MHz to 3.0 GHz (24MHz*N.x/M1/M0/P)	24.576 MHz 22.5792 MHz 24.576*4 MHz 22.5792*4 MHz	24.576 MHz	Yes	No	No	< 200 ps	500 us
PLL_PERI	180 MHz to 3.2 GHz (24*N/M1/M0)	Fvco/Div (Div:1-8)	1/2x: 1.2 GHz 1/3x: 800 MHz 1/5x: 480MHz	Yes	No	No	< 200 ps	500 us
PLL_Video(4X)	252 MHz to 3.0 GHz (24*N/M)	192 MHz to 2400 MHz	1x: 297 MHz 2x:594 MHz 4x:1188 MHz	Yes	No	No	< 200 ps	500 us
PLL_CSI (4X)	252 MHz to 3.0 GHz (24*N/M)	192 MHz to 2400 MHz	1x: 297 MHz 2x:594 MHz 4x:1188 MHz	Yes	No	No	< 200 ps	500 us
PLL_DDR	180 MHz to 3.0 GHz (24*N/M1/M0)	192 MHz to 2.0 GHz	432 MHz	Yes	No	No	200 MHz to 800 MHz (< 200 ps) 800 MHz to 1.3 GHz (< 140 ps) 1.3 GHz to 2.0 GHz (< 100 ps)	500us
PLL_NPU	180 MHz to 3.0 GHz (24*N/M1/M0)	500 MHz to 2.1 GHz	504MHz	Yes	No	No	< 200 ps	500 us

3.4.4 Programming Guidelines

3.4.4.1 Configuring the Frequency of PLL_CPU

The frequency configuration formula of PLL_CPU is shown below:

$$\text{PLL_CO_CPU} = 24\text{MHz} * \text{N}/\text{P}$$

The parameter N is the frequency-doubling factor of PLL. The next parameter can only be configured after the PLL relocks.

The parameter P is a digital post-frequency-division factor. It can be dynamically switched in real-time, without affecting the normal work of PLL.



PLL_CPU supports the dynamic adjustment (modifying the value of N). However, for the system stability, if you need to configure the frequency of the PLL_CPU from a higher value to a lower one, switch the CPU frequency to a medium one first, and then configure PLL_CPU to the target low frequency.

Follow the steps below to adjust the frequency of PLL_CPU:

1. Before you configure PLL_CPU, switch the clock source of CPU to PLL_PERI(1X).
2. Modify the parameters N and P of PLL_CPU.
3. Write the [PLL Lock Enable bit](#) (bit[29]) of [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 0 and then to 1.
4. Wait until the [Lock bit](#) (bit[28]) of [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) changes to 1.
5. Switch the clock source of the CPU to PLL_CPU.

3.4.4.2 Configuring the Frequency of PLL_AUDIO

The frequency configuration formula of PLL_AUDIO is shown below:

$$\text{PLL_AUDIO} = 24\text{MHz} * \text{N}/\text{M0}/\text{M1}/\text{P}$$

Changing any parameter of N, M0, M1, and P will make PLL be relocked, so PLL_AUDIO does not support the dynamic adjustment.

Generally, the frequency of PLL_AUDIO is either 24.576*4 MHz or 22.5792*4 MHz, and the two frequency points have the recommended configuration values. To implement the desired frequency point of PLL_AUDIO, follow the steps below:

1. Configure the N, M1, M0, and P factors.
2. Configure [PLL SDM_EN](#) (bit[24]) of [PLL_AUDIO_CTRL_REG \(Offset: 0x0078\)](#) to 1.
3. Configure [PLL_AUDIO_PATO_CTRL_REG \(Offset: 0x0178\)](#) to enable the digital spread spectrum
4. Write the [LOCK_ENABLE bit](#) (bit[29]) of [PLL_AUDIO_CTRL_REG \(Offset: 0x0078\)](#) to 0 and then to 1.
5. Wait until the [LOCK bit](#) (bit28) of [PLL_AUDIO_CTRL_REG \(Offset: 0x0078\)](#) changes to 1.

 **NOTE**

When the P factor of PLL_AUDIO is an odd number, the clock output is an unequal-duty-cycle signal.

The recommended values for configuration factors of PLL_AUDIO are as follows.

Table 3-5 Recommended Values for Configuration Factors of PLL_AUDIO

Mode	Clock Source (MHz)	Frequency-doubling N	VCO (MHz)	Post Frequency-Division	PLL Output (MHz)	Divisor	Actual Operating Frequency (MHz)	Description
Integer divider	24	128	3072	2	1536	4	384	Provide clock source for peripherals
						8	192	
						16	96	
							
				5		25	24.576	For audio-related modules
Decimal divider	24	98.304	2359.296	2	1179.648	2	589.824	Provides clock source for peripheral devices
						3	393.216	
						6	196.608	
						12	98.304	
						48	24.576	For audio-related modules
				5				

3.4.4.3 Configuring the Frequency of General PLLs

1. Make sure the PLL is enabled. If not, refer to section 3.4.4.4 Enabling the PLL to enable the PLL.
2. Configure the [PLL_OUTPUT_GATE bit](#) (bit[27]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) as 0 to disable the output gate of the PLL, because general PLLs are unavailable in the process of the frequency modulation.
3. Configure the N and M factors. (It is not suggested to configure the M1 factor)
4. Write the [LOCK_ENABLE bit](#) (bit[29]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 0 and then to 1.
5. Wait until the [LOCK bit](#) (bit[28]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) changes to 1.
6. Configure [PLL_OUTPUT_GATE bit](#) (bit[27]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 1.

3.4.4.4 Enabling the PLL

Follow the steps below to enable the PLL:

1. Configure the N, M, and P factors of the PLL control register.
2. Write the [PLL_OUTPUT_GATE bit](#) (bit[27]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 0.
3. Write the [PLL_ENABLE bit](#) (bit[31]) and the [LDO_EN bit](#) (bit[30]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 1.
4. Write the [LOCK_ENABLE bit](#) (bit[29]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 1.
5. Wait for the status of the Lock to change to 1.
6. Delay 20 us.
7. Write the [PLL_OUTPUT_GATE bit](#) (bit[27]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 1 and then the PLL will be available.

3.4.4.5 Disabling the PLL

Follow the steps below to disable the PLL:

1. Write the [PLL_ENABLE bit](#) (bit[31]) and the [LDO_EN](#) bit (bit[30]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 0.
2. Write the [LOCK_ENABLE bit](#) (bit[29]) of the [PLL_CPU_CTRL_REG \(Offset: 0x0000\)](#) to 0.



In the normal use of PLLs, it is unsuggested to enable and disable the PLLs frequently. Turning on and off the PLLs will cause mutual interference between PLLs, which will affect the stability of the system. When the clock is unnecessary, you can write 0 to the [PLL_OUTPUT_GATE](#) bit of the PLL control register to disable the output gate of the PLL, instead of writing 0 to the Enable bit to disable the PLL.

3.4.4.6 Configuring Bus Clock

The bus clock supports the dynamic switching, but remember to follow the two rules below during the switching process.

- From a higher frequency to a lower one: switch the clock source first, and then set the frequency division factor;
- From a lower frequency to a higher one: configure the frequency division factor first, and then switch the clock source.

3.4.4.7 Configuring Module Clocks

For the Bus Gating Reset register of a module, the reset bit is de-asserted first, and then the clock gating bit is enabled to avoid the potential problems caused by the asynchronous release of the reset signal.

For all module clocks except the DDR clock, configure the clock source and frequency division factor first, and then release the clock gating (sets it to 1). For the configuration order of the clock source and the frequency division factor, follow the rules below:

- With the increasing of the clock source frequency, configure the frequency division factor before the clock source;
- With the decreasing of the clock source frequency, configure the clock source before the frequency division factor.

3.4.4.8 Implementing Spread Spectrum

The spread spectrum technology is to convert a narrowband signal into a wideband signal. It helps to reduce the effect of electromagnetic interference (EMI) associated with the fundamental frequency of the signal.

For the general PLL frequency, the calculation formula is as follows:

$$f = \frac{N+1+X}{P \cdot (M_0+1) \cdot (M_1+1)} \cdot 24MHz, 0 < X < 1$$

Where,

P is the frequency division factor of module or PLL;

M₀ is the post-frequency division factor of PLL;

M₁ is the pre-frequency division factor of PLL;

N is the frequency doubling factor of PLL;

X is the amplitude coefficient of the spread spectrum.

The parameters N, P, M₁, and M₀ are for the frequency division.

When M₁ = 0, M₀ = 0, and P = 1 (no frequency division), the calculation formula of PLL frequency can be simplified as follows:

$$f = (N+1+X) \cdot 24MHz, 0 < X < 1$$

$$[f_1, f_2] = (N+1+[X_1, X_2]) \cdot 24MHz$$

$$SDM_BOT = 2^{17} \cdot X_1$$

$$WAVE_STEP = 2^{17} \cdot (X_2 - X_1) / (24MHz/PREQ) \cdot 2$$

Where, SDM_BOT and WAVE_STEP are bits of the PLL pattern control register, and PREQ is the frequency of the spread spectrum.



NOTE

Different PLLs have different calculate formulas, refer to the CTRL register of the corresponding PLL in section 3.4.6 Register Description

Configuration Procedure

Follow the steps below to implement the spread spectrum:

1. Configure the control register of the corresponding PLL
 - a) Calculate the factor N and decimal value X according to the PLL frequency and PLL frequency formula. Refer to the control register of the corresponding PLL (named PLL_xxx_CTRL_REG, where xxx is the module name) in 3.4.6 Register Description for the corresponding PLL frequency formula.
 - b) Write M₀, M₁, N, and PLL frequency to the PLL control register.
 - c) Configure the SDM_ENABLE bit (bit[24]) of the PLL control register to 1 to enable the spread spectrum function.
2. Configure the pattern control register of the corresponding PLL

- a) Calculate the SDM_BOT and WAVE_STEP of the pattern control register according to decimal value X and spread spectrum frequency (the bit[18:17] of the PLL_PAT register)
 - b) Configure the spread spectrum mode (SPR_FREQ_MODE, bit[30:29] of the PLL_PAT register) to 2 or 3.
 - c) If the PLL_INPUT_DIV2 of the PLL control register is 1, configure the spread spectrum clock source select bit (SDM_CLK_SEL, bit[19] of the PLL_PAT register) to 1. Otherwise, configure SDM_CLK_SEL to the default value 0.
 - d) Write SDM_BOT, WAVE_STEP, PREQ, SPR_FREQ_MODE, and SDM_CLK_SEL to the PLL pattern control register, and configure the SIG_DELT_PAT_EN bit (bit[31]) of this register to 1.
3. Delay 20 us

Configuration Example

The following example shows how to configure the spread spectrum frequency as 605.3 MHz to 609.7 MHz.

If M1 = 0, M0 = 0, P = 1, according to the formula $[f_1, f_2] = (N + 1 + [X_1, X_2]) \cdot 24\text{MHz}$, you can get:

$$\begin{aligned} N + 1 + [X_1, X_2] &= \frac{[605.3, 609.7]}{24} \\ &= \frac{600 + [5.3, 9.7]}{24} \\ &= 24 + 1 + [5.3/24, 9.7/24] \end{aligned}$$

Obviously,

$$N = 24, X_1 = 5.3/24, X_2 = 9.7/24$$

$$\text{SDM_BOT} = 217 * X_1 = 0x7111$$

$$\text{WAVE_STEP} = 217 * (X_2 - X_1) / (24M/\text{PREQ}) * 2 = 0x3f; \text{PREQ} = 31.5 \text{ kHz}$$

If M0 = 1, M1=0, P = 1, then total frequency division factor is $(M_0 + 1) * 1 = 2$, so the actual output frequency of PLL is 1212.1 MHz to 1219.4 MHz.

Similarly, you can get:

$$N = 49, X_1 = 12.1/24, X_2 = 19.4/24$$

Then calculate the values of SDM_BOT and WAVE_STEP according to the formulas, and follow the steps described in Configuration Procedure.

3.4.5 Register List

Module Name	Base Address	Comments
CCMU	0x02001000	

Register Name	Offset	Description
PLL_CPU_CTRL_REG	0x0000	PLL_CPU Control Register
PLL_DDR_CTRL_REG	0x0010	PLL_DDR Control Register
PLL_PERI_CTRL_REG	0x0020	PLL_PERI Control Register
PLL_VIDEO_CTRL_REG	0x0040	PLL_VIDEO Control Register
PLL_CSI_CTRL_REG	0x0048	PLL_CSI Control Register
PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_NPU_CTRL_REG	0x0080	PLL_NPU Control Register
PLL_DDR_PATO_CTRL_REG	0x0110	PLL_DDR Pattern0 Control Register
PLL_DDR_PAT1_CTRL_REG	0x0114	PLL_DDR Pattern1 Control Register
PLL_PERI_PATO_CTRL_REG	0x0120	PLL_PERI Pattern0 Control Register
PLL_PERI_PAT1_CTRL_REG	0x0124	PLL_PERI Pattern1 Control Register
PLL_VIDEO_PATO_CTRL_REG	0x0140	PLL_VIDEO Pattern0 Control Register
PLL_VIDEO_PAT1_CTRL_REG	0x0144	PLL_VIDEO Pattern1 Control Register
PLL_CSI_PATO_CTRL_REG	0x0148	PLL_CSI Pattern0 Control Register
PLL_CSI_PAT1_CTRL_REG	0x014C	PLL_CSI Pattern1 Control Register
PLL_AUDIO_PATO_CTRL_REG	0x0178	PLL_AUDIO Pattern0 Control Register
PLL_AUDIO_PAT1_CTRL_REG	0x017C	PLL_AUDIO Pattern1 Control Register
PLL_NPU_PATO_CTRL_REG	0x0180	PLL_NPU Pattern0 Control Register
PLL_NPU_PAT1_CTRL_REG	0x0184	PLL_NPU Pattern1 Control Register
PLL_CPU_BIAS_REG	0x0300	PLL_CPU Bias Register
PLL_DDR_BIAS_REG	0x0310	PLL_DDR Bias Register
PLL_PERI_BIAS_REG	0x0320	PLL_PERI Bias Register
PLL_VIDEO_BIAS_REG	0x0340	PLL_VIDEO Bias Register
PLL_CSI_BIAS_REG	0x0348	PLL_CSI Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_NPU_BIAS_REG	0x0380	PLL_NPU Bias Register
PLL_CPU_TUN_REG	0x0400	PLL_CPU Tuning Register
CPU_CLK_REG	0x0500	CPU Clock Register
CPU_GATING_REG	0x0504	CPU Gating Configuration Register
AHB_CLK_REG	0x0510	AHB Clock Register
APB0_CLK_REG	0x0520	APB0 Clock Register
APB1_CLK_REG	0x0524	APB1 Clock Register
MBUS_CLK_REG	0x0540	MBUS Clock Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
NPU_CLK_REG	0x06E0	NPU Clock Register

Register Name	Offset	Description
NPU_BGR_REG	0x06EC	NPU Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
MSGBOX_BGR_REG	0x071C	MSGBOX Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	SPINLOCK Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HSTIMER Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
IOMMU_BGR_REG	0x07BC	IOMMU Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MAT_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
SMHCO_CLK_REG	0x0830	SMHCO Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPI3_CLK_REG	0x094C	SPI3 Clock Register
SPIF_CLK_REG	0x0950	SPIF Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
EMAC_25M_CLK_REG	0x0970	EMAC_25M Clock Register
EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
I2S0_CLK_REG	0x0A10	I2S0 Clock Register
I2S1_CLK_REG	0x0A14	I2S1 Clock Register
I2S_BGR_REG	0x0A20	I2S Bus Gating Reset Register
DMIC_CLK_REG	0x0A40	DMIC Clock Register
DMIC_BGR_REG	0x0A4C	DMIC Bus Gating Reset Register
AUDIO_CODEC_DAC_CLK_REG	0x0A50	AUDIO_CODEC_DAC Clock Register
AUDIO_CODEC_ADC_CLK_REG	0x0A54	AUDIO_CODEC_ADC Clock Register
AUDIO_CODEC_BGR_REG	0x0A5C	AUDIO_CODEC Bus Gating Reset Register
USBO_CLK_REG	0x0A70	USBO Clock Register
USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
DPSS_TOP_BGR_REG	0x0ABC	DPSS_TOP Bus Gating Reset Register
DSI_CLK_REG	0x0B24	DSI Clock Register
DSI_BGR_REG	0x0B4C	DSI Bus Gating Reset Register
TCONLCD_CLK_REG	0x0B60	TCONLCD Clock Register

Register Name	Offset	Description
TCONLCD_BGR_REG	0x0B7C	TCONLCD Bus Gating Reset Register
CSI_CLK_REG	0x0C04	CSI Clock Register
CSI_MASTER0_CLK_REG	0x0C08	CSI Master0 Clock Register
CSI_MASTER1_CLK_REG	0x0C0C	CSI Master1 Clock Register
CSI_MASTER2_CLK_REG	0x0C10	CSI Master2 Clock Register
CSI_BGR_REG	0x0C2C	CSI Bus Gating Reset Register
WIEGAND_BGR_REG	0x0C7C	WIEGAND Bus Gating Reset Register
RISCV_CLK_REG	0x0D00	RISCV Clock Register
RISCV_GATING_RST_REG	0x0D04	RISCV Gating and Reset Configuration Register
RISCV_CFG_BGR_REG	0x0D0C	RISCV_CFG Bus Gating Reset Register
PLL_PRE_DIV_REG	0x0E00	PLL Pre Divider Register
AHB_GATE_EN_REG	0x0E04	AHB Gate Enable Register
PERIPLL_GATE_EN_REG	0x0E08	PERIPLL Gate Enable Register
CLK24M_GATE_EN_REG	0x0E0C	CLK24M Gate Enable Register
CCMU_SEC_SWITCH_REG	0x0F00	CCMU Security Switch Register
GPADC_CLK_SEL_REG	0x0F04	GPADC Clock Select Register
FRE_DET_CTRL_REG	0x0F08	Frequency Detect Control Register
FRE_UP_LIM_REG	0x0F0C	Frequency Up Limit Register
FRE_DOWN_LIM_REG	0x0F10	Frequency Down Limit Register
CCMU_FAN_GATE_REG	0x0F30	CCMU FANOUT CLOCK GATE Register
CLK27M_FAN_REG	0x0F34	CLK27M FANOUT Register
CLK_FAN_REG	0x0F38	CLK FANOUT Register
CCMU_FAN_REG	0x0F3C	CCMU FANOUT Register

3.4.6 Register Description

3.4.6.1 0x0000 PLL_CPU Control Register (Default Value: 0x4A00_1000)

Offset: 0x0000			Register Name: PLL_CPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>PLL_EN PLL Enable 0: Disable 1: Enable The CPUPLL= InputFreq*N.</p> <p>Note: The PLL_CPU output frequency must be in the range from 200 MHz to 3 GHz. And the default value of PLL_CPU is 408 MHz when the crystal oscillator is 24 MHz.</p>
30	R/W	0x1	<p>PLL_LDO_EN LDO Enable 0: Disable 1: Enable</p>

Offset: 0x0000			Register Name: PLL_CPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info 0: Unlocked 1: Locked (It indicates that the PLL has been stable)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:24	R/W	0x2	PLL_LOCK_TIME PLL lock time The bit indicates the step amplitude from one frequency to another.
23:16	/	/	/
15:8	R/W	0x10	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254 In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1:0	R/W	0x0	PLL_M PLL_M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3 Note: The M factor is only for testing.

3.4.6.2 0x0010 PLL_DDR Control Register (Default Value: 0x4800_2301)

Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>PLL_EN. PLL Enable 0: Disable 1: Enable The DDRPLL= InputFreq*N/M1/M0 Note: The default value of PLL_DDR is 432 MHz when the crystal oscillator is 24 MHz.</p>
30	R/W	0x1	<p>PLL_LDO_EN LDO enable 0: Disable 1: Enable</p>
29	R/W	0x0	<p>LOCK_ENABLE Lock Enable 0: Disable 1: Enable</p>
28	R	0x0	<p>LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)</p>
27	R/W	0x1	<p>PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.</p>
26:25	/	/	/
24	R/W	0x0	<p>PLL_SDM_EN PLL SDM Enable 0: Disable 1:Enable</p>
23:16	/	/	/
15:8	R/W	0x23	<p>PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254 In application, PLL_N shall be more than or equal to 11.</p>
7:6	R/W	0x0	<p>PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles</p>

Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1. M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0. M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

3.4.6.3 0x0020 PLL_PERI Control Register (Default Value: 0x4821_6310)

Offset: 0x0020			Register Name: PLL_PERI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable PERIPLL2X = 24MHz*N/M/P0 PERI_800M = 24MHz*N/M/P1 PERI_480M = 24MHz*N/M/P2 PERI_600M = 24MHz*N/M/P0/2 PERI_400M = 24MHz*N/M/P0/3 PERI_300M = PERI_600M/2 PERI_200M = PERI_400M/2 PERI_160M = PERI_480M/3 PERI_150M = PERI_300M/2 When the crystal oscillator is 24 MHz, the default frequency of PLL_PERI(2X) is 1.2 GHz, the default frequency of PLL_PERI(1X) is 480 MHz, and the default frequency of PLL_PERI(800M) is 800 MHz. Note: The output clock of PLL_PERI(2X) is fixed to 1.2 GHz and not suggested to change the parameter.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable

Offset: 0x0020			Register Name: PLL_PERI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable. Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x2	PLL_P1. PLL Output Div P1. P1=PLL_OUTPUT_DIV_P1 + 1 PLL_OUTPUT_DIV_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0. PLL Output Div P0. P0=PLL_OUTPUT_DIV_P0 + 1 PLL_OUTPUT_DIV_P0 is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 12.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Offset: 0x0020			Register Name: PLL_PERI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_P2. PLL Output Div P2. P2=PLL_OUTPUT_DIV_P2 + 1 PLL_OUTPUT_DIV_P2 is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV2. PLL Input Div M. M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	/	/	/

3.4.6.4 0x0040 PLL_VIDEO Control Register (Default Value: 0x4800_6203)

Offset: 0x0040			Register Name: PLL_VIDEO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. For application, VIDEOPLL4X = InputFreq *N/M. VIDEOPLL2X = InputFreq *N/M/2. VIDEOPLL1X = InputFreq *N/M/4. When the HOSC is 24 MHz, the default frequency of PLL_VIDEO0(4X) is 1188 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)

Offset: 0x0040			Register Name: PLL_VIDEO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV2. PLL Input Div M. M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2. PLL Output Div D. D=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. (The factor is only for testing) For test, VIDEOPLL4X = 24MHz*N/M/D

3.4.6.5 0x0048 PLL_CSI Control Register (Default Value: 0x4800_6203)

Offset: 0x0048			Register Name: PLL_CSI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>PLL_EN.</p> <p>PLL Enable.</p> <p>0: Disable.</p> <p>1: Enable.</p> <p>CSIPLL4X = InputFreq*N/M.</p> <p>CSIPLL2X = InputFreq*N/M/2.</p> <p>CSIPLL1X = InputFreq*N/M/4.</p> <p>When the HOSC is 24 MHz, the default frequency of PLL_CSI(4X) is 1188 MHz.</p>
30	R/W	0x1	<p>PLL_LDO_EN.</p> <p>LDO enable.</p> <p>0: Disable</p> <p>1: Enable</p>
29	R/W	0x0	<p>LOCK_ENABLE</p> <p>Lock Enable.</p> <p>0: Disable</p> <p>1: Enable</p>
28	R	0x0	<p>LOCK</p> <p>PLL Lock Info.</p> <p>0: Unlocked</p> <p>1: Locked (It indicates that the PLL has been stable.)</p>
27	R/W	0x1	<p>PLL_OUTPUT_GATE</p> <p>PLL Output Gating Enable.</p> <p>0: Disable</p> <p>1: Enable</p> <p>The bit is used to control the output enable of PLL.</p>
26:25	/	/	/
24	R/W	0x0	<p>PLL_SDM_EN.</p> <p>PLL SDM Enable.</p> <p>0: Disable.</p> <p>1: Enable.</p>
23:16	/	/	/
15:8	R/W	0x62	<p>PLL_FACTOR_N</p> <p>PLL Factor N.</p> <p>N= PLL_FACTOR_N +1</p> <p>PLL_FACTOR_N is from 0 to 254.</p> <p>In application, PLL_FACTOR_N shall be more than or equal to 11.</p>

Offset: 0x0048			Register Name: PLL_CSI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV2. PLL Input Div M. M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2. PLL Output Div D. D=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. (The factor is only for testing) For test, CSIPLL4X =24MHz*N/M/D

3.4.6.6 0x0078 PLL_AUDIO Control Register (Default Value: 0x4841_7F00)

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable The AUDIOPLL_DIV2 = 24MHz*N/M /P0 The AUDIOPLL_DIV5 = 24MHz*N/M /P1 The AUDIOPLL4X = AUDIOPLL_DIV2/AUDIOPLL4X_DIV(0x0E00). The AUDIOPLL1X = AUDIOPLL_DIV5/AUDIOPLL1X_DIV(0x0E00) The working frequency range of 24MHz/M*N is from 180 MHz to 3.0 GHz. AUDIOPLL_DIV2 default is 1536MHz, AUDIOPLL_DIV5 default is 614.4MHz(24.576Mhz*25).
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable) Note: The bit is only valid when the bit29 is set to 1.
27	R/W	0x1	PLL_OUTPUT_GATE. PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable. Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x4	PLL_P1. PLL Output Div P1. P1=PLL_OUTPUT_DIV_P1 + 1 PLL_OUTPUT_DIV_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0. PLL Output Div P0. P0=PLL_OUTPUT_DIV_P0 + 1 PLL_OUTPUT_DIV_P0 is from 0 to 7.
15:8	R/W	0x7F	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. Enable spread spectrum and decimal division.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2. PLL Input Div M. $M = \text{PLL_INPUT_DIV_M} + 1$ PLL_INPUT_DIV_M is from 0 to 1.
0	/	/	/

3.4.6.7 0x0080 PLL_NPU Control Register (Default Value: 0x4800_2901)

Offset: 0x0080			Register Name: PLL_NPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable The NPUPLL4X = 24MHz*N/M. The NPUPLL2X = 24MHz*N/M/2. The NPUPLL1X = 24MHz*N/M/4. The working frequency range of PLL_NPU(4X) is from 180 MHz to 3.5 GHz. The default frequency of PLL_NPU(4X) is 3072 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) Note: The bit is only valid when the bit29 is set to 1.

Offset: 0x0080			Register Name: PLL_NPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable. Enable spread spectrum and decimal division.
23:16	/	/	/
15:8	R/W	0x29	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2. PLL Input Div M. M=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2. PLL Output Div D. D=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. (The factor is only for testing) For test, NPUPLL4X = 24MHz*N/M/D

3.4.6.8 0x0110 PLL_DDR Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.9 0x0114 PLL_DDR Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.10 0x0120 PLL_PERI Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PLL_PERI_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.11 0x0124 PLL_PERI Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PLL_PERI_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.12 0x0140 PLL_VIDEO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.13 0x0144 PLL_VIDEO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.14 0x0148 PLL_CSI Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_CSI_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32Khz 10: 32.5Khz 11: 33Khz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.15 0x014C PLL_CSI Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PLL_CSI_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.16 0x0178 PLL_AUDIO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.17 0x017C PLL_AUDIO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PLL_AUDIO_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.18 0x0180 PLL_NPU Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PLL_NPU_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.19 0x0184 PLL_NPU Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: PLL_NPU_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.20 0x0300 PLL_CPU Bias Register (Default Value: 0x8010_0000)

Offset: 0x0300			Register Name: PLL_CPU_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PLL_VCO_RST_IN. VCO reset in.
30:21	/	/	/
20:16	R/W	0x10	PLL_CP. PLL current bias control.
15:0	/	/	/

3.4.6.21 0x0310 PLL_DDR Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.22 0x0320 PLL_PERI Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control .
15:0	/	/	/

3.4.6.23 0x0340 PLL_VIDEO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control .
15:0	/	/	/

3.4.6.24 0x0348 PLL_CSI Bias Register (Default Value: 0x0003_0000)

Offset: 0x0348			Register Name: PLL_CSI_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.25 0x0378 PLL_AUDIO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.26 0x0380 PLL_NPU Bias Register (Default Value: 0x0003_0000)

Offset: 0x0380			Register Name: PLL_NPU_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.27 0x0400 PLL_CPU Tuning Register (Default Value: 0x4440_4000)

Offset: 0x0400			Register Name: PLL_CPU_TUN_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x4	PLL_VCO. VCO range control.
27	/	/	/
26:24	R/W	0x4	PLL_VCO_GAIN. KVCO gain control.
23	/	/	/
22:16	R/W	0x40	PLL_CNT_INT. Counter initial control.
15	R/W	0x0	PLL_REG_OD. PLL REG ODO for verify.

Offset: 0x0400			Register Name: PLL_CPU_TUN_REG
Bit	Read/Write	Default/Hex	Description
14:8	R/W	0x40	PLL_B_IN. PLL B IN for verify.
7	R/W	0x0	PLL_REG_OD1. PLL REG OD1 for verify.
6:0	R	0x0	PLL_B_OUT. PLL B OUT for verify.

3.4.6.28 0x0500 CPU Clock Register (Default Value: 0x0000_0301)

Offset: 0x0500			Register Name: CPU_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CPU_CLK_SEL. Clock Source Select. 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPUPLL/P 100: PERI_600M_BUS 101: PERI_800M CPU_CLK = Clock Source. CPU_AXI Clock = CPU_CLK/M. CPU_APB Clock= CPU_CLK/N. Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	PLL_CPU_OUT_EXT_DIVP. Factor P. 00:1 01:2 10:4 11: \ Note: when the output clock is less than 288 MHz, use PLL_OUT_EXT_DIVP to output the required clock frequency.
15:10	/	/	/
9:8	R/W	0x3	CPU_APB_DIV_CFG. Factor N. (N = FACTOR_N +1) FACTOR_M is from 0 to 3 Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.
7:2	/	/	/

Offset: 0x0500			Register Name: CPU_CLK_REG:
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	CPU_AXI_DIV_CFG. Factor M:(M= FACTOR_M +1) FACTOR_M is from 1 to 3 Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.

3.4.6.29 0x0504 CPU Gating Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0504			Register Name: CPU_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD. CPU Gating Field. If CPU_GATING_FIELD == 16'h16AA, bit[15:0] can be configured.
15:1	/	/	/
0	R/W	0x1	CPU_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

3.4.6.30 0x0510 AHB Clock Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: AHB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI_600M_BUS AHB_CLK = Clock Source/M/N. Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.
23:10	/	/	/

Offset: 0x0510			Register Name: AHB_CLK_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>
7:5	/	/	/
4:0	R/W	0x0	<p>FACTOR_M Factor M. M= FACTOR_M +1 FACTOR_M is from 0 to 31.</p> <p>Note: This clock divider can be glitch-free switched, and supports the dynamic configuration.</p>

3.4.6.31 0x0520 APB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	<p>CLK_SRC_SEL. Clock Source Select. 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI_600M_BUS APB0_CLK = Clock Source/M/N.</p> <p>Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.</p>
23:10	/	/	/
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>
7:5	/	/	/

Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	<p>FACTOR_M Factor M. M= FACTOR_M +1 FACTOR_M is from 0 to 31.</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>

3.4.6.32 0x0524 APB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: APB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	<p>CLK_SRC_SEL. Clock Source Select. 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI_600M_BUS APB1_CLK = Clock Source/M/N.</p> <p>Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.</p>
23:10	/	/	/
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>
7:5	/	/	/
4:0	R/W	0x0	<p>FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>

3.4.6.33 0x0540 MBUS Clock Register (Default Value: 0x4000_0000)

Offset: 0x0540			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x1	MBUS_RST. MBUS Reset. 0: Assert 1: De-assert
29:0	/	/	/

3.4.6.34 0x0600 DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DE_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: PERI_300M 1: VIDEOPLL1X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.35 0x060C DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DE_RST. DE Reset. 0: Assert 1: De-assert
15:1	/	/	/

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DE_GATING. Gating Clock For DE. 0: Mask 1: Pass

3.4.6.36 0x0630 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	G2D_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON G2D_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: PERI_300M 1: VIDEOPLL1X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.37 0x063C G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	G2D_RST. G2D Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING. Gating Clock For G2D. 0: Mask 1: Pass

3.4.6.38 0x0680 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CE_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 001: PERI_400M 010: PERI_300M
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.39 0x068C CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CE_SYS_RST. CE_SYS Reset. 0: Assert 1: De-assert
16	R/W	0x0	CE_RST. CE Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	CE_SYS_GATING. Gating Clock For CE_SYS. 0: Mask 1: Pass
0	R/W	0x0	CE_GATING. Gating Clock For CE. 0: Mask 1: Pass

3.4.6.40 0x0690 VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON VE_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: PERI_300M 001: PERI_400M 010: PERI_480M 011: NPUPLL4X 100: VIDEOPLL4X 101: CSIPLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.41 0x069C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	VE_RST. VE Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING. Gating Clock For VE. 0: Mask 1: Pass

3.4.6.42 0x06E0 NPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x06E0			Register Name: NPU_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NPU_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON NPU_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: PERI_480M 001: PERI_600M 010: PERI_800M 011: NPUPLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.43 0x06EC NPU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06EC			Register Name: NPU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	NPU_RST. NPU Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	NPU_GATING. Gating Clock For NPU. 0: Mask 1: Pass

3.4.6.44 0x070C DMA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DMA_RST. DMA Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING. Gating Clock For DMA. 0: Mask 1: Pass

3.4.6.45 0x071C MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	MSGBOX1_RST. RISCV MSGBOX Reset. 0: Assert 1: De-assert
16	R/W	0x0	MSGBOX0_RST. CPU MSGBOX0 Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	MSGBOX1_GATING. Gating Clock For MSGBOX1 RISCV. 0: Mask 1: Pass
0	R/W	0x0	MSGBOX0_GATING. Gating Clock For MSGBOX0 CPU. 0: Mask 1: Pass

3.4.6.46 0x072C SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	SPINLOCK_RST. SPINLOCK Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING. Gating Clock For SPINLOCK. 0: Mask 1: Pass

3.4.6.47 0x073C HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST. HSTIMER Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HSTIMER_GATING. Gating Clock For HSTIMER. 0: Mask 1: Pass

3.4.6.48 0x0740 AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AVS_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON AVS_CLK = HOSC.
30:0	/	/	/

3.4.6.49 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST. DBGSYS Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING. Gating Clock For DBGSYS. 0: Mask 1: Pass

3.4.6.50 0x07AC PWM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PWM_RST. PWM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING. Gating Clock For PWM. 0: Mask 1: Pass

3.4.6.51 0x07BC IOMMU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07BC			Register Name: IOMMU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	IOMMU_GATING. Gating Clock For IOMMU. 0: Mask 1: Pass

3.4.6.52 0x0800 DRAM Clock Register (Default Value: 0x8000_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	DRAM_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DRAM_CLK = Clock Source/M/N.
30:28	/	/	/
27	R/WAC	0x0	DRAM_UPD. SDRCLK Configuration 0 update. 0:Invalid 1:Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. Here supports dram req/ack signal. When dram_update is set to 1, dram_clk_sel/dram_div2/dram_clk1 will be updated.
26:24	R/W	0x0	DRAM_CLK_SEL. Clock Source Select. 000: DDRPLL 001: PERIPLL2X 010: PEREIPLL_800M Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.
23:10	/	/	/
9:8	R/W	0x0	DRAM_DIV2. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	DRAM_DIV1. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31. Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.

3.4.6.53 0x0804 MBUS Master Clock Gating Register (Default Value: 0x003F_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x1	NPU_MBUS_GATE_SW_CFG. NPU MBUS Clock Gate Enable. 0:Disable 1:Enable
20	R/W	0x1	VID_IN_MBUS_GATE_SW_CFG. VID_IN MBUS Clock Gate Enable. 0:Disable 1:Enable
19	R/W	0x1	VID_OUT_MBUS_GATE_SW_CFG. VID_OUT MBUS Clock Gate Enable. 0:Disable 1:Enable
18	R/W	0x1	CE_MBUS_GATE_SW_CFG. CE MBUS Clock Gate Enable. 0:Disable 1:Enable
17	R/W	0x1	VE_MBUS_GATE_SW_CFG. VE MBUS Clock Gate Enable. 0:Disable 1:Enable
16	R/W	0x1	DMA_MBUS_GATE_SW_CFG. DMA MBUS Clock Gate Enable. 0:Disable 1:Enable
15:11	/	/	/
10	R/W	0x0	G2D_MCLK_EN. Gating MBUS Clock For G2D. 0: Mask 1: Pass
9	R/W	0x0	ISP_MCLK_EN. Gating MBUS Clock For ISP. 0: Mask 1: Pass
8	R/W	0x0	CSI_MCLK_EN. Gating MBUS Clock For CSI. 0: Mask 1: Pass
7:3	/	/	/

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CE_MCLK_EN. Gating MBUS Clock For CE. 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_EN. Gating MBUS Clock For VE. 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_EN. Gating MBUS Clock For DMA. 0: Mask 1: Pass

3.4.6.54 0x080C DRAM Bus Gating Reset Register (Default Value: 0x0000_0001)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DRAM_RST. DRAM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	DRAM_GATING. Gating Clock For DRAM. 0: Mask 1: Pass

3.4.6.55 0x0830 SMHCO Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHCO_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHCO_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHCO_CLK = Clock Source/M/N.
30:27	/	/	/

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_400M 010: PERI_300M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.56 0x0834 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_400M 010: PERI_300M
23:10	/	/	/

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.</p>
7:4	/	/	/
3:0	R/W	0x0	<p>FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.</p>

3.4.6.57 0x0838 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>SMHC2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC2_CLK = Clock Source/M/N.</p>
30:27	/	/	/
26:24	R/W	0x0	<p>CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_600M 010: PERI_400M</p>
23:10	/	/	/
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.</p>
7:4	/	/	/

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.58 0x084C SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	SMHC2_RST. SMHC2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST. SMHC1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	SMHCO_RST. SMHCO Reset. 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING. Gating Clock For SMHC2. 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING. Gating Clock For SMHC1. 0: Mask 1: Pass
0	R/W	0x0	SMHCO_GATING. Gating Clock For SMHCO. 0: Mask 1: Pass

3.4.6.59 0x090C UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	UART3_RST. UART3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST. UART2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST. UART1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST. UART0 Reset. 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	UART3_GATING. Gating Clock For UART3. 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING. Gating Clock For UART2. 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING. Gating Clock For UART1. 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING. Gating Clock For UART0. 0: Mask 1: Pass

3.4.6.60 0x091C TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	TWI4_RST. TWI4 Reset. 0: Assert 1: De-assert
19	R/W	0x0	TWI3_RST. TWI3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST. TWI2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	TWI4_GATING. Gating Clock For TWI4. 0: Mask 1: Pass
3	R/W	0x0	TWI3_GATING. Gating Clock For TWI3. 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING. Gating Clock For TWI2. 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING. Gating Clock For TWI1. 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING. Gating Clock For TWI0. 0: Mask 1: Pass

3.4.6.61 0x0940 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000:HOSC 001:PERI_300M 010:PERI_200M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.62 0x0944 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI1_CLK = Clock Source/M/N.
30:27	/	/	/

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_300M 010: PERI_200M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.63 0x0948 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SPI2_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI2_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_300M 010: PERI_200M
23:10	/	/	/

Offset: 0x0948			Register Name: SPI2_CLK_REG:
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>
7:4	/	/	/
3:0	R/W	0x0	<p>FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.</p>

3.4.6.64 0x094C SPI3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x094C			Register Name: SPI3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>SPI3_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI3_CLK = Clock Source/M/N.</p>
30:27	/	/	/
26:24	R/W	0x0	<p>CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_300M 010: PERI_200M</p>
23:10	/	/	/
9:8	R/W	0x0	<p>FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8</p> <p>Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.</p>
7:4	/	/	/

Offset: 0x094C			Register Name: SPI3_CLK_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.65 0x0950 SPIF Clock Register (Default Value: 0x0000_0000)

Offset: 0x0950			Register Name: SPIF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPIF_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPIF_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_400M 010: PERI_300M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 Note: This clock divider can be switched glitch-free, and supports the dynamic configuration.
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.66 0x096C SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	SPIF_RST. SPIF Reset. 0: Assert 1: De-assert
19	R/W	0x0	SPI3_RST. SPI3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	SPI2_RST. SPI2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST. SPI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	SPIO_RST. SPIO Reset. 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	SPIF_GATING. Gating Clock For SPIF. 0: Mask 1: Pass
3	R/W	0x0	SPI3_GATING. Gating Clock For SPI3. 0: Mask 1: Pass
2	R/W	0x0	SPI2_GATING. Gating Clock For SPI2. 0: Mask 1: Pass
1	R/W	0x0	SPI1_GATING. Gating Clock For SPI1. 0: Mask 1: Pass
0	R/W	0x0	SPIO_GATING. Gating Clock For SPIO. 0: Mask 1: Pass

3.4.6.67 0x0970 EMAC_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970			Register Name: EMAC_25M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EMAC_25M_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON EMAC_25M_CLK =PERI_150M/6=25M
30	R/W	0x0	EMAC_25M_CLK_SRC_GATING. Gating the Source Clock For Low Power Design. 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

3.4.6.68 0x097C EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EMAC_RST. EMAC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMAC_GATING. Gating Clock For EMAC. 0: Mask 1: Pass

3.4.6.69 0x09EC GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GPADC_RST. GPADC Reset. 0: Assert 1: De-assert
15:1	/	/	/

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	GPADC_GATING. Gating Clock For GPADC. 0: Mask 1: Pass

3.4.6.70 0x09FC THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			Register Name: THS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	THS_RST. THS Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING. Gating Clock For THS. 0: Mask 1: Pass

3.4.6.71 0x0A10 I2S0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A10			Register Name: I2S0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2S0_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.72 0x0A14 I2S1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A14			Register Name: I2S1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2S1_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.73 0x0A20 I2S Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A20			Register Name: I2S_BGR_REG:
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	I2S1_RST. I2S1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	I2S0_RST. I2S0 Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	I2S1_GATING. Gating Clock For I2S1. 0: Mask 1: Pass
0	R/W	0x0	I2S0_GATING. Gating Clock For I2S0. 0: Mask 1: Pass

3.4.6.74 0x0A40 DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A40			Register Name: DMIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMIC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DMIC_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.75 0x0A4C DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A4C			Register Name: DMIC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMIC_RST. DMIC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING. Gating Clock For DMIC. 0: Mask 1: Pass

3.4.6.76 0x0A50 AUDIO_CODEC_DAC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A50			Register Name: AUDIO_CODEC_DAC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUDIO_CODEC_DAC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_DAC_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.77 0x0A54 AUDIO_CODEC_ADC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A54			Register Name: AUDIO_CODEC_ADC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUDIO_CODEC_ADC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_ADC_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.78 0x0A5C AUDIO_CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A5C			Register Name: AUDIO_CODEC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST. AUDIO_CODEC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING. Gating Clock For AUDIO_CODEC. 0: Mask 1: Pass

3.4.6.79 0x0A70 USBO Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USBO_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USBO_CLKEN. Gating Clock For OHCI0. 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY0_RSTN. USB PHY0 Reset. 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USBO_CLK12M_SEL OHCI0 12M Source Select. 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: RTC_32K 11: /
23:0	/	/	/

3.4.6.80 0x0A8C USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	USBOTG0_RST. USBOTG0 Reset. 0: Assert 1: De-assert
23:21	/	/	/
20	R/W	0x0	USBEHCI0_RST. USBEHCI0 Reset. 0: Assert 1: De-assert
19:17	/	/	/
16	R/W	0x0	USBOHCI0_RST. USBOHCI0 Reset. 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USBOTG0_GATING. Gating Clock For USBOTG0. 0: Mask 1: Pass
7:5	/	/	/
4	R/W	0x0	USBEHCI0_GATING. Gating Clock For USBEHCI0. 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	USBOHCI0_GATING. Gating Clock For USBOHCI0. 0: Mask 1: Pass

3.4.6.81 0x0ABC DPSS_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ABC			Register Name: DPSS_TOP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DPSS_TOP_RST. DPSS_TOP Reset. 0: Assert 1: De-assert
15:1	/	/	/

Offset: 0x0ABC			Register Name: DPSS_TOP_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DPSS_TOP_GATING. Gating Clock For DPSS_TOP. 0: Mask 1: Pass

3.4.6.82 0x0B24 DSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: DSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DSI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000:HOSC 001:PERI_200M 010:PERI_150M
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.83 0x0B4C DSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: DSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSI_RST. DSI Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	DSI_GATING. Gating Clock For DSI. 0: Mask 1: Pass

3.4.6.84 0x0B60 TCONLCD Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCONLCD_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON TCONLCD_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000:VIDEOPLL4X 001:PERIPLL2X 010:CSIPLL4X
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.85 0x0B7C TCONLCD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCONLCD_BGR_REG:
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	TCONLCD_RST. TCON LCD Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	TCONLCD_GATING. Gating Clock For TCON LCD. 0: Mask 1: Pass

3.4.6.86 0x0C04 CSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: PERI_300M 001: PERI_400M 010: VIDEOPLL4X 011: CSIPLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.87 0x0C08 CSI Master0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: CSIPLL4X 010: VIDEOPLL4X 011: PERIPLL2X
23:10	/	/	/

Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.88 0x0C0C CSI Master1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI_MASTER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: CSIPLL4X 010: VIDEOPLL4X 011: PERIPLL2X
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.89 0x0C10 CSI Master2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C10			Register Name: CSI_MASTER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER2_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: CSIPLL4X 010: VIDEOPLL4X 011: PERIPLL2X
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.90 0x0C2C CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C2C			Register Name: CSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CSI_RST. CSI Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING. Gating Clock For CSI. 0: Mask 1: Pass

3.4.6.91 0x0C7C WIEGAND Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C7C			Register Name: WIEGAND_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	WIEGAND_RST. WIEGAND Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	WIEGAND_GATING. Gating Clock For WIEGAND. 0: Mask 1: Pass

3.4.6.92 0x0D00 RISCV Clock Register (Default Value: 0x0000_0100)

Offset: 0x0D00			Register Name: RISCV_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	RISCV_CLK_SEL. Clock Source Select. 000: HOSC 001: CLK32K 010: CLK16M_RC 011: PERI_600M 100: PERI_480M 101: CPUPLL RISCV_CLK = Clock Source/M. RISCV_AXI_CLK = RISCV_CLK/N.
23:10	/	/	/
9:8	R/W	0x1	RISCV_AXI_DIV_CFG. Factor N. N = FACTOR_N +1). FACTOR_N is from 1 to 3. Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.
7:5	/	/	/
4:0	R/W	0x0	RISCV_DIV_CFG. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.93 0x0D04 RISCV Gating and Reset Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0D04			Register Name: RISCV_GATING_RST_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	RISCV_GATING_RST_FIELD. RISCV Gating and Reset Field. If RISCV_GATING_RST_FIELD == 16'h16AA, the bit[15:0] can be configured.
15:3	/	/	/
2	R/W	0x0	RISCV_SYS_APB_SOFT_RSTN. Reset for RISCV Debug Bus. 0: Assert 1: De-assert
1	R/W	0x0	RISCV_SOFT_RSTN. Reset for RISCV. 0: Assert 1: De-assert
0	R/W	0x0	RISCV_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

3.4.6.94 0x0D0C RISCV_CFG Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D0C			Register Name: RISCV_CFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	RISCV_CFG_RST. RISCV Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	RISCV_CFG_GATING. Gating Clock For RISCV. 0: Mask 1: Pass

3.4.6.95 0x0E00 PLL Pre Divider Register (Default Value: 0x0000_0000)

Offset: 0x0E00			Register Name: PLL_PRE_DIV_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/

Offset: 0x0E00			Register Name: PLL_PRE_DIV_REG
Bit	Read/Write	Default/Hex	Description
9:5	R/W	0x0	AUDIOPLL4X_DIV. Factor N. Source is AUDIOPLL_DIV2. N= FACTOR_N +1. FACTOR_N is from 0 to 31.
4:0	R/W	0x0	AUDIOPLL1X_DIV. Factor M. Source is AUDIOPLL_DIV5. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.96 0x0E04 AHB Gate Enable Register (Default Value: 0x1000_3FFF)

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AHB_MONITOR_EN AHB bus auto clock gating function enable. 1: enable auto clock gate 0: disable auto clock gate
30	/	/	/
29	R/W	0x0	SD_MONITOR_EN SD bus auto clock gating function enable. 1: enable auto clock gate 0: disable auto clock gate
28	R/W	0x1	CPUS_HCLK_GATE_SW_CFG. CPUS AHB Clock Gate Enable. 0:Disable 1:Enable
27:14	/	/	/
13	R/W	0x1	EMAC_MBUS_AHB_GATE_SW_CFG. EMAC MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
12	R/W	0x1	SMHC2_MBUS_AHB_GATE_SW_CFG. SMHC2 MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
11	R/W	0x1	SMHC1_MBUS_AHB_GATE_SW_CFG. SMHC1 MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable

Offset: 0xE04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
10	R/W	0x1	SMHCO_MBUS_AHB_GATE_SW_CFG. SMHCO MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
9	R/W	0x1	USB_MBUS_AHB_GATE_SW_CFG. USB MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
8	R/W	0x1	EMAC_AHB_GATE_SW_CFG. EMAC AHB Clock Gate Enable. 0: Disable 1: Enable
7	R/W	0x1	SMHC2_AHB_GATE_SW_CFG. SMHC2 AHB Clock Gate Enable. 0: Disable 1: Enable
6	R/W	0x1	SMHC1_AHB_GATE_SW_CFG. SMHC1 AHB Clock Gate Enable. 0: Disable 1: Enable
5	R/W	0x1	SMHCO_AHB_GATE_SW_CFG. SMHCO AHB Clock Gate Enable. 0: Disable 1: Enable
4	R/W	0x1	USB_AHB_GATE_SW_CFG. USB AHB Clock Gate Enable. 0: Disable 1: Enable
3	R/W	0x1	VID_OUT_AHB_GATE_SW_CFG. Video Out AHB Clock Gate Enable. 0: Disable 1: Enable
2	R/W	0x1	VID_IN_AHB_GATE_SW_CFG. Video in AHB Clock Gate Enable. 0: Disable 1: Enable
1	R/W	0x1	VE_AHB_GATE_SW_CFG. VE AHB Clock Gate Enable. 0: Disable 1: Enable

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	NPU_AHB_GATE_SW_CFG. NPU AHB Clock Gate Enable. 0: Disable 1: Enable

3.4.6.97 0x0E08 PERIPLL Gate Enable Register (Default Value: 0xFFFF_0FFF)

Offset: 0x0E08			Register Name: PERIPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	PERIPLL2X_GATE_SW_CFG. PERIPLL2X Clock Gate Enable. 0:Disable 1:Enable
26	R/W	0x1	PERI_800M_GATE_SW_CFG. PERI 800M Clock Gate Enable. 0:Disable 1:Enable
25	R/W	0x1	PERI_600M_GATE_SW_CFG. PERI 600M Clock Gate Enable. 0:Disable 1:Enable
24	R/W	0x1	PERI_480M_GATE_ALL_CFG. PERI 480M Clock Gate Enable. 0:Disable 1:Enable
23	R/W	0x1	PERI_480M_GATE_SW_CFG. PERI 480M Clock Gate Enable. 0:Disable 1:Enable
22	R/W	0x1	PERI_160M_GATE_SW_CFG. PERI 160M Clock Gate Enable. 0:Disable 1:Enable
21	R/W	0x1	PERI_300M_GATE_ALL_CFG. PERI 300M Clock Gate Enable. 0:Disable 1:Enable
20	R/W	0x1	PERI_300M_GATE_SW_CFG. PERI 300M Clock Gate Enable. 0:Disable 1:Enable

Offset: 0x0E08			Register Name: PERIPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
19	R/W	0x1	PERI_150M_GATE_SW_CFG. PERI 150M Clock Gate Enable. 0:Disable 1:Enable
18	R/W	0x1	PERI_400M_GATE_ALL_CFG. PERI 400M Clock Gate Enable. 0:Disable 1:Enable
17	R/W	0x1	PERI_400M_GATE_SW_CFG. PERI 400M Clock Gate Enable. 0:Disable 1:Enable
16	R/W	0x1	PERI_200M_GATE_SW_CFG. PERI 200M Clock Gate Enable. 0:Disable 1:Enable
15:12	/	/	/
11	R/W	0x1	PERIPLL2X_AUTO_GATE_EN. PERIPLL2X Clock Auto Gate Enable. 0:Auto 1:No-Auto
10	R/W	0x1	PERI_800M_AUTO_GATE_EN. PERI 800M Clock Auto Gate Enable. 0:Auto 1:No-Auto
9	R/W	0x1	PERI_600M_AUTO_GATE_EN. PERI 600M Clock Auto Gate Enable. 0:Auto 1:No-Auto
8	R/W	0x1	PERI_480M_AUTO_GATE_EN_ALL. PERI 480M Clock Auto Gate Enable. 0:Auto 1:No-Auto
7	R/W	0x1	PERI_480M_AUTO_GATE_EN. PERI 480M Clock Auto Gate Enable. 0:Auto 1:No-Auto
6	R/W	0x1	PERI_160M_AUTO_GATE_EN. PERI 160M Clock Auto Gate Enable. 0:Auto 1:No-Auto

Offset: 0x0E08			Register Name: PERIPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x1	PERI_300M_AUTO_GATE_EN_ALL. PERI 300M Clock Auto Gate Enable. 0:Auto 1:No-Auto
4	R/W	0x1	PERI_300M_AUTO_GATE_EN. PERI 300M Clock Auto Gate Enable. 0:Auto 1:No-Auto
3	R/W	0x1	PERI_150M_AUTO_GATE_EN. PERI 150M Clock Auto Gate Enable. 0:Auto 1:No-Auto
2	R/W	0x1	PERI_400M_AUTO_GATE_EN_ALL. PERI 400M Clock Auto Gate Enable All. 0:Auto 1:No-Auto
1	R/W	0x1	PERI_400M_AUTO_GATE_EN. PERI 400M Clock Auto Gate Enable. 0:Auto 1:No-Auto
0	R/W	0x1	PERI_200M_AUTO_GATE_EN. PERI 200M Clock Auto Gate Enable. 0:Auto 1:No-Auto

3.4.6.98 0x0E0C CLK24M Gate Enable Register (Default Value: 0x0000_000F)

Offset: 0x0E0C			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x1	RES_DCAP_24M_GATE_EN. RES_DCAP 24M Clock Gate Enable. 0:Disable 1:Enable
2	R/W	0x1	GPADC_24M_GATE_EN. GPADC 24M Clock Gate Enable. 0:Disable 1:Enable
1	R/W	0x1	WIEGAND_24M_GATE_EN. WIEGAND 24M Clock Gate Enable. 0:Disable 1:Enable

Offset: 0x0E0C			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	USB_24M_GATE_EN. USB 24M Clock Gate Enable. 0:Disable 1:Enable

3.4.6.99 0x0F00 CCMU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCMU_SEC_SWITCH_REG:
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MBUS_SEC. MBUS clock register security. 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC. Bus relevant registers security. 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC. PLL relevant registers security. 0: Secure 1: Non-secure

3.4.6.100 0x0F04 GPADC Clock Select Register (Default Value: 0x0000_0000)

Offset: 0x0F04			Register Name: GPADC_CLK_SEL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Reserved
30:23	/	/	/
22:20	R/W	0x0	GPADC_24M_CLK_SEL GPADC 24M Clock Source Select. 000:HOSC/32 001:HOSC/16 010:HOSC/8 011:HOSC/4 100:HOSC/2 101:HOSC
19:0	/	/	/

3.4.6.101 0x0F08 Frequency Detect Control Register (Default Value: 0x0000_0020)

Offset: 0x0F08			Register Name: FRE_DET_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W0C	0x0	ERROR_FLAG. Error Flag. 0: Write 0 to clear 1: Error
30:9	/	/	/
8:4	R/W	0x2	DET_TIME Detect Time Time=1/32k*(2^RegValue) Note: RegValue is form 0 to 16.
3:2	/	/	/
1	R/W	0x0	FRE_DET_IRQ_EN. Frequency Detect IRQ Enable. 0: Disable 1: Enable
0	R/W	0x0	FRE_DET_FUN_EN. Frequency Detect Function Enable. 0: Disable 1: Enable

3.4.6.102 0x0F0C Frequency Up Limit Register (Default Value: 0x0000_0000)

Offset: 0x0F0C			Register Name: FRE_UP_LIM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FRE_UP_LIM. Frequency Up Limit. Note: The value of the register must be an integral multiple of 32. The unit is kHz.

3.4.6.103 0x0F10 Frequency Down Limit Register (Default Value: 0x0000_0000)

Offset: 0x0F10			Register Name: FRE_DOWN_LIM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FRE_DOWN_LIM. Frequency Down Limit. Note: The value of the register must be an integral multiple of 32. The unit is kHz.

3.4.6.104 0x0F30 CCMU FANOUT CLOCK GATE Register (Default Value:0x0000_0000)

Offset: 0x0F30			Register Name: CCMU_FAN_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CLK25M_EN. Gating for CLK25M . 0: Clock is OFF 1: Clock is ON
2	R/W	0x0	CLK16M_EN. Gating for CLK16M . 0: Clock is OFF 1: Clock is ON
1	R/W	0x0	CLK12M_EN. Gating for CLK12M . 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	CLK24M_EN. Gating for CLK24M . 0: Clock is OFF 1: Clock is ON

3.4.6.105 0x0F34 CLK27M FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F34			Register Name: CLK27M_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLK27M_EN. Gating for CLK27M. 0: Clock is OFF 1: Clock is ON SCLK=Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK27M_SCR_SEL. Clock Source Select. 000: VIDEOPLL1X 001: CSIPLL1X 010: PERI_300M 011: /
23:10	/	/	/

Offset: 0x0F34			Register Name: CLK27M_FAN_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	CLK27M_DIV1. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	CLK27M_DIV0. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.106 0x0F38 CLK FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F38			Register Name: CLK_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCLK_DIV_EN. Gating for PCLK. 0: Clock is OFF 1: Clock is ON PCLK = APB0_CLK/M/N.
30:10	/	/	/
9:5	R/W	0x0	PCLK_DIV1. Factor N. N= FACTOR_N +1. FACTOR_N is from 0 to 31.
4:0	R/W	0x0	PCLK_DIV. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.107 0x0F3C CCMU FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	Reserved
23	R/W	0x0	CLK_FANOUT2_EN. Gating for CLK_FANOUT2. 0: Clock is OFF 1: Clock is ON

Offset: 0x0F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
22	R/W	0x0	CLK_FANOUT1_EN. Gating for CLK_FANOUT1. 0: Clock is OFF 1: Clock is ON
21	R/W	0x0	CLK_FANOUT0_EN. Gating for CLK_FANOUT0. 0: Clock is OFF 1: Clock is ON
20:18	/	/	/
17:9	R/W	0x0	Reserved
8:6	R/W	0x0	CLK_FANOUT2_SEL. Clock Fanout2 Select. 000:CLK32K_FANOUT(From SYSRTC) 001:CLK12M(From DCXO/2) 010:CLK16M(From PERI_160M/10) 011:CLK24M(From DCXO) 100:CLK25M(From PERI_150M/6) 101:CLK27M 110:PCLK CLK_FANOUT2 can be selected to output from the above seven sources.
5:3	R/W	0x0	CLK_FANOUT1_SEL. Clock Fanout1 Select. 000:CLK32K_FANOUT(From SYSRTC) 001:CLK12M(From DCXO/2) 010:CLK16M(From PERI_160M/10) 011:CLK24M(From DCXO) 100:CLK25M(From PERI_150M/6) 101:CLK27M 110:PCLK CLK_FANOUT1 can be selected to output from the above seven sources.

Offset: 0x0F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	<p>CLK_FANOUT0_SEL. Clock Fanout0 Select.</p> <p>000:CLK32K_FANOUT(From SYSRTC) 001:CLK12M(From DCXO/2) 010:CLK16M(From PERI_160M/10) 011:CLK24M(From DCXO) 100:CLK25M(From PERI_150M/6) 101:CLK27M 110:PCLK</p> <p>CLK_FANOUT0 can be selected to output from the above seven sources.</p>



3.5 BROM System

3.5.1 Overview

The system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) that is considered the primary program-loader. On the startup process, the V853/V853S starts to fetch the first instruction from address 0x0, where is the BROM located at.

The BROM system is divided into two parts: the firmware exchange launch (FEL) module and the Medium Boot module. FEL is responsible for writing the external data to the local NVM, and Medium Boot is responsible for loading an effective and legitimate BOOT0 from NVM and running.

- The BROM system includes the following features:
- Supports CPU0 boot process
- Supports mandatory upgrade process through USB or SMHCO
- Supports eFuse to select the boot media type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Ensures that the Secure Boot is in a trusted environment

3.5.2 Functional Descriptions

The BROM configurations mainly select the boot medium and the boot mode.

3.5.2.1 Selecting the Boot Medium

The BROM system supports the following boot media:

- SD/EMMC
- SPI NOR
- SPI NAND

There are two ways to select the boot medium: GPIO Pin Select and eFuse Select. The BROM will read the state of BOOT_MODE first, and then select the boot medium according to the state of BOOT_MODE. The BOOT_MODE is the BROM_Config in the eFuse mapping.

The following table shows the BOOT_MODE setting:

Table 3-6 BOOT_MODE Setting

BOOT_MODE[0]	Boot Select Type
0	GPIO Pin Select
1	eFuse Select

GPIO Boot Select

If the state of the BOOT_MODE is 0, the boot medium is decided by the value of the GPIO pin. The following table shows the boot medium priority. The boot medium priority describes the possibility that each medium to be selected as the boot medium. The BROM reads the boot0 of the medium with the highest priority first. If the medium does not exist or has any problems, the BROM will try the next medium. Otherwise, the medium will be selected as the boot medium.

Table 3-7 GPIO Boot Select

Pin_Boot_Select[1:0]	Boot Medium Priority
00	SPI0 NAND->SPI0 NOR(4 wire)-> SPI NOR(1 wire)->USB
01	SPI0 NOR(4 wire)-> SPI0 NOR(1 wire)->SPI0 NAND->USB
10	SDC0->SPI0 NAND->SPI0 NOR(4 wire)-> SPI0 NOR(1 wire)->UART BRUN->USB
11	SDC0->SPI0 NOR(4 wire)-> SPI0 NOR(1 wire) -> EMMC2-> SPI0 NAND->UART BRUN->USB



The status of the GPIO boot select pin can be read by the bit[12:11] of the system configuration module (register: 0x03000024).

eFuse Boot Select

If the state of the BOOT_MODE is 1, the boot medium is decided by the value of eFuse_Boot_Select_Cfg. The eFuse_Boot_Select_Cfg is divided into 4 groups and each group is 3-bit. The following table shows the groups of eFUSE_Boot_Select.

Table 3-8 Groups of eFuse_Boot_Select

eFuse_Boot_Select_Cfg[11:0]	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

These four groups take effect with the following priority:

eFuse_Boot_Select_1 -> eFuse_Boot_Select_2 -> eFuse_Boot_Select_3 -> eFuse_Boot_Select_4

For example, eFuse_Boot_Select_2 will not take effect unless eFuse_Boot_Select_1 is set as 0x111, eFuse_Boot_Select_3 will not take effect unless eFuse_Boot_Select_2 is set as 0x111(skip), etc.

The following table shows the boot medium priority for the different values of eFuse_Boot_Select_n, where n = [4:1]. The eFuse_Boot_Select_1 to eFuse_Boot_Select_3 are the same setting. But for eFuse_Boot_Select_4,

if its value is 0x111, the BROM will select the boot medium in the Try mode. The BROM in the Try mode follows the order below to select the boot medium:

SMHC0 -> SPI NOR -> SPI NAND -> SMHC2

Table 3-9 eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot Medium Priority
000	Try
001	reserved
010	EMMC2_USER-> EMMC2_BOOT
011	SPI0 NOR(4 wire)-> SPI0 NOR(1 wire)
100	SPI0 NAND
101	SPI0 NOR(1 wire)-> SPI0 NOR(4 wire)
110	EMMC2_BOOT-> EMMC2_USER
111	When n is 1 to 3: The boot medium is decided by the value of eFuse_Boot_Select_(n + 1) . When n is 4: Select the boot medium in Try mode.

3.5.2.2 Selecting the Boot Mode

For SoCs that have implemented and enabled the ARM TrustZone technology, there are two boot modes: Normal BROM Mode and Secure BROM Mode.

Secure BROM Mode is designed to protect against attackers modifying the code or data areas in the programmable memory.

During the startup process, the BROM will select the boot mode according to the value of the Secure Enable bit. If the value of Secure Enable bit is 0, the system will boot in Normal BROM Mode. Otherwise, it will boot in Secure BROM Mode.



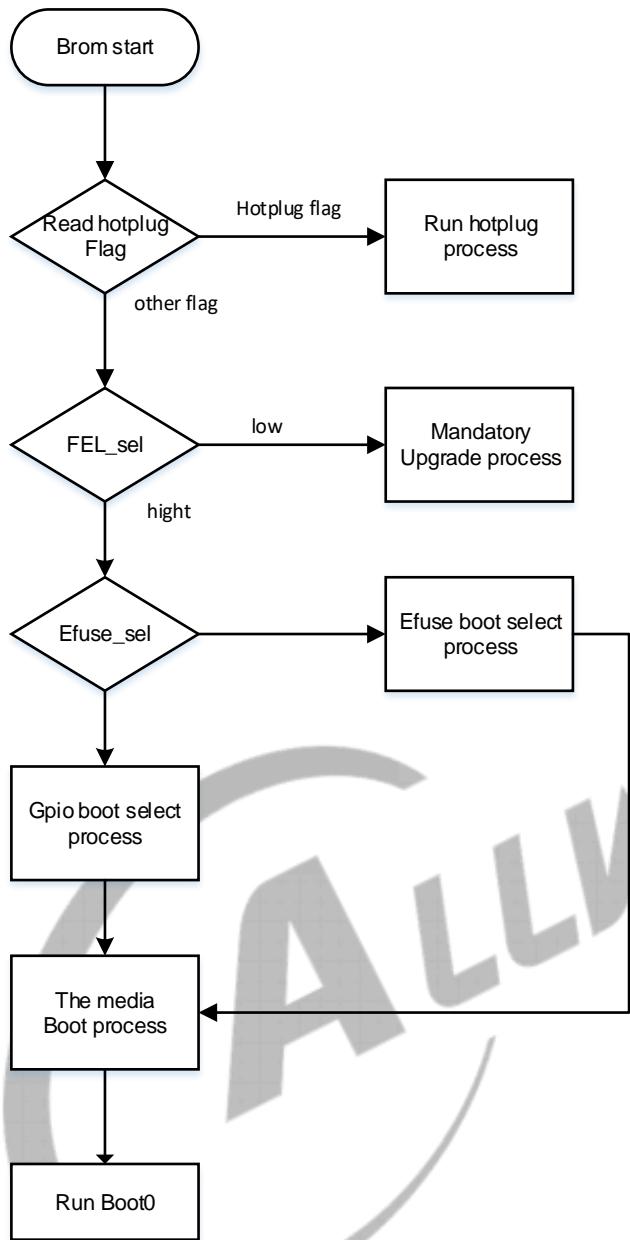
NOTE

The System on Chip (SoC) supports the ARM TrustZone technology. If the Secure Enable Bit is enabled, the BROM will be safely booted based on this ARM TrustZone technology.

Normal BROM Mode

In Normal BROM Mode, the system boot starts from CPU0, and then BROM will read the state of the FEL Pin. If the FEL Pin signal is high, then the system will jump to the boot process, or jump to the mandatory upgrade process.

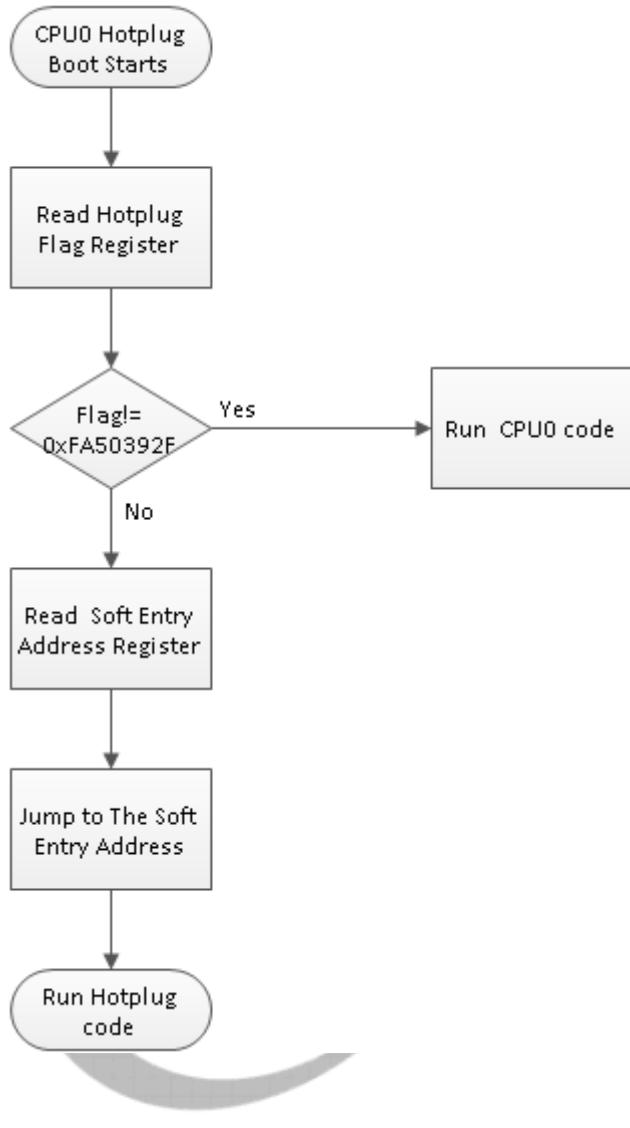
The following figure shows the boot process in Normal BROM Mode.

Figure 3-7 Boot Process in Normal BROM Mode

Hotplug Process

The Hotplug Flag determines whether the system will do Hotplug boot, if the CPU Hotplug Flag value is equal to 0xFA50392F, then read the Soft Entry Register and the system will jump to the Soft Entry Address. The following figure shows the CPU0 Hotplug Process.

Figure 3-8 CPU0 Hotplug Process Diagram



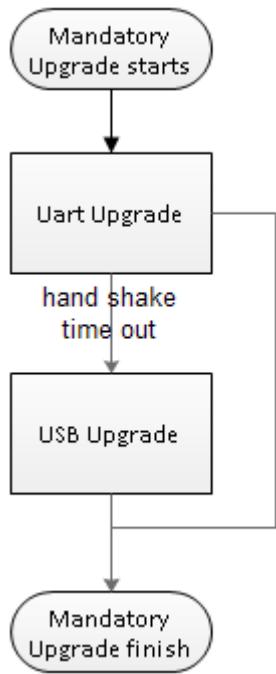
The Hotplug Flag Register is 0x070005C0.

The Soft Entry Address Register is 0x070005C4.

Mandatory Upgrade Process

If the FEL pin is detected to pull low, the system will jump to the mandatory upgrade process. The following figure shows the mandatory upgrade process.

Figure 3-9 Mandatory Upgrade Process



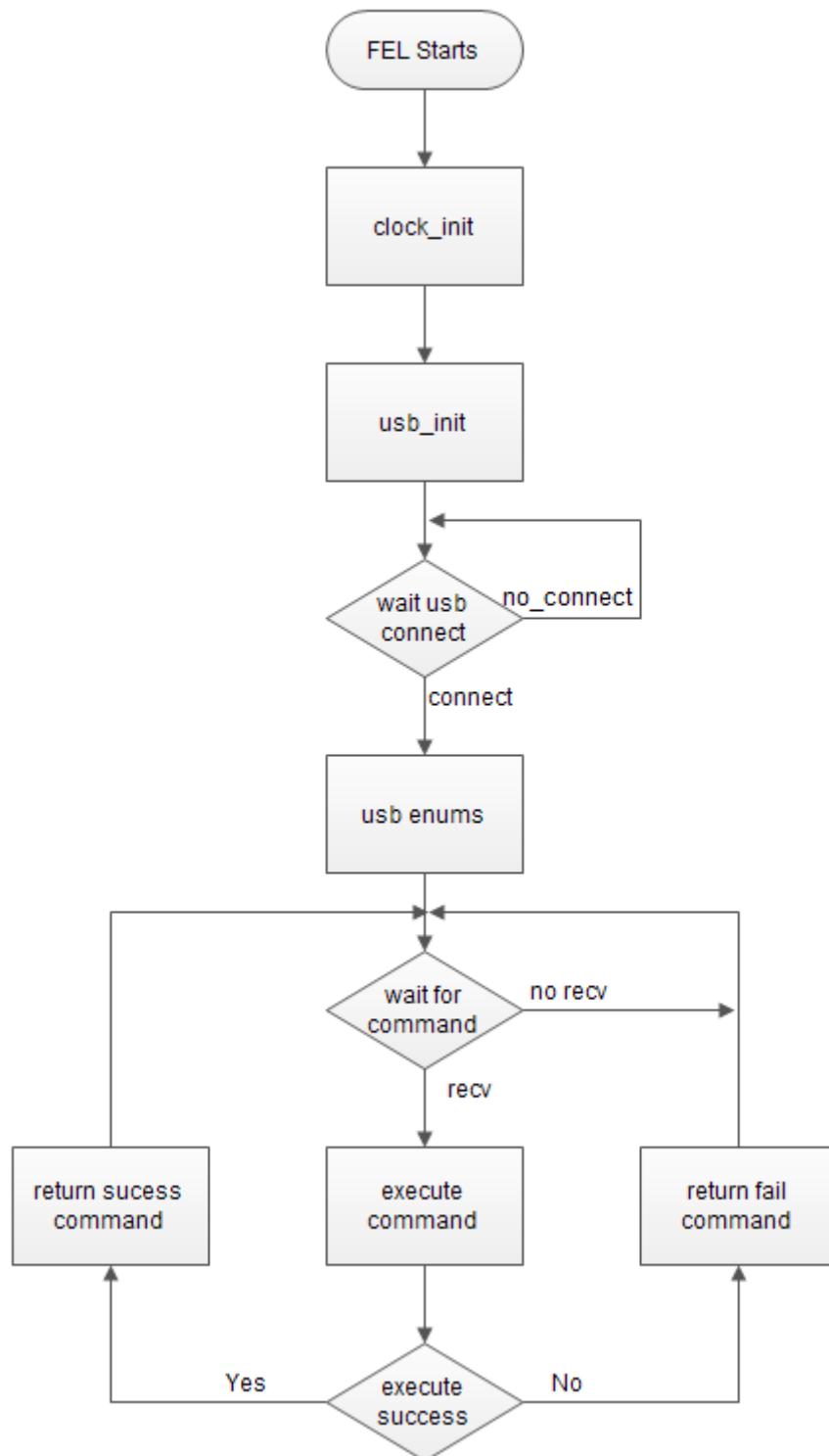
The FEL Address of the BROM is 0x20.

The status of the FEL pin is the bit[8] of the system configuration module (register: 0x03000024).

FEL Process

When the system chooses to enter the Mandatory Upgrade Process, the system will jump to the FEL process. The following figure shows the FEL upgrade process.

Figure 3-10 USB FEL Process

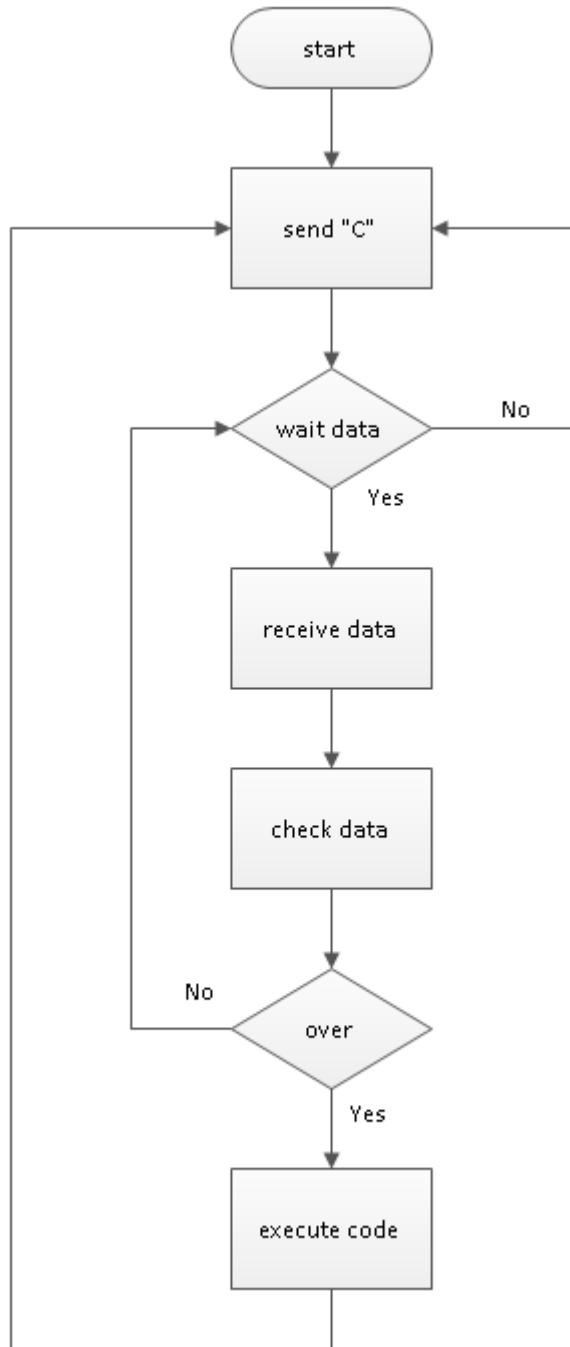


UART Upgrade Process

When the system chooses to enter Mandatory Upgrade Process, if the boot_select2 pin signal is detected to pulled to low level, then the system will jump to the Uart Upgrade Process.

The following figure shows the Uart Upgrade Process:

Figure 3-11 Uart Boot Process Diagram



Fast Boot Process

If the value of the Fast Boot register (0x07090120) in RTC module is not zero, the system will enter the Fast Boot Process. The following table shows the boot medium priority for different values of the Fast Boot register.

Table 3-10 Fast Boot Select Setting

Reg_bit[31:28]	Boot Select type
1	reserve
2	EMMC2_USR->EMMC2_BOOT
3	SPI NOR(1 wire)->SPI NOR(4 wire)
4	SPI NAND
5	EMMC2_BOOT->EMMC2_USR
6	reserve
7	reserve
8	SPI NOR(4 wire)->SPI NOR(1 wire)

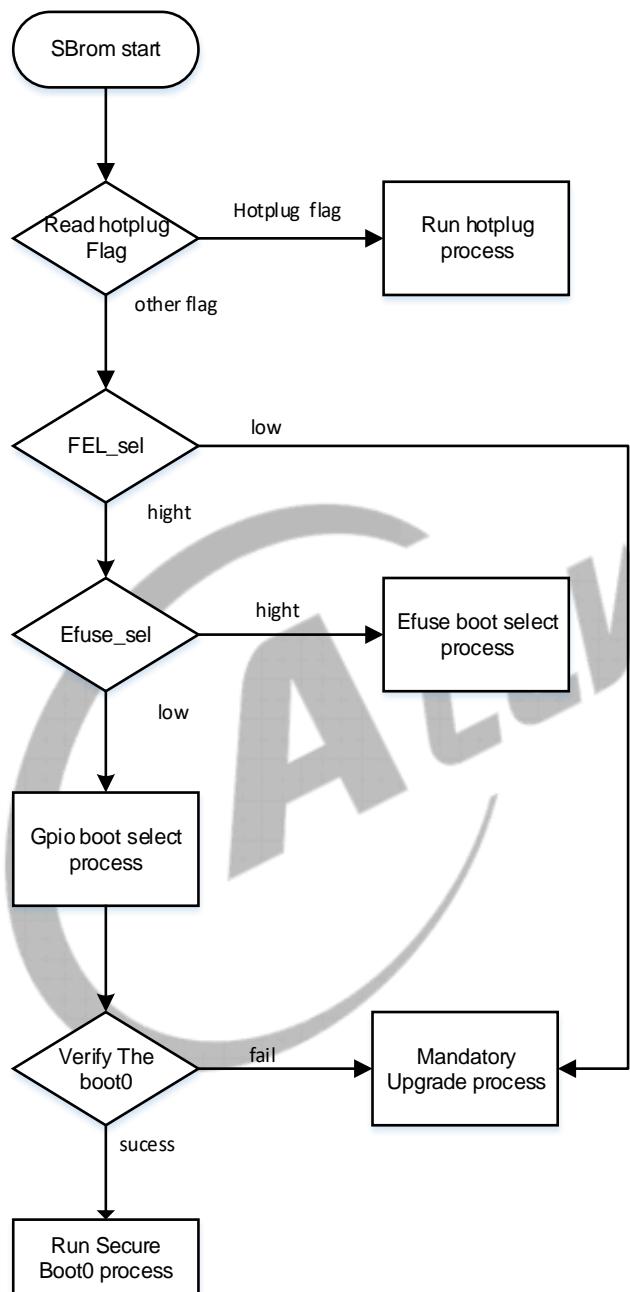


Secure BROM Mode

In Security boot mode, By comparison with Normal BROM, after the Try Media Boot process finishes, the system will go to run Security BROM software.

The following figure shows the Secure BROM Process:

Figure 3-12 Security BROM Process Diagram



3.6 System Configuration

3.6.1 Overview

The system configuration module is used to configure parameters for system domain, such as SRAM, CPU, PLL, BROM, and so on.

3.7 Timer

3.7.1 Overview

The timer module implements the timing and counting functions. The timer module includes timer0 to timer3, watchdog and audio video synchronization (AVS).

The main features for timer0 to timer3 are as follows:

- Alternative count clock: LOSC or OSC24M. The LOSC can be either the internal or external low-frequency clock, and the external one has more accuracy.
- Supports 8 prescale factors
- Programmable 32-bit down timer
- Supports two timing modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system. The main features for the watchdog are as follows:

- Single clock source: OSC24M/750
- Supports 12 initial values
- Supports the generation of timeout interrupts
- Supports the generation of reset signals
- Supports Watchdog Restart

The AVS is used to synchronize the audio and video. The AVS module includes AVS0 and AVS1, which are completely consistent. The main features for the AVS are as follows:

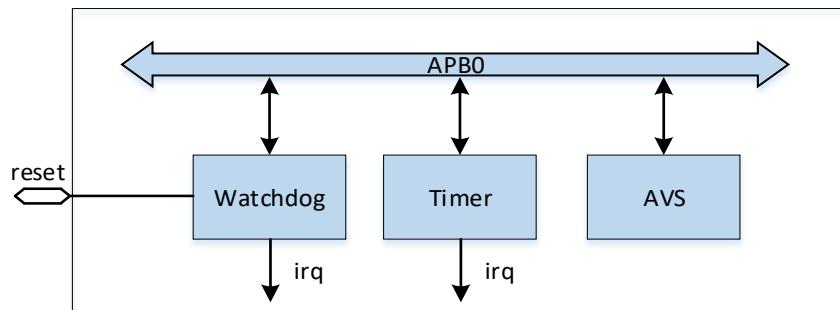
- Single clock source: OSC24M
- Programmable 33-bit up timer

- Supports updating the initial value anytime
- 12-bit frequency divider factor
- Supports Pause/Start function

3.7.2 Block Diagram

The following figure shows the functional block diagram of the timer module.

Figure 3-13 Timer Block Diagram



The watchdog, timer (including timer0, timer1, timer2 and timer3), and AVS are all mounted at the APBO bus. The system configures the parameters of these configure registers via APBO bus.

The timer and watchdog are both down counters and support generating interrupts after the counting value reaches 0.

For watchdog, the system is responsible for configuring the interval value. If the system fails to restart the watchdog regularly because of some exceptional situations, such as the bus hang, the watchdog will send out a Watchdog Reset External signal to reset the system. And the signal will be transmitted to the Reset pad to reset the PMIC.

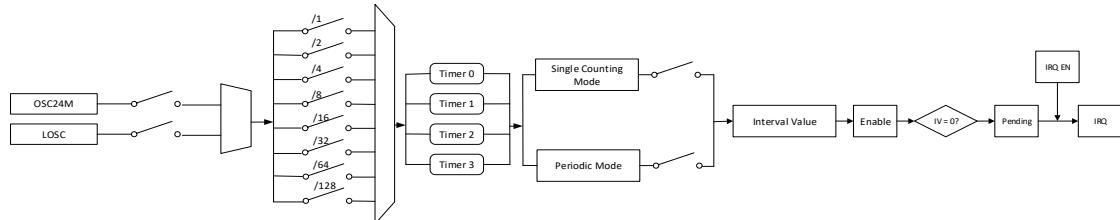
3.7.3 Functional Description

3.7.3.1 Timer

The timer (including timer0, timer1, timer2 and timer3), is a 32-bit down counter. The counter value is decremented by 1 on each rising edge of the timer clock.

The following figure shows the block diagram for the timer.

Figure 3-14 Block Diagram for the Timer



The clock source for the timer can be either OSC24M or LOSC. For LOSC, it can be either the internal or external low-frequency clock. The external one has more accuracy.

Each timer has a prescale that divides the working clock frequency by 1, 2, 4, 8, 16, 32, 64, or 128. And each timer can generate independent interrupts.

Timing Modes

The timer has two timing modes: the single counting mode and periodic mode. You can configure the timing mode via the bit[7] of [TMRn_CTRL_REG](#) (n = 0, 1, 2 or 3). The value 0 is for the period mode and value 1 is for the single counting mode.

- Single Counting Mode

In the single counting mode, the timer starts counting from the interval value and generates an interrupt after the counter decreases to 0, and then stops counting. It starts to count again only when a new interval value is loaded.

- Periodic Mode

In the periodic mode, the timer restarts another round of counting after generating the interrupt. It reloads data from the [TMRn_INTV_VALUE_REG](#) and then continues to count.

Formula for Calculating the Timer Time

The following formula describes the relationship among timer parameters.

$$T_{\text{timer}} = \frac{TMRn_INTV_VALUE_REG - TMRn_CUR_VALUE_REG}{TMRn_CLK_SRC} \times TMRn_CLK_PRES$$

Where,

The parameter n is either 0, 1, 2, or 3;

T_{timer} is the remaining time of the timer;

TMRn_INTV_VALUE_REG is the interval value of the timer;

TMRn_CUR_VALUE_REG is the current value of the timer;

TMRn_CLK_SRC is the frequency of the timer clock source;

TMRn_CLK_PRES is the prescale ratio of the timer clock.

Initializing the Timer

Follow the steps below to initialize the timer:

1. Configure the timer parameters clock source, prescale factor, and timing mode by writing [TMRn_CTRL_REG](#). There is no sequence requirement of configuring the parameters.

2. Write the interval value.
 - a) Write [TMRn_INTV_VALUE_REG](#) to configure the interval value for the timer.
 - b) Write bit[1] of [TMRn_CTRL_REG](#) to load the interval value to the timer. The value of the bit will be cleared automatically after loading the interval value.
3. Write bit[0] of [TMRn_CTRL_REG](#) to start the timer. To get the current value of the timer, read [TMRn_CUR_VALUE_REG](#).

Processing the Interrupt

Follow the steps below to process the interrupt:

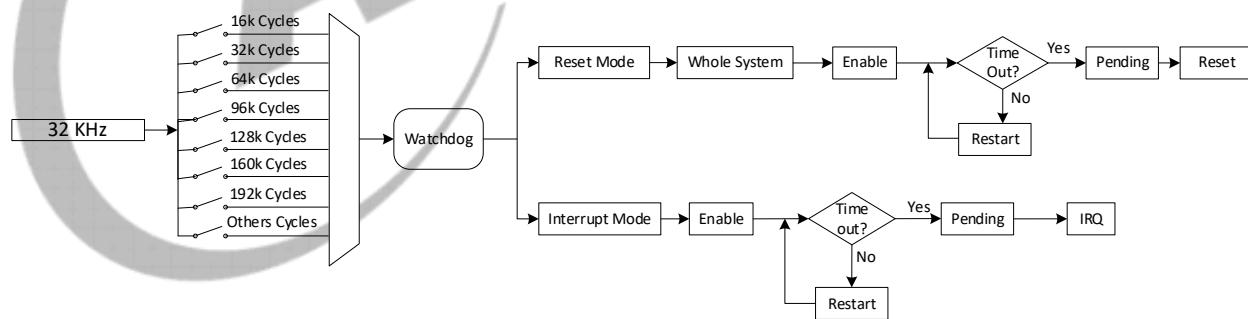
1. Enable interrupts for the timer: write the enable bit of the corresponding interrupt in [TMR IRQ_EN_REG](#) for the timer. The timer will generate an interrupt everytime the count value reaches 0.
2. After entering the interrupt process, write the pending bit of the corresponding interrupt in [TMR IRQ_STA_REG](#) to clear the interrupt pending, and execute the process of waiting for the interrupt.
3. Resume the interrupt and continue to execute the interrupted process.

3.7.3.2 Watchdog

The watchdog is a 32-bit down counter. The counter value is decremented by 1 on each rising edge of the count clock.

The following figure shows the block diagram for the watchdog.

Figure 3-15 Block Diagram for the Watchdog



The clock source of the watchdog is OSC24M/750. There are 12 configurable initial count values.

Operating Modes

The watchdog has two operating modes: the interrupt mode and reset mode.

- In the interrupt mode, when the counter value reaches 0 and WDOG_IRQ_EN_REG is enabled, the watchdog generates an interrupt.
- In the reset mode, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

You can configure the operating mode for the watchdog via the bit[1:0] of the WDOG_CFG_REG. The value 0x2 is for the interrupt mode and the value 0x1 is for the reset mode.

Both the interrupt mode and reset mode support Watchdog Restart. You can make the watchdog to count from the initial value at any time by configuring the WDOG_CTRL_REG: write 0xA57 to bit[12:1], then write 1 to bit[0].

Initializing the Watchdog

Follow the steps below to initialize the watchdog:

1. Write the bit[1:0] of [WDOG_CFG_REG](#) to configure the watchdog operating mode so that the watchdog can generate interrupts or output reset signals.
2. Write the bit[7:4] of [WDOG_MODE_REG](#) to configure the initial count value.
3. Write the bit[0] of [WDOG_MODE_REG](#) to enable the watchdog.

Processing the Interrupt

In the interrupt mode, the watchdog is used as a counter. It generates an interrupt everytime the count value reaches 0.

Follow the steps below to process the interrupt:

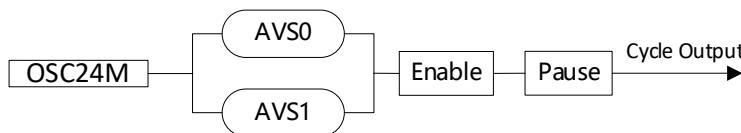
1. Write the enable bit of [WDOG_IRQ_EN_REG](#) to enable the interrupt.
2. After entering the interrupt process, write the pending bit of [WDOG_IRQ_STA_REG](#) to clear the interrupt pending and execute the process of waiting for the interrupt.
3. Resume the interrupt and continue to execute the interrupted process.

3.7.3.3 AVS

The AVS is a 33-bit up counter. The counter value is increased by 1 on each rising edge of the count clock. There is a clock gate in section 3.4 Clock Controller Unit (CCU) to control the output of the AVS counter. To operate the AVS, open the clock gate first.

The following figure shows the block diagram for the AVS.

Figure 3-16 Block Diagram for the AVS



The clock source of the AVS is OSC24M. There is a 12-bit division factor for each AVS, N0 for AVS0 and N1 for AVS1. When the timer increases from 0 to N1 or N2, the AVS counter adds 1. When the counter reaches 33-bit upper limit, the AVS will start to count from the initial value again.

The AVS supports changing the initial value and division factor at anytime. And the AVS supports restarting from the initial value or pausing at anytime.

Starting or Pausing the AVS

Follow the steps below:

1. Write [AVS_CNT_DIV_REG](#) to configure the division factor.
2. Write [AVS_CNTn_REG](#) ($n = 0$ or 1) to configure the initial value.
3. Write [AVS_CNT_CTL_REG](#) to enable the AVS. You can pause the AVS at any time.

3.7.4 Programming Guidelines

3.7.4.1 Configuring the Timer

The following example shows how to make a one-millisecond delay with the clock source selected as OSC24M, the operating mode sets as single counting mode, and the pre-scale sets as 2.

```
writel(0x2EE0, TMR_0_INTV);           //Set the interval value  
writel(0x94, TMR_0_CTRL);            //Select Single mode, 24 MHz clock source, 2 pre-scale  
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL); //Set the Reload bit  
while((readl(TMR_0_CTRL)>>1)&1);        //Waiting the Reload bit turns to 0  
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL); //Enable Timer0
```

3.7.4.2 Resetting the Watchdog

The following example shows how to make the watchdog to generate a reset signal to the whole system after 1 second. The clock source for the watchdog is OSC24M/750.

```
writel(0x1, WDOG_CONFIG);           //Set the operating mode as the reset mode.  
writel(0x10, WDOG_MODE);            //Set the interval value as 1 s.  
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE); //Enable the Watchdog.
```

3.7.4.3 Restarting the Watchdog

The following example shows how to restart the watchdog. In this example, the clock source is OSC24M/750, the interval value is 1 second, and the watchdog operating mode is the reset mode.

If the execution time of “other codes” is shorter than 1 second, the watchdog will restart from the interval value before it count to zero and generates the reset signal. Otherwise, the watchdog will reset the whole system before the code “writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0), WDOG_CTRL)” is executed.

```
writel(0x1, WDOG_CONFIG);           //To whole system
writel(0x10, WDOG_MODE);           //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE); //Enable Watchdog
---other codes---
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0), WDOG_CTRL); //Write 0xA57 at Key Field and Restart Watchdog
```

3.7.5 Register List

Module Name	Base Address
Timer	0x0205 0000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer IRQ Status Register
TMRO_CTRL_REG	0x0010	Timer 0 Control Register
TMRO_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMRO_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
TMR2_CTRL_REG	0x0030	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x0034	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x0038	Timer 2 Current Value Register
TMR3_CTRL_REG	0x0040	Timer 3 Control Register
TMR3_INTV_VALUE_REG	0x0044	Timer 3 Interval Value Register
TMR3_CUR_VALUE_REG	0x0048	Timer 3 Current Value Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_SOFT_RST_REG	0x00A8	Watchdog Software Reset Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register
WDOG_OUTPUT_CFG_REG	0x00BC	Watchdog Output Configuration Register
AVS_CNT_CTL_REG	0x00C0	AVS Counter Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Counter Divisor Register

3.7.6 Register Description

3.7.6.1 0x0000 Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TMR3_IRQ_EN. Timer 3 Interrupt Enable. 0: disable 1: enable
2	R/W	0x0	TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: disable 1: enable
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: disable 1: enable
0	R/W	0x0	TMRO_IRQ_EN. Timer 0 Interrupt Enable. 0: disable 1: enable

3.7.6.2 0x0004 Timer IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	TMR3_IRQ_PEND. Timer 3 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.
2	R/W1C	0x0	TMR2_IRQ_PEND. Timer 2 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.
0	R/W1C	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.

3.7.6.3 0x0010 Timer 0 Control Register (Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMRO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMRO_MODE. Timer 0 mode. 0: Periodic mode. When the interval value of the timer 0 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 0 is reached, the timer will stop counting.
6:4	R/W	0x0	TMRO_CLK_PRES. Select the prescale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMRO_CLK_SRC. Timer0 Clock Source. 00:LOSC 01: OSC24M 10: / 11: /

Offset: 0x0010			Register Name: TMRO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	<p>TMRO_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it's cleared automatically.</p>
0	R/W	0x0	<p>TMRO_EN. Timer 0 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.</p>

3.7.6.4 0x0014 Timer 0 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TMRO_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMRO_INTV_VALUE. Timer 0 Interval Value.



Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.5 0x0018 Timer 0 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer0 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.6 0x0020 Timer 1 Control Register (Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Periodic mode. When the interval value of the timer 1 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 1 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the prescale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer1 Clock Source. 00:LOSC 01:OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	<p>TMR1_EN.</p> <p>Timer 1 Enable.</p> <p>0: Stop/Pause</p> <p>1: Start</p> <p>By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0.</p> <p>By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer.</p> <p>The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1.</p> <p>Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.</p>

3.7.6.7 0x0024 Timer 1 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>TMR1_INTV_VALUE.</p> <p>Timer 1 Interval Value.</p>



Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.8 0x0028 Timer 1 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: TMR1_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>TMR1_CUR_VALUE.</p> <p>Timer1 current value is a 32-bit down-counter (from interval value to 0).</p>

3.7.6.9 0x0030 Timer 2 Control Register (Default Value: 0x0000_0004)

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR2_MODE. Timer 2 mode. 0: Periodic mode. When the interval value of the timer 1 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 1 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR2_CLK_PRES. Select the prescale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer2 Clock Source. 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	<p>TMR2_EN.</p> <p>Timer 2 Enable.</p> <p>0: Stop/Pause</p> <p>1: Start</p> <p>By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0.</p> <p>By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer.</p> <p>The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1.</p> <p>Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.</p>

3.7.6.10 0x0034 Timer 2 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TMR2_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>TMR2_INTV_VALUE.</p> <p>Timer 2 Interval Value.</p>



Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.11 0x0038 Timer 2 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: TMR2_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>TMR2_CUR_VALUE.</p> <p>Timer2 current value is a 32-bit down-counter (from interval value to 0).</p>

3.7.6.12 0x0040 Timer 3 Control Register (Default Value: 0x0000_0004)

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR3_MODE. Timer 3 mode. 0: Periodic mode. When the interval value of the timer 1 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 1 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR3_CLK_PRES. Select the prescale of timer 3 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR3_CLK_SRC. Timer3 Clock Source. 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR3_RELOAD. Timer 3 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	<p>TMR3_EN.</p> <p>Timer 3 Enable.</p> <p>0: Stop/Pause</p> <p>1: Start</p> <p>By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0.</p> <p>By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer.</p> <p>The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1.</p> <p>Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.</p>

3.7.6.13 0x0044 Timer 3 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: TMR3_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>TMR3_INTV_VALUE.</p> <p>Timer 3 Interval Value.</p>



Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.14 0x0048 Timer 3 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: TMR3_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>TMR3_CUR_VALUE.</p> <p>Timer3 current value is a 32-bit down-counter (from interval value to 0).</p>

3.7.6.15 0x00A0 Watchdog IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: WDOG_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: disable 1: enable.

3.7.6.16 0x00A4 Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: WDOG_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ_PEND. Watchdog IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, indicates that the interval value of the watchdog is reached.

3.7.6.17 0x00A8 Watchdog Software Reset Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: WDOG_SOFT_RST_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field To change the value of bit[0], this field should be filled with 0x16AA.
15:1	/	/	/
0	R/W1C	0x0	Soft Reset Enable 0: De-assert 1: Reset the system Note: To use the bit to reset the system, the watchdog first needs to be disabled.

3.7.6.18 0x00B0 Watchdog Control Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: WDOG_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

Offset: 0x00B0			Register Name: WDOG_CTRL_REG
Bit	Read/Write	Default/Hex	Description
12:1	W	0x0	WDOG_KEY_FIELD Watchdog Key Field It should be written to 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART Watchdog Restart 0: No effect 1: Restart the watchdog

3.7.6.19 0x00B4 Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name: WDOG_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field To change the value of bit[15:0], this field should be filled with 0x16AA.
15:9	/	/	/
8	R/W	0x0	WDOG_CLK_SRC Select the clock source for the watchdog. 0: HOSC_32K, that is, OSC24M/750. It is a 32 KHz clock divided from the OSC24M. 1: LOSC_32K. A clock provided by the LOSC.
7:2	/	/	/
1:0	R/W	0x1	WDOG_MODE Configure the operating mode for the watchdog 00: / 01: To whole system 10: Only interrupt mode 11: /

3.7.6.20 0x00B8 Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: WDOG_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field To change the value of bit[15:0], this field should be filled with 0x16AA.
15:8	/	/	/

Offset: 0x00B8			Register Name: WDOG_MODE_REG
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	<p>WDOG_INTV_VALUE Watchdog Interval Value 0000: 16000 cycles (0.5 s) 0001: 32000 cycles (1 s) 0010: 64000 cycles (2 s) 0011: 96000 cycles (3 s) 0100: 128000 cycles (4 s) 0101: 160000 cycles (5 s) 0110: 192000 cycles (6 s) 0111: 256000 cycles (8 s) 1000: 320000 cycles (10 s) 1001: 384000 cycles (12 s) 1010: 448000 cycles (14 s) 1011: 512000 cycles (16 s) Others: Reserved</p> <p>Note: The corresponding clock cycles for the interval value (IV) depends on the frequency of the clock: Cycles = $F_{CLK} * IV$. For example, to get a interval value of 0.5 second, if the clock source is HOSC_32K (whose frequency is 32 KHz), the cycle number is 16,000; if the clock source is LOSC_32K (whose frequency is 32.768 kHz), the cycle number is 16,384.</p>
3:1	/	/	/
0	R/W	0x0	<p>WDOG_EN Watchdog Enable 0: No effect 1: Enable the Watchdog</p>

3.7.6.21 0x00BC Watchdog Output Configuration Register (Default Value: 0x0000_001F)

Offset: 0x00BC			Register Name: WDOG_OUTPUT_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x1F	<p>WDOG OUTPUT CONFIG Configure the valid time for the watchdog reset signal. $T = 1/32ms*(N + 1)$ The default value is 1 ms.</p>

3.7.6.22 0x00C0 AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Do not pause. 1: Pause the AVS counter1.
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Do not pause. 1: Pause the AVS counter0.
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/Disable The clock source is OSC24M. 0: Disabled 1: Enabled
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 0 Enable/Disable The clock source is OSC24M. 0: Disabled 1: Enabled

3.7.6.23 0x00C4 AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	AVS_CNT0 The higher 32 bits of AVS counter0. AVS counter0 is a 33-bit up counter. The initial value consists of two parts: this register forms the bit[32:1] of AVS counter0 and the bit[0] is zero. You can set the initial value of the AVS counter0 by software. The initial value can be updated at anytime. You can also pause the counter by setting AVS_CNT0_PS to "1". The counter value will not increase when it is paused.

3.7.6.24 0x00C8 AVS Counter 1 Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: AVS_CNT1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>AVS_CNT1</p> <p>The higher 32 bits of AVS counter1.</p> <p>AVS counter1 is a 33-bit up counter. The initial value consists of two parts: this register forms the bit[32:1] of AVS counter0 and the bit[0] is zero.</p> <p>You can set the initial value of the AVS counter1 by software. The initial value can be updated at anytime. You can also pause the counter by setting AVS_CNT1_PS to "1". The counter value will not increase when it is paused.</p>

3.7.6.25 0x00CC AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset: 0x00CC			Register Name: AVS_CNT_DIV_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5DB	<p>AVS_CNT1_D</p> <p>N1, the divisor factor for AVS1.</p> <p>The clock for AVS1 is 24 MHz/N1.</p> <p>N1 = Bit[27:16] + 1.</p> <p>The valid value for N1 is from 1 to 0x7ff.</p> <p>There is an internal 12-bit counter maintained by the engine of the 33-bit AVS1. The 12-bit counter is used for counting the cycle number of the clock OSC24M. When the value of the 12-bit counter reaches N1, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again.</p> <p>You can change the value of N1 via the software at any time.</p>
15:12	/	/	/
11:0	R/W	0x5DB	<p>AVS_CNT0_D</p> <p>N0, the divisor factor for AVS0.</p> <p>The clock for AVS0 is 24MHz/N0.</p> <p>N0 = Bit[11:0] + 1.</p> <p>The valid value for N0 is from 1 to 0x7ff.</p> <p>There is an internal 12-bit counter maintained by the engine of the 33-bit AVS0. The 12-bit counter is used for counting the cycle number of the clock OSC24M. When the value of the 12-bit counter reaches N0, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again.</p> <p>You can change the value of N0 via the software at any time.</p>

3.8 High Speed Timer

3.8.1 Overview

The high speed timer (HSTimer) module implements more precise timing and counting functions.

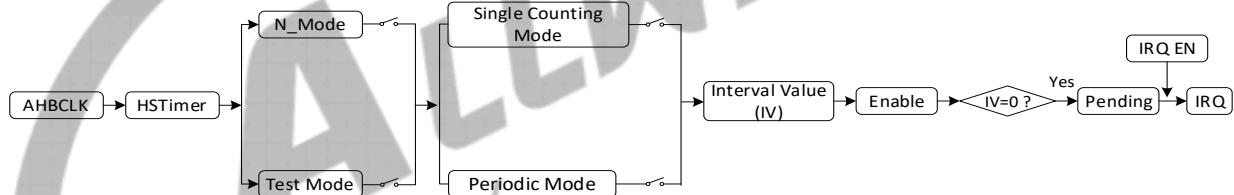
The HSTimer has the following features:

- Single clock source: AHB0
- Supports 5 prescale factors
- Configurable 56-bit down timer
- Supports 2 timing modes: periodic mode and one-shot mode
- Supports the test mode
- Generates an interrupt when the count is decreased to 0

3.8.2 Block Diagram

The following figure shows the block diagram of the HSTimer.

Figure 3-17 HSTimer Block Diagram



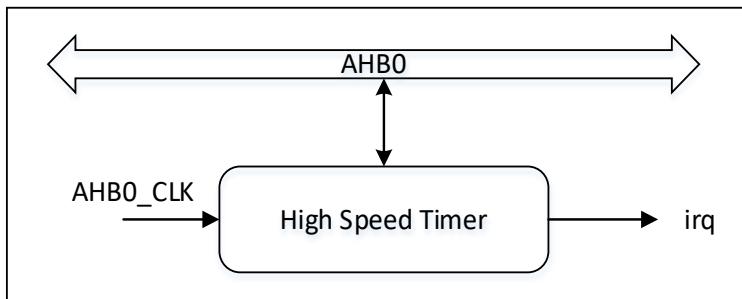
3.8.3 Functional Description

The HSTimers are 56-bit down counters. The counter value is decremented by 1 on each rising edge of the count clock. Each HSTimer has a prescaler that divides the working clock frequency of each working timer by 1, 2, 4, 8, or 16.

3.8.3.1 Typical Application

The following figure shows a typical application of HSTimer module.

Figure 3-18 Typical Application for HSTimer



The HSTimer module is mounted at AHBO, and can control the registers via AHBO. AHBO is the clock source of the HSTimer. When the count value reaches zero, the HSTimer generates an interrupt.

3.8.3.2 Count Modes

The HSTimer has two count modes: one-shot mode and periodic mode. You can configure the timing mode via the bit[7] of [HS_TMRn_CTRL_REG](#) (n = 0 or 1). The value 0 is for the period mode and value 1 is for the one-shot mode.

- One-shot Mode

When the count value of the HSTimer reaches 0, the HSTimer stops counting. The HSTimer starts to count again only when a new value is loaded.

- Periodic Mode

The HSTimer counts continuously. When the count value of the HSTimer reaches 0, the HSTimer reloads an initial value from [HS_TMRn_INTV_LO_REG](#) and [HS_TMRn_INTV_HI_REG](#) and then continues to count.

3.8.3.3 Operating Modes

The HSTimer has two operating modes: the normal mode and test mode. You can configure the operating mode via the bit[31] of [HS_TMRn_CTRL_REG](#). The value 0 is for the normal mode and value 1 is for the test mode.

- Normal Mode

In the normal mode, the HSTimer is used as a 56-bit down counter, which can finish one-shot counting and periodic counting. The interval value for the HSTimer consists of two parts: [HS_TMRn_INTV_LO_REG](#) forms the bit[31:0] and [HS_TMRn_INTV_HI_REG](#) forms the bit[55:32]. To read or write the interval value, [HS_TMRn_INTV_LO_REG](#) should be done before [HS_TMRn_INTV_HI_REG](#).

- Test Mode

In the test mode, the HSTimer is used as a 24-bit down counter. [HS_TMRn_INTV_LO_REG](#) must be set to 0x1, and [HS_TMRn_INTV_HI_REG](#) acts as the initial value for the HSTimer.

3.8.3.4 HSTimer Formula

The following formula describes the relationship among HSTimer parameters in the normal mode.

$$T_{HSTimer} = \frac{(HS_TMRn_INTV_HI_REG << 32 + HS_TMRn_INTV_LO_REG) - (HS_TMRn_CURNT_HI_REG << 32 + HS_TMRn_CURNT_LO_REG)}{AHB0CLK} \times HS_TMRn_CLK$$

Where,

The parameter n is either 0 or 1;

$T_{HSTimer}$ is the remaining time of the timer;

$HS_TMRn_INTV_HI_REG$ is bit[55:32] of the HSTimer interval value;

$HS_TMRn_INTV_LO_REG$ is bit[31:0] of the HSTimer interval value;

$HS_TMRn_CURNT_HI_REG$ is bit[55:32] of the HSTimer current value;

$HS_TMRn_CURNT_LO_REG$ is bit[31:0] of the HSTimer current value;

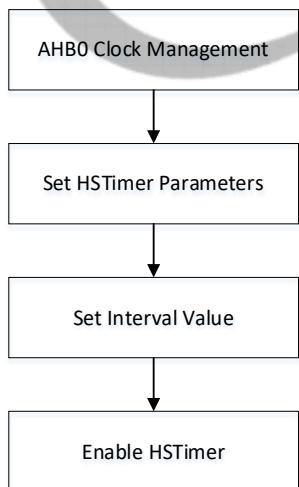
AHB0CLK is the frequency of AHB0 Clock (the HSTimer clock source);

HS_TMRn_CLK is the prescale ratio of the HSTimer clock.

3.8.3.5 Initializing the HSTimer

The following figure shows the process of HSTimer initialization.

Figure 3-19 HSTimer Initialization Process



1. AHBO clock management: Open the clock gate of AHBO and de-assert the soft reset of AHBO in CCU.

2. Configure the corresponding parameters of the HSTimer: clock source, prescaler factor, operating mode, and timing mode. There is no sequence requirement when writing the above parameters to [HS_TMRn_CTRL_REG](#).
3. Write the initial value: Write the lower 32 bits of the initial value to [HS_TMRn_INTV_LO_REG](#) first, and then the higher 24 bits to [HS_TMRn_INTV_HI_REG](#). Normally, write the bit[1] of [HS_TMRn_CTRL_REG](#) to load the initial value. If the HSTimer is in the timing stop stage, write 1 to the bit[1] and bit[0] of [HS_TMRn_CTRL_REG](#) at the same time to reload the initial value.
4. Enable HSTimer: Write the bit[0] of [HS_TMRn_CTRL_REG](#) to enable HSTimer to count.
5. Reading [HS_TMRn_CURNT_LO_REG](#) and [HS_TMRn_CURNT_HI_REG](#) can get current counting value.

3.8.3.6 Processing the HSTimer Interrupt

Follow the steps below to process the HSTimer interrupt:

1. Enable interrupt: Write the corresponding interrupt enable bit of [HS_TMR_IRQ_EN_REG](#), when the counting time of HSTimer reaches, the corresponding interrupt generates.
2. After entering the interrupt process, write [HS_TMR_IRQ_STAS_REG](#) to clear the interrupt pending.
3. Resume the interrupt and continue to execute the interrupted process.

3.8.3.7 Programming Guidelines

The following example shows how to make a 1 us delay with HSTimer0. The frequency of the AHB0 clock is 100 MHz, the operating mode is the normal mode, the timing mode is single counting mode, and the pre-scale is 2.

```
writel(0x32, HS_TMR0_INTV_LO);           //Set bit[31:0] of the interval value as 0x32.
writel(0x0, HS_TMR0_INTV_HI);           //Set bit[55:32] of the interval value as 0x0.
writel(0x90, HS_TMR0_CTRL);            //Set the operating mode as Normal Mode, the pre-scale as 2, and the timing mode as Single Counting Mode.
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL); //Set the reload bit.
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL); //Enable HSTimer0.
while(!(readl(HS_TMR_IRQ_STAS)&1));        //Wait for HSTimer0 to generate pending.
writel(1, HS_TMR_IRQ_STAS);              //Clear HSTimer0 pending.
```

3.8.4 Register List

Module Name	Base Address
HSTIMER	0x0300 8000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer IRQ Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0040	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0044	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0048	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x004C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0050	HS Timer 1 Current Value High Register

3.8.5 Register Description

3.8.5.1 0x0000 HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	HS_TMR1_INT_EN HSTimer1 Interrupt Enable 0: Disabled 1: Enabled
0	R/W	0x0	HS_TMR0_INT_EN HSTimer0 Interrupt Enable 0: Disabled 1: Enabled

3.8.5.2 0x0004 HS Timer IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W1C	0x0	HS_TMR1_IRQ_PEND HSTimer1 IRQ Pending The IRQ pending bit for HSTimer1. Write 1 to clear the pending status. 0: No effect 1: Pending, indicates that the initial value of the HSTimer is reached.

Offset: 0x0004			Register Name: HS_TMR IRQ STAS_REG
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	<p>HS_TMR0_IRQ_PEND HSTimer0 IRQ Pending</p> <p>The IRQ pending bit for HSTimer0. Write 1 to clear the pending status.</p> <p>0: No effect 1: Pending, indicates that the initial value of the HSTimer is reached.</p>

3.8.5.3 0x0020 HS Timer0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>HS_TMR0_TEST Select the operating mode for HSTimer0</p> <p>0: Normal mode 1: Test mode</p> <p>In the test mode, the HS_TMR0_INTV_LO_REG must be set to 0x1, and HS_TMR0_INTV_HI_REG acts as the initial value for HSTimer0.</p>
30:8	/	/	/
7	R/W	0x0	<p>HS_TMR0_MODE Select the timing mode for HSTimer0</p> <p>0: Periodic mode. When the count value is decreased to 0, the timer will restart another round of counting automatically. 1: One-shot mode. When the count value is decreased to 0, the timer will stop counting.</p>
6:4	R/W	0x0	<p>HS_TMR0_CLK Select the pre-scale for the HSTimer0 clock sources</p> <p>000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /</p>
3:2	/	/	/
1	R/W1S	0x0	<p>HS_TMR0_RELOAD HSTimer0 Reload</p> <p>0: No effect 1: Reload the interval value of the HSTimer0</p>

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	<p>HS_TMR0_EN HSTimer0 Enable 0: Stop/Pause 1: Start</p> <p>By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0.</p> <p>By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer.</p> <p>The timer supports updating the interval value in the pause state. To start from the updated interval value, set both the reload bit and enable bit to 1.</p> <p>Additionally, in the one-shot mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.</p>

3.8.5.4 0x0024 HS Timer0 Interval Value Low Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HS_TMR0_INTV_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO Bit[31:0] of the HSTimer0 interval value.

3.8.5.5 0x0028 HS Timer0 Interval Value High Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: HS_TMR0_INTV_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI Bit[55:32] of the HSTimer0 interval value.

 **NOTE**

HSTimer0 is a 56-bit counter. The interval value consists of two parts: HS_TMR0_INTV_VALUE_LO acts as the bit[31:0] and HS_TMR0_INTV_VALUE_HI acts as the bit[55:32]. To read or write the interval value, HS_TMR0_INTV_LO_REG should be done before HS_TMR0_INTV_HI_REG.

3.8.5.6 0x002C HS Timer0 Current Value Low Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO Bit[31:0] of the HSTimer0 current value.

3.8.5.7 0x0030 HS Timer0 Current Value High Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI Bit[55:32] of the HSTimer0 current value.

 **NOTE**

HSTimer0 is a 56-bit counter. The current value consists of two parts: HS_TMR0_CUR_VALUE_LO acts as the bit[31:0] and HS_TMR0_CUR_VALUE_HI acts as the bit[55:32]. To read or write the current value, HS_TMR0_CUR_VALUE_LO should be done before HS_TMR0_CUR_VALUE_HI.

3.8.5.8 0x0040 HS Timer1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS_TMR1_TEST Select the operating mode for HSTimer1. 0: Normal mode 1: Test mode In the test mode, the HS_TMR1_INTV_LO_REG must be set to 0x1, and HS_TMR1_INTV_HI_REG acts as the interval value for HSTimer1.
30:8	/	/	/

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	<p>HS_TMR1_MODE</p> <p>Select the timing mode for HSTimer1.</p> <p>0: Periodic mode. When the count value is decreased to 0, the timer will restart another round of counting automatically.</p> <p>1: One-shot mode. When the count value is decreased to 0, the timer will stop counting.</p>
6:4	R/W	0x0	<p>HS_TMR1_CLK</p> <p>Select the pre-scale of the HSTimer1 clock sources.</p> <p>000: /1</p> <p>001: /2</p> <p>010: /4</p> <p>011: /8</p> <p>100: /16</p> <p>101: /</p> <p>110: /</p> <p>111: /</p>
3:2	/	/	/
1	R/W1S	0x0	<p>HS_TMR1_RELOAD</p> <p>HSTimer1 Reload</p> <p>0: No effect</p> <p>1: Reload the HSTimer1 interval value.</p>
0	R/W	0x0	<p>HS_TMR1_EN</p> <p>HSTimer1 Enable</p> <p>0: Stop/Pause</p> <p>1: Start</p> <p>By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0.</p> <p>By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer.</p> <p>The timer supports updating the interval value in the pause state. To start from the updated interval value, set both the reload bit and enable bit to 1.</p> <p>Additionally, in the one-shot mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.</p>

3.8.5.9 0x0044 HS Timer1 Interval Value Low Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: HS_TMR1_INTV_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO Bit[31:0] of the HSTimer1 interval value

3.8.5.10 0x0048 HS Timer1 Interval Value High Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: HS_TMR1_INTV_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI Bit[55:32] of the HSTimer1 interval value



HSTimer1 is a 56-bit counter. The interval value consists of two parts: HS_TMR1_INTV_VALUE_LO acts as the bit[31:0] and HS_TMR1_INTV_VALUE_HI acts as the bit[55:32]. To read or write the interval value, HS_TMR1_INTV_LO_REG should be done before HS_TMR1_INTV_HI_REG.

3.8.5.11 0x004C HS Timer1 Current Value Low Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO Bit[31:0] of the HSTimer1 current value

3.8.5.12 0x0050 HS Timer1 Current Value Hi Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: HS_TMR1_CURNT_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI Bit[55:32] of the HSTimer1 current value

 NOTE

HSTimer1 is a 56-bit counter. The current value consists of two parts: HS_TMR1_CUR_VALUE_LO acts as the bit[31:0] and HS_TMR1_CUR_VALUE_HI acts as the bit[55:32]. To read or write the current value, HS_TMR1_CUR_VALUE_LO should be done before HS_TMR1_CUR_VALUE_HI.



3.9 Generic Interrupt Controller (GIC)

The following table describes the details of interrupt sources.

Table 3-11 Interrupt Sources

Interrupt Number	Interrupt Source	Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	CPUX_MBOX_CPUX	0x80	CPUX MSGBOX READ IRQ FOR CPUX
33	CPUX_MBOX_RISCV	0x84	CPUX MSGBOX WRITE IRQ FOR RISCV
34	UART0	0x88	
35	UART1	0x8C	

Interrupt Number	Interrupt Source	Vector	Description
36	UART2	0x90	
37	UART3	0x94	
38		0x98	
39		0x9C	
40		0xA0	
41	TWI0	0xA4	
42	TWI1	0xA8	
43	TWI2	0xAC	
44	TWI3	0xB0	
45	TWI4	0xB4	
46		0xB8	
47	SPI0	0xBC	
48	SPI1	0xC0	
49	SPI2	0xC4	
50	PWM	0xC8	
51	SPI_FLASH	0xCC	
52	WIEGAND	0xD0	
53	SPI3	0xD4	
54		0xD8	
55		0xDC	
56	DMIC	0xE0	
57	AUDIO_CODEC	0xE4	
58	I2S_PCM0	0xE8	
59	I2S_PCM1	0xEC	
60		0xF0	
61	USB_OTG	0xF4	
62	USB_EHCI	0xF8	
63	USB_OHCI	0xFC	
64		0x100	
65		0x104	
66		0x108	
67		0x10C	
68		0x110	
69		0x114	
70		0x118	
71		0x11C	
72	SMHC0	0x120	
73	SMHC1	0x124	
74	SMHC2	0x128	
75	MSI	0x12C	
76	SMC	0x130	

Interrupt Number	Interrupt Source	Vector	Description
77		0x134	
78	EMAC	0x138	
79		0x13C	
80	CCU_FERR	0x140	
81	AHB_HREADY_TIME_OUT	0x144	
82	DMA_CPUX_NS	0x148	
83	DMA_CPUX_S	0x14C	
84	CE_NS	0x150	
85	CE_S	0x154	
86	SPINLOCK	0x158	
87	HSTIMER0	0x15C	
88	HSTIMER1	0x160	
89	GPADC	0x164	
90	THS	0x168	
91	TIMER0	0x16C	
92	TIMER1	0x170	
93	TIMER2	0x174	
94	TIMER3	0x178	
95	WDG	0x17C	
96	IOMMU	0x180	
97	NPU	0x184	
98	VE	0x188	
99	GPIOA_NS	0x18C	
100	GPIOA_S	0x190	
101		0x194	
102		0x198	
103	GPIOC_NS	0x19C	
104	GPIOC_S	0x1A0	
105	GPIOD_NS	0x1A4	
106	GPIOD_S	0x1A8	
107	GPIOE_NS	0x1AC	
108	GPIOE_S	0x1B0	
109	GPIOF_NS	0x1B4	
110	GPIOF_S	0x1B8	
111	GPIOG_NS	0x1BC	
112	GPIOG_S	0x1C0	
113	GPIOH_NS	0x1C4	
114	GPIOH_S	0x1C8	
115	GPIOI_NS	0x1CC	
116	GPIOI_S	0x1D0	
117	DMAC_RISCV_NS	0x1D4	

Interrupt Number	Interrupt Source	Vector	Description
118	DMAC_RISCV_S	0x1D8	
119	DE	0x1DC	
120		0x1E0	
121	G2D	0x1E4	
122	LCD	0x1E8	
123		0x1EC	
124	DSI	0x1F0	
125		0x1F4	
126		0x1F8	
127	CSI_DMA0	0x1FC	
128	CSI_DMA1	0x200	
129	CSI_DMA2	0x204	
130	CSI_DMA3	0x208	
131		0x20C	
132	CSI_PARSER0	0x210	
133	CSI_PARSER1	0x214	
134	CSI_PARSER2	0x218	
135		0x21C	
136	CSI_CMB	0x220	
137	CSI_TDM	0x224	
138	CSI_TOP_PKT	0x228	
139		0x22C	
140	ISP0	0x230	
141	ISP1	0x234	
142	ISP2	0x238	
143	ISP3	0x23C	
144	VIPPO	0x240	
145	VIPP1	0x244	
146	VIPP2	0x248	
147	VIPP3	0x24C	
148		0x250	
149		0x254	
150		0x258	
151		0x25C	
152		0x260	
153		0x264	
154		0x268	
155		0x26C	
156		0x270	
157		0x274	
158		0x278	

Interrupt Number	Interrupt Source	Vector	Description
159		0x27C	
160	RISCV_MBOX_RISCV	0x280	RISCV MSGBOX READ IRQ FOR RISCV
161	RISCV_MBOX_CPUX	0x284	RISCV MSGBOX WRITE IRQ FOR CPUX
162	RISCV_WDG	0x288	
163	RISCV_TIMER0	0x28C	
164	RISCV_TIMER1	0x290	
165	RISCV_TIMER2	0x294	
166	RISCV_TIMER3	0x298	
167		0x29C	
168	NMI	0x2A0	
169	PPU	0x2A4	
170	ALARM	0x2A8	
171	AHBS_HREADY_TIME_OUT	0x2AC	CPUS AHB READY TIME OUT IRQ
172	PMC	0x2B0	
173	GIC_C0	0x2B4	Debug
174	TWD	0x2B8	
175		0x2BC	
176		0x2C0	
177		0x2C4	
178		0x2C8	
179		0x2CC	
180		0x2D0	
181		0x2D4	
182		0x2D8	
183		0x2DC	
184		0x2E0	
185		0x2E4	
186		0x2EC	
187		0x2F0	
188		0x2F4	
189		0x2F8	
190		0x2FC	
191		0x300	
CPUX Related			
192	C0_CTL0	0x304	C0_CTL0 interrupt
193	C0_CTL1	0x308	C0_CTL1 interrupt
194		0x30C	
195		0x310	
196	C0_COMMTX0	0x314	C0_COMMTX0 interrupt
197	C0_COMMTX1	0x318	C0_COMMTX1 interrupt

Interrupt Number	Interrupt Source	Vector	Description
198		0x31C	
199		0x320	
200	C0_COMMRX0	0x324	C0_COMMRX0 interrupt
201	C0_COMMRX1	0x328	C0_COMMRX1 interrupt
202		0x32C	
203		0x330	
204	C0_PMU0	0x334	C0_PMU0 interrupt
205	C0_PMU1	0x338	C0_PMU1 interrupt
206		0x33C	
207		0x340	
208	C0_AXI_ERROR	0x344	C0_AXI_ERROR interrupt
209		0x348	
210	AXI_WR_IRQ	0x34C	
211	AXI_RD_IRQ	0x350	
212	DBGPWRUPREQ_out[0]	0x354	
213	DBGPWRUPREQ_out[1]	0x358	
214		0x35C	
215		0x360	
216		0x364	
217		0x368	
218		0x36C	
219		0x370	
220		0x374	
221		0x378	
222		0x37C	
223		0x380	

3.10 Direct Memory Access Controller (DMAC)

3.10.1 Overview

The direct memory access (DMA) is a method of transferring data between peripherals and memories (including the SRAM and DRAM) without using the CPU. It is an efficient way to offload data transfer duties from the CPU. Without DMA, the CPU has to control all the data transfers. While with DMA, the DMAC directly transfers data between a peripheral and a memory, between peripherals, or between memories.

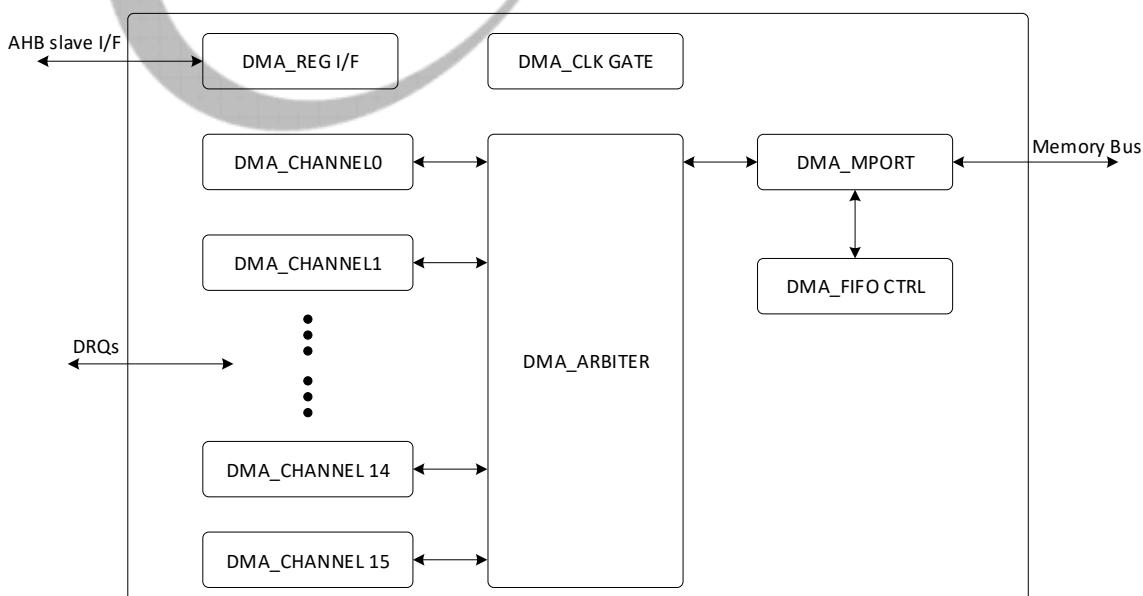
The DMAC has the following features:

- Up to 16 DMA channels
- Provides 32 peripheral DMA requests for data reading and 32 peripheral DMA requests for data writing
- Supports transferring data with a linked list
- Supports programmable 8-bit, 16-bit, 32-bit, and 64-bit data width
- Supports programmable DMA burst length
- DRQ response includes the waiting mode and handshake mode
- DMA channel supports pause function
- Memory devices support non-aligned transform

3.10.2 Block Diagram

The following figure shows a block diagram of DMAC.

Figure 3-20 DMAC Block Diagram



DMAC contains the following sub-blocks:

Table 3-12 DMAC Sub-blocks

Sub-block	Description
DMA_ARBITER	Arbitrates the DMA read/write requests from all channels, and converts the requests to the read/write requests of ports.
DMA_CHANNELS	DMA transfer engine. Each channel is independent. When the DMA requests from multiple peripherals are valid simultaneously, the channel with the highest priority starts data transfer first. The system uses the polling mechanism to decide the priorities of DMA channels. When DMA_ARBITER is idle, channel 0 has the highest priority, whereas channel 15 has the lowest priority. When DMA_ARBITER is busy processing the request from channel n, channel (n+1) has the highest priority. For n = 15, the channel (n + 1) should be channel 0.
DRQs	DMA requests. Peripherals use the DMA request signals to request a data transfer.
DMA_MPORT	Receives the read/write requests from DMA_ARBITER, and converts the requests to the corresponding MBUS access requests. It is mainly used for accessing the DRAM.
DMA_HPORT	The port for accessing the AHB Master. It is mainly used for accessing the SRAM and IO devices.
DMA_FIFO CTRL	Internal FIFO cell control module.
DMA_REG Interface	DMA_REG is the common register module that is mainly used to resolve AHB demands.
DMA_CLKGATE	The control module for hardware auto clock gating.

The DMAC integrates 16 independent DMA channels and each channel has an independent FIFO controller. When the DMA channel starts, the DMAC gets a DMA descriptor from the DMA_DESC_ADDR_REG and uses it as the configuration information for the data transfer of the current DMA package. Then the DMAC can transfer data between the specified devices. After transferring a DMA package, the DMAC judges if the current channel transfer is finished via the linked address in the descriptor. If the linked address shows all the packages are transferred, the DMAC will end the chain transmission and close the channel.

3.10.3 Functional Description

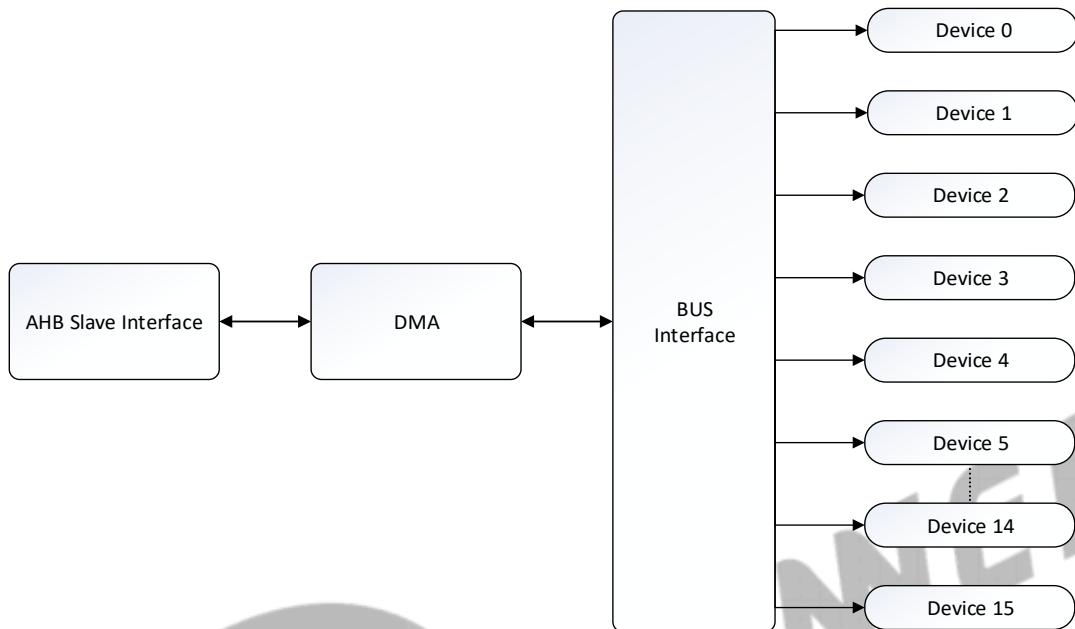
3.10.3.1 Clock

The DMAC is on MBUS. The clock of MBUS influences the transfer efficiency of the DMAC.

3.10.3.2 Typical Application

The following figure shows a typical application of the DMAC.

Figure 3-21 DMAC Typical Application Diagram



3.10.3.3 DRQ Port of Peripherals

The following table shows the source DRQ types and destination DRQ types of different ports.

Table 3-13 DMA DRQ Type

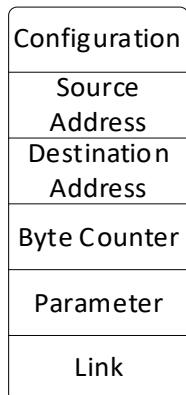
Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2		port2	
port3	I2S0_RX	port3	I2S0_TX
port4	I2S1_RX	port4	I2S1_TX
port5		port5	
port6		port6	
port7	AUDIO_CODEC	port7	AUDIO_CODEC
port8	DMIC	port8	
port9		port9	
port10		port10	
port11		port11	
port12	GPADC	Port12	
port13		port13	
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX

Source DRQ Type		Destination DRQ Type	
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX
port18		port18	
port19		port19	
port20		Port20	
port21		port21	
port22	SPI0-RX	port22	SPI0-TX
port23	SPI1-RX	port23	SPI1-TX
port24	SPI2-RX	port24	SPI2-TX
port25	SPI3-RX	port25	SPI3-TX
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	OTGO_EP1	Port30	OTGO_EP1
Port31	OTGO_EP2	Port31	OTGO_EP2
Port32	OTGO_EP3	Port32	OTGO_EP3
Port33	OTGO_EP4	Port33	OTGO_EP4
Port34	OTGO_EP5	Port34	OTGO_EP5
Port35		Port35	
Port36		Port36	
Port37		Port37	
Port38		Port38	
Port39		Port39	
Port40		Port40	
Port41		Port41	
Port42		Port42	
Port43	TWI0	Port43	TWI0
Port44	TWI1	Port44	TWI1
Port45	TWI2	Port45	TWI2
Port46	TWI3	Port46	TWI3
Port47	TWI4	Port47	TWI4
Port48		Port48	
Port49		Port49	
Port50		Port50	
Port51		Port51	
Port52		Port52	
Port53		Port53	

3.10.3.4 DMA Descriptor

The DMAC descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words: Configuration, Source Address, Destination Address, Byte Counter, Parameter, and Link. The following figure shows the structure of the DMA descriptor.

Figure 3-22 DMA Descriptor



1. **Configuration:** Configure the following information by DMA_CFG_REG.
 - DRQ type: DRQ type of the source and destination devices.
 - Address counting mode: For both the source and destination devices, there are two address counting modes: the IO mode and linear mode. The IO mode is for IO devices whose address is fixed during the data transfer and the linear mode is for the memory whose address is increasing during the data transfer.
 - Transferred block length: The amount of data that non-memory peripherals can transfer in a valid DRQ. The block length supports 1 bit, 4 bits, 8 bits, and 16 bits.
 - Transferred data width: The data width of operating the non-memory peripherals. The data width supports 8 bits, 16 bits, 32 bits, and 64 bits.



NOTE

The configuration supports BMODE mode. The BMODE is used in the following scenario: the source is an IO device, and the destination is a memory device. Setting the BMODE mode can limit the amount of block data transferred in DMA block transmission to the amount of data transferred when the DRQ threshold of the source IO device is 1. For example,

2. **Source Address:** Configure the address of the source device.
3. **Destination Address:** Configure the address of the destination device.

DMA reads data from the source address and then writes data to the destination address.

Both the DMA source and destination addresses have 34 bits. In the descriptor, because there are only 32 bits in the **Source/Destination Address** field, another 2 bits are stored in the **Parameter** field.

The following table shows the details of the related fields in the descriptor.

Table 3-14 Source/Destination Address Distribution

Descriptor Group	Bit	Description
Source Address	31:0	DMA transfers the lower 32 bits of the 34-bit source address
Destination Address	31:0	DMA transfers the lower 32 bits of the 34-bit destination address
Parameter	31:20	Reserved
	19:18	DMA transfers the higher 2 bits of the 34-bit destination address
	17:16	DMA transfers the high 2 bits of the 34-bit source address
	15:8	Reserved
	7:0	Wait Clock Cycles Set the waiting time in DRQ mode
Link	31:2	The address of the next group descriptor, the lower 30 bits of the word address
	1:0	The address of the next group descriptor, the higher 2 bits of the word address

From the above table, you can get:

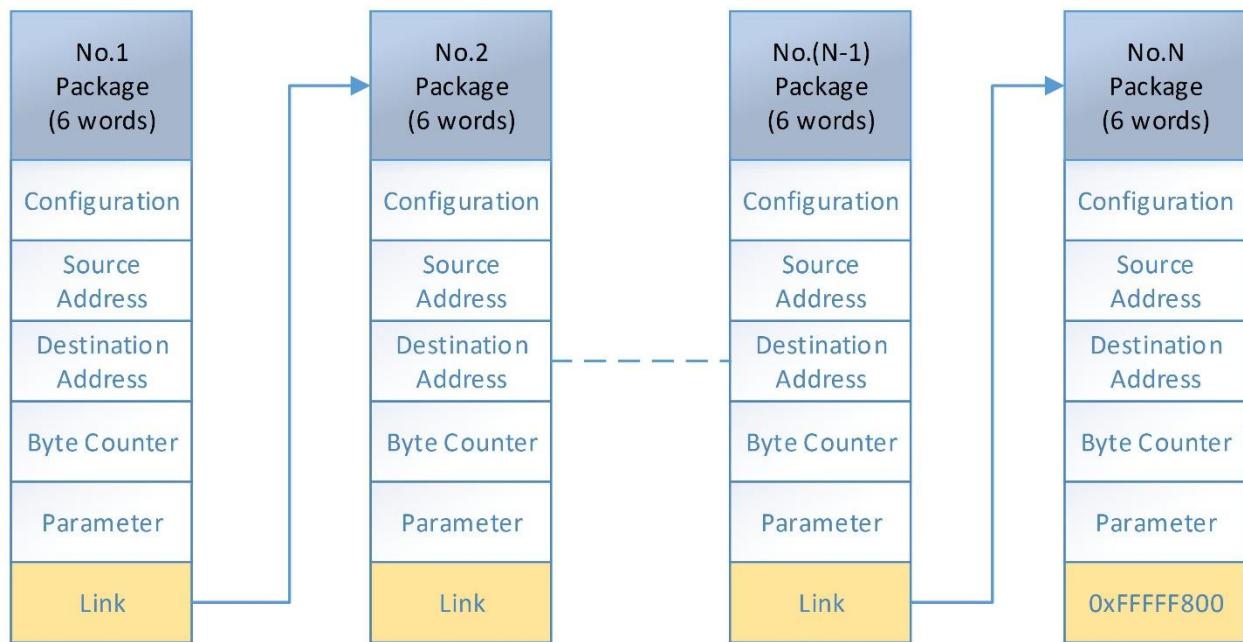
Real DMA source address (in byte mode) = {Parameter [17:16], Source Address [31:0]};

Real DMA destination address (in byte mode) = {Parameter [19:18], Destination Address [31:0]};

Real link address (in byte mode) = {Link[1:0], Link[31:2], 2'b00}.

4. **Byte counter:** Configure the data amount of a package. The maximum value is $(2^{25}-1)$ bytes. If the data amount of the package reaches the maximum value, DMA will stop the current transfer even if DRQ is valid.
5. **Parameter:** Configure the interval between the data block. The parameter is valid for the non-memory peripherals. When DMA detects the high DRQ, it transfers the data block and ignores the status changes of the DRQ until the data transfer finishes. After that, DMA waits for certain clock cycles (WAIT_CYC) and executes the next DRQ detection.
6. **Link:** If the link value is 0xFFFF800, the current package is at the end of the linked list. The DMAC will stop the data transfer after transferring the package; otherwise, the value of the link is considered as the descriptor address of the next package.

Figure 3-23 DMA Chain Transfer



3.10.3.5 Interrupts

There are three kinds of DMA interrupts: the half package interrupt, package end interrupt, and queue end interrupt.

Half package interrupt: When enabled, the DMAC sends out a half package interrupt after transferring half of a package.

Package end interrupt: When enabled, the DMAC sends out a package end interrupt after transferring a complete package.

Queue end interrupt: When enabled, the DMAC sends out a queue end interrupt after transferring a complete queue.

Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts are generated very closely, the later interrupt may override the former one. That is, from the perspective of the CPU, the DMAC has only a system interrupt source.



NOTE

The DMAC has 16 channels and 2 groups of interrupts. The channel [7:0] corresponds to one group of interrupt, the channel [15:8] corresponds to another group of interrupt.

3.10.3.6 Clock Gating

The DMA_CLK_GATE module is a hardware module for controlling the clock gating automatically. It provides clock sources for sub-modules in DMAC and the module local circuits.

The DMA_CLK_GATE module consists of two parts: the channel clock gate and the common clock gate.

Channel clock gate: Controls the DMA clock of the DMA channels. When the system accesses the register of the current DMA channel and the DMA channel is enabled, the channel clock gate automatically opens the DMA clock. With a 16-HCLK-cycle delay after the system finishes accessing the register or the DMA data transfer is completed, the channel clock gate automatically closes the DMA clock. Also, the clock for the related circuits, such as for the channel control and FIFO control modules, will be closed.

Common clock gate: Controls the clocks of the DMA common circuits. The common circuits include the common circuit of the FIFO control module, MPORT module, and MBUS. When all the DMA channels are enabled, the common clock gate automatically closes the clocks for the above circuits.

The DMA clock gating can support all the functions stated above or not by software.

3.10.3.7 Transfer Mode

DMAC supports two data transfer modes: the waiting mode and the handshake mode.

Waiting Mode

- When DMAC detects a valid external request signal, it starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ pulls low automatically.
- The internal DRQ holds low for certain clock cycles (WAIT_CYC), and then DMAC restarts to detect the external requests. If the external request signal is valid, the next transfer starts.

Handshake Mode

- When DMAC detects a valid external request signal, it starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ will be pulled down automatically. For the last data transfer of the block, the DMAC sends a DMA Last signal with the DMA commands to the peripheral device. The DMA Last signal will be packed as a part of the DMA commands and transmitted on the bus. It is used to inform the peripheral device that it is the end of the data transfer for the current DRQ.
- When the peripheral device receives the DMA Last signal, it can judge that the data transfer for the current DRQ is finished. To continue the data transfer, it sends a DMA Active signal to the DMAC.

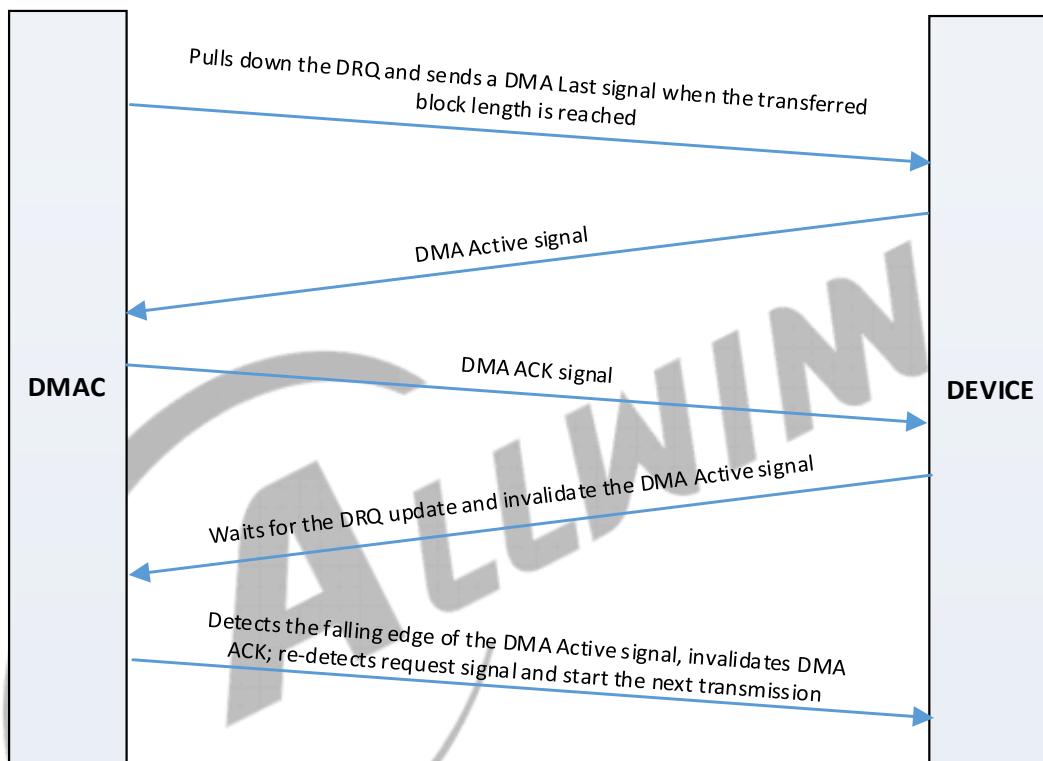


One DMA Active signal will be converted to one DRQ signal in the DMA module. To generate multiple DRQs, the peripheral device needs to send out multiple DMA Active signals via the bus protocol.

- When the DMAC received the DMA Active signal, it sends back a DMA ACK signal to the peripheral device.
- When the peripheral device receives the DMA ACK signal, it waits for all the operations on the local device completed, and both the FIFO and DRQ status refreshed. Then it invalidates the DMA Active signal.
- When the DMAC detects the falling edge of the DMA Active signal, it invalidates the corresponding DMA ACK signal, and restarts to detect the external request signals. If a valid request signal is detected, the next data transfer starts.

The following figure shows the workflow of the handshake mode.

Figure 3-24 Workflow of the DMAC Handshake Mode



3.10.3.8 Address Auto-Alignment

For the non-IO devices whose start address is not 32-byte-aligned, the DMAC will adjust the address to 32-byte-aligned through the burst transfer within 32 bytes. Adjusting address to 32-byte-aligned improves the DRAM access efficiency.

The following example shows how the DMAC adjusts the address: when the peripheral device of a DMA channel is a non-IO device whose start address is 0x86 (not 32-byte-aligned), the DMAC firstly uses a 26-byte burst transfer to align the address to 0xA0 (32-byte-aligned), and then transfers data by 64-byte burst (the maximum transfer amount that MBUS allows).

The IO devices do not support address alignment, so the bit width of IO devices must match the address offset; otherwise, the DMAC will ignore the inconsistency and directly transmit data of the corresponding bit width to the address.

The address of the DMA descriptor does not support the address auto-alignment. Make sure the address is word-aligned; otherwise the DMAC cannot identify the descriptor.

3.10.3.9 DMAC Clock Control

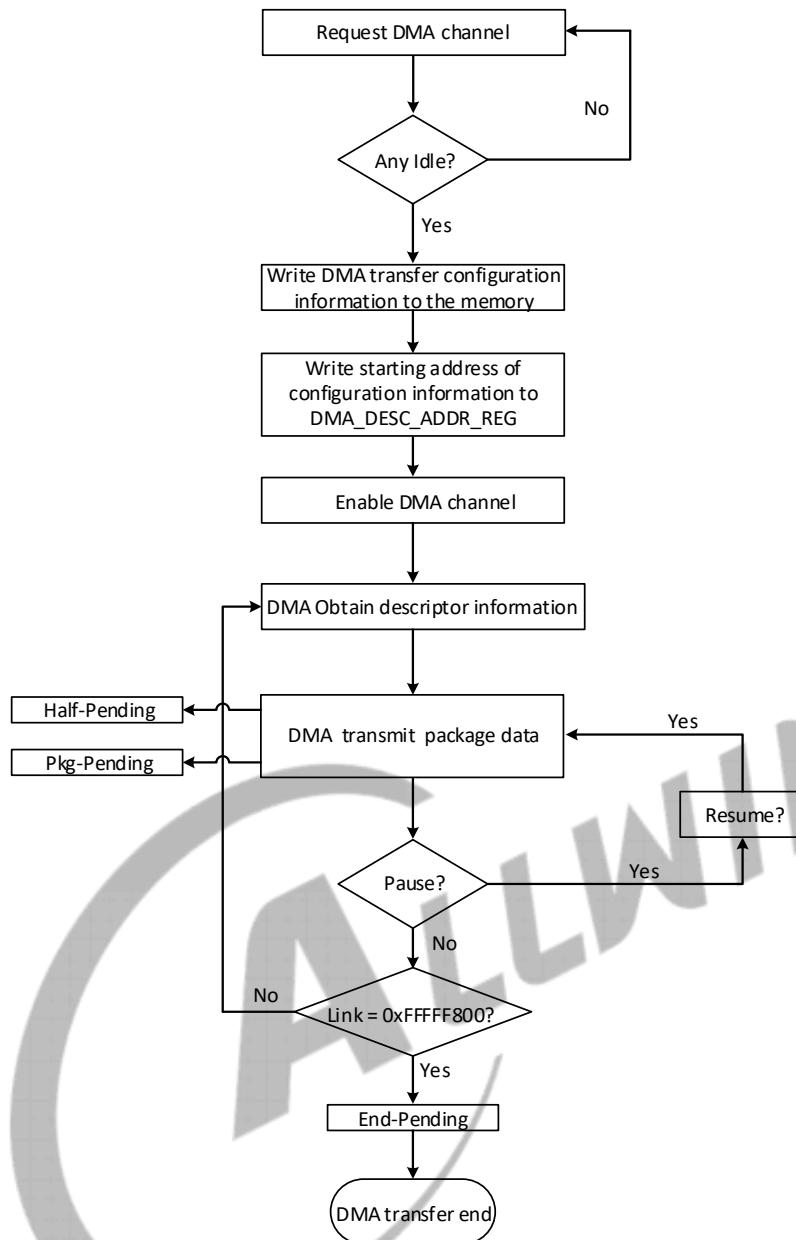
- The DMAC clock is synchronous with the AHBO clock. Make sure that the DMAC gating bit of AHBO clock is enabled before accessing the DMAC register.
- The reset input signal of the DMAC is asynchronous with AHBO and is low valid by default. Make sure that the reset signal of the DMAC is de-asserted before accessing the DMA register.
- To avoid the indefinite state within registers, de-assert the reset signal first, and then open the gating bit of AHBO.
- The DMAC supports Clock Auto Gating function to reduce power consumption, the system will automatically disable the DMAC clock in the DMAC idle state. Clock Auto Gating is enabled by default.

3.10.4 Programming Guidelines

3.10.4.1 Using DMAC Transfer Process

The DMAC transfer process is as follows.

1. Request DMA channel, and check if the DMA channel is idle by checking if it is enabled. A disabled channel indicates it is idle, while an enabled channel indicates it is busy.
2. Write the descriptor with 6 words into the memory. The descriptor must be word-aligned. For more details, refer to section 3.10.3.4 DMA Descriptor
3. Write the start address of the descriptor to [DMA_DESC_ADDR_REGN](#).
4. Enable the DMA channel, and write the corresponding channel to [DMAC_EN_REGN](#).
5. The DMA obtains the descriptor information.
6. Start to transmit a package. When half of the package is completed, the DMA sends a Half Package Transfer Interrupt; when a total package is completed, the DMA sends a Package End Transfer Interrupt. These interrupt status can be read by [DMAC_IRQ_PEND_REGO](#).
7. Set [DMAC_PAU_REGN](#) to pause or resume the data transfer.
8. After completing a total package transfer, the DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; otherwise, the next package starts to transmit. When the transfer ends, the DMA sends a Queue End Transfer Interrupt.
9. Disable the DMA channel.

Figure 3-25 DMAC Transfer Process

3.10.4.2 Processing DMAC Interrupt

Follow the steps below to process the DMAC interrupt:

1. Enable interrupt: write the corresponding interrupt enable bit of [DMA IRQ EN REG0](#). The system generates an interrupt when the corresponding condition is satisfied.
2. After entering the interrupt process, write [DMA IRQ PEND REG0](#) to clear the interrupt pending and execute the interrupt process.
3. Resume the interrupt and continue to execute the interrupted process.

3.10.4.3 Configuring DMAC

Refer to the guidelines below to configure the DMAC:

- Make sure the transfer bit width of IO devices is consistent with the offset of the start address.
- The MBUS protocol does not support the read operation of non-integer words. For the devices whose bit width is not word-aligned, after receiving the read command, they should resolve the read command according to their FIFO bit width instead of the command bit width, and ignore the redundant data caused by the inconsistency of the bit width.
- When the DMA transfer is paused, DRQ is invalid. Because there is a certain time delay between DMA transfer commands, the DMAC will not stop data transfer until the DMAC finishes processing the current command and the commands in Arbiter (at most 32-byte data).

DMAC application example:

```
writel(0x00000000, mem_address + 0x00); //Sets configurations. The mem_address must be word-aligned.  
writel(0x00001000, mem_address + 0x04); // Sets the start address for the source device.  
writel(0x20000000, mem_address + 0x08); //Sets the start address for the destination device.  
writel(0x00000020, mem_address + 0x0C); // Sets the data package size.  
writel(0x00000000, mem_address + 0x10); //Sets the parameters.  
writel(0xFFFFF800, mem_address + 0x14); //Sets the start address for the next descriptor.  
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Sets the start address for the DMA channel0 descriptor.  
do{  
    If(mem_address == readl(0x01C02000 + 0x100 + 0x08));  
    break;  
}while(1); //Make sure that the writing operation is valid.  
writel(0x00000001, 0x01C02000 + 0x100 + 0x00); // Enables DMA channel0 transfer.
```

The DMAC supports increasing data package in the transfer, pay attention to the following points:

- The 0xFFFFF800 value of [DMA_FDESC_ADDR_REG](#) indicates that the DMA channel has got back the descriptor of the last package. The DMA channel will automatically stop the data transfer after transferring the current package.
- To add a package during the data transfer, check if the DMA channel has got back the descriptor of the last package. If yes, do not add any package in the current queue. Request another DMA channel with a new DRQ to transfer the package. Otherwise, add the package by modifying the [DMA_FDESC_ADDR_REG](#) of the last package from 0xFFFFF800 to the start address of the to-be-added package.

- To ensure that the modification is valid, read the value of [DMA_FDESC_ADDR_REG](#) after the modification. The value 0xFFFFF800 indicates the modification failure and other values indicate you have successfully added packages to the queue.
- Another problem is, the system needs some time to process the modification, during which the DMA channel may get back the descriptor of the last package. You can read the value of [DMA_CUR_SRC_REG](#) and [DMA_CUR_DEST_REG](#) and check whether the increasing memory address is in accordance with the information of the added package. If yes, the package is added successfully; otherwise, the modification failed.
- To ensure a higher rate of success, it is recommended to add the package before the half package interrupt of the penultimate package.

3.10.5 Register List

Module Name	Base Address	Comments
DMA	0x0300 2000	DMA configuration register

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register 1
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Status Register 0
DMA_IRQ_PEND_REG1	0x0014	DMA IRQ Pending Status Register 1
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+0x0000+N*0x0040 (N=0~15)	DMA Channel Enable Register
DMA_PAU_REG	0x0100+0x0004+N*0x0040 (N=0~15)	DMA Channel Pause Register
DMA_DESC_ADDR_REG	0x0100+0x0008+N*0x0040 (N=0~15)	DMA Channel Descriptor Address Register
DMA_CFG_REG	0x0100+0x000C+N*0x0040 (N=0~15)	DMA Channel Configuration Register
DMA_CUR_SRC_REG	0x0100+0x0010+N*0x0040 (N=0~15)	DMA Channel Current Source Address Register
DMA_CUR_DEST_REG	0x0100+0x0014+N*0x0040 (N=0~15)	DMA Channel Current Destination Address Register
DMA_BCNT_LEFT_REG	0x0100+0x0018+N*0x0040 (N=0~15)	DMA Channel Byte Counter Left Register
DMA_PARA_REG	0x0100+0x001C+N*0x0040 (N=0~15)	DMA Channel Parameter Register
DMA_MODE_REG	0x0100+0x0028+N*0x0040 (N=0~15)	DMA Mode Register

Register Name	Offset	Description
DMA_FDESC_ADDR_REG	0x0100+0x002C+N*0x0040 (N=0~15)	DMA Former Descriptor Address Register
DMA_PKG_NUM_REG	0x0100+0x0030+N*0x0040 (N=0~15)	DMA Package Number Register

3.10.6 Register Description

3.10.6.1 0x0000 DMAC IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.6.2 0x0004 DMAC IRQ Enable Register1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
31	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	DMA12_QUEUE_IRQ_EN DMA 12 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA9 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA9 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA9 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.6.3 0x0010 DMAC IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

3.10.6.4 0x0014 DMAC IRQ Pending Status Register 1 (Default Value: 0x0000_0000)

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND. DMA 15 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_PEND DMA 15 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_PEND DMA 14 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
21	R/W1C	0x0	DMA13_PKG_IRQ_PEND DMA 13 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND. DMA 13 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_PEND DMA 12 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_PEND DMA 10 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_PEND DMA 9 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA8 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	DMA8_PKG_IRQ_PEND DMA 8 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA8 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

3.10.6.5 0x0028 DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable



When the DMA Controller is initialized, the bit[2] should be set up.

3.10.6.6 0x0030 DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0	MBUS_FIFO_STATUS MBUS FIFO Status 0: Empty 1: Not Empty
30:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy

Offset:0x0030			Register Name: DMA_STA_REG
Bit	Read/Write	Default/Hex	Description
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle 1: Busy

3.10.6.7 0x0100 + N*0x0040 DMAC Channel Enable Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0000+N*0x0040 (N=0~15)			Register Name: DMA_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Offset:0x0100+0x0000+N*0x0040 (N=0~15)			Register Name: DMA_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

3.10.6.8 0x0104 + N*0x0040 DMAC Channel Pause Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0004+N*0x0040 (N=0~15)			Register Name: DMA_PAU_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

3.10.6.9 0x0108 + N*0x0040 DMAC Channel Descriptor Address Register N (Default Value: 0x0000_0000)

Offset: 0x0100+0x0008+N*0x0040 (N = 0 to 15)			Register Name: DMAC_DESC_ADDR_REGN
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	DMA_DESC_ADDR Lower 30 bits of DMA channel descriptor address The descriptor address must be word-aligned.
1:0	R/W	0x0	DMA_DESC_HIGH_ADDR Higher 2 bits of DMA channel descriptor high address The real address is as follows. DMA Channel Descriptor Address = {bit[1:0], bit[31:2], 2'b00}

3.10.6.10 0x010C + N*0x0040 DMAC Channel Configuration Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x000C+N*0x0040 (N=0~15)			Register Name: DMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R	0x0	BMODE_SEL Mode select 0: Normal Mode 1: BMODE

Offset:0x0100+0x000C+N*0x0040 (N=0~15)			Register Name: DMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
29:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.10.6.11 0x0110 + N*0x0040 DMAC Channel Current Source Address Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0010+N*0x0040 (N=0~15)			Register Name: DMA_CUR_SRC_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

3.10.6.12 0x0114 + N*0x0040 DMA Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+0x0014+N*0x0040 (N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

3.10.6.13 0x0118 + N*0x0040 DMAC Channel Byte Counter Left Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0018+N*0x0040 (N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

3.10.6.14 0x011C + N*0x0040 DMAC Channel Parameter Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x001C+N*0x0040 (N=0~15)			Register Name: DMA PARA_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

3.10.6.15 0x0128 + N*0x0040 DMAC Mode Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0028+N*0x0040 (N=0~15)			Register Name: DMA_MODE_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/

Offset:0x0100+0x0028+N*0x0040 (N=0~15)			Register Name: DMA_MODE_REG
Bit	R/W	Default/Hex	Description
3	R/W	0x0	DMA_DST_MODE. Destination communication Mode Select 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. Source communication Mode Select 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

3.10.6.16 0x012C + N*0x0040 DMAC Former Descriptor Address Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x002C+N*0x0040 (N=0~15)			Register Name: DMA_FDESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to storing the former value of DMA Channel Descriptor Address Register.

3.10.6.17 0x0130 + N*0x0040 DMAC Package Number Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0030+N*0x0040 (N=0~15)			Register Name: DMA_PKG_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

3.11 Thermal Sensor Controller (THS)

3.11.1 Overview

The thermal sensors are common elements in wide range of modern system on chips (SoCs) platform. The thermal sensors are used to constantly monitor the temperature on the chip.

The thermal sensor controller (THS) embeds three thermal sensors located in the CPU. When the temperature reaches a certain thermal threshold, the thermal sensor can generate interrupts to the software to lower the temperature via the dynamic voltage and frequency scaling (DVFS) technology.

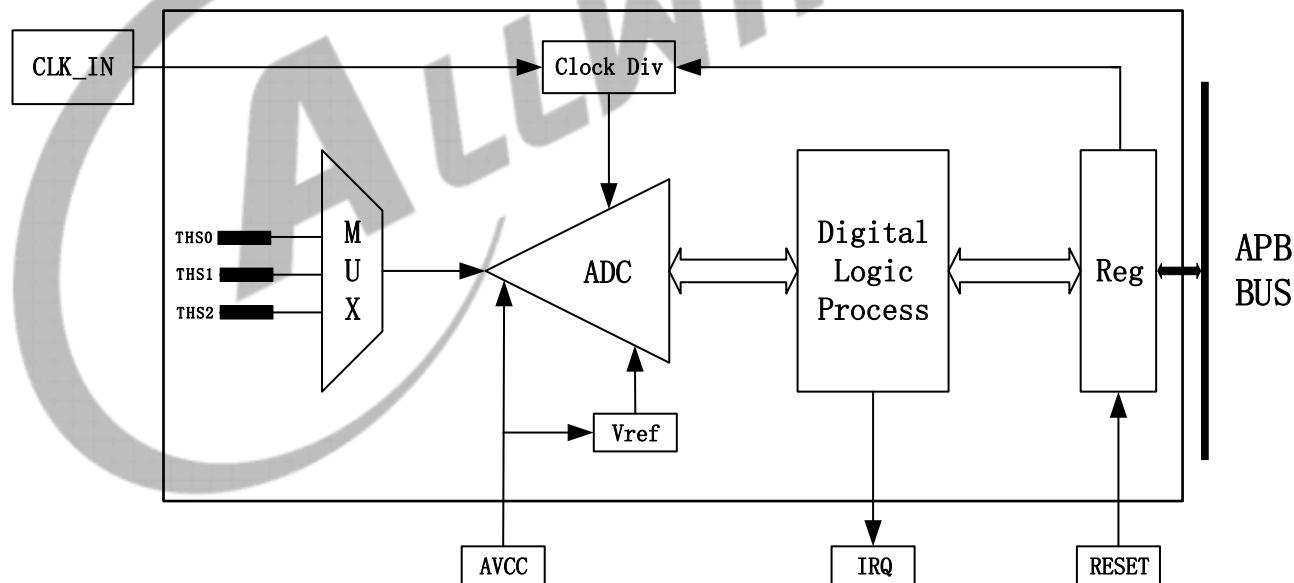
The THS has the following features:

- Temperature accuracy: $\pm 3^{\circ}\text{C}$ from 0°C to $+100^{\circ}\text{C}$, $\pm 5^{\circ}\text{C}$ from -25°C to $+125^{\circ}\text{C}$
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.11.2 Block Diagram

The following figure shows a block diagram of the THS.

Figure 3-26 THS Block Diagram



3.11.3 Functional Description

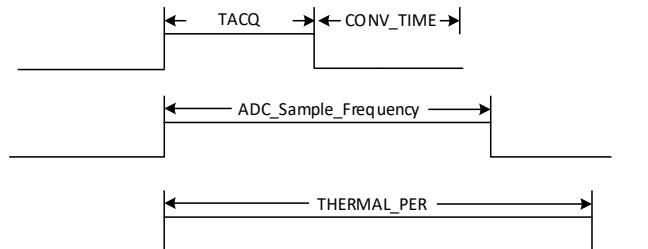
3.11.3.1 Clock Source

The THS gets one clock source: OSC24M. For details about clock configurations, refer to section 3.4 Clock Controller Unit (CCU).

3.11.3.2 Timing Requirements

The following figure shows the timing requirements for the THS.

Figure 3-27 Thermal Sensor Timing Requirement



CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = $1/24\text{ MHz} \times 14\text{ Cycles} = 0.583\text{ us}$

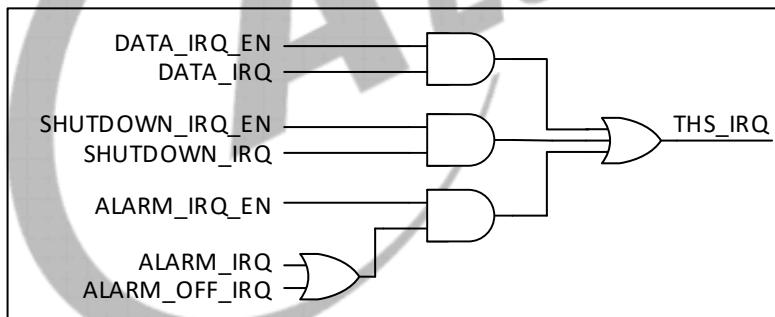
TACQ > $1/24\text{ MHz} \times 24\text{ Cycles}$

THERMAL_PER > ADC_Sample_Frequency > TACQ + CONV_TIME

3.11.3.3 Interrupts

The THS has four interrupt sources: DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ, and ALARM_OFF_IRQ. The following figure shows thermal sensor interrupt sources.

Figure 3-28 Thermal Sensor Controller Interrupt Source



DATA_IRQ: The interrupt is generated when the measured sensor_data is updated.

SHUTDOWN_IRQ: The interrupt is generated when the temperature is higher than the shutdown threshold.

ALARM_IRQ: The interrupt is generated when the temperature is higher than the Alarm_Threshold.

ALARM_OFF_IRQ: The interrupt is generated when the temperature drops to lower than the Alarm_Off_Threshold. It is triggered at the fall edge.

3.11.3.4 THS Temperature Conversion Formula

$$\text{Sensor_data} > 1869: T = (\text{sensor_data} - 2796)/(-14.26)$$

$$\text{Sensor_data} \leq 1869: T = (\text{sensor_data} - 2822)/(-14.60)$$

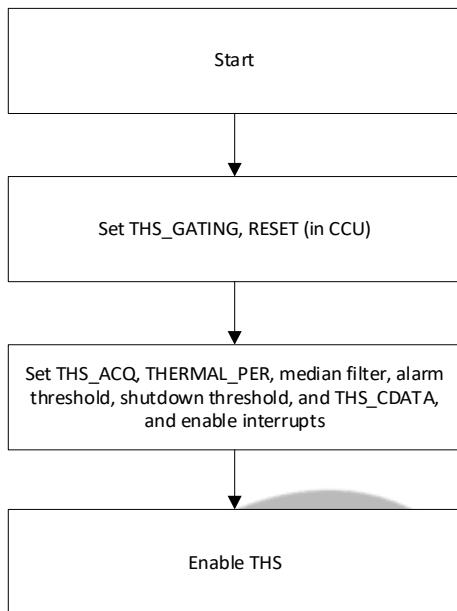
Unit of T: Celsius degree (°C).

The sensor_data is read from the sensor data register.

3.11.4 Programming Guidelines

The initial process of the THS is as follows.

Figure 3-29 THS Initial Process



In the final test (FT) stage, the THS is calibrated through the ambient temperature, and the calibration value is written in the SID module. The following table shows the THS information in the SID.

Table 3-15 THS Information in the SID

Base Address: 0x14	Register Name: THS
Bit	Description
31:28	The highest 4 bits of the Audio_bias calibration value.
27:16	The calibration value of the T-sensor.
15:12	The lowest 4 bits of the Audio_bias calibration value.
11:0	The value of the ambient temperature.

Before enabling THS, read eFuse value and write the value to [THSn_CDATA](#) (n = 0,1 or 2).

Query Mode

1. Write 0x1 to the bit[16] of [THS_BGR_REG](#) to dessert the reset.
2. Write 0x1 to the bit[0] of [THS_BGR_REG](#) to open the THS clock.
3. Write 0x2F to the bit[15:0] of [THS_CTRL](#) to set the ADC acquire time.
4. Write 0x1DF to the bit[31:16] of [THS_CTRL](#) to set the ADC sample frequency divider.
5. Write 0x3A to the bit[31:12] of [THS_PER](#) to set the THS work period.

6. Write 0x1 to the bit[2] of [THS FILTER](#) to enable the temperature convert filter.
7. Write 0x1 to the bit[1:0] of [THS FILTER](#) to select the filter type.
8. Read THS eFuse value from SID, then write the eFuse value to [THSn CDATA](#) (n = 0,1 or 2) to calibrate THS.
9. Write 0x1 to the bit[0] of [THS EN](#) to enable THS.
10. Read the bit[0] of [THS DATA INTS](#). If it is 1, the temperature conversion is complete.
11. Read the bit[11:0] of [THSn DATA](#) (n = 0,1 or 2), and calculate the THS temperature based on section 3.11.3.4 THS Temperature Conversion Formula

Interrupt Mode

1. Write 0x1 to the bit16 of [THS BGR REG](#) to dessert the reset.
2. Write 0x1 to the bit0 of [THS BGR REG](#) to open the THS clock.
3. Write 0x2F to the bit[15:0] of [THS CTRL](#) to set the ADC acquire time.
4. Write 0x1DF to the bit[31:16] of [THS CTRL](#) to set the ADC sample frequency divider.
5. Write 0x3A to the bit[31:12] of [THS PER](#) to set the THS work period.
6. Write 0x1 to the bit2 of [THS FILTER](#) to enable the temperature convert filter.
7. Write 0x1 to the bit[1:0] of [THS FILTER](#) to select the filter type.
8. Read THS eFuse value from SID, and then write the eFuse value to [THSn CDATA](#) (n = 0,1 or 2)) to calibrate THS.
9. Write 0x1 to the bit[0] of [THS DATA INTC](#) to enable the interrupt of THS.
10. Set interrupt based on PLIC module.
11. Put the interrupt handler address into the interrupt vector table.
12. Write 0x1 to the bit[0] of [THS EN](#) to enable THS.
13. Read the bit[0] of [THS DATA INTS](#). If it is 1, the temperature conversion is complete.
14. Read the bit[11:0] of [THSn DATA](#) (n = 0,1 or 2), and calculate the THS temperature based on section 3.11.3.4 THS Temperature Conversion Formula

3.11.5 Register List

Module Name	Base Address
THS	0x02009400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register

Register Name	Offset	Description
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
THS0_ALARM_CTRL	0x0040	THS0 Alarm threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm threshold Control Register
THS0&THS1_SHUTDOWN_CTRL	0x0080	THS0 & THS1 Shutdown threshold Control Register
THS2_SHUTDOWN_CTRL	0x0084	THS2 Shutdown threshold Control Register
THS0&THS1_CDATA	0x00A0	THS0 & THS1 Calibration Data
THS2_CDATA	0x00A4	THS2 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register

3.11.6 Register Description

3.11.6.1 0x0000 THS Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC acquire time CLK_IN/(n + 1) The default value is 2 us.
15:0	R/W	0x2F	Reserved

3.11.6.2 0x0004 THS Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0:Disable 1:Enable

Offset: 0x0004			Register Name: THS_EN
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	THS1_EN Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_EN Enable temperature measurement sensor0 0:Disable 1:Enable

3.11.6.3 0x0008 THS Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature measurement period $4096*(n + 1)/\text{CLK_IN}$ The default value is 10 ms.
11:0	/	/	/

3.11.6.4 0x0010 THS Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	THS2_DATA_IRQ_EN Selects Temperature measurement data of sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects Temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects Temperature measurement data of sensor0 0:Disable 1:Enable

3.11.6.5 0x0014 THS Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INTO_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.11.6.6 0x0018 THS Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS_ALARM_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	ALARM_INT2_EN Selects Alarm interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects Alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INTO_EN Selects Alarm interrupt for sensor0 0:Disable 1:Enable

3.11.6.7 0x0020 THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	THS2_DATA_IRQ_STS Data interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ_STS Data interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ_STS Data interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.8 0x0024 THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.9 0x0028 THS Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	ALARM_OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

3.11.6.10 0x002C THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INTO_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

3.11.6.11 0x0030 Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter enable 0: Disabled 1: Enabled
1:0	R/W	0x1	FILTER_TYPE Averaging filter type 00: 2 01: 4 10: 8 11: 16

3.11.6.12 0x0040 THS0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARMO_T_HOT Thermal sensor0 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARMO_T_HYST Thermal sensor0 Alarm threshold for hysteresis temperature

3.11.6.13 0x0044 THS1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal sensor1 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal sensor1 Alarm threshold for hysteresis temperature

3.11.6.14 0x0048 THS2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: THS2_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal sensor2 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal sensor2 Alarm threshold for hysteresis temperature

3.11.6.15 0x0080 THS0 & THS1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: THS0&THS1_SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal sensor1 Shutdown Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal sensor0 Shutdown Threshold for hot temperature

3.11.6.16 0x0084 THS2 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0084			Register Name: THS2_SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal sensor2 Shutdown Threshold for hot temperature

3.11.6.17 0x00A0 THS0 & THS1 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS0&THS1_CDATA
Bit	Read/Write	Default/Hex	Description
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

3.11.6.18 0x00A4 THS2 Calibration Data (Default Value: 0x0000_0800)

Offset: 0x00A4			Register Name: THS2_CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

3.11.6.19 0x00C0 THS0 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	Read/Write	Default/Hex	Description
32:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

3.11.6.20 0x00C4 THS1 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

3.11.6.21 0x00C8 THS2 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: THS2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

3.12 Spinlock

3.12.1 Overview

The spinlock provides a hardware synchronization mechanism in multi-core systems. With the lock operation, the spinlock prevents multiple processors from handling the sharing data simultaneously and thus ensure the coherence of data.

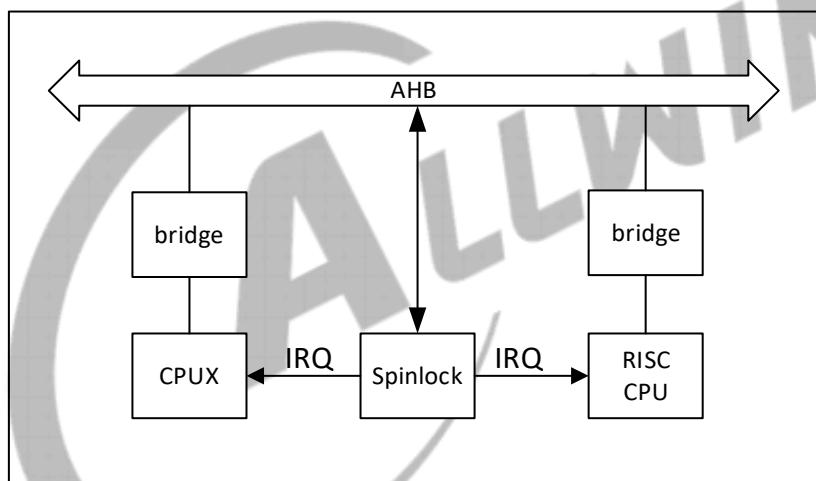
The spinlock has the following features:

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

3.12.2 Block Diagram

The following figure shows the block diagram of the spinlock.

Figure 3-30 Spinlock Block Diagram



3.12.3 Functional Descriptions

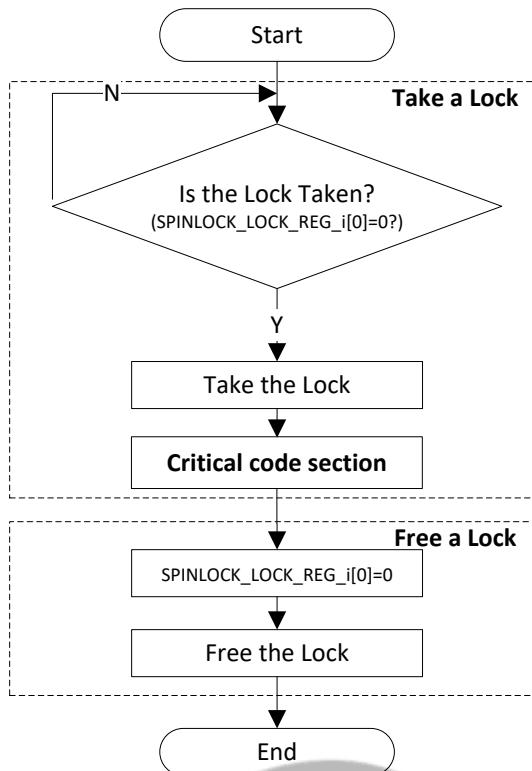
3.12.3.1 Clock and Reset

The spinlock is on AHB. Before accessing the spinlock registers, you need to de-assert the reset signal and then open the corresponding gating signal on AHB.

3.12.3.2 Typical Application

The following figure shows a typical application of the spinlock. A processor locks spinlock0 before executing specific codes, and then unlocks the codes. After the lock is freed, other processors can read or write the data.

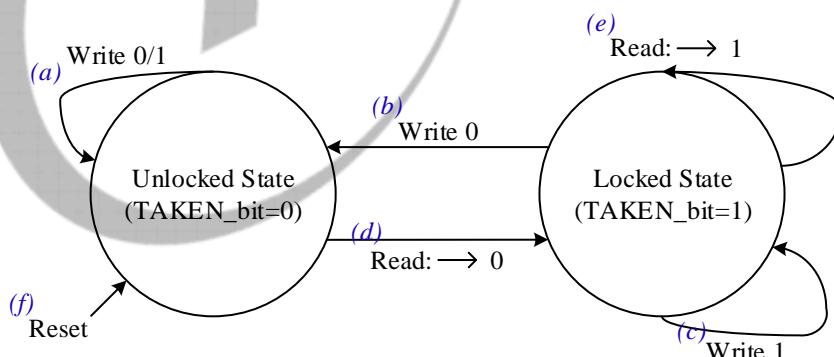
Figure 3-31 Spinlock Typical Application Diagram



3.12.3.3 Spinlock State Machine

When a processor uses spinlock, it needs to acquire the spinlock status through [SPINLOCK_STATUS_REG](#). The following figure shows the spinlock state machine.

Figure 3-32 Spinlock State Machine



1. When spinlock is in the Unlocked state, writing 0/1 has no effect;
2. When spinlock is in the Locked state, writing 0 can convert the corresponding spinlock to the Unlocked state;
3. When spinlock is in the Locked state, writing 1 has no effect;
4. When spinlock is in the Unlocked state, reading the bit can return 0 (it indicates spinlock enters into the Locked state);

5. When spinlock is in the Locked state, reading the bit can return 1 (it indicates spinlock is in the Locked state);
6. After resetting, spinlock is in the Unlock state by default.

3.12.4 Programming Guidelines

3.12.4.1 Switching the Status

Follow the steps below to switch the lock status of a spinlock.

1. When the read value from [SPINLOCKN_LOCK_REG](#) is 0, the spinlock comes into the Locked status.
2. Execute the application codes, and the status of [SPINLOCK_STATUS_REG](#) is 1.
3. Write 0 to [SPINLOCKN_LOCK_REGD](#), the spinlock converts into the Unlocked status, and the corresponding spinlock is released.

3.12.4.2 Processing the Interrupt

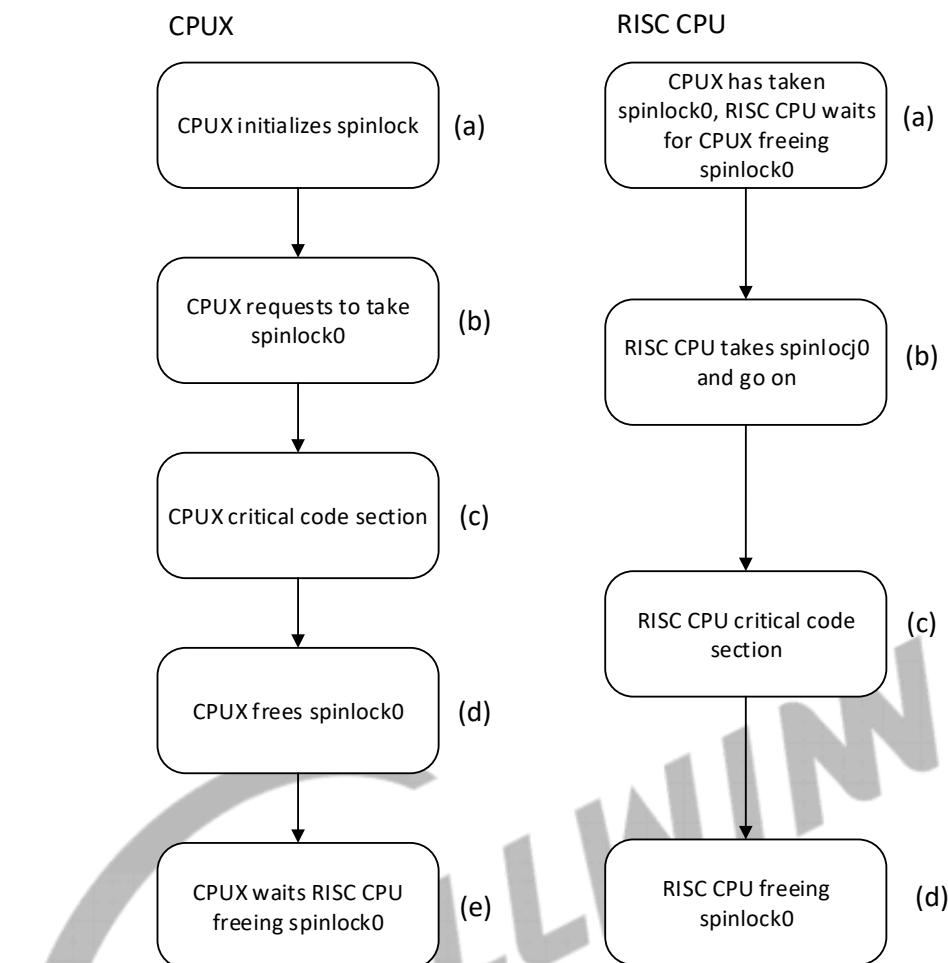
The spinlock generates an interrupt when a lock is freed (the lock status converts from Locked to Unlocked).

Follow the steps below to process the interrupt:

1. Configure the interrupt enable bit of the corresponding spinlock in [SPINLOCK_IRQ_EN_REG](#) to enable the interrupt.
2. The spinlock generates an interrupt when its status converts from Locked to Unlocked, and the corresponding bit of the [SPINLOCK_IRQ_STA_REG](#) turns to 1.
3. Execute the interrupt handle function and clear the pending bit.

3.12.4.3 Taking/Freeing Spinlock

Take Spinlock0 as an example, the CPUX takes the spinlock0 firstly in the instance. To take/free spinlock0, the CPUX and RISC CPU perform the following steps:

Figure 3-33 CPUX and RISC CPU Taking/Freeing Spinlock0 Process**CPUX:**

1. The CPUX initializes Spinlock.
2. Firstly, check lock register0 (SPINLOCK_STATUS_REG0) status. if it is taken, check till CPUX frees spinlock0. Then request to take spinlock0. Otherwise, retry till lock register0 is taken.
3. Execute CPUX critical code.
4. After executing CPUX critical code, the CPUX frees spinlock0.
5. The CPUX waits for RISCV CPU to free spinlock0.

RISCV CPU:

1. If the CPUX has taken spinlock0, the RISC CPU waits for CPUX to free spinlock0.
2. The RISC CPU requests to take spinlock0. if fail, retry till lock register0 is taken.
3. Execute RISC CPU critical code.
4. After executing RISC CPU critical code, the RISC CPU frees spinlock0.

The following codes are for reference.

-----CPUX of Cluster0-----

1. CPUX initializes Spinlock

```
put_wvalue(SPINLOCK_BGR_REG,0x00010000);  
put_wvalue(SPINLOCK_BGR_REG,0x00010001);
```

2. CPUX requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG0);           //Check lock register0 status  
if(rdata != 0)    writel(0, SPINLOCK_LOCK_REG0); //If it is taken, check till CPUX frees spinlock0  
rdata=readl(SPINLOCK_LOCK_REG0);             //Request to take spinlock0  
if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0); //If it fails, retry till lock register0 is taken
```

----- CPUX critical code section -----

3. CPUX free spinlock0

```
writel(0, SPINLOCK_LOCK_REG0);                //CPUX frees spinlock0
```

4. CPUX waits for RISC CPU' freeing spinlock0

```
writel(readl(SPINLOCK_STATUS_REG0) == 1);      //CPUX waits for RISC CPU' freeing spinlock0
```

-----RISC CPU-----

1. CPUX has taken spinlock0, RISC CPU waits for CPUX' freeing spinlock0

```
while(readl(SPINLOCK_STATUS_REG0) == 1);          //RISC CPU waits for CPUX' freeing spinlock0
```

2. RISC CPU takes spinlock0 and go on

```
rdata=readl(SPINLOCK_LOCK_REG0);                 //Request to take spinlock0
```

```
if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0); //If it fails, retry till lock register0 is taken
```

----- RISC CPU critical code section -----

3. RISC CPU frees spinlock0

```
writel(0, SPINLOCK_LOCK_REG0);                  //RISC CPU frees spinlock0
```

3.12.5 Register List

Module Name	Base Address
Spinlock	0x03005000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	SpinLock System Status Register
SPINLOCK_STATUS_REG	0x0010	SpinLock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	SpinLock Interrupt Enable Register
SPINLOCK_IRQ_STA_REG	0x0040	SpinLock Interrupt Status Register
SPINLOCK_LOCKID0_REG	0x0080	SpinLock Lockid0 Register
SPINLOCK_LOCKID1_REG	0x0084	SpinLock Lockid1 Register
SPINLOCK_LOCKID2_REG	0x0088	SpinLock Lockid2 Register
SPINLOCK_LOCKID3_REG	0x008C	SpinLock Lockid3 Register
SPINLOCK_LOCKID4_REG	0x0090	SpinLock Lockid4 Register
SPINLOCKN_LOCK_REG	0x0100+N*0x0004 (N=0~31)	SpinLock Register N

3.12.6 Register Description

3.12.6.1 0x0000 Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM. Number of lock registers implemented. 00: This instance has 256 lock registers. 01: This instance has 32 lock registers. 10: This instance has 64 lock registers. 11: This instance has 128 lock registers.
27:9	/	/	/
8	R	0x0	IU0. Use Flag0. In-Use flag0, covering lock register0-31. 0: All lock register 0-31 are in the Not Taken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

3.12.6.2 0x0010 SpinLock Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS SpinLock[i] status (i=0~31) 0: The Spinlock is free 1: The Spinlock is taken

3.12.6.3 0x0020 SpinLock Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
[i] (i=0~31)	R/W	0x0	LOCK_IRQ_EN SpinLock[i] interrupt enable. 0: Disable 1: Enable

3.12.6.4 0x0040 SpinLock Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
[i] (i=0~31)	R/W1C	0x0	LOCK_IRQ_STATUS SpinLock[i] interrupt status. 0: No effect 1: Pending Writing 1 will clear this bit.

3.12.6.5 0x0100 + N*0x0004 SpinLock Register N (N = 0 to 31) (Default Value: 0x0000_0000)

Offset: 0x0100 + N*0x0004 (N = 0 to 31)			Register Name: SPINLOCKN_LOCK_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TAKEN. Lock State. Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must be retried. Write 0x1: No update to the lock value.

3.13 I/O Memory Management Unit (IOMMU)

3.13.1 Overview

The I/O Memory management unit (IOMMU) is designed for the specific memory requirements of products. It maps the virtual address (sent by peripheral access memory) to the physical address. The IOMMU allows multiple ways to manage the location of physical address, and it can use physical address which has potentially conflict mapping for different processes to allocate memory space, and also allow application of non-continuous address mapping to continuous virtual address space.

Features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports the parallel address mapping of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports the independent bypass function of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports the independent pre-fetch function of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports the independent interrupt handing mechanism of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports 2 levels TLB (level 1 TLB for special using, and level 2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled function
- Triggers the PTW behavior when TLB is missed
- Supports the permission checking

3.13.2 Block Diagram

The internal module of IOMMU mainly includes the following parts.

Micro TLB: Level1 TLB, 64 words. Each peripheral corresponds to a TLB, which caching the level2 page table for the peripheral.

Macro TLB: Level2 TLB, 4K words. Each peripheral shares a level2 TLB for caching the level2 page table.

Pre-fetch Logic: Each Micro TLB corresponds to a Pre-fetch Logic. By monitoring each master device to predict the bus access, the secondary page table corresponding to the address to be accessed can be read from the memory and stored in the secondary TLB to improve the hit ratio.

PTW Logic: Page Table Walk, mainly contains PTW Cache and PTW. The PTW Cache is used to store the level1 page table; when the virtual address is missed in the level1 and level2 TLB, it will trigger the PTW. PTW Cache can store 512 level1 page tables, that is, 512 words.

PMU: Performance Monitoring Unit, which is used to count the hit efficiency and the latency.

APB Interface: IOMMU register instantiation module. CPU reads and writes the IOMMU register by APB bus.

The following figure shows the internal block diagram of IOMMU.

Figure 3-34 IOMMU Block Diagram

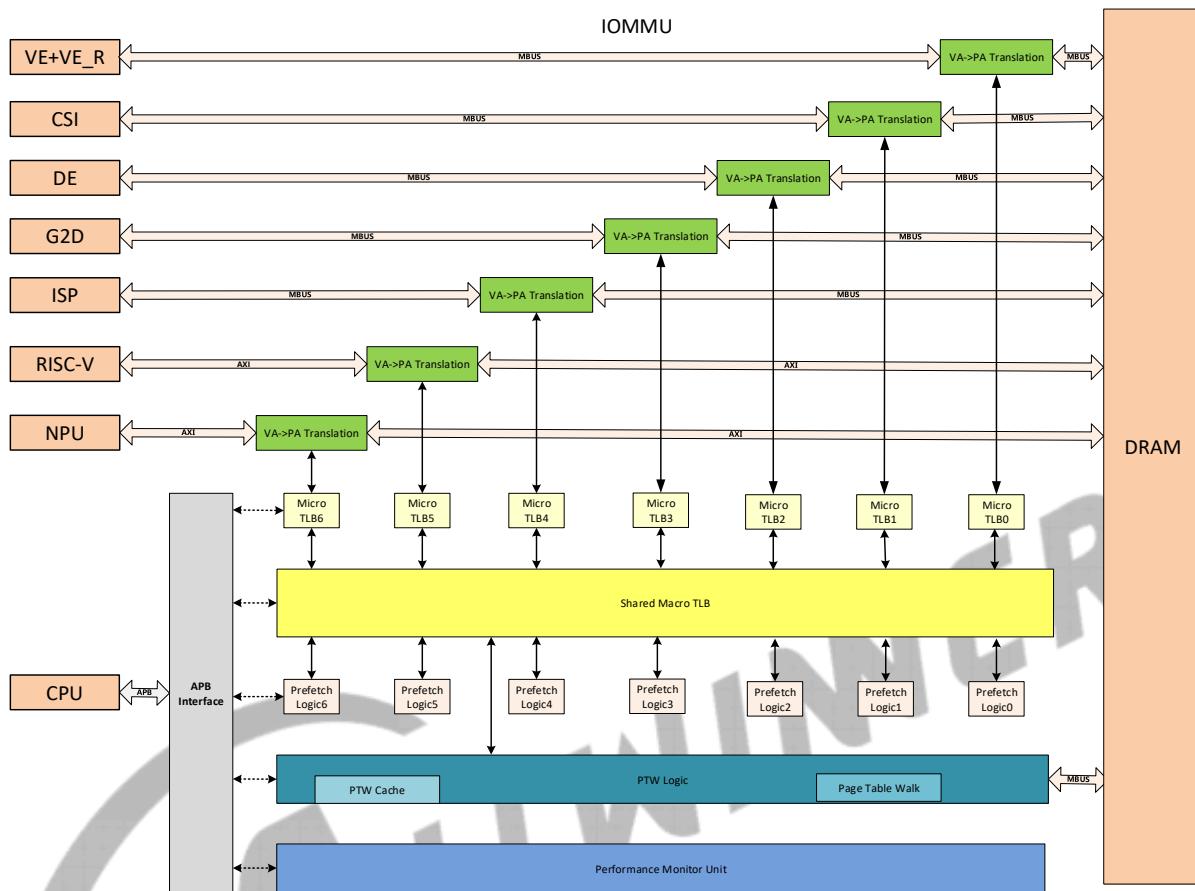


Table 3-16 Correspondence Relation between Master and Module

Master Number	Module
Master0	VE+VE_R
Master1	CSI
Master2	DE
Master3	G2D
Master4	ISP
Master5	RISC-V
Master6	NPU

3.13.3 Function Descriptions

3.13.3.1 Initialization

- Release the IOMMU reset signal by writing 1 to the bit[31] of the [IOMMU RESET REG \(Offset: 0x0010\)](#);
- Write the base address of the first TLB to the [IOMMU TTB REG \(Offset: 0x0050\)](#);
- Set the [IOMMU INT_ENABLE REG \(Offset: 0x0100\)](#);

- Enable the IOMMU by configuring the [IOMMU_ENABLE_REG \(Offset: 0x0020\)](#) in the final.

3.13.3.2 Address Translation

In the process of address mapping, the peripheral virtual address [31:12] are retrieved in the Level1 TLB. When TLB is hit, the mapping is finished. Otherwise, they are retrieved in the Level2 TLB in the same way. If TLB is hit, the hit mapping will be written to the Level1 TLB, and hit in Level1 TLB. If Level1 and Level2 TLB are retrieved fail, the PTW will be triggered. After opening the peripheral bypass function by setting IOMMU_BYPASS_REG (Offset: 0x0030), IOMMU will not map the address typed by this peripheral, and it will output the virtual address as the physical address. The typical applications are as follows.

Micro TLB hit

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is hit, it will return a Level2 page table containing the corresponding physical addresses and the permission Index;
3. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB hit

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is missed, continue to search Macro TLB;
3. If Macro TLB is hit, it will return the Level2 page table to Micro TLB;
4. Micro TLB receives this page table, puts it in Micro TLB (If this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;
5. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache hit

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is missed, continue to search Macro TLB;
3. If Macro TLB is missed, send the request to the PTW to return the corresponding page table;
4. PTW first accesses PTW Cache. If the required Level1 page table exists in the PTW Cache, send the page table to PTW logic;

5. PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;
6. Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;
7. Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;
8. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache miss

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is missed, continue to search Macro TLB;
3. If Macro TLB is missed, send the request to the PTW to return the corresponding page table;
4. PTW accesses PTW Cache, there is no necessary Level1 page table;
5. PTW accesses the memory, gets the corresponding Level1 page table and stores it in the PTW Cache (the replace activities may happen);
6. PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;
7. Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;
8. Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;
9. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Permission error

1. The permission checking is always performed during the process of translating the address;
2. Once the permission checking makes mistake, the new access of the master suspends, but the access before this checking can be continued;
3. Set the error status register;
4. Trigger the interrupt.

Invalid Level1 page table

1. The invalid Level1 page table is checked when PTW logic reads the new level page table from the memory;
2. The PTW reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the PTW cache;
3. If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.



NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in PTW Cache with target page table is found to be invalid after using;

If a page table is invalid, invalidate the total cache line (that is two page tables).

Invalid Level2 page table

1. The invalid Level2 page table is checked when Macro TLB reads the new level page table from the memory;
2. The Macro TLB reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the Macro TLB;
3. If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.



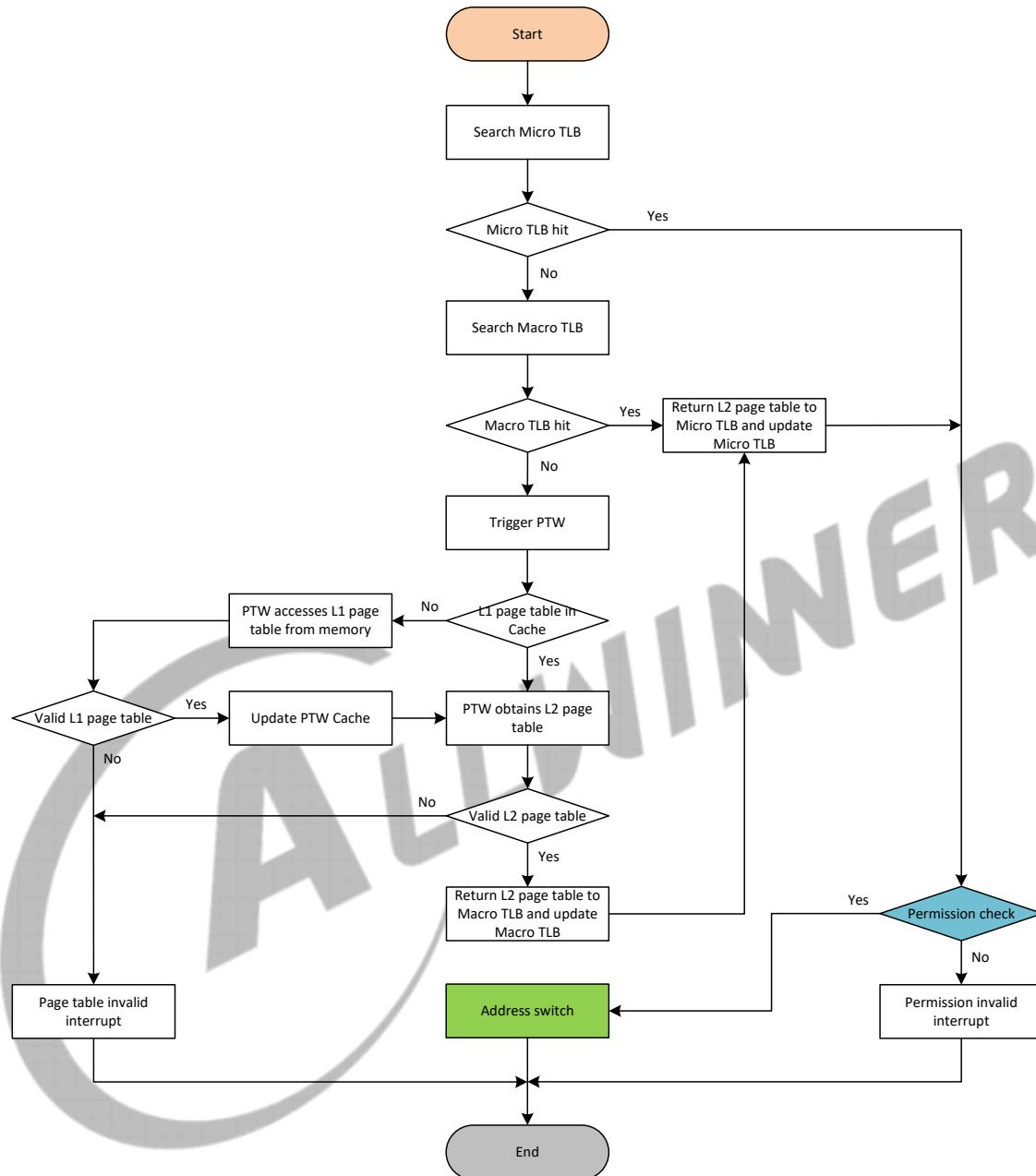
NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in Macro TLB with target page table is found to be invalid after using;

If a page table is invalid, invalidate the total cache line (that is two page tables).

The internal address translation process is shown in the following figure.

Figure 3-35 Internal Switch Process



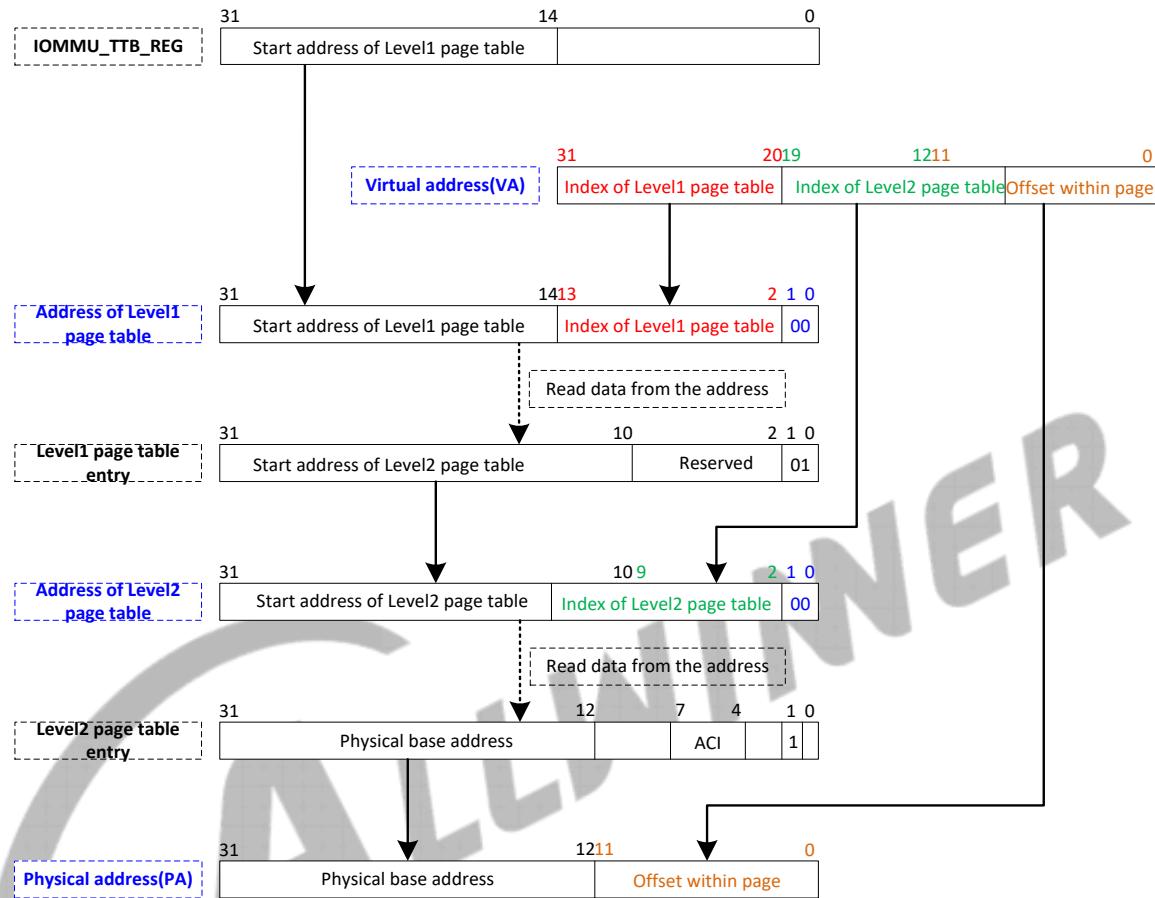
3.13.3.3 VA-PA Mapping

IOMMU page table is defined as the Level2 mapping. The first level is 1M address space mapping, the second level is 4K address space. This version does not support 1K, 16K and other page table sizes. IOMMU only supports a page table, the meaning is:

- All peripherals connected to IOMMU use the same virtual address space;
- The virtual address space of the peripherals can overlap;
- Different virtual addresses can map to the same physical address space;

Base address of this page table is defined by the software, and it needs 16 KB address alignment. The page table of the Level2 table item needs 1 KB address alignment. A complete VA-PA address translation process is shown in the following figure.

Figure 3-36 VA-PA Switch Process



3.13.3.4 Clearing and Invalidating TLB

When multi page table contents are refreshed or table address changes, all VA-PA mappings which have been cached in TLB will be invalid. You need to configure [IOMMU_TLB_FLUSH_ENABLE_REG \(Offset: 0x0080\)](#) to clear the TLB or PTW Cache according to the following steps:

1. Suspend the access to TLB or Cache.
2. Configure the corresponding Flush bit of [IOMMU_TLB_FLUSH_ENABLE_REG \(Offset: 0x0080\)](#).
3. After the operation takes effect, the related peripherals can continue to send the new access memory operations.

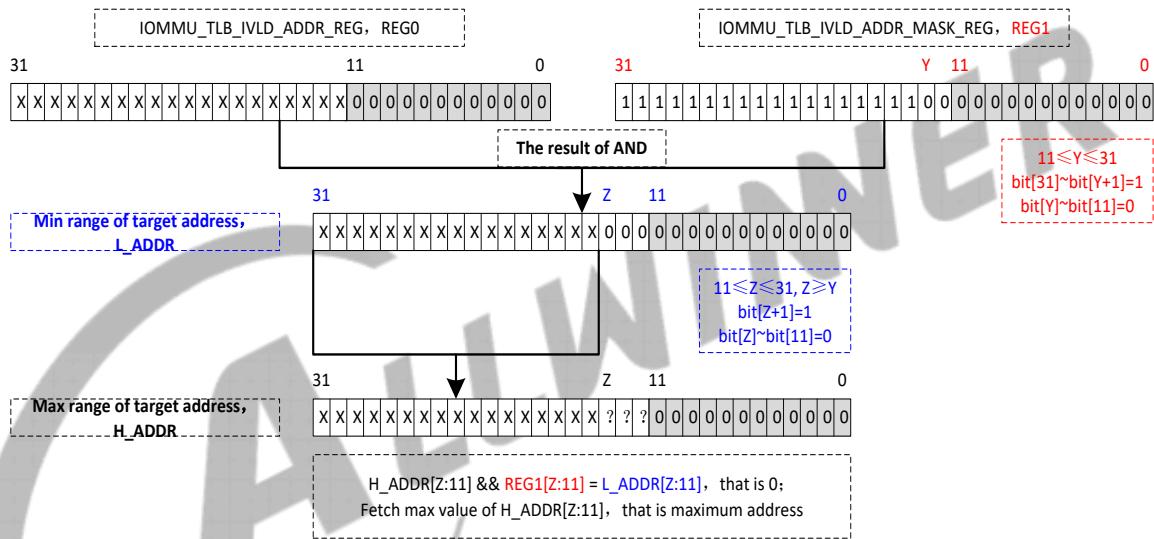
When some page table is invalid or the mapping is incorrect, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. The invalid TLB supports the following two modes:

Mode0

1. Set [IOMMU_TLB_IVLD_MODE_SEL_REG \(Offset: 0x0084\)](#) to 0 and select mode0;
2. Write the target address to [IOMMU_TLB_IVLD_ADDR_REG \(Offset: 0x0090\)](#);

3. Set the configuration values to [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#), the requirements are as follows:
 - The value of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) cannot be less than the [IOMMU_TLB_IVLD_ADDR_REG \(Offset: 0x0090\)](#).
 - The higher bit of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) must be continuous 1, the lower bit must be continuous 0. For example, 0xFFFFF000, 0xFFFFE000, 0xFFFFC000, 0xFFFF8000, and 0xFFFF0000 are legal values; while 0xFFFFD000, 0xFFFFB000, 0xFFFFA000, 0xFFFF9000, and 0xFFFF7000 are illegal values.
4. Configure [IOMMU_TLB_IVLD_ENABLE_REG \(Offset: 0x0098\)](#) to enable the invalid operation. Among the way to determine the invalid address is to get the maximum valid bit and determine the target address range by the target address AND the mask address. The process is shown as follows.

Figure 3-37 Invalid TLB Address Range



The examples are shown below:

- When the value of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) is 0xFFFFF000 by default, the result of AND is target address. That is, only the target address is invalid.
- When the value of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) is 0xFFFF0000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEF000.
- When the value of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) is 0xFFFFC000, the value of (0x0090) is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEB000.
- When the value of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) is 0xFFFF8000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEC000, then target address range is from 0xEEEE8000 to 0xEEEF000.
- When the value of [IOMMU_TLB_IVLD_ADDR_MASK_REG \(Offset: 0x0094\)](#) is 0xFFFFC000, the value of [IOMMU_TLB_IVLD_ADDR_REG \(Offset: 0x0090\)](#) is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEE3000.

Mode1

1. Set [IOMMU_TLB_IVLD_MODE_SEL_REG \(Offset: 0x0084\)](#) to 1 and select mode1;
2. Set the starting address and the ending address of the invalid TLB by [IOMMU_TLB_IVLD_STA_ADDR_REG \(Offset: 0x0088\)](#);
3. Configure [IOMMU_TLB_IVLD_ENABLE_REG \(Offset: 0x0098\)](#) to enable the invalid operation, then the TLB invalidating operation can be completed.

3.13.3.5 Clearing and Invalidating PTW Cache**Mode0**

1. Set [IOMMU_PC_IVLD_MODE_SEL_REG \(Offset: 0x009C\)](#) to 0 and select mode0.
2. Invalid the [IOMMU_PC_IVLD_ADDR_REG \(Offset: 0x00A0\)](#), 1MB aligned.
3. Configure [IOMMU_PC_IVLD_ENABLE_REG \(Offset: 0x00A8\)](#) to enable the invalid operation, then you can invalid one piece of CacheLine.

Mode1

1. Set [IOMMU_PC_IVLD_MODE_SEL_REG \(Offset: 0x009C\)](#) to 1 and select mode1.
2. Set the starting address and the ending address of the invalid TLB by [IOMMU_PC_IVLD_STA_ADDR_REG \(Offset: 0x00A4\)](#).
3. Configure [IOMMU_PC_IVLD_ENABLE_REG \(Offset: 0x00A8\)](#) to enable the invalid operation, then you can invalid a period of sections.

3.13.3.6 Level1 Page Table

The format of Level1 page table is as follows.

Figure 3-38 Level1 Page Table Format

31	10 9	2 1 0
Start address of Level2 page table	Reserved	01

Bit[31:10]: Base address of Level2 page table;

Bit[9:2]: Reserved;

Bit[1:0]: 01 is a valid page table; other values are fault;

3.13.3.7 Level2 Page Table

The format of Level2 page table is as follows.

Figure 3-39 Level2 Page Table Format

31	12	7	4	1 0
Physical base address		ACI		1

Bit[31:12]: Physical address of 4K address;

Bit[11:8]: Reserved;

Bit[7:4]: ACI, permission control index; correspond to permission control bit of **IOMMU Domain Authority Control Register**;

Bit[3:2]: Reserved;

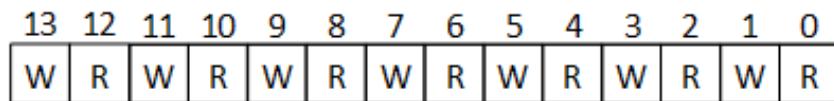
Bit[1]: 1 is a valid page table; 0 is fault;

Bit[0]: Reserved

3.13.3.8 Permission Index

The read/write access control of series register such as **IOMMU Domain Authority Control Register** is as follows.

Figure 3-40 Read/Write Permission Control



Bit[1:0]/Bit[17:16]: Master0 read/write permission control;

Bit[3:2]/Bit[19:18]: Master1 read/write permission control;

Bit[5:4]/Bit[21:20]: Master2 read/write permission control;

Bit[7:6]/Bit[23:22]: Master3 read/write permission control;

Bit[9:8]/Bit[25:24]: Master4 read/write permission control;

Bit[11:10]/Bit[27:26]: Master5 read/write permission control;

Bit[13:12]/Bit[29:28]: Master6 read/write permission control.

The value of **IOMMU Domain Authority Control Register** is read-only by default. Other registers can configure through the system requirement. During the address switch process, the corresponding relation between ACI and Domain is as follows.

Table 3-17 Relation between ACI and Domain

ACI	Domain	Register
0	Domain 0	IOMMU Domain Authority Control Register 0
1	Domain 1	IOMMU Domain Authority Control Register 0
2	Domain 2	IOMMU Domain Authority Control Register 1
3	Domain 3	IOMMU Domain Authority Control Register 1
4	Domain 4	IOMMU Domain Authority Control Register 2
5	Domain 5	IOMMU Domain Authority Control Register 2
6	Domain 6	IOMMU Domain Authority Control Register 3
7	Domain 7	IOMMU Domain Authority Control Register 3

ACI	Domain	Register
8	Domain 8	IOMMU Domain Authority Control Register 4
9	Domain 9	IOMMU Domain Authority Control Register 4
10	Domain 10	IOMMU Domain Authority Control Register 5
11	Domain 11	IOMMU Domain Authority Control Register 5
12	Domain 12	IOMMU Domain Authority Control Register 6
13	Domain 13	IOMMU Domain Authority Control Register 6
14	Domain 14	IOMMU Domain Authority Control Register 7
15	Domain 15	IOMMU Domain Authority Control Register7

After enabled **IOMMU Domain Authority Overwrite Register**, the read/write control permission can override all **IOMMU Domain Authority Control Register**.

3.13.4 Programming Guidelines

3.13.4.1 Resetting IOMMU

Before the IOMMU module software reset operation, make sure IOMMU is never opened, or all bus operations are completed, or DRAM and peripherals already open the corresponding switch, to shield the influence of IOMMU reset.

3.13.4.2 Enabling IOMMU

Before opening the IOMMU address mapping function, [IOMMU_TTB_REG \(Offset: 0x0050\)](#) should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

3.13.4.3 Configuring TTB

Operating the register must close IOMMU address mapping function, namely [IOMMU_ENABLE_REG \(Offset: 0x0020\)](#) is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

3.13.4.4 Clearing TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

3.13.4.5 Reading/Writing VA Data

For the virtual address, read and write the corresponding physical address data to make sure whether IOMMU module address mapping function is normal. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after the operation is finished, check if the results are as expected.

3.13.4.6 PMU Statistics

When PMU function is used for the first time, set [IOMMU PMU ENABLE REG \(Offset: 0x0200\)](#) to enable statistics function; when reading the relevant Register, clear the enable bit of [IOMMU PMU ENABLE REG \(Offset: 0x0200\)](#); when PMU function is used next time, first [IOMMU PMU CLR REG \(Offset: 0x0210\)](#) is set, after counter is cleared, set the enable bit of [IOMMU PMU ENABLE REG \(Offset: 0x0200\)](#).

Given a Level2 page table administers continuous 4KB address, if Micro TLB misses in continuous virtual address, a Level2 page table needs to be returned from Macro TLB to hit; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So the true hit rate calculation is as follows:

$$\text{Hit Rate} = N1/M1 + (1-N1/M1)*N2/M2$$

N1: Micro TLB hit number

M1: Micro TLB access number

N2: Macro TLB hit number

M2: Macro TLB access number

3.13.5 Register List

Module Name	Base Address
IOMMU	0x0201_0000

Register Name	Offset	Description
IOMMU_RESET_REG	0x0010	IOMMU Reset Register
IOMMU_ENABLE_REG	0x0020	IOMMU Enable Register
IOMMU_BYPASS_REG	0x0030	IOMMU Bypass Register
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto Gating Register
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table Base Register
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB Enable Register
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB Prefetch Register
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_MODE_SEL_REG	0x0084	IOMMU TLB Invalidation Mode Select Register
IOMMU_TLB_IVLD_STA_ADDR_REG	0x0088	IOMMU TLB Invalidation Start Address Register
IOMMU_TLB_IVLD_END_ADDR_REG	0x008C	IOMMU TLB Invalidation End Address Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register
IOMMU_PC_IVLD_MODE_SEL_REG	0x009C	IOMMU PC Invalidation Mode Select Register
IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register
IOMMU_PC_IVLD_STA_ADDR_REG	0x00A4	IOMMU PC Invalidation Start Address Register

Register Name	Offset	Description
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_PC_IVLD_END_ADDR_REG	0x00AC	IOMMU PC Invalidation End Address Register
IOMMU_DM_AUT_CTRL0_REG	0x00B0	IOMMU Domain Authority Control 0 Register
IOMMU_DM_AUT_CTRL1_REG	0x00B4	IOMMU Domain Authority Control 1 Register
IOMMU_DM_AUT_CTRL2_REG	0x00B8	IOMMU Domain Authority Control 2 Register
IOMMU_DM_AUT_CTRL3_REG	0x00BC	IOMMU Domain Authority Control 3 Register
IOMMU_DM_AUT_CTRL4_REG	0x00C0	IOMMU Domain Authority Control 4 Register
IOMMU_DM_AUT_CTRL5_REG	0x00C4	IOMMU Domain Authority Control 5 Register
IOMMU_DM_AUT_CTRL6_REG	0x00C8	IOMMU Domain Authority Control 6 Register
IOMMU_DM_AUT_CTRL7_REG	0x00CC	IOMMU Domain Authority Control 7 Register
IOMMU_DM_AUT_OVWT_REG	0x00D0	IOMMU Domain Authority Overwrite Register
IOMMU_INT_ENABLE_REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR_REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA_REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR0_REG	0x0110	IOMMU Interrupt Error Address 0 Register
IOMMU_INT_ERR_ADDR1_REG	0x0114	IOMMU Interrupt Error Address 1 Register
IOMMU_INT_ERR_ADDR2_REG	0x0118	IOMMU Interrupt Error Address 2 Register
IOMMU_INT_ERR_ADDR3_REG	0x011C	IOMMU Interrupt Error Address 3 Register
IOMMU_INT_ERR_ADDR4_REG	0x0120	IOMMU Interrupt Error Address 4 Register
IOMMU_INT_ERR_ADDR5_REG	0x0124	IOMMU Interrupt Error Address 5 Register
IOMMU_INT_ERR_ADDR6_REG	0x0128	IOMMU Interrupt Error Address 6 Register
IOMMU_INT_ERR_ADDR7_REG	0x0130	IOMMU Interrupt Error Address 7 Register
IOMMU_INT_ERR_ADDR8_REG	0x0134	IOMMU Interrupt Error Address 8 Register
IOMMU_INT_ERR_DATA0_REG	0x0150	IOMMU Interrupt Error Data 0 Register
IOMMU_INT_ERR_DATA1_REG	0x0154	IOMMU Interrupt Error Data 1 Register
IOMMU_INT_ERR_DATA2_REG	0x0158	IOMMU Interrupt Error Data 2 Register
IOMMU_INT_ERR_DATA3_REG	0x015C	IOMMU Interrupt Error Data 3 Register
IOMMU_INT_ERR_DATA4_REG	0x0160	IOMMU Interrupt Error Data 4 Register
IOMMU_INT_ERR_DATA5_REG	0x0164	IOMMU Interrupt Error Data 5 Register
IOMMU_INT_ERR_DATA6_REG	0x0168	IOMMU Interrupt Error Data 6 Register
IOMMU_INT_ERR_DATA7_REG	0x0170	IOMMU Interrupt Error Data 7 Register
IOMMU_INT_ERR_DATA8_REG	0x0174	IOMMU Interrupt Error Data 8 Register
IOMMU_L1PG_INT_REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT_REG	0x0184	IOMMU L2 Page Table Interrupt Register
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE_REG	0x0200	IOMMU PMU Enable Register
IOMMU_PMU_CLR_REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW0_REG	0x0230	IOMMU PMU Access Low 0 Register
IOMMU_PMU_ACCESS_HIGH0_REG	0x0234	IOMMU PMU Access High 0 Register
IOMMU_PMU_HIT_LOW0_REG	0x0238	IOMMU PMU Hit Low 0 Register

Register Name	Offset	Description
IOMMU_PMU_HIT_HIGH0_REG	0x023C	IOMMU PMU Hit High 0 Register
IOMMU_PMU_ACCESS_LOW1_REG	0x0240	IOMMU PMU Access Low 1 Register
IOMMU_PMU_ACCESS_HIGH1_REG	0x0244	IOMMU PMU Access High 1 Register
IOMMU_PMU_HIT_LOW1_REG	0x0248	IOMMU PMU Hit Low 1 Register
IOMMU_PMU_HIT_HIGH1_REG	0x024C	IOMMU PMU Hit High 1 Register
IOMMU_PMU_ACCESS_LOW2_REG	0x0250	IOMMU PMU Access Low 2 Register
IOMMU_PMU_ACCESS_HIGH2_REG	0x0254	IOMMU PMU Access High 2 Register
IOMMU_PMU_HIT_LOW2_REG	0x0258	IOMMU PMU Hit Low 2 Register
IOMMU_PMU_HIT_HIGH2_REG	0x025C	IOMMU PMU Hit High 2 Register
IOMMU_PMU_ACCESS_LOW3_REG	0x0260	IOMMU PMU Access Low 3 Register
IOMMU_PMU_ACCESS_HIGH3_REG	0x0264	IOMMU PMU Access High 3 Register
IOMMU_PMU_HIT_LOW3_REG	0x0268	IOMMU PMU Hit Low 3 Register
IOMMU_PMU_HIT_HIGH3_REG	0x026C	IOMMU PMU Hit High 3 Register
IOMMU_PMU_ACCESS_LOW4_REG	0x0270	IOMMU PMU Access Low 4 Register
IOMMU_PMU_ACCESS_HIGH4_REG	0x0274	IOMMU PMU Access High 4 Register
IOMMU_PMU_HIT_LOW4_REG	0x0278	IOMMU PMU Hit Low 4 Register
IOMMU_PMU_HIT_HIGH4_REG	0x027C	IOMMU PMU Hit High 4 Register
IOMMU_PMU_ACCESS_LOW5_REG	0x0280	IOMMU PMU Access Low 5 Register
IOMMU_PMU_ACCESS_HIGH5_REG	0x0284	IOMMU PMU Access High 5 Register
IOMMU_PMU_HIT_LOW5_REG	0x0288	IOMMU PMU Hit Low 5 Register
IOMMU_PMU_HIT_HIGH5_REG	0x028C	IOMMU PMU Hit High 5 Register
IOMMU_PMU_ACCESS_LOW6_REG	0x0290	IOMMU PMU Access Low 6 Register
IOMMU_PMU_ACCESS_HIGH6_REG	0x0294	IOMMU PMU Access High 6 Register
IOMMU_PMU_HIT_LOW6_REG	0x0298	IOMMU PMU Hit Low 6 Register
IOMMU_PMU_HIT_HIGH6_REG	0x029C	IOMMU PMU Hit High 6 Register
IOMMU_PMU_ACCESS_LOW7_REG	0x02D0	IOMMU PMU Access Low 7 Register
IOMMU_PMU_ACCESS_HIGH7_REG	0x02D4	IOMMU PMU Access High 7 Register
IOMMU_PMU_HIT_LOW7_REG	0x02D8	IOMMU PMU Hit Low 7 Register
IOMMU_PMU_HIT_HIGH7_REG	0x02DC	IOMMU PMU Hit High 7 Register
IOMMU_PMU_ACCESS_LOW8_REG	0x02E0	IOMMU PMU Access Low 8 Register
IOMMU_PMU_ACCESS_HIGH8_REG	0x02E4	IOMMU PMU Access High 8 Register
IOMMU_PMU_HIT_LOW8_REG	0x02E8	IOMMU PMU Hit Low 8 Register
IOMMU_PMU_HIT_HIGH8_REG	0x02EC	IOMMU PMU Hit High 8 Register
IOMMU_PMU_TL_LOW0_REG	0x0300	IOMMU Total Latency Low 0 Register
IOMMU_PMU_TL_HIGH0_REG	0x0304	IOMMU Total Latency High 0 Register
IOMMU_PMU_ML0_REG	0x0308	IOMMU Max Latency 0 Register
IOMMU_PMU_TL_LOW1_REG	0x0310	IOMMU Total Latency Low 1 Register
IOMMU_PMU_TL_HIGH1_REG	0x0314	IOMMU Total Latency High 1 Register
IOMMU_PMU_ML1_REG	0x0318	IOMMU Max Latency 1 Register
IOMMU_PMU_TL_LOW2_REG	0x0320	IOMMU Total Latency Low 2 Register
IOMMU_PMU_TL_HIGH2_REG	0x0324	IOMMU Total Latency High 2 Register
IOMMU_PMU_ML2_REG	0x0328	IOMMU Max Latency 2 Register

Register Name	Offset	Description
IOMMU_PMU_TL_LOW3_REG	0x0330	IOMMU Total Latency Low 3 Register
IOMMU_PMU_TL_HIGH3_REG	0x0334	IOMMU Total Latency High 3 Register
IOMMU_PMU_ML3_REG	0x0338	IOMMU Max Latency 3 Register
IOMMU_PMU_TL_LOW4_REG	0x0340	IOMMU Total Latency Low 4 Register
IOMMU_PMU_TL_HIGH4_REG	0x0344	IOMMU Total Latency High 4 Register
IOMMU_PMU_ML4_REG	0x0348	IOMMU Max Latency 4 Register
IOMMU_PMU_TL_LOW5_REG	0x0350	IOMMU Total Latency Low 5 Register
IOMMU_PMU_TL_HIGH5_REG	0x0354	IOMMU Total Latency High 5 Register
IOMMU_PMU_ML5_REG	0x0358	IOMMU Max Latency 5 Register
IOMMU_PMU_TL_LOW6_REG	0x0360	IOMMU Total Latency Low 6 Register
IOMMU_PMU_TL_HIGH6_REG	0x0364	IOMMU Total Latency High 6 Register
IOMMU_PMU_ML6_REG	0x0368	IOMMU Max Latency 6 Register

3.13.6 Register Description

3.13.6.1 0x0010 IOMMU Reset Register (Default Value: 0x8003_007F)

Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	<p>IOMMU_RESET IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; Or all bus operations are completed; Or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset.</p>
30:18	/	/	/
17	R/W	0x1	<p>PTW_CACHE_RESET PTW Cache address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used to reset PTW Cache individually.</p>
16	R/W	0x1	<p>MACRO_TLB_RESET Macro TLB address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Macro TLB occurs abnormal, the bit is used to reset Macro TLB individually.</p>
15:7	/	/	/

Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x1	<p>MASTER6_RESET Master6 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master6 occurs abnormal, the bit is used to reset Master6 individually.</p>
5	R/W	0x1	<p>MASTER5_RESET Master5 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, the bit is used to reset Master5 individually.</p>
4	R/W	0x1	<p>MASTER4_RESET Master4 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, the bit is used to reset Master4 individually.</p>
3	R/W	0x1	<p>MASTER3_RESET Master3 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, the bit is used to reset Master3 individually.</p>
2	R/W	0x1	<p>MASTER2_RESET Master2 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, the bit is used to reset Master2 individually.</p>
1	R/W	0x1	<p>MASTER1_RESET Master1 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master1 occurs abnormal, the bit is used to reset Master1 individually.</p>
0	R/W	0x1	<p>MASTER0_RESET Master0 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, the bit is used to reset Master0 individually.</p>

3.13.6.2 0x0020 IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	<p>ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU</p> <p>Before opening the IOMMU address mapping function, configure the Translation Table Base register; or ensure all masters are in the bypass status or the status without sending a bus command (such as reset)</p>

3.13.6.3 0x0030 IOMMU Bypass Register (Default Value: 0x0000_007F)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	<p>MASTER6_BYPASS Master6 bypass switch After bypass function is opened, IOMMU cannot map the address of Master6 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>
5	R/W	0x1	<p>MASTER5_BYPASS After bypass function is opened, IOMMU cannot map the address of Master5 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>
4	R/W	0x1	<p>MASTER4_BYPASS Master4 bypass switch After bypass function is opened, IOMMU cannot map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x1	<p>MASTER3_BYPASS Master3 bypass switch After bypass function is opened, IOMMU cannot map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>
2	R/W	0x1	<p>MASTER2_BYPASS Master2 bypass switch After bypass function is opened, IOMMU cannot map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>
1	R/W	0x1	<p>MASTER1_BYPASS Master1 bypass switch After bypass function is opened, IOMMU cannot map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>
0	R/W	0x1	<p>MASTER0_BYPASS Master0 bypass switch After bypass function is opened, IOMMU cannot map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function</p>



Operating the register belongs to a non-accurate timing sequence control function. That is, before the function is valid, the master operation will complete the address mapping function. The operation after this will not perform the address mapping. It is suggested that the master is in the reset state or the status without sending a bus command before operating the register.

3.13.6.4 0x0040 IOMMU Auto Gating Register (Default Value: 0x0000_0001)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	IOMMU_AUTO_GATING IOMMU circuit auto gating control. The purpose is decreasing power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

3.13.6.5 0x0044 IOMMU Write Buffer Control Register (Default Value: 0x0000_007F)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	MASTER6_WBUF_CTRL Master6 write buffer control bit 0: Disable write buffer 1: Enable write buffer Note: the hardware does not have the configuration, this bit is invalid.
5	R/W	0x1	MASTER5_WBUF_CTRL Master5 write buffer control bit 0: Disable write buffer 1: Enable write buffer Note: the hardware does not have the configuration, this bit is invalid.
4	R/W	0x1	MASTER4_WBUF_CTRL Master4 write buffer control bit 0: Disable write buffer 1: Enable write buffer Note: the hardware does not have the configuration, this bit is invalid.
3	R/W	0x1	MASTER3_WBUF_CTRL Master3 write buffer control bit 0: Disable write buffer 1: Enable write buffer Note: the hardware does not have the configuration, this bit is invalid.

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x1	<p>MASTER2_WBUF_CTRL Master2 write buffer control bit 0: Disable write buffer 1: Enable write buffer</p> <p>Note: the hardware does not have the configuration, this bit is invalid.</p>
1	R/W	0x1	<p>MASTER1_WBUF_CTRL Master1 write buffer control bit 0: Disable write buffer 1: Enable write buffer</p> <p>Note: the hardware does not have the configuration, this bit is invalid.</p>
0	R/W	0x1	<p>MASTER0_WBUF_CTRL Master0 write buffer control bit 0: Disable write buffer 1: Enable write buffer</p> <p>Note: the hardware does not have the configuration, this bit is invalid.</p>

3.13.6.6 0x0048 IOMMU Out of Order Control Register (Default Value: 0x0000_007F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	<p>MASTER6_OOO_CTRL Master6 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order</p>
5	R/W	0x1	<p>MASTER5_OOO_CTRL Master5 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order</p>
4	R/W	0x1	<p>MASTER4_OOO_CTRL Master4 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order</p>
3	R/W	0x1	<p>MASTER3_OOO_CTRL Master3 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order</p>

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x1	MASTER2_OOO_CTRL Master2 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
1	R/W	0x1	MASTER1_OOO_CTRL Master1 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
0	R/W	0x1	MASTER0_OOO_CTRL Master0 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order

3.13.6.7 0x004C IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_007F)

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	MASTER6_4KB_BDY_PRT_CTRL Master6 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect Note: the hardware does not have the configuration, this bit is invalid.
5	R/W	0x1	MASTER5_4KB_BDY_PRT_CTRL Master5 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect Note: the hardware does not have the configuration, this bit is invalid.
4	R/W	0x1	MASTER4_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect Note: the hardware does not have the configuration, this bit is invalid.
3	R/W	0x1	MASTER3_4KB_BDY_PRT_CTRL Master3 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect Note: the hardware does not have the configuration, this bit is invalid.

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x1	MASTER2_4KB_BDY_PRT_CTRL Master2 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
1	R/W	0x1	MASTER1_4KB_BDY_PRT_CTRL Master1 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
0	R/W	0x1	MASTER0_4KB_BDY_PRT_CTRL Master0 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect



 **NOTE**

When the virtual address sent by master is over the 4KB boundary, the 4KB protection unit will split it into two serial accesses.

3.13.6.8 0x0050 IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: IOMMU_TTB_REG
Bit	Read/Write	Default/Hex	Description
31:14	R/W	0x0	TTB Level1 page table starting address, aligned to 16 KB. When operating the register, the IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0; Or the Bypass function of all masters is set to 1, or the Bypass function does not transfer the bus commands (such as setting).
13:0	/	/	/

3.13.6.9 0x0060 IOMMU TLB Enable Register (Default Value: 0x0003_007F)

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	PTW_CACHE_ENABLE PTW Cache enable bit. 0: Disable 1: Enable
16	R/W	0x1	MACRO_TLB_ENABLE Macro TLB enable bit 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	MICRO_TLB6_ENABLE Micro TLB6 enable bit 0: Disable 1: Enable
5	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable
3	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
1	R/W	0x1	MICRO_TLB1_ENABLE Micro TLB1 enable bit 0: Disable 1: Enable
0	R/W	0x1	MICRO_TLB0_ENABLE Micro TLB0 enable bit 0: Disable 1: Enable

3.13.6.10 0x0070 IOMMU TLB Pre-fetch Register (Default Value: 0x0003_0000)

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	PREFETCH_VALID_PAGE_TO_PC 0: Disabled 1: Enabled Note: If this function is enabled, the pre-fetch operation will not update the invalid level1 page table to the PTW Cache.
16	R/W	0x1	PREFETCH_VALID_PAGE_TO_TLB 0: Disabled 1: Enabled Note: If this function is enabled, the pre-fetch operation will not update the invalid level2 page table to TLB.
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_PREFETCH Micro TLB6 pre-fetch enable bit 0: Disabled 1: Enabled

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	MICRO_TLB5_PREFETCH Micro TLB5 pre-fetch enable bit 0: Disabled 1: Enabled
4	R/W	0x0	MICRO_TLB4_PREFETCH Micro TLB4 pre-fetch enable bit 0: Disabled 1: Enabled
3	R/W	0x0	MICRO_TLB3_PREFETCH Micro TLB3 pre-fetch enable bit 0: Disabled 1: Enabled
2	R/W	0x0	MICRO_TLB2_PREFETCH Micro TLB2 pre-fetch enable bit 0: Disabled 1: Enabled
1	R/W	0x0	MICRO_TLB1_PREFETCH Micro TLB1 pre-fetch enable bit 0: Disabled 1: Enabled
0	R/W	0x0	MICRO_TLB0_PREFETCH Micro TLB0 pre-fetch enable bit 0: Disabled 1: Enabled

3.13.6.11 0x0080 IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PTW_CACHE_FLUSH Clear PTW Cache 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
16	R/WAC	0x0	MACRO_TLB_FLUSH Clear Macro TLB 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
15:7	/	/	/
6	R/WAC	0x0	<p>MICRO_TLB6_FLUSH Clear Micro TLB6 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.</p>
5	R/WAC	0x0	<p>MICRO_TLB5_FLUSH Clear Micro TLB5 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.</p>
4	R/WAC	0x0	<p>MICRO_TLB4_FLUSH Clear Micro TLB4 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.</p>
3	R/WAC	0x0	<p>MICRO_TLB3_FLUSH Clear Micro TLB3 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.</p>
2	R/WAC	0x0	<p>MICRO_TLB2_FLUSH Clear Micro TLB2 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.</p>
1	R/WAC	0x0	<p>MICRO_TLB1_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.</p>

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	MICRO_TLBO_FLUSH Clear Micro TLBO 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.



When performing flush operation, all TLB/Cache access will be paused.

Before flush starts, the operation that has entered TLB continues to complete.

3.13.6.12 0x0084 IOMMU TLB Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TLB_IVLD_MODE_SEL 0: invalid TLB with Mask mode 1: invalid TLB with Start and End mode

3.13.6.13 0x0088 IOMMU TLB Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: IOMMU_TLB_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_STA_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.13.6.14 0x008C IOMMU TLB Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: IOMMU_TLB_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_END_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.13.6.15 0x0090 IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

Operation:

1. Set the virtual address which needs to be operated in IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090).
2. Set the mask of virtual address which needs to be operated in IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094).
3. Write '1' to IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098).
4. Read IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098), when it is '0', indicating that invalidation behavior is finished.

**NOTE**

Performing the invalidation operation does not affect the TLB/Cache operations.

There is no absolute relationship between operating the Invalidation and converting the same address.

3.13.6.16 0x0094 IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB invalid address mask register, 4KB aligned.
11:0	/	/	/

3.13.6.17 0x0098 IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	<p>TLB_IVLD_ENABLE Enable TLB invalid operation 0: No-operation or operation completed 1: Enable is invalid After the invalidation operation is completed, the bit can be cleared to 0 automatically.</p> <p>Note: Performing the invalidation operation does not affect the TLB/Cache operations. There is no absolute relationship between operating the Invalidation and converting the same address.</p>

3.13.6.18 0x009C IOMMU PC Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: IOMMU_PC_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	<p>PC_IVLD_MODE_SEL 0: Invalid PTW Cache using the default method 1: Invalid PTW Cache using the Start and End methods</p>

3.13.6.19 0x00A0 IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	<p>PC_IVLD_ADDR PTW Cache invalid address, 1 MB aligned.</p>
19:0	/	/	/

3.13.6.20 0x00A4 IOMMU PC Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: IOMMU_PC_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	<p>PC_IVLD_STA_ADDR PTW Cache invalid address, 1 MB aligned.</p>
19:0	/	/	/

3.13.6.21 0x00A8 IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: IOMMU_PC_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	<p>PC_IVLD_ENABLE Enable PTW Cache invalid operation 0: No-operation or operation completed 1: Enable is invalid</p> <p>After the invalidation operation is completed, the bit can be cleared to 0 automatically.</p> <p>Note: Performing the invalidation operation does not affect the TLB/Cache operations. There is no absolute relationship between operating the Invalidation and converting the same address.</p>

3.13.6.22 0x00AC IOMMU PC Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: IOMMU_PC_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_END_ADDR PTW Cache invalid address, 1 MB aligned.
19:0	/	/	/

3.13.6.23 0x00B0 IOMMU Domain Authority Control 0 Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	<p>DM1_M6_WT_AUT_CTRL Domain1 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation</p>
28	R/W	0x0	<p>DM1_M6_RD_AUT_CTRL Domain1 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation</p>
27	R/W	0x0	<p>DM1_M5_WT_AUT_CTRL Domain1 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation</p>

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	DM1_M5_RD_AUT_CTRL Domain1 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM1_M4_WT_AUT_CTRL Domain1 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM1_M4_RD_AUT_CTRL Domain1 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM1_M3_WT_AUT_CTRL Domain1 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM1_M3_RD_AUT_CTRL Domain1 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM1_M2_WT_AUT_CTRL Domain1 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM1_M2_RD_AUT_CTRL Domain1 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM1_M1_WT_AUT_CTRL Domain1 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM1_M1_RD_AUT_CTRL Domain1 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM1_M0_WT_AUT_CTRL Domain1 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DM1_M0_RD_AUT_CTRL Domain1 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R	0x0	DM0_M6_WT_AUT_CTRL Domain0 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R	0x0	DM0_M6_RD_AUT_CTRL Domain0 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R	0x0	DM0_M5_WT_AUT_CTRL Domain0 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R	0x0	DM0_M5_RD_AUT_CTRL Domain0 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R	0x0	DM0_M4_WT_AUT_CTRL Domain0 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R	0x0	DM0_M4_RD_AUT_CTRL Domain0 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R	0x0	DM0_M3_WT_AUT_CTRL Domain0 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R	0x0	DM0_M3_RD_AUT_CTRL Domain0 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R	0x0	DM0_M2_WT_AUT_CTRL Domain0 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	Read/Write	Default/Hex	Description
4	R	0x0	DM0_M2_RD_AUT_CTRL Domain0 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R	0x0	DM0_M1_WT_AUT_CTRL Domain0 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R	0x0	DM0_M1_RD_AUT_CTRL Domain0 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R	0x0	DM0_M0_WT_AUT_CTRL Domain0 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R	0x0	DM0_M0_RD_AUT_CTRL Domain0 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

 **NOTE**

- The software can be set up 15 different permission control types, which are set in IOMMU_DM_AUT_CTRL_REG0 ~ 7. The domain0 is a default access control type. The read/write operation of DOMIAN1 ~ 15 is unlimited by default.
- The software needs to set the corresponding permission control domain index of the page table item in the level2 page table entries[7:4]. The default value is 0. Using the domian0 does not control the read/write operation.
- Setting REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All Level2 page table types are covered by the type of REG_ARD_OVWT. The read/write operation is permitted by default.

3.13.6.24 0x00B4 IOMMU Domain Authority Control 1 Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM3_M6_WT_AUT_CTRL Domain3 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM3_M6_RD_AUT_CTRL Domain3 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM3_M5_WT_AUT_CTRL Domain3 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM3_M5_RD_AUT_CTRL Domain3 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM3_M4_WT_AUT_CTRL Domain3 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM3_M4_RD_AUT_CTRL Domain3 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM3_M3_WT_AUT_CTRL Domain3 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM3_M3_RD_AUT_CTRL Domain3 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM3_M2_WT_AUT_CTRL Domain3 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL1_REG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	DM3_M2_RD_AUT_CTRL Domain3 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM3_M1_WT_AUT_CTRL Domain3 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM3_M1_RD_AUT_CTRL Domain3 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM3_M0_WT_AUT_CTRL Domain3 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM3_M0_RD_AUT_CTRL Domain3 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM2_M6_WT_AUT_CTRL Domain2 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM2_M6_RD_AUT_CTRL Domain2 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM2_M5_WT_AUT_CTRL Domain2 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM2_M5_RD_AUT_CTRL Domain2 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM2_M4_WT_AUT_CTRL Domain2 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL1_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	DM2_M4_RD_AUT_CTRL Domain2 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM2_M3_WT_AUT_CTRL Domain2 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM2_M3_RD_AUT_CTRL Domain2 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM2_M2_WT_AUT_CTRL Domain2 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM2_M2_RD_AUT_CTRL Domain2 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM2_M1_WT_AUT_CTRL Domain2 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM2_M1_RD_AUT_CTRL Domain2 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM2_M0_WT_AUT_CTRL Domain2 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM2_M0_RD_AUT_CTRL Domain2 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.25 0x00B8 IOMMU Domain Authority Control 2 Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	Read/Write	Default/Hex	Description
29	R/W	0x0	DM5_M6_WT_AUT_CTRL Domain5 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM5_M6_RD_AUT_CTRL Domain5 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM5_M5_WT_AUT_CTRL Domain5 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM5_M5_RD_AUT_CTRL Domain5 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM5_M4_WT_AUT_CTRL Domain5 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM5_M4_RD_AUT_CTRL Domain5 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM5_M3_WT_AUT_CTRL Domain5 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM5_M3_RD_AUT_CTRL Domain5 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM5_M2_WT_AUT_CTRL Domain5 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM5_M2_RD_AUT_CTRL Domain5 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	DM5_M1_WT_AUT_CTRL Domain5 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM5_M1_RD_AUT_CTRL Domain5 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM5_M0_WT_AUT_CTRL Domain5 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM5_M0_RD_AUT_CTRL Domain5 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM4_M6_WT_AUT_CTRL Domain4 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM4_M6_RD_AUT_CTRL Domain4 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM4_M5_WT_AUT_CTRL Domain4 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM4_M5_RD_AUT_CTRL Domain4 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM4_M4_WT_AUT_CTRL Domain4 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM4_M4_RD_AUT_CTRL Domain4 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	DM4_M3_WT_AUT_CTRL Domain4 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM4_M3_RD_AUT_CTRL Domain4 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM4_M2_WT_AUT_CTRL Domain4 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM4_M2_RD_AUT_CTRL Domain4 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM4_M1_WT_AUT_CTRL Domain4 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM4_M1_RD_AUT_CTRL Domain4 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM4_M0_WT_AUT_CTRL Domain4 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM4_M0_RD_AUT_CTRL Domain4 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.26 0x00BC IOMMU Domain Authority Control 3 Register (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM7_M6_WT_AUT_CTRL Domain7 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	DM7_M6_RD_AUT_CTRL Domain7 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM7_M5_WT_AUT_CTRL Domain7 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM7_M5_RD_AUT_CTRL Domain7 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM7_M4_WT_AUT_CTRL Domain7 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM7_M4_RD_AUT_CTRL Domain7 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM7_M3_WT_AUT_CTRL Domain7 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM7_M3_RD_AUT_CTRL Domain7 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM7_M2_WT_AUT_CTRL Domain7 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM7_M2_RD_AUT_CTRL Domain7 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM7_M1_WT_AUT_CTRL Domain7 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	DM7_M1_RD_AUT_CTRL Domain7 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM7_M0_WT_AUT_CTRL Domain7 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM7_M0_RD_AUT_CTRL Domain7 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM6_M6_WT_AUT_CTRL Domain6 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM6_M6_RD_AUT_CTRL Domain6 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM6_M5_WT_AUT_CTRL Domain6 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM6_M5_RD_AUT_CTRL Domain6 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM6_M4_WT_AUT_CTRL Domain6 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM6_M4_RD_AUT_CTRL Domain6 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM6_M3_WT_AUT_CTRL Domain6 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	DM6_M3_RD_AUT_CTRL Domain6 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM6_M2_WT_AUT_CTRL Domain6 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM6_M2_RD_AUT_CTRL Domain6 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM6_M1_WT_AUT_CTRL Domain6 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM6_M1_RD_AUT_CTRL Domain6 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM6_M0_WT_AUT_CTRL Domain6 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM6_M0_RD_AUT_CTRL Domain6 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.27 0x00C0 IOMMU Domain Authority Control 4 Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM9_M6_WT_AUT_CTRL Domain9 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM9_M6_RD_AUT_CTRL Domain9 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	Read/Write	Default/Hex	Description
27	R/W	0x0	DM9_M5_WT_AUT_CTRL Domain9 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM9_M5_RD_AUT_CTRL Domain9 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM9_M4_WT_AUT_CTRL Domain9 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM9_M4_RD_AUT_CTRL Domain9 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM9_M3_WT_AUT_CTRL Domain9 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM9_M3_RD_AUT_CTRL Domain9 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM9_M2_WT_AUT_CTRL Domain9 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM9_M2_RD_AUT_CTRL Domain9 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM9_M1_WT_AUT_CTRL Domain9 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM9_M1_RD_AUT_CTRL Domain9 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	DM9_M0_WT_AUT_CTRL Domain9 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM9_M0_RD_AUT_CTRL Domain9 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM8_M6_WT_AUT_CTRL Domain8 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM8_M6_RD_AUT_CTRL Domain8 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM8_M5_WT_AUT_CTRL Domain8 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM8_M5_RD_AUT_CTRL Domain8 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM8_M4_WT_AUT_CTRL Domain8 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM8_M4_RD_AUT_CTRL Domain8 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM8_M3_WT_AUT_CTRL Domain8 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM8_M3_RD_AUT_CTRL Domain8 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	DM8_M2_WT_AUT_CTRL Domain8 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM8_M2_RD_AUT_CTRL Domain8 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM8_M1_WT_AUT_CTRL Domain8 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM8_M1_RD_AUT_CTRL Domain8 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM8_M0_WT_AUT_CTRL Domain8 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM8_M0_RD_AUT_CTRL Domain8 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.28 0x00C4 IOMMU Domain Authority Control 5 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM11_M6_WT_AUT_CTRL Domain11 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM11_M6_RD_AUT_CTRL Domain11 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM11_M5_WT_AUT_CTRL Domain11 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	DM11_M5_RD_AUT_CTRL Domain11 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM11_M4_WT_AUT_CTRL Domain11 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM11_M4_RD_AUT_CTRL Domain11 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM11_M3_WT_AUT_CTRL Domain11 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM11_M3_RD_AUT_CTRL Domain11 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM11_M2_WT_AUT_CTRL Domain11 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM11_M2_RD_AUT_CTRL Domain11 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM11_M1_WT_AUT_CTRL Domain11 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM11_M1_RD_AUT_CTRL Domain11 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM11_M0_WT_AUT_CTRL Domain11 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DM11_M0_RD_AUT_CTRL Domain11 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM10_M6_WT_AUT_CTRL Domain10 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM10_M6_RD_AUT_CTRL Domain10 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM10_M5_WT_AUT_CTRL Domain10 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM10_M5_RD_AUT_CTRL Domain10 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM10_M4_WT_AUT_CTRL Domain10 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM10_M4_RD_AUT_CTRL Domain10 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM10_M3_WT_AUT_CTRL Domain10 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM10_M3_RD_AUT_CTRL Domain10 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM10_M2_WT_AUT_CTRL Domain10 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	DM10_M2_RD_AUT_CTRL Domain10 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM10_M1_WT_AUT_CTRL Domain10 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM10_M1_RD_AUT_CTRL Domain10 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM10_M0_WT_AUT_CTRL Domain10 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM10_M0_RD_AUT_CTRL Domain10 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.29 0x00C8 IOMMU Domain Authority Control 6 Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM13_M6_WT_AUT_CTRL Domain13 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM13_M6_RD_AUT_CTRL Domain13 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM13_M5_WT_AUT_CTRL Domain13 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM13_M5_RD_AUT_CTRL Domain13 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	Read/Write	Default/Hex	Description
25	R/W	0x0	DM13_M4_WT_AUT_CTRL Domain13 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM13_M4_RD_AUT_CTRL Domain13 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM13_M3_WT_AUT_CTRL Domain13 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM13_M3_RD_AUT_CTRL Domain13 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM13_M2_WT_AUT_CTRL Domain13 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM13_M2_RD_AUT_CTRL Domain13 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM13_M1_WT_AUT_CTRL Domain13 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM13_M1_RD_AUT_CTRL Domain13 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM13_M0_WT_AUT_CTRL Domain13 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM13_M0_RD_AUT_CTRL Domain13 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	DM12_M6_WT_AUT_CTRL Domain12 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM12_M6_RD_AUT_CTRL Domain12 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM12_M5_WT_AUT_CTRL Domain12 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM12_M5_RD_AUT_CTRL Domain12 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM12_M4_WT_AUT_CTRL Domain12 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM12_M4_RD_AUT_CTRL Domain12 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM12_M3_WT_AUT_CTRL Domain12 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM12_M3_RD_AUT_CTRL Domain12 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM12_M2_WT_AUT_CTRL Domain12 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM12_M2_RD_AUT_CTRL Domain12 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	DM12_M1_WT_AUT_CTRL Domain12 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM12_M1_RD_AUT_CTRL Domain12 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM12_M0_WT_AUT_CTRL Domain12 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM12_M0_RD_AUT_CTRL Domain12 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.30 0x00CC IOMMU Domain Authority Control 7 Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM15_M6_WT_AUT_CTRL Domain15 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM15_M6_RD_AUT_CTRL Domain15 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM15_M5_WT_AUT_CTRL Domain15 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM15_M5_RD_AUT_CTRL Domain15 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM15_M4_WT_AUT_CTRL Domain15 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	DM15_M4_RD_AUT_CTRL Domain15 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM15_M3_WT_AUT_CTRL Domain15 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM15_M3_RD_AUT_CTRL Domain15 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM15_M2_WT_AUT_CTRL Domain15 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM15_M2_RD_AUT_CTRL Domain15 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM15_M1_WT_AUT_CTRL Domain15 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM15_M1_RD_AUT_CTRL Domain15 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM15_M0_WT_AUT_CTRL Domain15 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM15_M0_RD_AUT_CTRL Domain15 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM14_M6_WT_AUT_CTRL Domain14 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	DM14_M6_RD_AUT_CTRL Domain14 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM14_M5_WT_AUT_CTRL Domain14 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM14_M5_RD_AUT_CTRL Domain14 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM14_M4_WT_AUT_CTRL Domain14 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM14_M4_RD_AUT_CTRL Domain14 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM14_M3_WT_AUT_CTRL Domain14 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM14_M3_RD_AUT_CTRL Domain14 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM14_M2_WT_AUT_CTRL Domain14 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM14_M2_RD_AUT_CTRL Domain14 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM14_M1_WT_AUT_CTRL Domain14 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	DM14_M1_RD_AUT_CTRL Domain14 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM14_M0_WT_AUT_CTRL Domain14 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM14_M0_RD_AUT_CTRL Domain14 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.31 0x00D0 IOMMU Domain Authority Overwrite Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DM_AUT_OVWT_ENABLE Domain write/read authority overwrite enable 0: Disabled 1: Enabled
30:14	/	/	/
13	R/W	0x0	M6_WT_AUT_OVWT_CTRL Master6 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	M6_RD_AUT_OVWT_CTRL Master6 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	M5_WT_AUT_OVWT_CTRL Master5 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	M5_RD_AUT_OVWT_CTRL Master5 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	M4_WT_AUT_OVWT_CTRL Master4 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	M4_RD_AUT_OVWT_CTRL Master4 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	M3_WT_AUT_OVWT_CTRL Master3 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	M3_RD_AUT_OVWT_CTRL Master3 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	M2_WT_AUT_OVWT_CTRL Master2 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	M2_RD_AUT_OVWT_CTRL Master2 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	M1_WT_AUT_OVWT_CTRL Master1 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	M1_RD_AUT_OVWT_CTRL Master1 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	M0_WT_AUT_OVWT_CTRL Master0 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	M0_RD_AUT_OVWT_CTRL Master0 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation

 NOTE

Setting the REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All the property of Level2 are covered by the property defined in REG_ARD_OVWT. Allow read and write for all by default.

3.13.6.32 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	DBG_PF_L2_PAGE_TABLE_INVALID_EN Debug or Prefetch, the interrupt enable bit for fetching the invalid level1 page table in TLB. 0: Masks interrupt 1: Enables interrupt
19	R/W	0x0	DBG_PF_PC_L1_PAGE_TABLE_INVALID_EN Debug or Prefetch is hit, the interrupt enable bit for fetching the invalid level1 page table in PTW Cache. 0: Masks interrupt 1: Enables interrupt
18	R/W	0x0	DBG_PF_DRAM_L1_PAGE_TABLE_INVALID_EN Debug or Prefetch is not hit, the interrupt enable bit for fetching the invalid level1 page table in DRAM. 0: Masks interrupt 1: Enables interrupt
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN Micro TLB6 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt

 **NOTE**

- Due to the invalid page table and authority errors, one or more devices in the system will not work properly.
- The authority error usually occurs in Micro TLB. This error generates the interrupt, and waits for the software processing.
- While the invalid page table usually occurs in Macro TLB. This error does not affect the access of other devices. So the error page table needs to be returned in the same way, but it should not be written into TLB at all levels.

3.13.6.33 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt

3.13.6.34 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs

3.13.6.35 0x0110 IOMMU Interrupt Error Address 0 Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR0 The virtual address, it makes Micro TLB0 be interrupted

3.13.6.36 0x0114 IOMMU Interrupt Error Address 1 Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR1 The virtual address, it makes Micro TLB1 be interrupted

3.13.6.37 0x0118 IOMMU Interrupt Error Address 2 Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR2 The virtual address, it makes Micro TLB2 be interrupted

3.13.6.38 0x011C IOMMU Interrupt Error Address 3 Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR3 The virtual address, it makes Micro TLB3 be interrupted

3.13.6.39 0x0120 IOMMU Interrupt Error Address 4 Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR4 The virtual address, it makes Micro TLB4 be interrupted

3.13.6.40 0x0124 IOMMU Interrupt Error Address 5 Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR5 The virtual address, it makes Micro TLB5 be interrupted

3.13.6.41 0x0128 IOMMU Interrupt Error Address 6 Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR6 The virtual address, it makes Micro TLB6 be interrupted

3.13.6.42 0x0130 IOMMU Interrupt Error Address 7 Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR7 The virtual address, it makes L1 page table be interrupted

3.13.6.43 0x0134 IOMMU Interrupt Error Address 8 Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR_REG8
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR8 The virtual address, it makes L2 page table be interrupted

3.13.6.44 0x0150 IOMMU Interrupt Error Data 0 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA0 The corresponding page table of the virtual address that made Micro TLB0 be interrupted

3.13.6.45 0x0154 IOMMU Interrupt Error Data 1 Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA1 The corresponding page table of the virtual address that made Micro TLB1 be interrupted

3.13.6.46 0x0158 IOMMU Interrupt Error Data 2 Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA2 The corresponding page table of the virtual address that made Micro TLB2 be interrupted

3.13.6.47 0x015C IOMMU Interrupt Error Data 3 Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA3 The corresponding page table of the virtual address that made Micro TLB3 be interrupted

3.13.6.48 0x0160 IOMMU Interrupt Error Data 4 Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA4 The corresponding page table of the virtual address that made Micro TLB4 be interrupted

3.13.6.49 0x0164 IOMMU Interrupt Error Data 5 Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA5 The corresponding page table of the virtual address that made Micro TLB5 be interrupted

3.13.6.50 0x0168 IOMMU Interrupt Error Data 6 Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA6 The corresponding page table of the virtual address that made Micro TLB6 be interrupted

3.13.6.51 0x0170 IOMMU Interrupt Error Data 7 Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA7 The corresponding page table of the virtual address that made L1 page table be interrupted

3.13.6.52 0x0174 IOMMU Interrupt Error Data 8 Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA8 The corresponding page table of the virtual address that made L2 page table be interrupted

3.13.6.53 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L1PG_INT L1 page table interrupted caused by the Debug Mode address translation.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT L1 page table interrupted caused by the Master6 address translation.
5	R	0x0	MASTER5_L1PG_INT L1 page table interrupted caused by the Master5 address translation.
4	R	0x0	MASTER4_L1PG_INT L1 page table interrupted caused by the Master4 address translation.
3	R	0x0	MASTER3_L1PG_INT L1 page table interrupted caused by the Master3 address translation.
2	R	0x0	MASTER2_L1PG_INT L1 page table interrupted caused by the Master2 address translation.
1	R	0x0	MASTER1_L1PG_INT L1 page table interrupted caused by the Master1 address translation.

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	MASTER0_L1PG_INT L1 page table interrupted caused by the Master0 address translation.

3.13.6.54 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L2PG_INT L2 page table interrupted caused by the Debug Mode address translation.
30:7	/	/	/
6	R	0x0	MASTER6_L2PG_INT L2 page table interrupted caused by the Master6 address translation.
5	R	0x0	MASTER5_L2PG_INT L2 page table interrupted caused by the Master5 address translation.
4	R	0x0	MASTER4_L2PG_INT L2 page table interrupted caused by the Master4 address translation.
3	R	0x0	MASTER3_L2PG_INT L2 page table interrupted caused by the Master3 address translation.
2	R	0x0	MASTER2_L2PG_INT L2 page table interrupted caused by the Master2 address translation.
1	R	0x0	MASTER1_L2PG_INT L2 page table interrupted caused by the Master1 address translation.
0	R	0x0	MASTER0_L2PG_INT L2 page table interrupted caused by the Master0 address translation.

3.13.6.55 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA Read/write virtual address

3.13.6.56 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA_DATA Data of read/write virtual address

3.13.6.57 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MODE_ESL 0: Prefetch 1: Debug Mode It is used to choose the prefetch mode or the debug mode.
30:9	/	/	/
8	R/W	0x0	VA_CONFIG 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation completes 1: Start After the operation completes, the bit can be cleared to 0 automatically.

Read operation process:

1. Write IOMMU_VA_REG[31:0];
2. Write IOMMU_VA_CONFIG_REG[8] to 0;
3. Write IOMMU_VA_CONFIG_REG[0] to 1 to start the read-process;
4. Query IOMMU_VA_CONFIG_REG[0] until it is 0;
5. Read IOMMU_VA_DATA_REG[31:0];

Write operation process:

1. Write IOMMU_VA_REG[31:0];
2. Write IOMMU_VA_DATA_REG[31:0];
3. Write IOMMU_VA_CONFIG_REG[8] to 1;
4. Write IOMMU_VA_CONFIG_REG[0] to 1 to start the read-process;
5. Query IOMMU_VA_CONFIG_REG[0] until it is 0.

3.13.6.58 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disables statistical function 1: Enables statistical function

3.13.6.59 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation completes 1: Clears the counter data After the operation completes, the bit can be cleared to 0 automatically.

3.13.6.60 0x0230 IOMMU PMU Access Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW0 Record the total number of Micro TLB0 access, lower 32-bit register.

3.13.6.61 0x0234 IOMMU PMU Access High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record the total number of Micro TLB0 access, higher 11-bit register.

3.13.6.62 0x0238 IOMMU PMU Hit Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW0 Record the total number of Micro TLB0 hit, lower 32-bit register.

3.13.6.63 0x023C IOMMU PMU Hit High 0 Register (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record the total number of Micro TLB0 hit, higher 11-bit register.

3.13.6.64 0x0240 IOMMU PMU Access Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW1 Record the total number of Micro TLB1 access, lower 32-bit register.

3.13.6.65 0x0244 IOMMU PMU Access High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record the total number of Micro TLB1 access, higher 11-bit register.

3.13.6.66 0x0248 IOMMU PMU Hit Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW1 Record the total number of Micro TLB1 hit, lower 32-bit register.

3.13.6.67 0x024C IOMMU PMU Hit High 1 Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record the total number of Micro TLB1 hit, higher 11-bit register.

3.13.6.68 0x0250 IOMMU PMU Access Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW2 Record the total number of Micro TLB2 access, lower 32-bit register.

3.13.6.69 0x0254 IOMMU PMU Access High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record the total number of Micro TLB2 access, higher 11-bit register.

3.13.6.70 0x0258 IOMMU PMU Hit Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW2 Record the total number of Micro TLB2 hit, lower 32-bit register.

3.13.6.71 0x025C IOMMU PMU Hit High 2 Register (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record the total number of Micro TLB2 hit, higher 11-bit register.

3.13.6.72 0x0260 IOMMU PMU Access Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW3 Record the total number of Micro TLB3 access, lower 32-bit register.

3.13.6.73 0x0264 IOMMU PMU Access High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record the total number of Micro TLB3 access, higher 11-bit register.

3.13.6.74 0x0268 IOMMU PMU Hit Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW3 Record the total number of Micro TLB3 hit, lower 32-bit register.

3.13.6.75 0x026C IOMMU PMU Hit High 3 Register (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record the total number of Micro TLB3 hit, higher 11-bit register.

3.13.6.76 0x0270 IOMMU PMU Access Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW4 Record the total number of Micro TLB4 access, lower 32-bit register.

3.13.6.77 0x0274 IOMMU PMU Access High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record the total number of Micro TLB4 access, higher 11-bit register.

3.13.6.78 0x0278 IOMMU PMU Hit Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW4 Record the total number of Micro TLB4 hit, lower 32-bit register.

3.13.6.79 0x027C IOMMU PMU Hit High 4 Register (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record the total number of Micro TLB4 hit, higher 11-bit register.

3.13.6.80 0x0280 IOMMU PMU Access Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW5 Record the total number of Micro TLB5 access, lower 32-bit register.

3.13.6.81 0x0284 IOMMU PMU Access High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record the total number of Micro TLB5 access, higher 11-bit register.

3.13.6.82 0x0288 IOMMU PMU Hit Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW5 Record the total number of Micro TLB5 hit, lower 32-bit register.

3.13.6.83 0x028C IOMMU PMU Hit High 5 Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record the total number of Micro TLB5 hit, higher 11-bit register.

3.13.6.84 0x0290 IOMMU PMU Access Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW6 Record the total number of Micro TLB6 access, lower 32-bit register.

3.13.6.85 0x0294 IOMMU PMU Access High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record the total number of Micro TLB6 access, higher 11-bit register.

3.13.6.86 0x0298 IOMMU PMU Hit Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW6 Record the total number of Micro TLB6 hit, lower 32-bit register.

3.13.6.87 0x029C IOMMU PMU Hit High 6 Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record the total number of Micro TLB6 hit, higher 11-bit register.

3.13.6.88 0x02D0 IOMMU PMU Access Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW7 Record the total number of Macro TLB access, lower 32-bit register.

3.13.6.89 0x02D4 IOMMU PMU Access High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record the total number of Macro TLB access, higher 11-bit register.

3.13.6.90 0x02D8 IOMMU PMU Hit Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW7 Record the total number of Macro TLB hit, lower 32-bit register.

3.13.6.91 0x02DC IOMMU PMU Hit High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record the total number of Macro TLB hit, higher 11-bit register.

3.13.6.92 0x02E0 IOMMU PMU Access Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW8 Record the total number of PTW Cache access, lower 32-bit register.

3.13.6.93 0x02E4 IOMMU PMU Access High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH8 Record the total number of PTW Cache access, higher 11-bit register.

3.13.6.94 0x02E8 IOMMU PMU Hit Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW8 Record the total number of PTW Cache hit, lower 32-bit register.

3.13.6.95 0x02EC IOMMU PMU Hit High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record the total number of PTW Cache hit, higher 11-bit register.

3.13.6.96 0x0300 IOMMU Total Latency Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW0 Record the total latencies of Master0, lower 32-bit register.

3.13.6.97 0x0304 IOMMU Total Latency High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record the total latencies of Master0, higher 18-bit register.

3.13.6.98 0x0308 IOMMU Max Latency 0 Register (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML0 Record the maximum latency of Master0.

3.13.6.99 0x0310 IOMMU Total Latency Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW1 Record the total latencies of Master1, lower 32-bit register.

3.13.6.100 0x0314 IOMMU Total Latency High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record the total latencies of Master1, higher 18-bit register.

3.13.6.101 0x0318 IOMMU Max Latency 1 Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML1 Record the maximum latency of Master1.

3.13.6.102 0x0320 IOMMU Total Latency Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW2 Record the total latencies of Master2, lower 32-bit register.

3.13.6.103 0x0324 IOMMU Total Latency High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record the total latencies of Master2, higher 18-bit register.

3.13.6.104 0x0328 IOMMU Max Latency 2 Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML2 Record the maximum latency of Master2.

3.13.6.105 0x0330 IOMMU Total Latency Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW3 Record the total latencies of Master3, lower 32-bit register.

3.13.6.106 0x0334 IOMMU Total Latency High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record the total latencies of Master3, higher 18-bit register.

3.13.6.107 0x0338 IOMMU Max Latency 3 Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML3 Record the maximum latency of Master3.

3.13.6.108 0x0340 IOMMU Total Latency Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW4 Record the total latencies of Master4, lower 32-bit register.

3.13.6.109 0x0344 IOMMU Total Latency High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record the total latencies of Master4, higher 18-bit register.

3.13.6.110 0x0348 IOMMU Max Latency 4 Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML4 Record the maximum latency of Master4.

3.13.6.111 0x0350 IOMMU Total Latency Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW5 Record the total latencies of Master5, lower 32-bit register.

3.13.6.112 0x0354 IOMMU Total Latency High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
17:0	R	0x0	PMU_TL_HIGH5 Record the total latencies of Master5, higher 18-bit register.

3.13.6.113 0x0358 IOMMU Max Latency 5 Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML5 Record the maximum latency of Master5.

3.13.6.114 0x0360 IOMMU Total Latency Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW6 Record the total latencies of Master6, lower 32-bit register.

3.13.6.115 0x0364 IOMMU Total Latency High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record the total latencies of Master6, higher 18-bit register.

3.13.6.116 0x0368 IOMMU Max Latency 6 Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: IOMMU_PMU_ML6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML6 Record the maximum latency of Master6.

3.14 RTC

3.14.1 Overview

The Real Time Clock (RTC) is used to implement time counter and timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing the power-off information
- Multiple special registers for recording the BROM information
- Supports PMC and external PMU
 - Supports power-on, wake-up, and interrupt through PWR-ON keypress, VBUS insertion, or IRQ pin interrupt
 - Supports interrupt only, restart and forced power-off through long PWR-ON keypress
 - Supports power-on and wake-up through alarm
 - Supports restart, system reset, and global reset through watchdog
 - Power-on source record, power-off source record, and abnormal power-off record
 - Configurable power-on and power-off sequence
 - Configurable power status in standby state

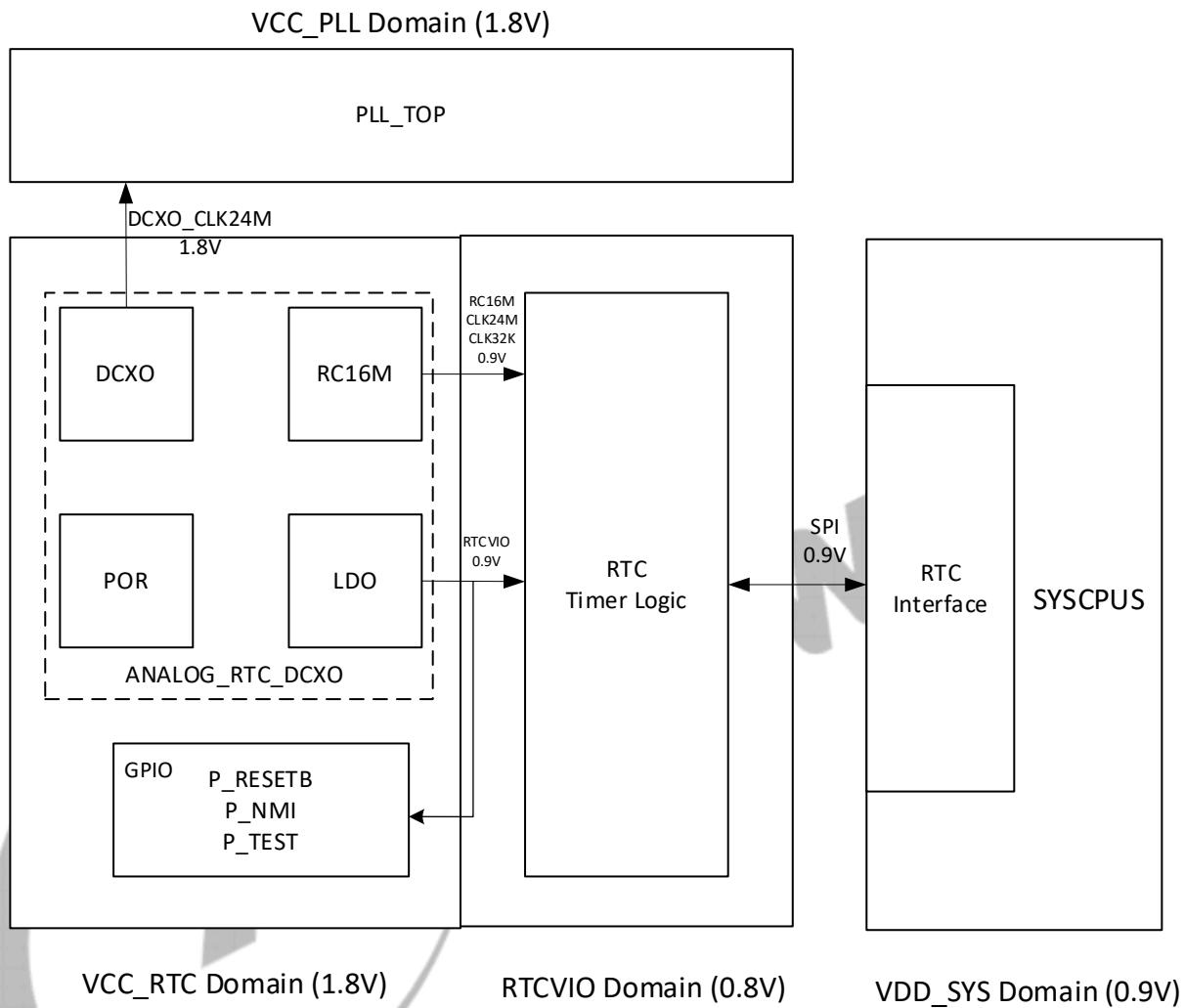


The register configuration of RTC is AHB bus, it only can support word operation, not byte operation and half-word operation.

3.14.2 Block Diagram

The following figure shows the block diagram of the RTC.

Figure 3-41 RTC Block Diagram



3.14.3 Functional Description

3.14.3.1 External Signals

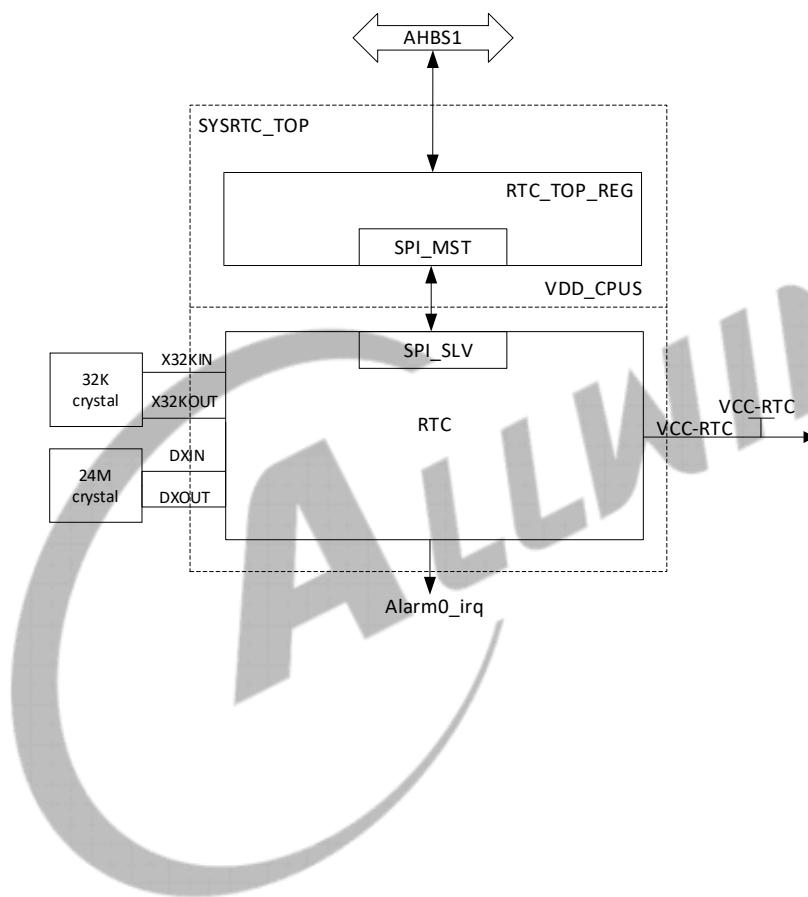
Table 3-18 RTC External Signals

Signal	Description	Type
X32KIN	32.768 kHz oscillator input	I
X32KOUT	32.768 kHz oscillator output	O
DXIN	24MHz oscillator input	I
DXOUT	24MHz oscillator output	O
VCC-RTC	RTC high voltage, generated via external power	IO
GND	Ground	IO
NMI	Non-maskable Interrupt	I

Signal	Description	Type
RESET	Reset Signal (low active)	I
PWRON	Power-on Keypress Input	I
PWR-STARTUP	VBUS Insertion detection	I
PWR-EN[2:0]	LDO/DCDC Enable	O
PMC-BYP	PMC Bypass Control	I

3.14.3.2 Typical Application

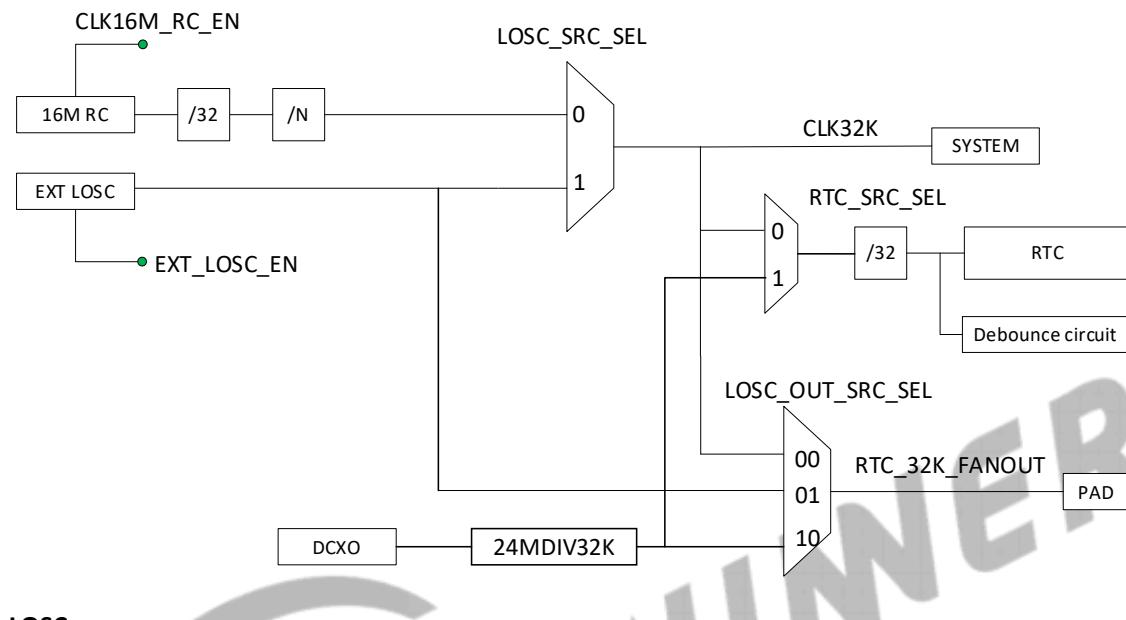
Figure 3-42 RTC Application Diagram



3.14.3.3 Clock Tree

The following figure shows the clock tree of the RTC.

Figure 3-43 RTC Clock Tree



LOSC

The LOSC has 2 clock sources: internal RC, external low frequency crystal. The LOSC selects the internal RC by default, when the system starts, the LOSC can select by software the external low frequency crystal to provide much accuracy clock. The clock accurate of the LOSC is related to the accurate of the external low frequency crystal. Usually select 32.768 kHz crystal with ± 20 ppm frequency tolerance. When using internal RC, the clock can be changed by changing division ratio. When using external clock, the clock cannot be changed.

RTC

The clock sources of RTC can be selected by related switches, including 32K divided by internal 16 MHz RC, 32K divided by external DCXO, and external 32.768 kHz crystal.

System 32K

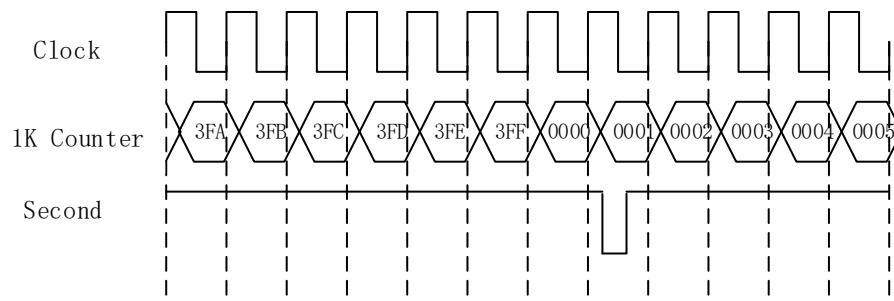
The clock sources of system 32K are from external 32.768 kHz crystal and 32K divided by the internal 16 MHz RC.

RTC_32K_FANOUT

The clock source of RTC_32K_FANOUT can select CLK32K, external 32.768 kHz crystal or 32K divided by external DCXO.

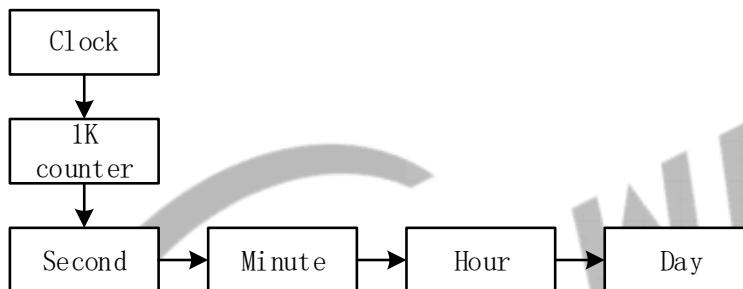
3.14.3.4 Real Time Clock

Figure 3-44 RTC Counter



The 1K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1K counter starts to count again from 0, and the second counter adds 1. The step structure of 1 kHz counter is as follows.

Figure 3-45 RTC 1 kHz Counter Step Structure



According to above implementation, the changing range of each counter is as follows.

Table 3-19 RTC Counter Changing Range

Counter	Range
Second	0 to 59
Minute	0 to 59
Hour	0 to 23
Day	0 to 65535 (The year, month, day need be transformed by software according to day counter)



CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

3.14.3.5 Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC need set a new scheduled time, the next interrupt can be generated.

3.14.3.6 Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.14.3.7 VDD-RTC

The RTC module has a LDO, the input source of the LDO is VCC_RTC, the output of the LDO is RTC_VIO, the value of RTC_VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

3.14.3.8 Power Management Controller (PMC)

Power-on/Wake-up Source

- PWR-ON key
 - In power-off state, PMC power-on is triggered after the PWR-ON key is pressed for longer than 256ms by default. You can configure the time to 128ms, 512ms, 1s, or 2s as well.
 - In standby state, PMC is woken up by a PWR-ON key interrupt. Refer to the Interrupt of this section for details.
 - In normal or standby state, PMC forced power-off (default configuration) or restart is triggered by pressing the PWR-ON key for 8s by default. You can configure the time to 6s, 8s, or 16s, and the triggering outcome to interrupt generation only, or a forced restart or power-off.
 - A debounce time of two 32 KHz clock cycles is set for the PWR-ON key. Electrical level shorter than the two cycles will be ignored.
- VBUS insertion (power state pin)

In power-off/standby state, detect the duration of the high electrical level triggered by the VBUS insertion. If the high electrical level maintains longer than 256ms (default time), PMC power-on or wake-up is triggered. You can configure the detection duration to 16ms, 32ms, 64ms, 128ms, 256ms, or 512ms.
- IRQ pin interrupt
 - After the initial power-on, you can configure the IRQ pin interrupt as the power-on/wake-up source.

- A lower electrical level triggers the interrupt which triggers power-on/wake-up in turn. The interrupt is triggered if the IRQ key is pressed for longer than the interrupt recognition threshold. The threshold is 16ms by default, and you can configure it to 4ms, 8ms, or 16ms as well.
 - A debounce time of two 32 KHz clock cycles is set for the IRQ pin. Electrical level shorter than the two cycles will be ignored.
- RTC alarm interrupt
- PMC can be powered on/woken up by an interrupt generated by the RTC internal alarm. You need to enable this function after the initial PMC power-on.
- From power-off to power-on, a low electrical level is maintained for reset. First, enable the power controller, and detect whether the power-on process completes by VCC_IO and VCC_SYS. (The VCC_IO power detection function is disabled by default at the initial power-on and needs to be enabled after that). After power-on completed, the reset low electrical level will be maintained for some time more, and then reset will be released. This time duration is configurable. The default value is 8ms, and you can configure it to 4ms, 8ms, 16ms, 32ms, or 64ms as well.
 - After the release from global reset controlled by PMC, DCXO is enabled and a release delay of some time is set on global reset. This time duration is configurable. The default value is 4ms, and you can configure it to 1ms, 2ms, 3ms, or 4ms as well.

**NOTE**

For the initial power-on, only the PWR-ON key or VBUS insertion can realize PMC power-on or wake-up. The RTC alarm interrupt pin and IRQ interrupt pin need to be configured on registers.

Some related register configurations are as follows.

Table 3-20 power-on event configurations

Function	Register	Remarks
PWR-ON keypress delay selection	PMC_DLY_CTRL_REG[7:5]	The keypress delay can be configured to 128ms, 256ms (default), 512ms, 1s, or 2s.
High level duration detection after VBUS insertion	PMC_DLY_CTRL_REG[2:0]	The high level duration can be configured to 16ms, 32ms, 64ms, 128ms, 256ms (default), or 512ms.
Interval selection between power-on and power-off	RST_DLY_SEL_REG[6:4]	The interval can be configured to 1ms (default), 2ms, 8ms, or 16ms.
Power-on and off sequence	SW_CFG_REG[11:9]	
Enabling of VCC_IO power detection	VDD_OFF_GATING_CTRL_REG[0]	

Function	Register	Remarks
Configuration of PMC status after VCC_IO is powered off	PMC_CTRL_EN_REG[5]	
Power-on reset time delay selection	RST_DLY_SEL_REG[6:4]	The reset time delay can be configured to 4ms, 8ms (default), 16ms, 32ms, or 64ms.
Power-on reset delay status	PMC_STATUS_REG[7]	This register is used to check whether there is a 64ms delay after the reset.
DCXO delay selection	RST_DLY_SEL_REG[1:0]	The DCXO delay can be configured to 1ms, 2ms, 3ms, or 4ms (default).
Configuration of IRQ as power-on and wake-up source	PMC_CTRL_EN_REG[1]	
Interrupt recognition time threshold selection	PMC_DLY_CTRL_REG[4:3]	The threshold time can be configured to 4ms, 8ms, or 16ms.
Configuration of RTC alarm as power-on/wake-up source	PMC_CTRL_EN_REG[2]	
Power-on source read	PMC_STATUS_REG[3:0]	

Standby/Wake-up

- The system can configure PMC to enter into the standby state. The difference between the standby state and power-off state is that the power en control of some powers can remain enabled in standby state. All interrupt sources are ignored when PMC is entering into the standby state.
- PMC can be woken up by PWR-ON key falling edge interrupt, VBUS insertion detection interrupt, IRQ pin interrupt, and RTC alarm interrupt. The wake-up processes and sequence and those of power-on are the same except that the power staying enabled in the standby state remains permanently enabled.

Some related register configurations are as follows.

Table 3-21 wake-up event configurations

Function	Register	Remarks
Functions for the PWR-ON key	PMC_CTRL_EN_REG[10:6]	PMC can be configured to be woken up by a falling edge (default), rising edge, short-keypress, long keypress, or super-long keypress.

Function	Register	Remarks
Options for long press threshold of the PWR-ON key interrupt	PMC_DLY_CTRL_REG[11:10]	
Configuration of VBUS insertion as wake-up source	PMC_CTRL_EN_REG[15]	
Configuration of IRQ interrupt as wake-up source	PMC_CTRL_EN_REG[1]	
Configuration of RTC alarm as power-on/wake-up source	PMC_CTRL_EN_REG[2]	
Configuration of USB interrupt as wake-up source	USB_STBY_CTRL_REG[4]	
Enabling of some powers in the standby state	SW_CFG_REG[8:6]	
Power-on source read	PMC_STATUS_REG[3:0]	

Power-off

- The system can configure PMC to perform the power-off process and switch to the power-off state via software.
- PMC can be force powered off by pressing the PWR-ON key for more than the power-off time threshold. By default, the threshold is 8s, and you can configure it to 6s, 8s, or 16s.
- PMC has the function of detecting the internal 3.3V and 0.9V powers. If the two powers are found to be disconnected, PMC instantly resets itself and lowers the electrical level, switches to the power-off state at the same time, and records the power-off source as abnormal power-off. This function is disabled by default and needs to be configured.
- PMC can be reset by the external reset key and after that, PMC returns to the power-off state and disables the external IRQ interrupt power-on function. After the external reset is cancelled, PMC will detect power-on source again and performs the next power-on action.
- After PMC is powered off, the power-off source will be recorded for future query.
- During power-off, PMC performs the global reset and lowers the electrical level, which triggers DCXO closing (configurable; closed by default) and power-off. During power-off, PMC does not detect VCC_IO or VDD_SYS, directly powers off according to the sequence, and waits for power-on incident in power-off state. All interrupt wake-up sources will be ignored during power-off.



NOTE

DCXO close function is disabled by default and needs to be configured.

Some related register configurations are as follows.

Table 3-22 power-off event configurations

Function	Register	Description
Configuration for software PMC status switch	SW_CFG_REG[0]	
Configuration for software PMC status switch	SW_CFG_REG[2:1]	PMC status can be configured as power-off, standby or restart.
Functions for the PWR-ON key super-long press	SW_CFG_REG[5:4]	The function of super-long keypress can be configured as power-off or restart.
Watchdog reset configuration function	SW_CFG_REG[3]	After the first power-on, PMC can be configured to restart when detecting a watchdog reset.
Functions for extra power-off record	PMC_CTRL_EN_REG [5]	
Power-on source read	PMC_STATUS_REG[6:4]	
Restart delay selection	PMC_CTRL_EN_REG[14:12]	

Interrupt

- After power-on, the PWR-ON key, VBUS detection, and IQR pin can all generate interrupts.
- For the PWR-ON key, a debounce time of 16ms is set and pressing it for more than 16ms generates an interrupt. The following table shows the five generated interrupts.

Table 3-23 PWE-ON key interrupts

Interrupt	Conditions	Remarks
Short-press interrupt	16ms<pressing duration<1.5s (default)	
Long-press interrupt	$\geq 1.5\text{s}$ (default)	The threshold for a long-press is 1.5s by default and can be configured to 1s, 2s, or 2.5s as well.
Super-long press interrupt	8s	The threshold for a super-long-press is 8s by default and can be configured to 6s or 16s as well.
Rising-edge interrupt	$>16\text{ms}$	
Falling-edge interrupt	16ms	

- VBUS detection

After VBUS is inserted, a rising-edge is detected. If the high electrical level remains for more than 256ms (default time), an insertion interrupt is generated. After VBUS is unplugged, a falling edge is detected and triggers the generation of an unplug interrupt instantly.

- IRQ pin

For IRQ interrupt, refer to the [IRQ pin](#) description this section.

Reset

- PMC supports internal and external reset. Global reset is controlled by the PMC module.
- PMC has two reset sources—POR of RTC and the external reset. For the first source, when RTC is powered on, a reset lasting 2 to 4ms will be generated to reset the PMC module. For the second one, the external reset will reset the PMC module when a debounce time of 1ms is surpassed. The PMC module turns to the power-off state after being reset and the system reset remains pulled down.
- The internal watchdog transfers the generated global reset signal to PMC, and after detecting the validity of the signal, PMC determines the next step between power-off and restart and system reset based on configurations. This function is disabled by default and needs to be enabled after power-on.
- The internal reset can choose whether to have an output. By default, no output is chosen. If an output is configured, PMC ignores the reset signal, the signal is returned by the reset pad and resets PMC after the 1ms debounce time, generating a global reset and cancelling the watch dog reset. The system returns to the power-off state.
- If the chip contains a PMC module, a reset pin is required; therefore, the reset input enable is enabled by default. If the chip does not contain a PMC module, the reset pin is not required; therefore, the reset input enable is disabled by default.

Power Control

- PMC controls LDO/ACDC power switches through 3 GPIOs to control power-on and off. By default, the output level of the three GPIOs is pulled down and the GPIOs are disabled to ensure a minimum power consumption. When the PMC is powered on, the GPIOs are configured to output-valid and the low input level is disabled to reduce power leakage.
- The power-on and power-off sequence of the three power control pins can be configured and their power-on and power-off intervals can be independently configured. You can configure the interval to 1ms, 2ms, 8ms, and 16ms. The default interval is 1ms.
- PMC is integrated in the SYSRTC subsystem. The isolation between VDD_RTC and VDD_SYS is realized by VDD_SYS power detection and PMC module state control.

Restart

- PWR-ON key long-press and internal watch dog output can both be configured as the source to trigger PMC restart.
- PMC first powers off and then powers on to complete the restart. Under such circumstance, power-off/power-on source is recorded as restart.

- All interrupts or keypress are ignored during restart. The interval between the power-off state and the power-on state can be configured to 32ms, 64ms, 128ms, 256ms, 512ms , 1s, or 2s. The default interval is 512ms.

PMC Bypass

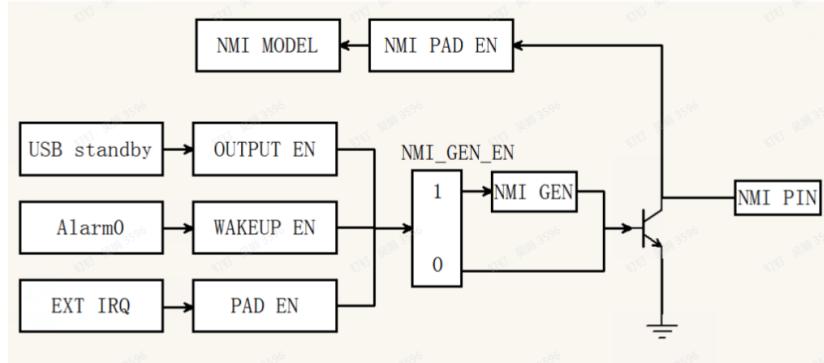
PMC module has a PMC_BYP pin which can realize PMC bypass. The default output level of this pin is high level, which indicates the PMC module is used. To bypass PMC, the PMC_BYP pin needs to be grounded. After the pin is grounded, the PMC module will be reset, and the reset pin, interrupt pin and the internal reset generation logic will be switched to the state where PMC does not exist. The internal register can read the state, but all registers regarding PMC-related configurations are invalid.

NMI Interrupt

RTC has a NMI interrupt generation module included. It can collect the ALARM interrupts and USB wake-up interrupts, generate a square signal whose period is configurable, and output this signal through NMI to PMU to wake up it. This function can be masked, and if so, the ALARM interrupt and USB wake-up interrupt will be sent to PMU through the NMI PIN intact.

The following figure shows the block diagram of NMI.

Figure 3-46 NMI Block Diagram



OUTPUT EN: bit4 of [USB_STBY_CTRL_REG](#)

WAKEUP EN: bit0 of [ALARM_CONFIG_REG](#)

NMI_GEN_EN: bit8 of [PAD_CTRL_REG](#)

NMI PAD EN: bit30 of [PWR_EN_CFG_REG](#)

3.14.3.9 RC Calibration Usage Scenario

Power-on: Select non-accurate 32K divided by internal RC.

Normal scenario: Select 32K divided by internal RC, or external accurate 32K.

Standby or power-off scenario: Select 32K divided by internal RC , or external accurate 32K.

3.14.4 Programming Guidelines

3.14.4.1 RTC Clock Control

1. Select clock source: Select clock source by the bit0 of [LOSC_CTRL_REG](#), the clock source is the internal RC oscillator by default. When the system starts, the clock source can be switched to the external 32K oscillator by software.
2. Auto switch: After enabled the bit[15:14] of [LOSC_CTRL_REG](#), the RTC automatically switches clock source to the internal oscillator when the external crystal could not output waveform, the switch status can query by the bit[1] of [LOSC_AUTO_SWT_STA_REG](#).



NOTE

If only configuring the bit[15] of [LOSC_CTRL_REG](#), the clock source status bit cannot be changed after the auto switch is valid, because the two functions are independent.

Here is the basic code samples.

```
Write (0x16aa4000,LOSC_Ctrl); //Write key field  
Write (0x16aa4001,LOSC_Ctrl); //Select the external 32K clock
```

3.14.4.2 RTC Calendar

1. Write time initial value: Write the current time to [RTC_DAY_REG](#) and [RTC_HH_MM_SS_REG](#).
2. After updated time, the RTC restarts to count again. The software can read the current time anytime.



NOTE

The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.

Ensure the bit[8:7] of [LOSC_CTRL_REG](#) is 0 before the next time configuration is performed.

Here is the basic code samples.

For example: set time to 21st, 07:08:09 and read it.

```
RTC_DAY_REG = 0x000000015;  
RTC_HH_MM_SS_REG = 0x000070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)  
Read (RTC_DAY_REG);  
Read (RTC_HH_MM_SS_REG);
```

3.14.4.3 Alarm0

1. Enable alram0 interrupt by writing [ALARMO IRQ EN](#).
2. Set the counter comparator, write the count-down day, hour, minute, second number to [ALARMO DAY SET REG](#) and [ALARMO HH-MM-SS SET REG](#).
3. Enable alarm0 function by writing [ALARMO ENABLE REG](#), then the software can query alarm count value in real time by [ALARMO DAY SET REG](#) and [ALARMO HH-MM-SS SET REG](#). When the setting time reaches, [ALARMO IRQ STA REG](#) is set to 1 to generate interrupt.
4. After enter the interrupt process, write [ALARMO IRQ STA REG](#) to clear the interrupt pending, and execute the interrupt process.
5. Resume the interrupt and continue to execute the interrupted process.
6. The power-off wakeup is generated via SoC hardware and PMIC, the software only needs to set the pending condition of alarm0, and set [ALARM CONFIG REG](#) to 1.

3.14.5 Register List

Module Name	Base Address
RTC	0x0709 0000

Register Name	Offset	Description
VDD_RTC Power Domain		
LOSC_CTRL_REG	0x0000	LOSC Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_Mm_SS_SET_REG	0x0014	RTC Hour-Minute-Second Register
ALARMO_DAY_SET_REG	0x0020	Alarm 0 Day Set Register
ALARMO_HH_MM_SS_SET_REG	0x0024	Alarm 0 Hour-Minute-Second Set Register
ALARMO_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARMO_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARMO_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
TIMER_SOFT_RST_REG	0x0040	Timer Software Reset Register
ALARMO_CONFIG_REG	0x0050	Alarm 0 Configuration Register
CLK32K_FOUT_CTR_REG	0x0060	CLK32K Fanout Control register
GP_DATA_REGn	0x0100+N*0x004 (N=0~7)	General Purpose Register
FBOOT_INFO_REG0	0x0120	Fast Boot Info Register0
FBOOT_INFO_REG1	0x0124	Fast Boot Info Register1
XO_CTRL_WP_REG	0x015C	XO Control Write Protect Register
XO_CTRL_REG	0x0160	XO Control Register
VDD_RTC_REG	0x0190	VDD RTC Regulation Register

Register Name	Offset	Description
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_OFF_GATING_CTRL_REG	0x01F4	VDD Off Gating Control Register
SP_STDBY_FLAG_REG	0x1F8	Super Standby Flag Register
SP_STDBY_SOFT_ENTRY_REG	0x1FC	Super Standby Software Entry Register
USB_STBY_CTRL_REG	0x0200	USB Standby Control Register
EFUSE_HV_PWR SWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
PAD_CTRL_REG	0x0208	PAD Control Register
PMC_CTRL_EN_REG	0x0210	PMC Control Enable Register
PMC_DLY_CTRL_REG	0x0214	PMC Delay Control Register
SW_CFG_REG	0x0218	Software Configure State Switch Register
PWRON_INT_EN_REG	0x021C	Power on Interrupt Enable and Pending Register
PMC_STATUS_REG	0x0220	Power on or off Source Status Register
PWR_EN_CFG_REG	0x0230	Power en pin Control Register
RST_DLY_SEL_REG	0x0234	Reset Delay Select Register
PMC_BYP_ST_REG	0x0238	PMC Bypass Status Register
VDD_SYS Power Domain		
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

3.14.6 Register Description

3.14.6.1 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit0 and bit1 can be written with the new value.
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K CLK source select enable 0: Disable. When the LOSC losts, the 32k CLK source will not change to RC 1: Enable. When the LOSC losts, the 32k CLK source will change to RC (LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	<p>RTC_HHMMSS_ACCE RTC Hour Minute Second access After writing the RTC HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS Register, the RTC HH-MM-SS Register will be refreshed for at most one second.</p> <p>Note: Make sure that the bit is 0 for time configuration.</p>
7	R/W	0x0	<p>RTC_DAY_ACCE RTC DAY access After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second.</p> <p>Note: Make sure that the bit is 0 for time configuration.</p>
6:5	/	/	/
4	R/W	0x1	<p>EXT_LOSC_EN External 32.768 kHz Crystal Enable 0: Disable 1: Enable</p>
3:2	R/W	0x0	<p>EXT_LOSC_GSM External 32.768 kHz Crystal GSM 00: Low 01: / 10: / 11: High When GSM is changed, the 32K oscillation circuit will arise transient instability. If the autoswitch function (bit 15) is enabled, 32K changes to RC16M with certain probability. The GSM can influence the time of 32K starting oscillation, the more the GSM, the shorter the time of starting oscillation. So modifying GSM is not recommended. If you need to modify the GSM, firstly disable the auto switch function (bit 15), with a delay of 50 us, then change the GSM, the 32K clock source is changed to external clock.</p>
1	R/W	0x0	<p>RTC_SRC_SEL RTC_TIMER Clock Source Select 0: LOSC_SRC 1: 24MDIV32K Before switching the bit, make sure that the 24MDIV32K function is enabled, that is, the bit16 of the 32K Fanout Control Register is 1.</p>

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock Source Select 0: Low frequency clock from 16M RC 1: External 32.768 kHz OSC

 **NOTE**

If the bit[8:7] of LOSC_CTRL_REG is set, the RTC HH-MM-SS, DD and ALARM DD-HH-MM-SS register cannot be written.

3.14.6.2 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when the auto switch function is enabled. 0: External 32.768 kHz OSC work normally 1: External 32.768 kHz OSC work abnormally
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending 0: No effect 1: Auto switch pending, it means LOSC_SRC_SEL is changed from 1 to 0. Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC clock source status 0: Low frequency clock from 16M RC 1: External 32.768 kHz OSC

3.14.6.3 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Offset:0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescalar value N. The clock output = Internal RC/32/N. 00000: 1 00001: 2 00002: 3 11111: 32

3.14.6.4 0x0010 RTC Year-Month-DAY Register (Default Value: UDF)

Offset:0x0010			Register Name: RTC_DAY_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	UDF	DAY Set Day Range from 0 to 65535.

3.14.6.5 0x0014 RTC Hour-Minute-Second Register (Default Value: UDF)

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Set hour Range from 0 to 23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Set minute Range from 0 to 59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Set second Range from 0 to 59.

3.14.6.6 0x0020 Alarm 0 Day Setting Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset:0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is based on Day.

3.14.6.7 0x0024 Alarm0 Hour-Minute-Second Set Register (Default Value: 0x0000_0000)

Offset:0x0024			Register Name: ALARM0_HH_MM_SS_SET_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Current hour Range from 0 to 23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Current minute Range from 0 to 59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Current second Range from 0 to 59.

3.14.6.8 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable 0: Disable 1: Enable

3.14.6.9 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.14.6.10 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	<p>ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 IRQ enable is set to 1, the pending bit will be sent to the interrupt controller.</p>

3.14.6.11 0x0040 Timer Software Reset Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: TIMER_SOFT_RST_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	<p>Key Filed. Write Protect. To configure Timer soft reset write protection on software, first configure bits [31:16] to 0x16AA and write 0xAA16_XXX before writing bits [15:0].</p>
15:1	/	/	/
0	R/WAC	0x0	<p>TIMER_SOFT_RST Timer RTC logic software reset. 0: No-effect 1: Reset Note: Make sure that the bit is 0 for time configuration.</p>

3.14.6.12 0x0050 Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	<p>ALARM_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output</p>

3.14.6.13 0x0060 32K Fanout Control Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: 32K_FOUT_CTRL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	HOSC_TO_32K_DIVIDER_ENABLE HOSC to 32k divider enable 0: Disable the HOSC 24M to 32K divider circuit 1: Enable the HOSC 24M to 32K divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL LOSC output source select 00: RTC_32K (select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: LOSC 10: HOSC divided 32K
0	R/W	0x0	32K_FANOUT_GATING LOSC out gating enable Configuration of LOSC output, and there is no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

3.14.6.14 0x0100+N*0x0004 General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0 to 7)			Register Name: GP_DATA_REGN
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA Data [31:0]

**NOTE**

General purpose register 0 to 7 value can be stored if the RTC-VIO is larger than 0.7 V.

3.14.6.15 0x0120 Fast Boot Information Register0 (Default Value: 0x0000_0000)

Offset:0x0120			Register Name: FBOOT_INFO_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO0 Fast Boot info Fast Boot Information 0, refer to section 3.5 BROM System

3.14.6.16 0x0124 Fast Boot Information Register1 (Default Value: 0x0000_0000)

Offset:0x0124			Register Name: FBOOT_INFO_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO1 Fast Boot info Fast Boot Information 1, refer to section 3.5 BROM System.

3.14.6.17 0x015C XO Control Write Protect Register (Default Value:0x0000_0000)

Offset: 0x015C			Register Name: XO_CTRL_WP_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	Key Field. Write protection for XO_CTRL_REG(0x0160). Write this field as 0x16AA before configuring XO_CTRL_REG(0x0160) and this field will be automatically cleared to 0 after XO_CTRL_REG is configured.

3.14.6.18 0x0160 XO Control Register (Default Value: 0x883F_10F7)

Offset:0x0160			Register Name: XO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CLK_REQ_ENB Clock REQ enable 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value The capacity cell is 55 fF.
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: For external CLK input mode 1: For normal mode

Offset:0x0160			Register Name: XO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO RFCLK enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5 pF, 0x1 for 10 pF, 0x2 for 15 pF, 0x3 for 20 pF.
3	/	/	/
2	R/W	0x1	RSTO_DLY_SEL For Debug Use Only. It cannot configure to 0 in normal state.
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN 1: Enable 0: Disable The related register configuration is necessary to ensure the reset debounce circuit has a stable clock source. The first time SoC starts up, by default, the reset debounce circuit of SoC uses 32K divided by RC16M. In power-off, software reads the related bit to ensure whether EXT32K is working normally, if it is normal, first switch the clock source of debounce circuit to EXT32K, then close RC16M. Without EXT32K scenario or external RTC scenario, software confirms firstly whether EXT32K is working normally before switching, or software does not close RC16M.

3.14.6.19 0x0190 RTC_VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name: RTC_VIO_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	V_SEL VDD Select 0: Resistance divider 1: Band gap
3	/	/	/

Offset:0x0190			Register Name: RTC_VIO_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x4	<p>RTC_VIO_REGU RTC_VIO Voltage Select The RTC-VIO is provided power for RTC digital part. These bits are useful for regulating the RTC_VIO from 0.65 V to 1.3 V.</p> <p>000: 1.0 V 001: 0.65 V (the configuration can cause RTC reset) 010: 0.7 V 011: 0.8 V 100: 0.9 V 101: 1.1 V 110: 1.2 V 111: 1.3 V</p>

3.14.6.20 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0			Register Name: IC_CHARA_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	<p>KEY_FIELD Key Field The field should be written as 0x16AA. Writing any other value in this field aborts the write-operation.</p>
15:0	R/W	0x0	<p>ID_DATA Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.</p>

3.14.6.21 0x01F4 VDD Off Gating Control Register (Default Value: 0x0000_0021)

Offset:0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	<p>KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit 15 can be configured.</p>
15	WAC	0x0	<p>PWROFF_GAT_RTC_Cfg (For Debug Use Only) Power off gating control signal When use VDD_SYS to RTC isolation software control, write this bit to 1. It will only be cleared by resetb release.</p>
14:12	/	/	/

Offset:0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
11:4	R/W	0x2	<p>VCCIO_DET_SPARE</p> <p>Bit [7:5]: Reserved, default=0</p> <p>Bit [4]: Bypass debounce circuit, defaule=0</p> <p>Bit [3]: Enable control, defaule=0</p> <p>0: Disable VCC-IO detection</p> <p>1: Force the detection output</p> <p>Bit [2:0]: Gear adjustment</p> <p>000: Detection threshold is 2.5 V</p> <p>001: Detection threshold is 2.6 V</p> <p>010: Detection threshold is 2.7 V (default)</p> <p>011: Detection threshold is 2.8 V</p> <p>100: Detection threshold is 2.9 V</p> <p>101: Detection threshold is 3 V</p> <p>110: N/A</p> <p>111: N/A</p>
3:1	/	/	/
0	R/W	0x1	<p>VCCIO_DET_BYPASS_EN</p> <p>0: not bypass</p> <p>1: bypass</p>

3.14.6.22 0x01F8 Super Standby Flag Register (Default Value: 0x0000_0000)

Offset: 0x01F8			Register Name: SP_STDBY_FLAG_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	<p>SP_STDBY_FLAG.</p> <p>Key Field.</p> <p>Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only follow the appropriate process, the super standby flag can be written in the lower 16 bits.</p>
15:0	R/W	0x0	<p>SUP_STANBY_FLAG_DATA.</p> <p>When system is turned on, the value in the Super Standby Flag Register low 16 bits should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written with 0x16AA at first. Then, software programmer must write 0xAA16XXXX in the Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID.</p>

3.14.6.23 0x01FC Super Standby Software Entry Register (Default Value: 0x0000_0000)

Offset: 0x01FC			Register Name: SP_STDBY_SOFT_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SP_STBY_SW_ENTRY_ADDR. CPU software entry register when acting from supper standby.

3.14.6.24 0x0200 USB Standby Control Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: USB_STBY_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	USB POWER OFF GATING Gating the VDD_SYS to VDD_USB signal in USB standby mode. It must be set to 1 before entering USB standby mode and set to 0 when exiting Normal mode. 0: disable 1: enable
15:9	/	/	/
8	R/W	0x0	USB_STBY_IRQ_POWER_OFF_GATING Gating the USB standby IRQ signal to RTC module when USB module is power off. It must be set to 1 in USB Standby mode and must set to 0 in Other mode. 0: disable 1: enable
7:5	/	/	/
4	R/W	0x0	USB_STBY_IRQ_OUTPUT_GATING Mask the USB standby IRQ output to NMI pad. It must be set to 1 in USB standby mode and set to 0 in other mode. 0: disable IRQ output 1: enable IRQ output
3:0	/	/	/

3.14.6.25 0x0204 Efuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset:0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EFUSE_1.8V_POWER_SWITCH_CONTROL 1: Open power switch 0: Close power switch

3.14.6.26 0x0208 PAD Control Register (Default Value: 0x0000_00C0)

Offset:0x208			Register Name: PAD_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/WAC	0x0	NMI_PENDING IRQ Pending bit. 0: No effect 1: Pending, Set 1 to this bit will clear it.
15:9	/	/	/
8	R/W	0x0	NMI_GEN_EN 0: Disable 1: Enable
7:6	R/W	0x3	NMI_DLY_SEL 00: 8ms 01: 16ms 10: 32ms 11: 64ms
5	R/W	0x0	Reserved
4:0	/	/	/

**NOTE**

This register is used when PMC is bypassed and PMU is used instead. PMU can be awakened by configuring NMI output.

3.14.6.27 0x0210 PMC Control Enable Register (Default Value:0x0000_A840)

Offset: 0x0210			Register Name: PMC_CTRL_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/WAC	0x0	Key Field. PMC control enable write protection. Configure bits [31:16] to 0x16AA before writing bits [15:0].
15	R/W	0x1	VBUS_WAKEUP_EN VBUS WAKEUP enable. 0: Disable 1: Enable in standby state, wake-up function is enabled by default.

Offset: 0x0210			Register Name: PMC_CTRL_EN_REG
Bit	Read/Write	Default/Hex	Description
14:12	R/W	0x2	<p>RESTART_DLY_SEL Restart delay select. 000:128ms 001:256ms 010:512ms(default) 011:1s 100:2s</p>
11	R/W	0x1	<p>VBUS_CTRL_EN VBUS control enable. 0: Disable 1: Enable In operating state, by default PMC will power on automatically after it is forced to power off.</p>
10	R/W	0x0	<p>PWRON_WAKEUP_INT_EN Power On key super-long press interrupt to awaken PMC from standby enable. 0: Disable 1: Enable</p>
9	R/W	0x0	<p>PWRON_WAKEUP_INT_LLVL_EN Power On key long press interrupt to awaken PMC from standby enable. 0: Disable 1: Enable</p>
8	R/W	0x0	<p>PWRON_WAKEUP_INT_SLVL_EN Power On key short press interrupt to awaken PMC from standby enable. 0: Disable 1: Enable</p>
7	R/W	0x0	<p>PWRON_WAKEUP_INT_POS_EN Power On key rising edge interrupt to awaken PMC from standby enable. 0: Disable 1: Enable</p>
6	R/W	0x1	<p>PWRON_WAKEUP_INT_NEG_EN Power On key falling edge interrupt to awaken PMC from standby enable. 0: Disable 1: Enable</p>
5	R/W	0x0	<p>ON2OFF_EXTRA_EN Extra power off function enable. 0: Disable 1: Enable</p>

Offset: 0x0210			Register Name: PMC_CTRL_EN_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	WDGRST_OUT_EN Watchdog reset output enable. 0: Disable 1: Enable
3	R/W	0x0	WDGRST_EN Watchdog reset function enable. 0: Disable 1: Enable
2	R/W	0x0	ALARM_WAKEUP_EN Alarm turn-on/awakening enable. 0: disable 1: enable
1	R/W	0x0	IRQ_CTRL_EN IRQ turn-on/awakening enable. 0: Disable 1: Enable
0	R/W	0x0	IRQ_EN IRQ interrupt function enable. 0: Disable 1: Enable

3.14.6.28 0x0214 PMC Delay Control Register (Default Value:0x0924_9534)

Offset: 0x0214			Register Name: PMC_DLY_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:27	R/W	0x1	PWROFF_SEQ2_DLY_CFG Power off seq2 delay select. 000:0ms(1T 32k cycle) 001:1ms 010:2ms 011:8ms 100:16ms
26:24	R/W	0x1	PWROFF_SEQ1_DLY_CFG Power off seq1 delay select. 000:0ms(1T 32k cycle) 001:1ms 010:2ms 011:8ms 100:16ms

Offset: 0x0214			Register Name: PMC_DLY_CTRL_REG
Bit	Read/Write	Default/Hex	Description
23:21	R/W	0x1	PWROFF_SEQ0_DLY_CFG Power off seq0 delay select. 000:0ms (1T 32k cycle) 001:1ms 010:2ms 011:8ms 100:16ms
20:18	R/W	0x1	PWRON_SEQ2_DLY_CFG Power on seq2 delay select. 000:0ms (1T 32k cycle) 001:1ms 010:2ms 011:8ms 100:16ms
17:15	R/W	0x1	PWRON_SEQ1_DLY_CFG Power on seq1 delay select. 000:0ms(1T 32k cycle) 001:1ms 010:2ms 011:8ms 100:16ms
14:12	R/W	0x1	PWRON_SEQ0_DLY_CFG Power on seq0 delay select. 000:0ms (1T 32k cycle) 001:1ms 010:2ms 011:8ms 100:16ms
11:10	R/W	0x1	PWRON_INT_DLY_SEL Options for long press threshold of Power On key interrupt: 00:1s 01:1.5s 10:2s 11:2.5s
9:8	R/W	0x1	PWRON_SUPER_DLY Configuration for Power On key super-long press duration: 00:6s 01:8s 10:16s

Offset: 0x0214			Register Name: PMC_DLY_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:5	R/W	0x1	PWRON_DLY_SEL Options for Power On key press detection time: 000:128ms 001:256ms 010:512ms 011:1s 100:2s
4:3	R/W	0x2	IRQ_DLY_SEL_CFG Configuration for IRQ interrupt detection threshold: 00:4ms 01:8ms 10:16ms
2:0	R/W	0x4	VBUS_DLY_SEL VBUS detect delay select. 000:16ms 001:32ms 010:64ms 011:128ms 100:256ms 101:512ms

3.14.6.29 0x0218 Software Configure State Switch Register (Default Value:0x0000_8000)

Offset: 0x0218			Register Name: SW_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	Key Field. To configure PMC status write protection on software, first configure bits [31:16] to 0x16AA and write 0xAA16_XXX before writing bits [15:0].
15	R/W	0x1	PMC_CLK_EN 0: disable 1: enable Some PMC ctrl gatings are enabled by default. To reduce power consumption, you can configure this bit to 0 after PMC is turned on to enable hardware to auto control the PMC ctrl clock gating.
14	R/W	0x0	POWER_EN2_CFG Power en2 software configuration: 0:Close 1:Open

Offset: 0x0218			Register Name: SW_CFG_REG
Bit	Read/Write	Default/Hex	Description
13	R/W	0x0	POWER_EN1_CFG Power en1 software configuration: 0:Close 1:Open
12	R/W	0x0	POWER_EN0_CFG Power en0 software configuration: 0:Close 1:Open
11:9	R/W	0x0	SEQ_SEL_CFG SEQ0-2 power-on sequence configuration: 000:en0→en1→en2 001:en0→en2→en1 010:en1→en0→en2 011:en1→en2→en0 100:en2→en0→en1 101:en2→en1→en0 The power-off sequence and power-on sequence are opposite.
8	R/W	0x0	SEQ2_MASK_EN During standby, SEQ2 is masked separately. 0:Close 1:Open
7	R/W	0x0	SEQ1_MASK_EN During standby, SEQ1 is masked separately. 0:Close 1:Open
6	R/W	0x0	SEQ0_MASK_EN During standby, SEQ0 is masked separately. 0:Close 1:Open
5:4	R/W	0x0	PWRON_KEY_CFG Function options for power On key super-long press: 00:power off 01:restart 10:only interrupt.
3	R/W	0x0	WDGRST_CFG Watchdog reset configure function. 0:restart 1:only generate system reset.

Offset: 0x0218			Register Name: SW_CFG_REG
Bit	Read/Write	Default/Hex	Description
2:1	R/W	0x0	SW_CFG Configuration for software PMC status switch: 00:power off 01:restart 10:standby
0	R/W1T	0x0	SW_CFG_EN PMC status switch software configuration enable: 0: Disable 1: Enable If PMC status switch enable is configured for this register, 1 will be automatically deleted.

3.14.6.30 0x021C Power on Interrupt Enable and Pending Register (Default Value:0x0000_0000)

Offset: 0x021C			Register Name: PWRON_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	PWR_VBUS_OUT_INT_PEND VBUS out pending bit. 0: No effect 1:Pending, write 1 to clear
23	R/W1C	0x0	PWR_VBUS_IN_INT_PEND VBUS in pending bit. 0: No effect 1:Pending, write 1 to clear
22	R/W1C	0x0	IRQ_INT_NEG_PEND IRQ negedge pending bit. 0: No effect 1:Pending, write 1 to clear
21	R/W1C	0x0	IRQ_INT_POS_PEND IRQ posedge pending bit. 0: No effect 1:Pending, write 1 to clear
20	R/W1C	0x0	PWRON_INT_SUPER_KEY_PEND Power on super key pending bit. 0: No effect 1:Pending, write 1 to clear
19	R/W1C	0x0	PWRON_INT_LLVL_PEND Power on long level pending bit. 0: No effect 1:Pending, write 1 to clear

Offset: 0x021C			Register Name: PWRON_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	PWRON_INT_SLVL_PEND Power on short level pending bit. 0: No effect 1:Pending, write 1 to clear
17	R/W1C	0x0	PWRON_INT_POS_PEND Power on posedge pending bit. 0: No effect 1:Pending, write 1 to clear
16	R/W1C	0x0	PWRON_INT_NEG_PEND Power on negedge pending bit. 0: No effect 1:Pending, write 1 to clear
15:9	/	/	/
8	R/W	0x0	PWR_VBUS_OUT_INT_EN VBUS out interrupt enable. 0: Disable 1:Enable
7	R/W	0x0	PWR_VBUS_IN_INT_EN VBUS in interrupt enable. 0: Disable 1: Enable
6	R/W	0x0	IRQ_INT_NEG_EN IRQ negedge interrupt enable. 0: Disable 1: Enable
5	R/W	0x0	IRQ_INT_POS_EN IRQ posedge interrupt enable. 0: Disable 1: Enable
4	R/W	0x0	PWRON_INT_SUPER_KEY_EN Power on super key interrupt enable. 0: disable 1: enable
3	R/W	0x0	PWRON_INT_LLVL_EN Power on long level interrupt enable. 0: Disable 1:Enable
2	R/W	0x0	PWRON_INT_SLVL_EN Power on short level interrupt enable. 0: Disable 1: Enable

Offset: 0x021C			Register Name: PWRON_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PWRON_INT_POS_EN Power on posedge interrupt enable. 0: Disable 1: Enable
0	R/W	0x0	PWRON_INT_NEG_EN Power on negedge interrupt enable. 0: Disable 1: Enable

3.14.6.31 0x0220 Power on or off Source Status Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: PMC_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R	0x0	VBUS_STATUS VBUS Detect status 0: no VBUS 1: VBUS in
7	R	0x0	RST_DLY_STATUS Reset Delay Status. 0: no DLY 1: DLY During system reset and release, dcxo en is released after the default 8ms delay. If the power is not stable after the 8 ms delay, wait for the fixed another 64 ms delay for the power to turn stable. If the system did wait for another 64 ms, the bit status should be 1. The reset release waiting time can be configured longer on the software for optimization.
6:4	R	0x0	PWROFF_STATUS Records power-off source 000: Initial power-off status 001: Long-press turn-off 010: Long-press restart 011: Watchdog restart 100: Abnormal power disconnection 101: Software power-off configuration 110: Software restart configuration

Offset: 0x0220			Register Name: PMC_STATUS_REG
Bit	Read/Write	Default/Hex	Description
3:0	R	0x0	<p>PWRON_STATUS Power-on source record: 0000: Reset status 0001: Power On key power-on 0010: VBUS insertion and power-on 0011: IRQ detection power-on 0100: Alarm power-on 0101: Restart 0110: Power On key awakening 0111: VBUS insertion awakening 1000: IRQ detection awakening 1001: Alarm awakening 1010: USB interrupt awakening</p>

3.14.6.32 0x0230 Power EN pin Control Register (Default Value:0xC02A_0000)

Offset: 0x0230			Register Name: PWR_EN_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	<p>RESETB_IE Resetb input enable 0: Enable 1: Disable Note: If PMC is available in V853/V853S, this bit is not configurable.</p>
30	R/W	0x1	<p>NMI_IE NMI input enable 0: Enable 1: Disable Note: If PMC is available in V853/V853S, this bit is not configurable.</p>
29	R/W	0x0	<p>PWRON_IE PWRON input enable 0: Enable 1: Disable Note: If PMC is bypassed, this bit is not configurable.</p>
28:22	/	/	/
21:20	R/W	0x2	<p>PWR_EN2_PULL Power en2 pull up/down select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved</p>

Offset: 0x0230			Register Name: PWR_EN_CFG_REG
Bit	Read/Write	Default/Hex	Description
19:18	R/W	0x2	PWR_EN1_PULL Power en1 pull up/down select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x2	PWR_EN0_PULL Power en0 pull up/down select. 00: Pull_up/down disable 01: Pull_up 10: Pull_down 11: Reserved
15:11	/	/	/
10	R/W	0x0	PWR_EN2_OE Power en2 output enable 0: Enable 1: Disable
9	R/W	0x0	PWR_EN1_OE Power en1 output enable 0: Enable 1: Disable
8	R/W	0x0	PWR_EN0_OE Power en0 output enable 0: Enable 1: Disable
7:6	/	/	/
5:4	R/W	0x0	PWR_EN2_DRV Power en2 Multi driving Select 00:Level0(200Ω) 01:Level1(100Ω) 10:Level2(66Ω) 11:Level3(50Ω)
3:2	R/W	0x0	PWR_EN1_DRV Power en1 Multi driving Select 00:Level0(200Ω) 01:Level1(100Ω) 10:Level2(66Ω) 11:Level3(50Ω)

Offset: 0x0230			Register Name: PWR_EN_CFG_REG
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	<p>PWR_ENO_DRV Power en0 Multi driving Select 00:Level0(200 Ω) 01:Level1(100 Ω) 10:Level2(66 Ω) 11:Level3(50 Ω)</p>

3.14.6.33 0x0234 Reset Delay Select Register (Default Value:0x0000_0013)

Offset: 0x0234			Register Name: RST_DLY_SEL_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	<p>DCXO_DLY_DONE Output a stable flag bit after DCXO is enabled 0: Close 1: Open</p>
30:12	/	/	/
11:7	R/W	0x0	Reserved
6:4	R/W	0x1	<p>PWRON_DLY_SEL_CFG Options for the time waited between stable power and release from reset: 000: 4ms 001: 8ms 010: 16ms 011: 32ms 100:64ms If the chip has a PMC module and the Watch dog reset generates only the global reset, the time waited for release from reset is the time configured by this register.</p>
3:2	/	/	/
1:0	R/W	0x3	<p>DCXO_DLY_SEL_CFG Options for the time waited before DCXO turning stable after being enabled: 00: 1ms 01: 2ms 10: 3ms 11: 4ms</p>

3.14.6.34 0x0238 PMC Bypass Status Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: PMC_BYP_ST_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	<p>Key Field.</p> <p>To configure PMC status write protection on software, first configure bits [31:16] to 0x16AA and write 0xAA16_XXX before writing bits [15:0].</p>
15:2	/	/	/
1	R/W	0x0	<p>PMC_BYP_PULL</p> <p>PMC Bypass pull register.</p> <p>0: NO PULL-UP</p> <p>1: PULL-UP</p>
0	R	0x0	<p>PMC_BYP_ST</p> <p>PMC bypass status</p> <p>0: Bypass</p> <p>1: PMC</p>

3.14.6.35 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0009)

Offset:0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>RTC REG CFG SPI Clock Gating</p> <p>0: Gating</p> <p>1: Not Gating</p> <p>Before configuring RTC register, the clock divider of SPI needs be configured firstly, then clock gating needs be enabled.</p> <p>Note: Frequency division and clock gating can not be set at the same time.</p>
30:5	/	/	/
4:0	R/W	0x9	<p>RTC REG CFG SPI Clock Divider: M</p> <p>Actual SPI Clock = AHBS1/(M+1), (0 to 15)</p> <p>The default frequency of AHBS1 is 200 MHz, and the default frequency of SPI Clock is 20 MHz.</p> <p>Note: The SPI clock can not exceed 50 MHz, or else the RTC register may be abnormal.</p>

3.15 Message Box

3.15.1 Overview

The Message Box (MSGBOX) provides the interrupt communication mechanism for the on-chip processor.

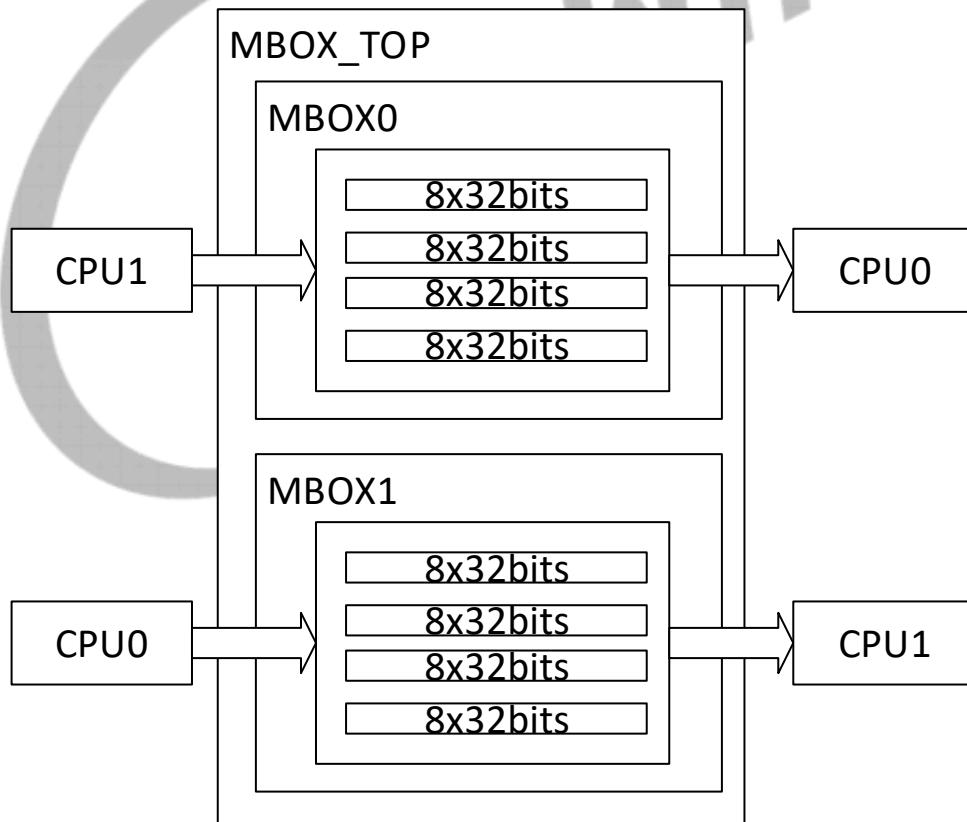
The MSGBOX has the following features:

- Supports communication between two CPUs through one-way channels. Each CPU has one MSGBOX and can only read or write in one communication.
 - CPU 0: ARM CPU
 - CPU 1: RISC CPU
- Supports four channels between the two CPUs and the FIFO depth of the channels is 8 x 32 bits
- Supports interrupts

3.15.2 Block Diagram

The following figure shows the block diagram of the message box.

Figure 3-47 Message Box Block Diagram



For MSGBOX0, CPU1: write; CPU0: read

For MSGBOX1, CPU0: write; CPU1: read

The two message boxes use the same AHB interface.

- Select MSG0 and MSG1 through the bit[11:10].
- Select the CPU used for sending messages through the bit[9:8].
- Visit a register with the fixed address using the FIFO method.
- Use the master ID to distinguish the read and write function. This design sets the user1 as write and the user0 as read.

In the MSGBOX0, RISC CPU is designed for writing, and A7 is designed for reading. In the MSGBOX1, A7 is designed for writing, and RISC CPU is designed for reading. In this way, two CPUs can send message to each other. Each CPU is assigned four channels. The software can make two of them as normal and another two as secure. The two normal channels can be configured as a synchronous box, and the other two channels are working as an asynchronous box.

3.15.3 Functional Descriptions

3.15.3.1 Clock and Reset

The MSGBOX is on AHB. Before accessing the MSGBOX registers, you need to de-assert the MSGBOX reset signal and then open the MSGBOX gating signal.

3.15.3.2 Typical Application

Two different CPUs can build communication by configuring the MSGBOX. The communication parties have 8 bidirectional channels. One CPU acts as a transmitter and the other acts as a receiver. During the communication process, the current status can be judged through the interrupt or FIFO status.

3.15.4 Operation Modes

3.15.4.1 Checking the Transfer Status via the Interrupt Status

1. Interrupt enable bit: configure the interrupt enable bit of transmitter/receiver through `MSGBOX_IRQ_EN_REG`.
2. When FIFO is not full, an interrupt pending generates to remind the transmitter to transmit data. At this time, write data to FIFO in interrupt handler, clear the pending bit and the enable bit of Transmitter IRQ.
3. When FIFO has new data, an interrupt pending generates to remind the receiver to receive data. At this time, read data from FIFO in interrupt handler, clear the pending bit and the enable bit of Receiver IRQ.

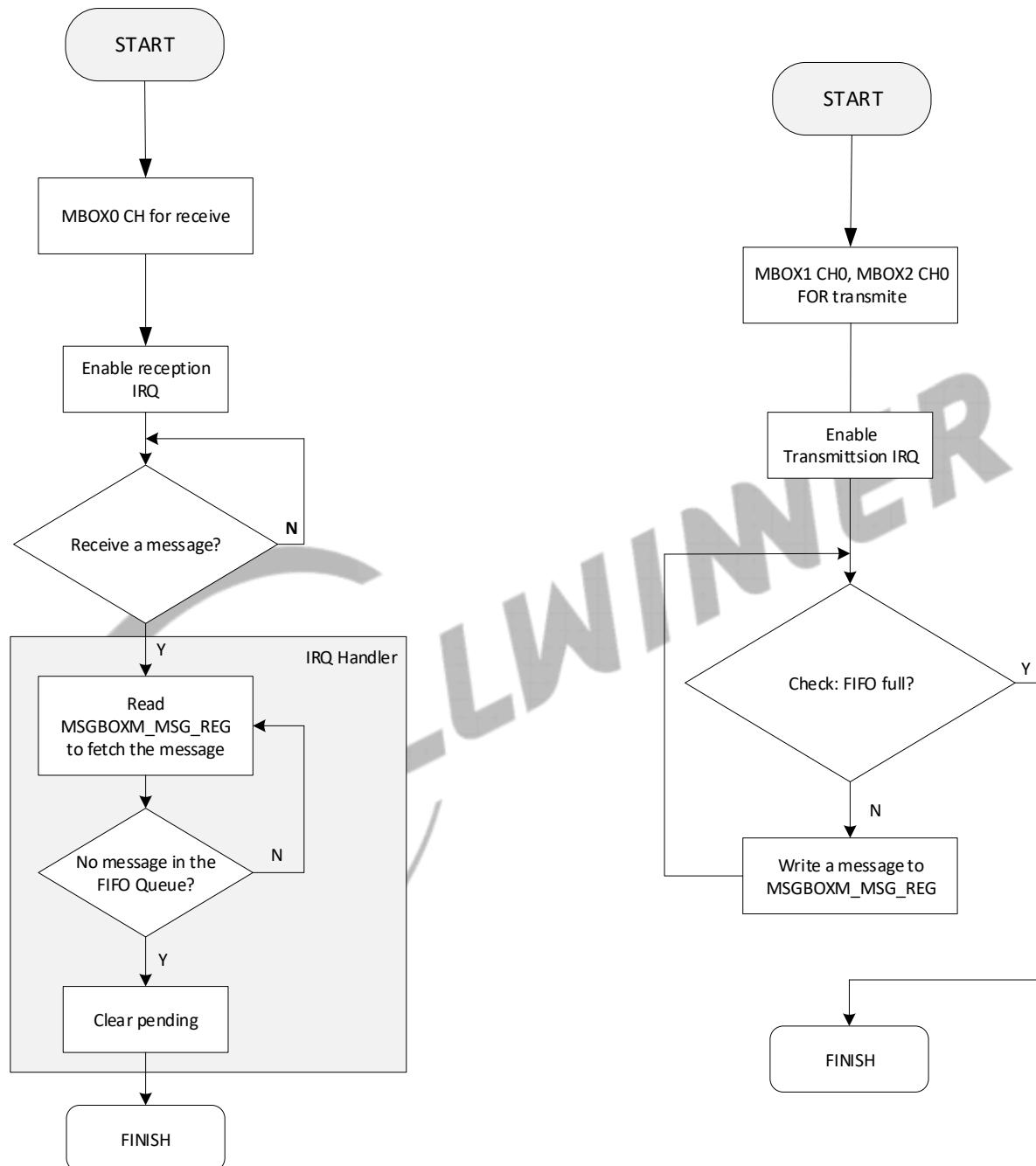
3.15.4.2 Checking the Transfer Status via the FIFO Status

1. When FIFO is not full, the transmitter fills FIFO to 8*32 bits.
2. When the receiver considers FIFO is full, the receiver reads the FIFO data, and reads `MSGBOXM_MSG_STATUS_REG` to require the current FIFO number.

3.15.5 Programming Guidelines

The working process of CPU0 is as follows:

Figure 3-48 CPU0 Working Process



3.15.6 Register List

Module Name	Base Address	Comments
MBOX(CPUX)	0x0300 3000	base address for CPUX
MBOX(RISC CPU)	0x0602 0000	base address for RISC CPU

Parameter	Description
N	0~1 The number of CPUs communicating with the current CPU. There is only 1 item in V853/V853S, so the N value is fixed at 0.
P	0~3 Number of channels between two CPUs.

Register Name	Offset	Description
MSGBOX (CPUX)		
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100(N=0)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100(N=0)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100(N=0)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100(N=0)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100(N=0)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004(N=0) (P=0~3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004(N=0) (P=0~3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004(N=0) (P=0~3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESH_OLD_REG	0x0080+N*0x0100+P*0x0004(N=0) (P=0~3)	MSGBOX Write IRQ Threshold Register
MBOX (RISC CPU)		
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100(N=0~1)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100(N=0~1)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100(N=0~1)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100(N=0~1)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100(N=0~1)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESH_OLD_REG	0x0080+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX Write IRQ Threshold Register

Note:

MBOX	CPU	N Value
MBOX(CPUX)	RISC CPU -> CPUX	N=0

3.15.7 CPUX MSGBOX Register Description

3.15.7.1 0x0020+N*0x0100(N=0) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0020+N*0x0100(N=0)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN. Reception Channel3 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 3 has received a new message.)
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN. Reception Channel2 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 2 has received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN. Reception Channel1 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 1 has received a new message.)
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN. Reception Channel0 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

3.15.7.2 0x0024+N*0x0100(N=0) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0024+N*0x0100(N=0)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/

Offset:0x0024+N*0x0100(N=0)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND. Reception Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Set one to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. Reception Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Set one to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND. Reception Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Set one to this bit will clear it.
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND. Reception Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Set one to this bit will clear it.

3.15.7.3 0x0030+N*0x0100(N=0) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0030+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN. Transmit Channel3 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 3 empty level reach the configured threshold.)
6	/	/	/

Offset:0x0030+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN. Transmit Channel2 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 2 empty level reach the configured threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN. Transmit Channel1 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 1 empty level reach the configured threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. Transmit Channel0 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 0 empty level reach the configured threshold.)
0	/	/	/

3.15.7.4 0x0034+N*0x0100(N=0) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0034+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND. Transmit Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configured threshold. Set one to this bit will clear it.
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND. Transmit Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configured threshold. Set one to this bit will clear it.
4	/	/	/

Offset:0x0034+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND. Transmit Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configured threshold. Set one to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND. Transmit Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configured threshold. Set one to this bit will clear it.
0	/	/	/

3.15.7.5 0x0040+N*0x0100(N=0) MSGBOX Debug Register (Default Value: 0x0000_0000)

Offset:0x0040+N*0x0100(N=0)			Register Name: MSGBOX_DEBUG_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0x0	FIFO_CTRL. FIFO Control. MQ [7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE. Debug Mode. In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

3.15.7.6 0x0050+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX FIFO Status Register (Default Value: 0x0000_0000)

Offset:0x0050+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	R/W	Default/Hex	Description
31: 1	/	/	/

Offset:0x0050+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	R/W	Default/Hex	Description
0	R	0x0	FIFO_NOT_AVA_FLAG. FIFO is not available flag. 0: The Message FIFO queue empty level reached the configured threshold 1: The Message FIFO queue empty level is not reached the configured threshold This FIFO status register has the status related to the message queue.

3.15.7.7 0x0060+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset:0x0060+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	MSG_NUM. Message Number. Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001~1111:/

3.15.7.8 0x0070+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset:0x0070+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_MSG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	MSG_QUE. The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

3.15.7.9 0x0080+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset:0x0080+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Configure the FIFO empty level to trigger the write interrupt for user1. 00: 1 01: 2 10: 4 11: 8

3.15.8 RISC CPU MSGBOX Register Description

3.15.8.1 0x0020+N*0x0100(N=0~1) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0020+N*0x0100(N=0~1)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN. Reception Channel3 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 3 has received a new message.)
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN. Reception Channel2 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 2 has received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN. Reception Channel1 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 1 has received a new message.)
1	/	/	/

Offset:0x0020+N*0x0100(N=0~1)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN. Reception Channel0 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

3.15.8.2 0x0024+N*0x0100(N=0~1) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0024+N*0x0100(N=0~1)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND. Reception Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Set one to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. Reception Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Set one to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND. Reception Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Set one to this bit will clear it.
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND. Reception Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Set one to this bit will clear it.

3.15.8.3 0x0030+N*0x0100(N=0~1) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0030+N*0x0100(N=0~1)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN. Transmit Channel3 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 3 empty level reach the configed threshold.)
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN. Transmit Channel2 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 2 empty level reach the configed threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN. Transmit Channel1 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 1 empty level reach the configed threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. Transmit Channel0 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 0 empty level reach the configed threshold.)
0	/	/	/

3.15.8.4 0x0034+N*0x0100(N=0~1) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0034+N*0x0100(N=0~1)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND. Transmit Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configed threshold. Set one to this bit will clear it.
6	/	/	/

Offset:0x0034+N*0x0100(N=0~1)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND. Transmit Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configed threshold. Set one to this bit will clear it.
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND. Transmit Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configed threshold. Set one to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND. Transmit Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configed threshold. Set one to this bit will clear it.
0	/	/	/

3.15.8.5 0x0040+N*0x0100(N=0~1) MSGBOX Debug Register(Default Value: 0x0000_0000)

Offset:0x0040+N*0x0100(N=0~1)			Register Name: MSGBOX_DEBUG_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0x0	FIFO_CTRL. FIFO Control. MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE. Debug Mode. In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

3.15.8.6 0x0050+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX FIFO Status Register(Default Value: 0x0000_0000)

Offset:0x0050+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	R/W	Default/Hex	Description
31: 1	/	/	/
0	R	0x0	<p>FIFO_NOT_AVA_FLAG. FIFO is not available flag.</p> <p>0: The Message FIFO queue empty level reached the configed threshold</p> <p>1: The Message FIFO queue empty level is not reached the configed threshold</p> <p>This FIFO status register has the status related to the message queue.</p>

3.15.8.7 0x0060+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset:0x0060+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	<p>MSG_NUM. Message Number.</p> <p>Number of unread messages in the message queue. Here, limited to eight messages per message queue.</p> <p>0000: There is no message in the message FIFO queue.</p> <p>0001: There is 1 message in the message FIFO queue.</p> <p>0010: There are 2 messages in the message FIFO queue.</p> <p>0011: There are 3 messages in the message FIFO queue.</p> <p>0100: There are 4 messages in the message FIFO queue.</p> <p>0101: There are 5 messages in the message FIFO queue.</p> <p>0110: There are 6 messages in the message FIFO queue.</p> <p>0111: There are 7 messages in the message FIFO queue.</p> <p>1000: There are 8 messages in the message FIFO queue.</p> <p>1001~1111:/</p>

3.15.8.8 0x0070+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset:0x0070+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_MSG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	MSG_QUE. The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

3.15.8.9 0x0080+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset:0x0080+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Config the FIFO empty level to trigger the write interrupt for user1. 00: 1 01: 2 10: 4 11: 8

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4 Memory

4.1 SDRAM Controller (DRAMC)

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all in-dusty-standard DDR3/DDR3L. It supports up to a 24G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings. To simplify chip system integration, DDR controller works in the half rate mode.

The DRAMC has the following features:

- Supports 16-bit one channel
- Supports 2 chip select signals
- Support DDR3/DDR3L SDRAM
- Supports the power voltage of different memory devices: 1.35V and 1.5V
- Supports clock frequency up to 933 MHz for DDR3/ DDR3L
- Supports memory capacity up to 1 GB
- 16 address lines and three bank address lines per channel
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Priority of transferring through multiple ports is programmable
- Supports random read or write operation
- Clock frequency can be changed for different application(MDFS supported)
- Controller clock on/off hardware automatically support
- Auto Self-Refresh Entry(ASRE)/Exit(ASRX) support
- Clock pad enable/disable hardware automatically support when ASRE/ASRX



NOTE

V853S is embedded with 128MB DDR3L

4.2 SD/MMC Host Controller (SMHC)

4.2.1 Overview

The SMHC controls the read/write operations on the secure digital (SD) cards, multimedia cards (MMC), and various extended devices that is based on the secure digital input/output (SDIO) protocol. The processor provides three SMHC interfaces for controlling the SD cards, MMCs, and SDIO devices.

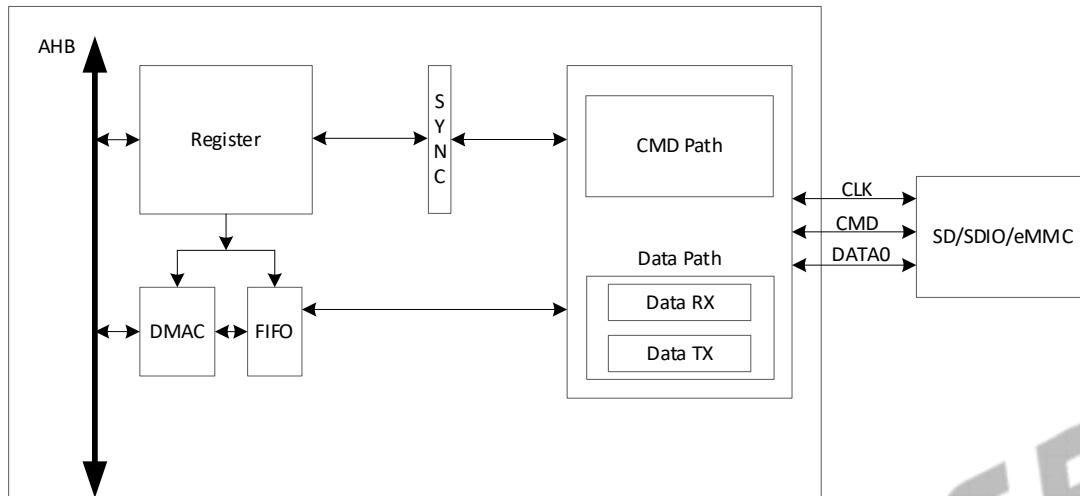
The SMHC has the following features:

- Supports Secure Digital memory protocol commands (up to SD3.0)
- Supports Secure Digital I/O protocol commands (up to SDIO3.0)
- Supports Multimedia Card protocol commands (up to MMC5.1)
- Supports eMMC boot operation and alternative boot operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD (Version1.0 to 3.0) or MMC (Version3.3 to 5.1)
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports block size of 1 to 65535 bytes
- Supports descriptor based on internal DMA controller
- Internal 1K Bytes FIFO for data transfer
- SMHC0/1 is an instantiation of SMHC v5.30, supports 1-bit and 4-bit data bus width
 - SDR mode 150 Mhz@1.8V IO pad
 - DDR mode 50 Mhz@1.8V IO pad
 - SDR mode 50 Mhz@3.3V IO pad
- SMHC2 is an instantiation of SMHC v5.30, supports 1-bit, 4-bit, and 8-bit data bus width
 - SDR mode 150Mhz@1.8V IO pad
 - DDR mode 150Mhz@1.8V IO pad
 - DDR mode 50Mhz@3.3V IO pad
 - SDR mode 50Mhz@3.3V IO pad

4.2.2 Block Diagram

The following figure shows a block diagram of the SMHC.

Figure 4-1 SMHC Block Diagram



SMHC contains the following sub-blocks:

Table 4-1 SMHC Sub-blocks

Sub-block	Description
Register	Used to configure the control signal for reading or writing the SD/SDIO/eMMC.
DMAC	The DMA controller that controls the data transfer between the memory and SMHC.
FIFO	A buffer for the data stream between the memory and the SMHC asynchronous clock domain.
SYNC	Synchronizes the signals from the AHB clock domain to the SMHC clock domain.
CMD Path	Sends commands to or receives commands from the SD/SDIO/eMMC.
Data Path	Consists of Data TX and Data RX sub-modules. The Data TX sends data blocks and the CRC codes to the SD/SDIO/eMMC. The Data RX receives data blocks and the CRC codes from the SD/SDIO/eMMC.

4.2.3 Functional Descriptions

4.2.3.1 External Signals

The following table describes the external signals of SMHC.

Table 4-2 SMHC External Signals

Signal	Description	Width	Type
SMHC0			

Signal	Description	Width	Type
SDC0_CLK	Card Clock Output	1	O
SDC0_CMD	Card Command Output	1	O
SDC0_D[3:0]	Card Data Input/Output	4	I/O
SMHC1			
SDC1_CLK	Card Clock Output	1	O
SDC1_CMD	Card Command Output	1	O
SDC1_D[3:0]	Card Data Input/Output	4	I/O
SMHC2			
SDC2_CLK	Clock for eMMC	1	O
SDC2_CMD	Command Signal for eMMC	1	O
SDC2_D[7:0]	Data Input and Output for eMMC	8	I/O
SDC2_RST	Reset for eMMC	1	O

4.2.3.2 Clock Sources

Table 4-3 SMHC Clock Sources

Module	Module Clock	Source	Description
SMHC0	SMHC0_CLK	CCU	Refer to section 3.4 Clock Controller Unit (CCU) for detailed information.
	AHB2_CLK	CCU	
	CLK32K	CCU	
SMHC1	SMHC1_CLK	CCU	Refer to section 3.4 Clock Controller Unit (CCU) for detailed information.
	AHB2_CLK	CCU	
	CLK32K	CCU	
SMHC2	SMHC2_CLK	CCU	Refer to section 3.4 Clock Controller Unit (CCU) for detailed information.
	AHB2_CLK	CCU	
	CLK32K	CCU	

4.2.3.3 Timing Diagram

Refer to the following relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard (4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard (5.0)

4.2.3.4 Data Path

The SMHC and SD/SDIO/eMMC contains the following interface buses: CLK, CMD, and DATA 1/4. During one clock cycle, the SMHC can transmit one bit command with one or two bits data in 1-ch DATA mode, or four or eight bits data in 4-ch DATA mode. The CMD is a bidirection channel for initializing the SD/SDIO/eMMC and transmitting commands. It can work in both the open-drain mode and push-pull mode. The DATA is also a bidirection channel. It works in the push-pull mode.

Reading Data from the SD/SDIO/eMMC

The register configures the signals for the read operation, and synchronize the signals to the SMHC clock domain. Then the Data RX reads data from the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses and writes the data in the FIFO. After that, the DMAC transfers the data from the FIFO to the memory.

Writing Data to the SD/SDIO/eMMC

The register configures the signals for the write operation, and synchronize the signals to the SMHC clock domain. Then the DMAC reads data from the memory and writes the data to the FIFO. After that, the Data TX reads the data from the FIFO and writes the data to the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses.

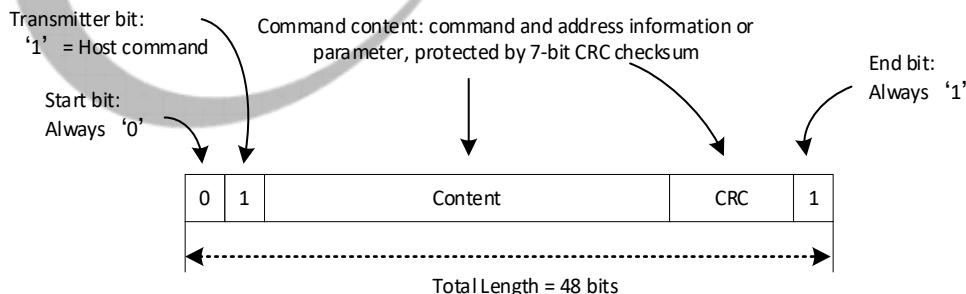
4.2.3.5 Package Format

Data transfer over the SD/eMMC bus is based on command and data bitstreams that are initiated by a start bit and terminated by a stop bit. There are three types of SD/eMMC packets: command token, response token, and data packet.

Command Tokens

The command token starts an operation. A command is sent from the host to a device. It is transferred serially on the CMD line. Command tokens have the following coding scheme:

Figure 4-2 Command Token Format



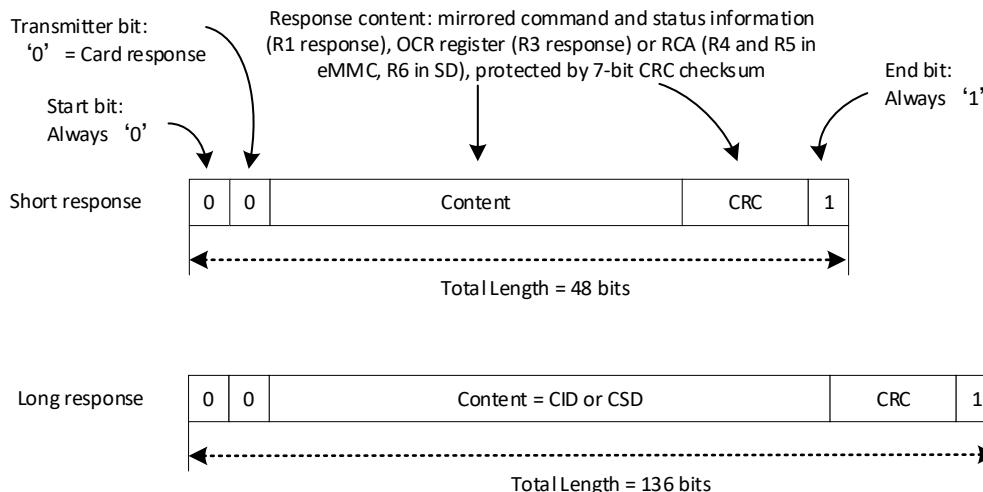
Each command token has 48 bits, preceded by a start bit ('0') and succeeded by an end bit ('1'). To detect transmission errors, each token is protected by CRC bits.

Response Tokens

After receiving a command, the card returns a 48-bit or 136-bit response based on the command type.

A response token is sent from the device to the host as an answer to a previously received command. It is transferred serially on the CMD line.

Figure 4-3 Response Token Format



Data Packets

Data can be transferred from the device to the host or vice versa. Data are transferred via the data lines.

Figure 4-4 Data Packet Format for SDR

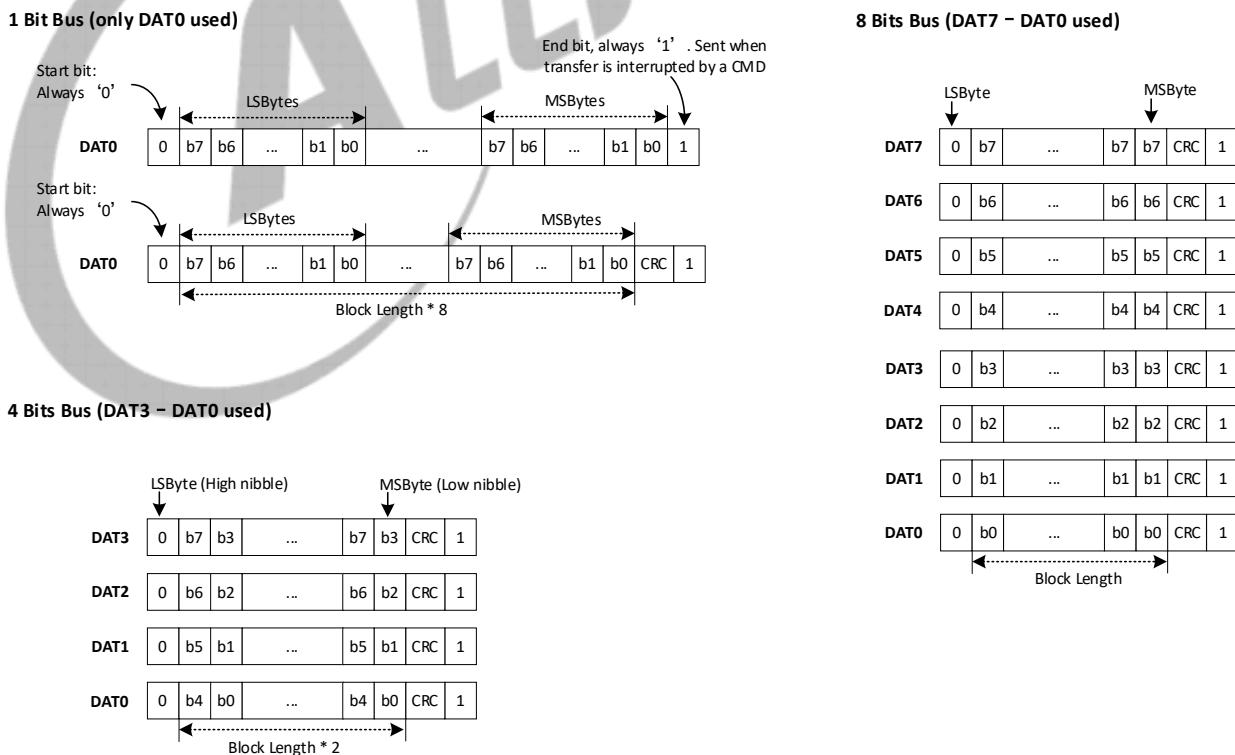
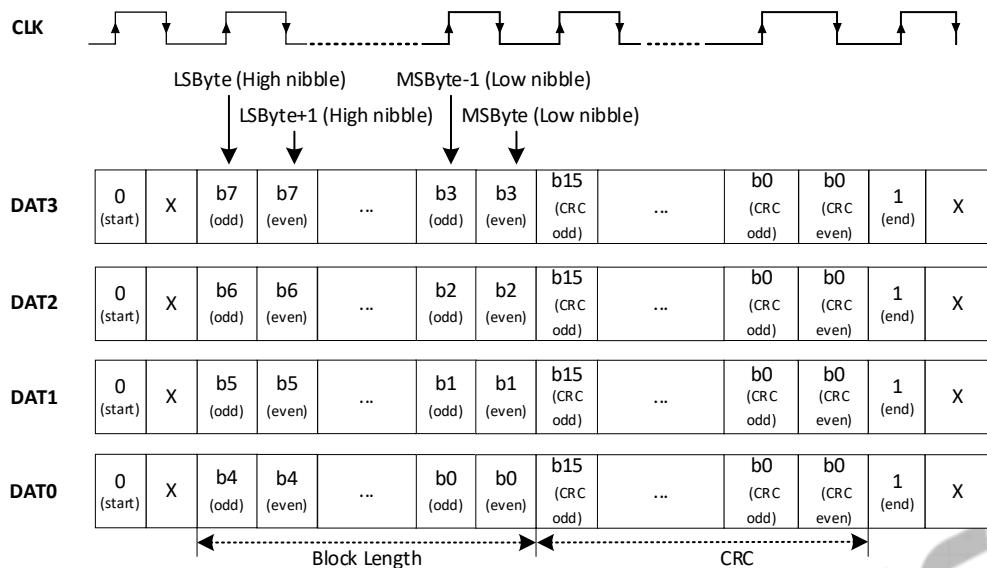
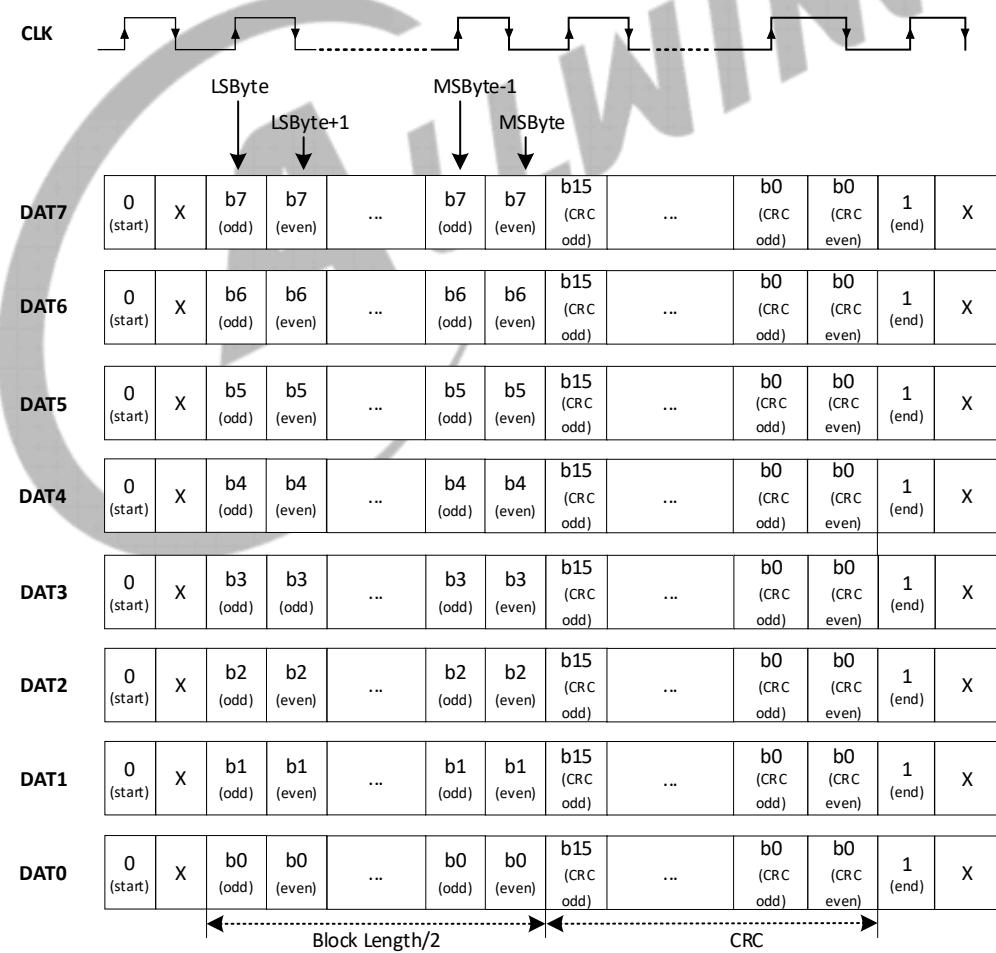


Figure 4-5 Data Packet Format for DDR

4 Bits Bus DDR (DAT3 – DAT0 used)



8 Bits Bus DDR (DAT7 – DAT0 used)



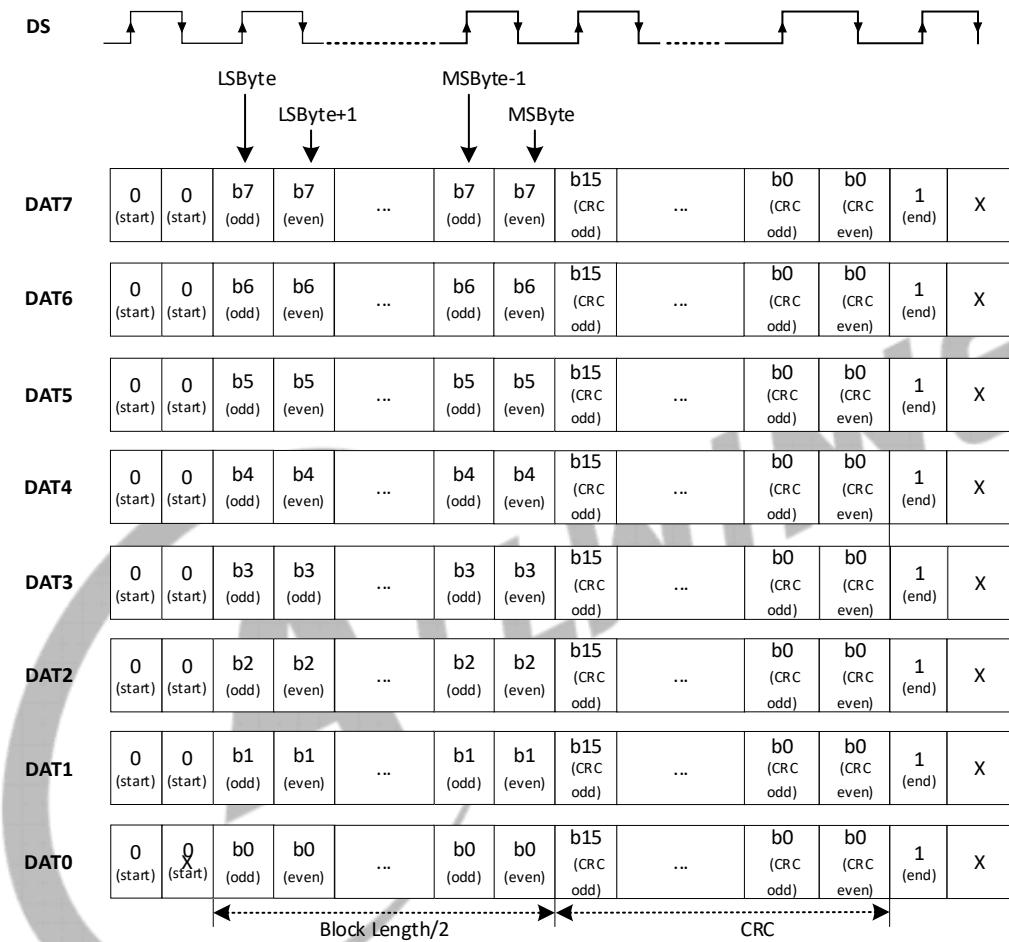


Bytes data are not interleaved but CRCs are interleaved.

Start and end bits are only valid on the rising edge ("X" indicates "undefined").

Figure 4-6 Data Packet Format for DDR in HS400 Mode

8 Bits Bus DDR for HS400 Output (DAT7 – DAT0 used)



Bytes data are not interleaved but CRCs are interleaved.

Start bits are valid when Data Strobe is High and Low.

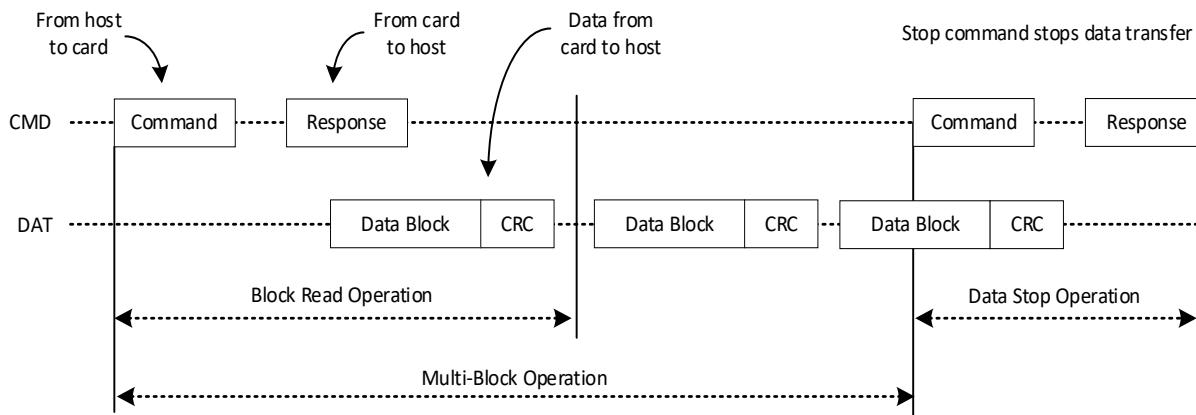
End bits are only valid when Data Strobe is High ("X" indicates "undefined").

Data Transfer

Data transfers to or from the SD/eMMC card are done in blocks. Single and multiple block operations are widely used during data transfer.

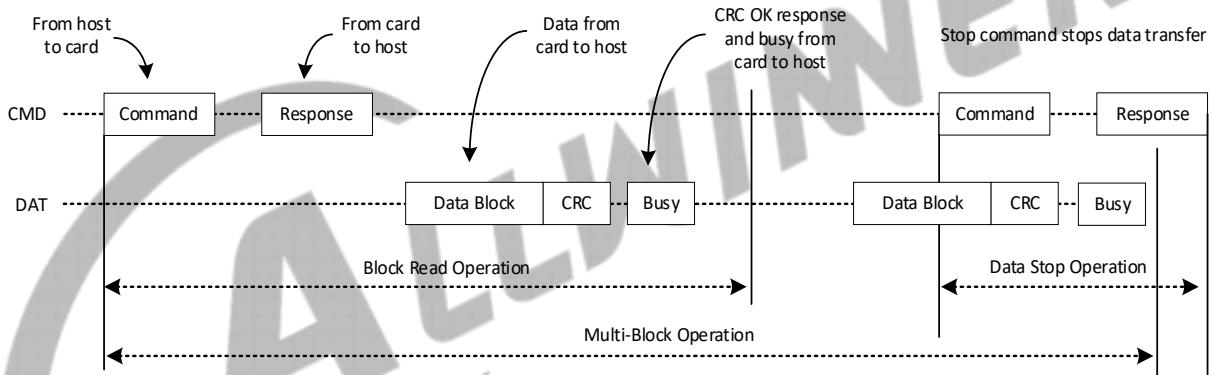
The following figure shows the single-block and multi-block read operation.

Figure 4-7 Single-Block and Multi-Block Read Operation



The following figure shows the single-block and multi-block write operation.

Figure 4-8 Single-Block and Multi-Block Write Operation



4.2.3.6 Internal DMA Controller Description

The SMHC has an internal DMA controller (IDMAC) to transfer data between the host memory and SMHC port. With a descriptor, the IDMAC can efficiently move data from the source to destination by automatically loading the next DMA transfer arguments, which needs less CPU intervention. Before transferring data in the IDMAC, the host driver should construct a descriptor list, configure arguments of every DMA transfer, and then launch the descriptor and start the DMA.

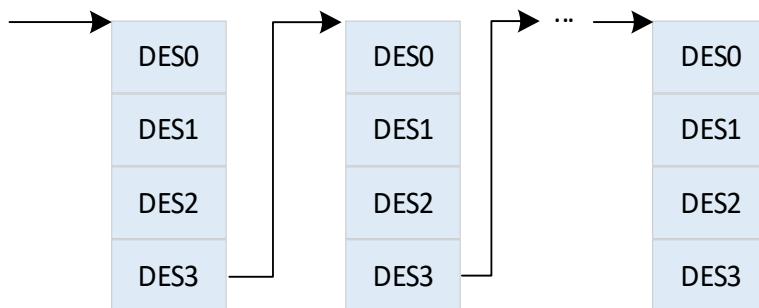
The IDMAC has an interrupt controller. When enabled, it generates an interrupt to the HOST CPU in situations such as data transmission is completed or some error is happened.

IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

The following figure shows the internal formats of a descriptor.

Figure 4-9 IDMAC Descriptor Structure Diagram



This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 corresponds to the [31:0] bits, DES1 corresponds to the [63:32] bits, DES2 corresponds to the [95:64] bits, and DES3 corresponds to the [127:96] bits in a descriptor.

The following table shows the bit definition of DES0.

Table 4-4 DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:6	/	/
5	/	Not used
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

The following table shows the bit definition of DES1.

Table 4-5 DES1 Definition

Bits	Name	Descriptor
31:13	/	/
12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor.

The following table shows the bit definition of DES2.

Table 4-6 DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. It is a word(4byte) address

The following table shows the bit definition of DES3.

Table 4-7 DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present. It is a word(4byte) address.

4.2.3.7 Calibrating the Delay Chain

There are two delay chains in SMHC: data strobe delay chain and sample delay chain.

Data strobe delay chain: used to generate delay to make proper timing between Data Strobe and data signals.

Sample delay chain: used to generate delay to make proper timing between the internal card clock signal and data signals.

Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

Follow the steps below to calibrate the delay chain:

1. Enable SMHC. In order to calibrate the delay chain by the operation registers in SMHC, the SMHC must be enabled through [SMHC Bus Gating Reset Register \(Offset: 0x084C\)](#) and [SMHCx Clock Register \(Offset: 0x0830\)](#).
2. Configure a proper clock for SMHC. The delay chain calibration is based on the clock for SMHC from Clock Control Unit (CCU). The delay chain calibration is an internal function in SMHC and needs no

devices. So it is unnecessary to open the clock signal for devices. The recommended clock frequency is 200 MHz.

3. Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain** (bit[5:0]). Then write 0x0 to **delay control register** to clear the value.
4. Write 0x8000 to **delay control register** to start calibrating the delay chain.
5. Wait until the flag (bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at bit[13:8] in **delay control register**. The delay time generated by these delay cells is equal to the cycle of the SMHC clock nearly. This value is the result of calibration.
6. Calculate the delay time of one delay cell according to the cycle of the SMHC clock and the result of calibration.

4.2.4 Programming Guidelines

4.2.4.1 Initializing SMHC

Before data and commands are exchanged between a card and the SMHC, the SMHC needs to be initialized. Follow the steps below to initialize the SMHC:

1. Configure the corresponding GPIO register as an SMHC by the Port Controller module; reset the clock by writing 1 to [SMHC_BGR_REG](#)[SMHC_x_RST], and open clock gating by writing 1 to [SMHC_BGR_REG](#)[SMHC_x_GATING]; select clock sources and set the division factor by configuring the [SMHC_x_CLK_REG](#) (x = 0, 1) register.
2. Configure [SMHC_CTRL \(Offset: 0x0000\)](#) to reset the FIFO and controller, and enable the global interrupt; configure [SMHC_INTMASK \(Offset: 0x0030\)](#) to 0xFFCE to enable normal interrupts and error abnormal interrupts, and then register the interrupt function.
3. Configure [SMHC_CLKDIV \(Offset: 0x0004\)](#) to open clock for devices; configure [SMHC_CMD \(Offset: 0x0018\)](#) as the change clock command (for example 0x80202000); send the update clock command to deliver clocks to devices.
4. Configure [SMHC_CMD \(Offset: 0x0018\)](#) as a normal command. Configure [SMHC_CMDARG \(Offset: 0x001C\)](#) to set command parameters. Configure [SMHC_CMD \(Offset: 0x0018\)](#) to set parameters like whether to send the response, the response type, and the response length and then send the commands. According to the initialization process in the protocol, you can finish SMHC initialization by sending the corresponding command one by one.

4.2.4.2 Writing a Single Data Block

To write a single data block, follow the steps below:

1. Write 0x1 to [SMHC_CTRL \(Offset: 0x0000\)](#) [DMA_RST] to reset the internal DMA controller; write 0x82 to [SMHC_DMAC \(Offset: 0x0080\)](#) to enable the IDMAC interrupt and configure AHB master burst transfers; configure [SMHC_IDIE \(Offset: 0x008C\)](#) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

2. Configure [SMHC_FIFOTH \(Offset: 0x0040\)](#) to determine the burst size and TX/RX trigger level. For example, if [SMHC_FIFOTH \(Offset: 0x0040\)](#) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure [SMHC_DLBA \(Offset: 0x0084\)](#) to determine the start address of the DMA descriptor.
3. To write one block data to sector1, configure [SMHC_BYTCNT \(Offset: 0x0014\)](#) [BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD24 (Single Data Block Write) to 0x1, write 0x80002758 to [SMHC_CMD \(Offset: 0x0018\)](#), and send CMD24 command to write data to the device.
4. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.
5. Check whether [SMHC_IDST \(Offset: 0x0088\)](#) [TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to [SMHC_IDST \(Offset: 0x0088\)](#) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
6. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [DTC] is 1. If yes, the data transfer and CMD24 writing operations are completed. Otherwise, abnormality exists. Read [SMHC_RINTSTS \(Offset: 0x0038\)](#) and [SMHC_STATUS \(Offset: 0x003C\)](#) to query the existing abnormality.
7. Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set [SMHC_CMDARG \(Offset: 0x001C\)](#) to 0x12340000, write 0x8000014D to [SMHC_CMD \(Offset: 0x0018\)](#), go to step 4 to ensure command transfer completed, and then check whether the highest bit of [SMHC_RESP0 \(Offset: 0x0020\)](#) (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

4.2.4.3 Reading a Single Data Block

To read a single data block, follow the steps below:

1. Write 0x1 to [SMHC_CTRL \(Offset: 0x0000\)](#) [DMA_RST] to reset the internal DMA controller; write 0x82 to [SMHC_DMAC \(Offset: 0x0080\)](#) to enable the IDMAC interrupt and configure AHB master burst transfers; configure [SMHC_IDIE \(Offset: 0x008C\)](#) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure [SMHC_FIFOTH \(Offset: 0x0040\)](#) to determine the burst size and TX/RX trigger level. For example, if [SMHC_FIFOTH \(Offset: 0x0040\)](#) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure [SMHC_DLBA \(Offset: 0x0084\)](#) to determine the start address of the DMA descriptor.
3. To read one block data from sector1, configure [SMHC_BYTCNT \(Offset: 0x0014\)](#) [BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD17 command (Single Data Block Read) to 0x1, write 0x80002351 to [SMHC_CMD \(Offset: 0x0018\)](#), and send CMD17 command to read data from the device to DRAM/SRAM.
4. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

5. Check whether [SMHC_IDST \(Offset: 0x0088\)](#) [RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to [SMHC_IDST \(Offset: 0x0088\)](#) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
6. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [DTC] is 1. If yes, data transfer and CMD17 reading operation are completed. Otherwise, abnormality exists. Read [SMHC_RINTSTS \(Offset: 0x0038\)](#) and [SMHC_STATUS \(Offset: 0x003C\)](#) to query the existing abnormality.

4.2.4.4 Writing Open-Ended Multiple Data Blocks (CMD25 + Auto CMD12)

To write open-ended multiple data blocks, follow the steps below:

1. Write 0x1 to [SMHC_CTRL \(Offset: 0x0000\)](#) [DMA_RST] to reset the internal DMA controller; write 0x82 to [SMHC_DMAC \(Offset: 0x0080\)](#) to enable the IDMAC interrupt and configure AHB master burst transfers; configure [SMHC_IDIE \(Offset: 0x008C\)](#) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure [SMHC_FIFOTH \(Offset: 0x0040\)](#) to determine the burst size and TX/RX trigger level. For example, if [SMHC_FIFOTH \(Offset: 0x0040\)](#) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure [SMHC_DLBA \(Offset: 0x0084\)](#) to determine the start address of the DMA descriptor.
3. To write three blocks of data to sectors begin with sector0, configure [SMHC_BYTCNT \(Offset: 0x0014\)](#) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80003759 to [SMHC_CMD \(Offset: 0x0018\)](#), and send CMD25 command to read data from the device to DRAM/SRAM.
4. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.
5. Check whether [SMHC_IDST \(Offset: 0x0088\)](#) [RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to [SMHC_IDST \(Offset: 0x0088\)](#) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
6. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [ACD] and [SMHC_RINTSTS \(Offset: 0x0038\)](#) [DTC] are both 1. If yes, the data transfer, CMD12 transfer, and CMD25 writing operations are completed. Otherwise, abnormality exists. Read [SMHC_RINTSTS \(Offset: 0x0038\)](#) and [SMHC_STATUS \(Offset: 0x003C\)](#) to query the existing abnormality.
7. Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set [SMHC_CMDARG \(Offset: 0x001C\)](#) to 0x12340000, write 0x8000014D to [SMHC_CMD \(Offset: 0x0018\)](#), go to step 4 to ensure command transfer completed, and then check whether the highest bit of [SMHC_RESP0 \(Offset: 0x0020\)](#) (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

4.2.4.5 Reading Open-Ended Multiple Data Blocks (CMD18 + Auto CMD12)

To read open-ended multiple data blocks, follow the steps below:

1. Write 0x1 to [SMHC_CTRL \(Offset: 0x0000\)](#) [DMA_RST] to reset the internal DMA controller; write 0x82 to [SMHC_DMAC \(Offset: 0x0080\)](#) to enable the IDMAC interrupt and configure AHB master burst transfers; configure [SMHC_IDIE \(Offset: 0x008C\)](#) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure [SMHC_FIFOTH \(Offset: 0x0040\)](#) to determine the burst size and TX/RX trigger level. For example, if [SMHC_FIFOTH \(Offset: 0x0040\)](#) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure [SMHC_DLBA \(Offset: 0x0084\)](#) to determine the start address of the DMA descriptor.
3. To read three blocks of data from sectors begin with sector0, configure [SMHC_BYTCNT \(Offset: 0x0014\)](#) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 command (Multiple Data Blocks Read) to 0x0, write 0x80003352 to [SMHC_CMD \(Offset: 0x0018\)](#), and send CMD18 command to read data to the device. When the data transfer is completed, CMD12 will be sent automatically.
4. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.
5. Check whether [SMHC_IDST \(Offset: 0x0088\)](#) [RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to [SMHC_IDST \(Offset: 0x0088\)](#) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
6. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [ACD] and [SMHC_RINTSTS \(Offset: 0x0038\)](#) [DTC] are both 1. If yes, data transfer, CMD12 transfer, and CMD18 reading operation are completed. Otherwise, abnormality exists. Read [SMHC_RINTSTS \(Offset: 0x0038\)](#) and [SMHC_STATUS \(Offset: 0x003C\)](#) to query the existing abnormality.

4.2.4.6 Writing Pre-Defined Multiple Data Blocks (CMD23 + CMD25)

To write pre-defined multiple data blocks, follow the steps below:

1. Write 0x1 to [SMHC_CTRL \(Offset: 0x0000\)](#) [DMA_RST] to reset the internal DMA controller; write 0x82 to [SMHC_DMAC \(Offset: 0x0080\)](#) to enable the IDMAC interrupt and configure AHB master burst transfers; configure [SMHC_IDIE \(Offset: 0x008C\)](#) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure [SMHC_FIFOTH \(Offset: 0x0040\)](#) to determine the burst size and TX/RX trigger level. For example, if [SMHC_FIFOTH \(Offset: 0x0040\)](#) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure [SMHC_DLBA \(Offset: 0x0084\)](#) to determine the start address of the DMA descriptor.
3. To write three blocks of data, configure [SMHC_CMDARG \(Offset: 0x001C\)](#) to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to [SMHC_CMD \(Offset: 0x0018\)](#) to send the CMD23 command. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

4. Configure [SMHC_BYTCNT \(Offset: 0x0014\)](#) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80002759 to [SMHC_CMD \(Offset: 0x0018\)](#), and send CMD25 command to write data to the device.
5. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.
6. Check whether [SMHC_IDST \(Offset: 0x0088\)](#) [TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to [SMHC_IDST \(Offset: 0x0088\)](#) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
7. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [DTC] is 1. If yes, the data transfer and CMD25 writing operations are completed. Otherwise, abnormality exists. Read [SMHC_RINTSTS \(Offset: 0x0038\)](#) and [SMHC_STATUS \(Offset: 0x003C\)](#) to query the existing abnormality.
8. Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set [SMHC_CMDARG \(Offset: 0x001C\)](#) to 0x12340000, write 0x8000014D to [SMHC_CMD \(Offset: 0x0018\)](#), go to step 4 to ensure command transfer completed, and then check whether the highest bit of [SMHC_RESP0 \(Offset: 0x0020\)](#) (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

4.2.4.7 Reading Pre-Defined Multiple Data Blocks (CMD23 + CMD18)

To read pre-defined multiple data blocks, follow the steps below:

1. Write 0x1 to [SMHC_CTRL \(Offset: 0x0000\)](#) [DMA_RST] to reset the internal DMA controller; write 0x82 to [SMHC_DMAC \(Offset: 0x0080\)](#) to enable the IDMAC interrupt and configure AHB master burst transfers; configure [SMHC_IDIE \(Offset: 0x008C\)](#) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure [SMHC_FIFOTH \(Offset: 0x0040\)](#) to determine the burst size and TX/RX trigger level. For example, if [SMHC_FIFOTH \(Offset: 0x0040\)](#) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure [SMHC_DLBA \(Offset: 0x0084\)](#) to determine the start address of the DMA descriptor.
3. To read three blocks of data, configure [SMHC_CMDARG \(Offset: 0x001C\)](#) to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to [SMHC_CMD \(Offset: 0x0018\)](#) to send the CMD23 command. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.
4. Configure [SMHC_BYTCNT \(Offset: 0x0014\)](#) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 (Multiple Data Blocks Read) to 0x0, write 0x80002352 to [SMHC_CMD \(Offset: 0x0018\)](#), and send CMD18 command to read data from device to DRAM/SRAM.
5. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

6. Check whether [SMHC_IDST \(Offset: 0x0088\)](#) [TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to [SMHC_IDST \(Offset: 0x0088\)](#) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
7. Check whether [SMHC_RINTSTS \(Offset: 0x0038\)](#) [DTC] is 1. If yes, the data transfer and CMD18 writing operations are completed. Otherwise, abnormality exists. Read [SMHC_RINTSTS \(Offset: 0x0038\)](#) and [SMHC_STATUS \(Offset: 0x003C\)](#) to query the existing abnormality.

4.2.5 Register List

Module Name	Base Address	Comments
SMHC0	0x04020000	
SMHC1	0x04021000	SMHC1 register is the same with SMHC0
SMHC2	0x04022000	SMHC2 register is the same with SMHC0

Register Name	Offset	Description
SMHC_CTRL	0x0000	SMHC Global Control Register
SMHC_CLKDIV	0x0004	SMHC Clock Control Register
SMHC_TMOUT	0x0008	SMHC Timeout Register
SMHC_CTYPE	0x000C	SMHC Bus Width Register
SMHC_BLKSIZ	0x0010	SMHC Block Size Register
SMHC_BYTCNT	0x0014	SMHC Byte Count Register
SMHC_CMD	0x0018	SMHC Command Register
SMHC_CMDARG	0x001C	SMHC Command Argument Register
SMHC_RESP0	0x0020	SMHC Response 0 Register
SMHC_RESP1	0x0024	SMHC Response 1 Register
SMHC_RESP2	0x0028	SMHC Response 2 Register
SMHC_RESP3	0x002C	SMHC Response 3 Register
SMHC_INTMASK	0x0030	SMHC Interrupt Mask Register
SMHC_MINTSTS	0x0034	SMHC Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	SMHC Raw Interrupt Status Register
SMHC_STATUS	0x003C	SMHC Status Register
SMHC_FIFOTH	0x0040	SMHC FIFO Water Level Register
SMHC_FUNS	0x0044	SMHC FIFO Function Select Register
SMHC_TBC0	0x0048	SMHC Transferred Byte Count Register 0
SMHC_TBC1	0x004C	SMHC Transferred Byte Count Register 1
SMHC_CSDC	0x0054	SMHC CRC Status Detect Control Register
SMHC_A12A	0x0058	SMHC Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SMHC New Timing Set Register
SMHC_HWRST	0x0078	SMHC Hardware Reset Register
SMHC_DMAC	0x0080	SMHC DMAC Control Register
SMHC_DLBA	0x0084	SMHC Descriptor List Base Address Register
SMHC_IDST	0x0088	SMHC DMAC Status Register

Register Name	Offset	Description
SMHC_IDIE	0x008C	SMHC DMAC Interrupt Enable Register
SMHC_THLD	0x0100	SMHC Card Threshold Control Register
SMHC_SFC	0x0104	SMHC Sample FIFO Control Register
SMHC_A23A	0x0108	SMHC Auto Command 23 Argument Register
SMHC_EXT_CMD	0x0138	SMHC Extended Command Register
SMHC_EXT RESP	0x013C	SMHC Extended Response Register
SMHC_DRV_DL	0x0140	SMHC Drive Delay Control Register
SMHC_SAMP_DL	0x0144	SMHC Sample Delay Control Register
SMHC_DS_DL	0x0148	SMHC Data Strobe Delay Control Register
SMHC_FIFO	0x0200	SMHC FIFO Register

4.2.6 Register Description

4.2.6.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this field should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
8	R/W	0x1	CD_DBC_ENB Card Detect (Data [3] status) De-bounce Enable 0: disable de-bounce 1: enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

4.2.6.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MASK_DAT0 Mask Data0 0: Do not mask data0 when update clock; 1: Mask data0 when update clock;
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1 : Turn off card clock when FSM in IDLE state

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

4.2.6.3 0x0008 SMHC Timeout Register (Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0xffffffff	<p>DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device, this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command (ACMD51, CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect. Note: Under the following 3 conditions, the timeout limit is half of the set time. 1> DDR8 mode 2> DDR4 and SMHC_NTSR[MODE_SELEC] (0x5C [31]) high 3> HS400 and SMHC_NTSR[HS400_NEW_SAMPLE_EN](0x5C[0]) high</p>
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

4.2.6.4 0x000C SMHC Bus Width Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

4.2.6.5 0x0010 SMHC Block Size Register (Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

4.2.6.6 0x0014 SMHC Byte Count Register (Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

4.2.6.7 0x0018 SMHC Command Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit will be set in SMHC_RINTSTS register. You should not write any other command before this bit is cleared.
30:29	/	/	/

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABТ Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABТ_CMD Stop Abort Command 0: normal command sending 1: send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command

Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bits) 1: Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

4.2.6.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CMD_ARG Command argument

4.2.6.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

4.2.6.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

4.2.6.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

4.2.6.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

4.2.6.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

4.2.6.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	M_CARD_REMOVAL_INT Card Removed

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
30	R	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token or received CRC status token is negative.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M.DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M.RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M.DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative.
6	R	0x0	M.RCE_INT Response CRC Error

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

4.2.6.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token or received CRC status token is negative. This is write-1-to-clear bits.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. It is valid at 4-bit or 8-bit bus mode, when it set, host found start bit at data0, but not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared after the last block. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0(1-bit bus) or data0~data3(4-bit bus) or data0~data7(8-bit bus). This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

4.2.6.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA [0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data [3] status level of DATA [3]; checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA Command FSM states: 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn't reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn't reach receive trigger level 1: FIFO reached receive trigger level

4.2.6.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD(4Byte). A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: BSIZE_OF_TRANS = 3, MSize = 16, TX_TL = 240, RX_TL = 15 FIFO_DEPTH = 256 FIFO_SIZE = 256 * 32 = 1K
27:24	R	0x0	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. 15 (means greater than 15)
15:8	R	0x0	/

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	<p>TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240) 240(means less than or equal to 240)</p>

4.2.6.18 0x0044 SMHC FIFO Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	<p>ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.</p>
1	R/W	0x0	<p>READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait</p>
0	R/W	0x0	<p>HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.</p>

4.2.6.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.2.6.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.2.6.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA CRC Detect Para 110: HS400 speed mode 011: Other speed mode Others: Reserved

4.2.6.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFF	A12A Auto CMD12 Argument The argument of command 12 automatically send by controller with this field.

4.2.6.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MODE_SEL Mode Select 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:26	/	/	/
25	R/W	0x0	BOOT_DAT_RX_PHASE_CLR After boot ack, before receive boot data, clear data lines' input phase. 0: Disable 1: Enable
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock operation, clear command line's and data lines' input phase. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines' input phase. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines' input phase. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines' input phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command RX phase clear 0: Disable 1: Enable
15:10	/	/	/

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	DAT_SAM_TIM_PHS Data Sample Timing Phase 00: Sample timing phase offset 90° 01: Sample timing phase offset 180° 10: Sample timing phase offset 270° 11: Sample timing phase offset 0° (only for SD2 hs400 mode) Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAM_TIM_PHS Command Sample Timing Phase 00: Sample timing phase offset 90° 01: Sample timing phase offset 180° 10: Sample timing phase offset 270° 11: Ignore Default value: 00
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAM_EN HS400 New Sample Enable 1: enable hs400 new sample method 0: disable hs400 new sample method

4.2.6.24 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	HW_RST Hardware Reset 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

4.2.6.25 0x0080 SMHC DMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	Read/Write	Default/Hex	Description
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

4.2.6.26 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor. It is a word(4byte) address

4.2.6.27 0x0088 SMHC DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
16:13	R	0x0	Reserved
12:10	R	0x0	<p>DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (SMHC_IDST [2]) set. This field does not generate an interrupt.</p> <p>001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved This bit is read-only.</p>
9	R/W1C	0x0	<p>AIS Abnormal Interrupt Summary. Logical OR of the following: SMHC_IDST [2]: Fatal Bus Interrupt SMHC_IDST [4]: Descriptor unavailable bit Interrupt SMHC_IDST [5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.</p>
8	R/W1C	0x0	<p>NIS Normal Interrupt Summary. Logical OR of the following: SMHC_IDST [0]: Transmit Interrupt SMHC_IDST [1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.</p>
7:6	/	/	/
5	R/W1C	0x0	<p>ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.</p>

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DESO[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (SMHC_IDST [12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.

4.2.6.28 0x008C SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	Reserved
8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set, Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set, Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

4.2.6.29 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	CARD_WR_THLD Card Read/write Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disable 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

4.2.6.30 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
4:1	R/W	0x3	<p>STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving.</p> <p>This field is used to control the position of stopping clock. The value can be change between 0x0 and 0xF, but actually the available value and the position of stopping clock must be decided by the actual situation.</p> <p>The value increase one in this field is linked to one cycle(two cycle in DDR mode) that the position of stopping clock moved up.</p>
0	R/W	0x0	<p>BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.</p>

4.2.6.31 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.</p>

4.2.6.32 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.</p>
30:1	/	/	/

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	<p>HALF_START_BIT Control for start bit detection mechanism inside host controller based on duration of start bit.</p> <p>For eMMC 4.5, start bit can be:</p> <p>0: Full cycle 1: Less than one full cycle</p> <p>Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.</p>

4.2.6.33 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	<p>AUTO_CMD23_EN Send CMD23 Automatically</p> <p>When set this bit, send CMD23 automatically before send command specified in SMHC_CMD register.</p> <p>When SOFT_RST set, this field will be cleared.</p>

4.2.6.34 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	<p>SMHC_EXT_RESP</p> <p>When AUTO_CMD23_EN is set, this register stores the response of CMD23.</p>

4.2.6.35 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	<p>DAT_DRV_PH_SEL Data Drive Phase Select</p> <p>0: Data drive phase offset is: 90° at SDR mode, 45° at DDR8 mode, 90° at DDR4 mode when 0x5C[31] is low, 45° at DDR4 mode when 0x5C[31] is high, 90° at HS400 mode when 0x5C[0] is low, 45° at HS400 mode when 0x5C[0] is high.</p> <p>1: Data drive phase offset is: 180° at SDR mode, 90° at DDR8 mode, 180° at DDR4 mode when 0x5C[31] is low, 90° at DDR4 mode when 0x5C[31] is high, 180° at HS400 mode when 0x5C[0] is low, 90° at HS400 mode when 0x5C[0] is high.</p>
16	R/W	0x1	<p>CMD_DRV_PH_SEL Command Drive Phase Select</p> <p>0: Command drive phase offset is: 90° at SDR mode, 45° at DDR8 mode, 90° at DDR4 mode when 0x5C[31] is low, 45° at DDR4 mode when 0x5C[31] is high, 90° at HS400 mode</p> <p>1: Command drive phase offset is: 180° at SDR mode, 90° at DDR8 mode, 180° at DDR4 mode when 0x5C[31] is low, 90° at DDR4 mode when 0x5C[31] is high, 180° at HS400 mode.</p>
15:0	/	/	/

4.2.6.36 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	<p>SAMP_DL_CAL_START Sample Delay Calibration Start</p> <p>When set, start sample delay chain calibration.</p>

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

4.2.6.37 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

4.2.6.38 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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5 Video and Graphics

5.1 Display Engine (DE)

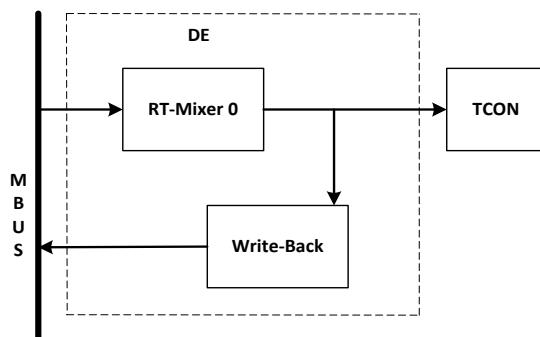
The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports three-channel windows to blend, and supports image post-processing in the video channel.

The DE has the following features:

- Supports output size up to 2048x2048
- Supports three alpha blending channels for main display and each channel has independent scaler
- Supports four overlay layers for each channel
- Supports potter-duff compatible blending operation
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Supports input format palette only for UI channel
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
 - Adaptive color enhancement (Blue-stretch, Green-stretch and fresh tone correction) and flesh tone protection
 - Hue gain, Saturation gain, and Value gain controlled
 - Fully programmable color matrix
 - Dynamic gamma
- Supports write back only for verification.

The following figure shows the diagram of DE system.

Figure 5-1 DE System Block Diagram



5.2 Graphic 2D Engine (G2D)

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Supports layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer

5.3 Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPGE). The VE supports H.264 and H.265 encoding, and JPGE supports JPEG/MJPEG encoding.

5.3.1 VE

The VE is a CODEC that supports H.264 and H.265 protocol based on ASIC. It is custom-made for the IPC usage and features high compressing rate, low CPU usage, short delay and low power consumption.

The VE has the following features:

- Supports 1TU-T H.265 Main Profile @Level 6.0 Main-Tier encoding
 - Motion compensation with 1/2 or 1/4 pixel precision
 - Four prediction unit (PU) types of 16x16, 16x8, 8x16 and 8x8 for inter-prediction
 - Three PU types of 16x16, 8x8 and 4x4 for intra-prediction
 - Max merge candidate number is 2
 - Supports three transform uinit size: 16x16, 8x8 and 4x4
 - De-blocking filtering
- Supports 1TU-T H.264 high profile /Main Profile/baseline profile @Level 5.0 encoding.
 - Motion compensation with 1/2 or 1/4 pixel precision
 - Four prediction unit (PU) types of 16x16, 16x8, 8x16 and 8x8 for inter-prediction
 - Three PU types of 16x16, 8x8 and 4x4 for intra-frame
 - Transform 4x4 and transform 8x8
 - CABAC and CAVLC entropy encoding
 - De-blocking filtering
 - Multi-slice encoding
- Supports QpMap function.
- Supports special functions: variable frame rate (VFR), 2-D filtering, dynamic search window range
- Supports normal functions: Macroblock rate control, 2D and 3D denoising, intrarefresh, inter-only-in-P-frame
- Statistical information output based on 16x16 QP\mad\sse
- Supports output picture format of semi-planar YCbCr4:2:0.
- picture resolutions
 - Minimum picture resolution: 64x64 for I frame, 176x32 for P frame.

- Maximum picture resolution: 4096x4096
- Supports region of interest(ROI) encoding.
 - A maximum of eight ROIs
 - Independent enable/disable control for the encoding function of each ROI
- Supports three bit rate control modes: constant bit rate(CBR), variable bit rate(VBR), and FIXEDQP.
- Supports the output bit rate ranging from 2 Kbit/s to 100 Mbit/s.
- Supports loss and lossless compression for reference frame.
- Supports OSD front-end overlaying.
 - OSD overlaying before encoding for a maximum of sixty-four regions
 - OSD overlaying with any size and at any position (within the size and position ranges of the picture)
 - Supports four adaptive anti-color modes and optional width/height of 16, 32 or 64 for anti-color units
 - OSD overlaying control (enabled or disabled)
- input frame supports loss and lossless compression mode

5.3.2 JPEG

The JPGE is a high-performance JPEG encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPGE has the following features:

- ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
 - Supports multiple input picture formats:
 - › Semi-planar YCbCr4:2:0
 - › YCbCr4:2:2
 - › YCbCr4:4:4
 - Supports configurable picture resolutions:
 - › Minimum picture resolution: 192x96
 - › Maximum picture resolution: 8192x8192
 - Supports configurable quantization tables.
 - › An independent quantization table for the Y component, Cb component, and Cr component respectively.
- Supports OSD front-end overlaying.
 - OSD overlaying before encoding for a maximum of sixty-four regions

- OSD overlaying with any size and at any position (within the size and position ranges of the picture)
 - Supports four adaptive anti-color modes and optional width/height of 16, 32 or 64 for anti-color units
 - OSD overlaying control (enabled or disabled)
- input frame supports loss and lossless compression mode



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6 Video Input Interfaces

6.1 CSIC

6.1.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface and store the data in memory directly.

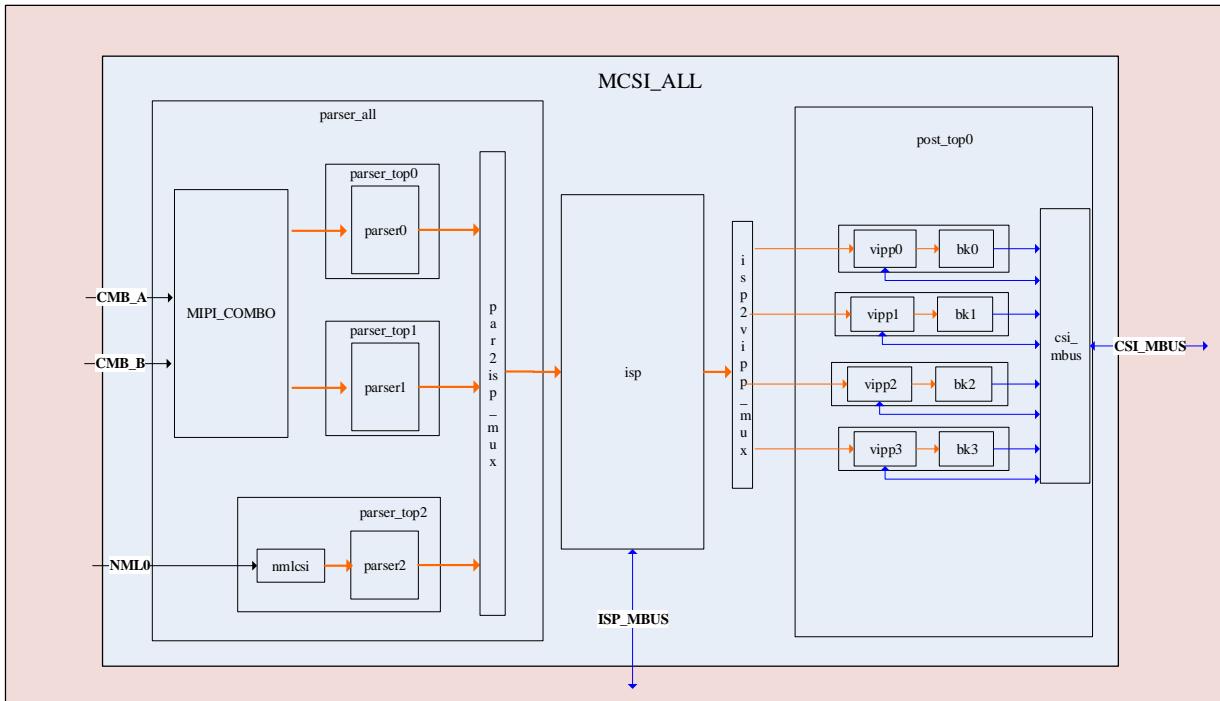
The CSIC includes the following features:

- Supports one 4-lane or two 2-lane MIPI Interface
 - Supports MIPI CSI2 V1.1 and MIPI DPHY V1.1
 - Supports 1.2 Gbps/lane
- Supports 12-bit digital camera interface
- Supports BT656 and BT1120 interface
 - Supports time-multiplexed format
 - Supports dual data rate sample mode with pixel clock up to 148.5MHz
- Supports BT601 Interface
- Supports crop function
- Supports frame rate down
- Supports 4 DMA for 4 video stream storage
 - Supports deinterlacing for interlace video input
 - Supports conversion for YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
 - Supports horizontal and vertical flip

6.1.2 Block Diagram

The following shows block diagram of the CSIC.

Figure 6-1 CSIC Block Diagram



6.1.3 Functional Description

6.1.3.1 External Signals

Table 6-1 CSIC External Signals

Signal	Description	Type
MIPI CSI		
MIPI_MCLK0	MIPIO Sensor reference clock	O
MIPI_MCLK1	MIPI1 Sensor reference clock	O
CSI_SM_VS	Sensor External Vsync/ Frame Sync	O
CSI_SM_HS	Sensor External Hsync	O
MIPIA-CSI-CKON	MIPI CSI controller A clock negative signal	AI
MIPIA-CSI-CKOP	MIPI CSI controller A clock positive signal	AI
MIPIA-CSI-DON	MIPI CSI controller A data0 negative signal	AI
MIPIA-CSI-DOP	MIPI CSI controller A data0 positive signal	AI
MIPIA-CSI-D1N	MIPI CSI controller A data1 negative signal	AI
MIPIA-CSI-D1P	MIPI CSI controller A data1 positive signal	AI
MIPIB-CSI-CKON	MIPI CSI controller B clock negative signal	AI
MIPIB-CSI-CKOP	MIPI CSI controller B clock positive signal	AI

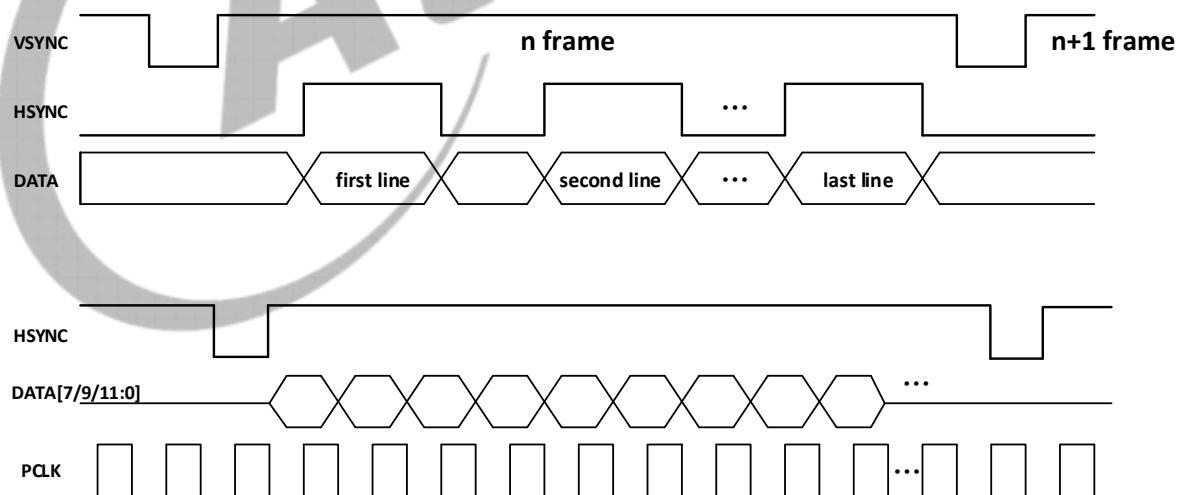
Signal	Description	Type
MIPIB-CSI-D0N/MIPIA-CSI-D2N	MIPI CSI controller B data0 negative signal/MIPI CSI controller A data2 negative signal	AI
MIPIB-CSI-D0P/MIPIA-CSI-D2P	MIPI CSI controller B data0 positive signal/MIPI CSI controller A data2 positive signal	AI
MIPIB-CSI-D1N/MIPIA-CSI-D3N	MIPI CSI controller B data1 negative signal/MIPI CSI controller A data3 negative signal	AI
MIPIB-CSI-D1P/MIPIA-CSI-D3P	MIPI CSI controller B data1 positive signal/MIPI CSI controller A data3 positive signal	AI
Parallel CSI		
NCSI_MCLK	Parallel CSI Master Clock	O
NCSI_PCLK	Parallel CSI Pixel Clock	I
NCSI_VSYNC	Parallel CSI Vertical Synchronous	I
NCSI_HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI_D[15:0]	Parallel CSI Data Bit	I

6.1.3.2 Typical Application

CSIC Input Timing

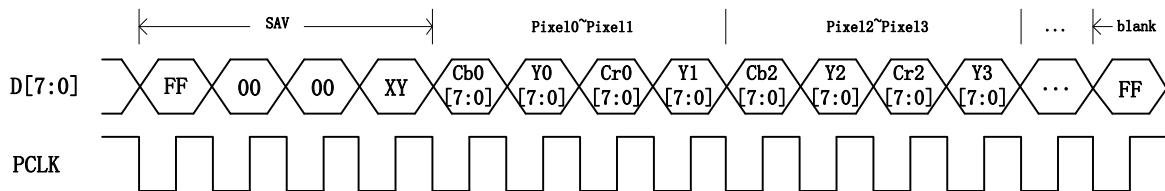
The following figure shows the timing of 8bit CMOS Sensor Interface, in this figure clock active at the rising edge, VSYNC valid at positive, HSYNC valid at positive.

Figure 6-2 8-bit DC Sensor Interface Timing



The following figure shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT656).

Figure 6-3 8-bit YCbCr4:2:2 with embedded syncs (BT656)



The following table shows the header code of BT656.

Table 6-2 BT656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

The following table shows the Header Data Bit Definition of BT656.

Table 6-3 BT656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

CSIC Memory Storage

The following table describes the memory storage of pixel data.

Table 6-4 CSIC Memory Storages

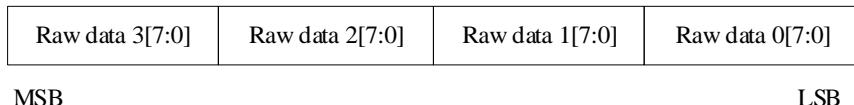
Input format	YUV422/YUV420		Raw
Output format	Planar	UV combined	Raw
FIFO0	Y	Y	All pixels data
FIFO1	Cb (U)	CbCr (UV)	-

Input format	YUV422/YUV420		Raw
FIFO2	Cr (V)	-	-

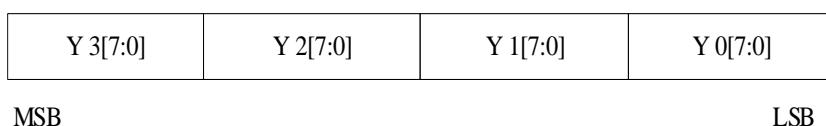
The following figure shows the Pixel Format Arrangement.

Figure 6-4 Pixel Format Arrangement

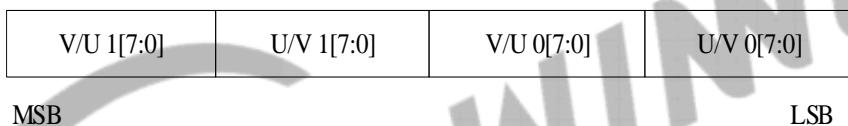
RAW-8:



Y:



UV Combined:



6.1.3.3 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

For YUV422 format, pixel unit is a YU/YV combination.

For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.

For Bayer and RAW format, pixel unit is a R/G/B single component.

For RGB565, pixel unit is 2 bytes of RGB565 package.

For RGB888, pixel unit is 3 bytes of RGB combination.

6.1.3.4 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of Y0U0Y1V1 will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of Y1U0Y0V1 will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

6.1.4 Register List

Module Name	Base Address	Comments
CSIC_CCU	0x05800000	
CSIC_TOP	0x05800800	
CSIC_PARSER0	0x05820000	
CSIC_PARSER1	0x05821000	CSIC_PARSER1 register is the same with CSIC_PARSER0.
CSIC_PARSER2	0x05822000	CSIC_PARSER2 register is the same with CSIC_PARSER0.
CSIC_DMA0	0x05830000	
CSIC_DMA1	0x05831000	CSIC_DMA1 register is the same with CSIC_DMA0.
CSIC_DMA2	0x05832000	CSIC_DMA2 register is the same with CSIC_DMA0.
CSIC_DMA3	0x05833000	CSIC_DMA3 register is the same with CSIC_DMA0.
Register Name	Offset	Description
CSIC_CCU		
CSIC_CCU_CLK_MODE_REG	0x0000	CSIC CCU Clock Mode Register
CSIC_CCU_PARSER_CLK_EN_REG	0x0004	CSIC CCU Parser Clock Enable Register
CSIC_CCU_POST0_CLK_EN_REG	0x000C	CSIC CCU Post0 Clock Enable Register
CSIC_TOP		
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISPO_INPUT0_SEL_REG	0x0030	CSIC ISPO Input0 Select Register
CSIC_ISPO_INPUT1_SEL_REG	0x0034	CSIC ISPO Input1 Select Register
CSIC_ISPO_INPUT2_SEL_REG	0x0038	CSIC ISPO Input2 Select Register
CSIC_ISPO_INPUT3_SEL_REG	0x003C	CSIC ISPO Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_BIST_CTRL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_ADDR_REG	0x00E4	CSIC BIST Start Address Register
CSIC_BIST_END_ADDR_REG	0x00E8	CSIC BIST End Address Register

Register Name	Offset	Description
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_FEATURE_LIST_REG	0x01F0	CSIC Feature List Register
CSIC_PARSER0		
CSIC_PRS_EN_REG	0x0000	CSIC Parser Enable Register
CSIC_PRS_NCSIC_IF_CFG_REG	0x0004	CSIC Parser NCSIC Interface Configuration Register
CSIC_PRS_CAP_REG	0x000C	CSIC Parser Capture Register
CSIC_PRS_SIGNAL_STA_REG	0x0010	CSIC Parser Signal Status Register
CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	CSIC Parser NCSIC BT656 Header Configuration Register
CSIC_PRS_CHO_INFMT_REG	0x0024	CSIC Parser Channel_0 Input Format Register
CSIC_PRS_CHO_OUTPUT_HSIZE_REG	0x0028	CSIC Parser Channel_0 Output Horizontal Size Register
CSIC_PRS_CHO_OUTPUT_VSIZE_REG	0x002C	CSIC Parser Channel_0 Output Vertical Size Register
CSIC_PRS_CHO_INPUT_PARAO_REG	0x0030	CSIC Parser Channel_0 Input Parameter0 Register
CSIC_PRS_CHO_INPUT_PARA1_REG	0x0034	CSIC Parser Channel_0 Input Parameter1 Register
CSIC_PRS_CHO_INPUT_PARA2_REG	0x0038	CSIC Parser Channel_0 Input Parameter2 Register
CSIC_PRS_CHO_INPUT_PARA3_REG	0x003C	CSIC Parser Channel_0 Input Parameter3 Register
CSIC_PRS_CHO_INT_EN_REG	0x0040	CSIC Parser Channel_0 Interrupt Enable Register
CSIC_PRS_CHO_INT_STA_REG	0x0044	CSIC Parser Channel_0 Interrupt Status Register
CSIC_PRS_CHO_LINE_TIME_REG	0x0048	CSIC Parser Channel_0 Line Time Register
CSIC_PRS_CH1_INFMT_REG	0x0124	CSIC Parser Channel_1 Input Format Register
CSIC_PRS_CH1_OUTPUT_HSIZE_REG	0x0128	CSIC Parser Channel_1 Output Horizontal Size Register
CSIC_PRS_CH1_OUTPUT_VSIZE_REG	0x012C	CSIC Parser Channel_1 Output Vertical Size Register
CSIC_PRS_CH1_INPUT_PARAO_REG	0x0130	CSIC Parser Channel_1 Input Parameter0 Register
CSIC_PRS_CH1_INPUT_PARA1_REG	0x0134	CSIC Parser Channel_1 Input Parameter1 Register
CSIC_PRS_CH1_INPUT_PARA2_REG	0x0138	CSIC Parser Channel_1 Input Parameter2 Register
CSIC_PRS_CH1_INPUT_PARA3_REG	0x013C	CSIC Parser Channel_1 Input Parameter3 Register
CSIC_PRS_CH1_INT_EN_REG	0x0140	CSIC Parser Channel_1 Interrupt Enable Register
CSIC_PRS_CH1_INT_STA_REG	0x0144	CSIC Parser Channel_1 Interrupt Status Register
CSIC_PRS_CH1_LINE_TIME_REG	0x0148	CSIC Parser Channel_1 Line Time Register
CSIC_PRS_CH2_INFMT_REG	0x0224	CSIC Parser Channel_2 Input Format Register
CSIC_PRS_CH2_OUTPUT_HSIZE_REG	0x0228	CSIC Parser Channel_2 Output Horizontal Size Register
CSIC_PRS_CH2_OUTPUT_VSIZE_REG	0x022C	CSIC Parser Channel_2 Output Vertical Size Register
CSIC_PRS_CH2_INPUT_PARAO_REG	0x0230	CSIC Parser Channel_2 Input Parameter0 Register
CSIC_PRS_CH2_INPUT_PARA1_REG	0x0234	CSIC Parser Channel_2 Input Parameter1 Register
CSIC_PRS_CH2_INPUT_PARA2_REG	0x0238	CSIC Parser Channel_2 Input Parameter2 Register
CSIC_PRS_CH2_INPUT_PARA3_REG	0x023C	CSIC Parser Channel_2 Input Parameter3 Register
CSIC_PRS_CH2_INT_EN_REG	0x0240	CSIC Parser Channel_2 Interrupt Enable Register

Register Name	Offset	Description
CSIC_PRS_CH2_INT_STA_REG	0x0244	CSIC Parser Channel_2 Interrupt Status Register
CSIC_PRS_CH2_LINE_TIME_REG	0x0248	CSIC Parser Channel_2 Line Time Register
CSIC_PRS_CH3_INFMT_REG	0x0324	CSIC Parser Channel_3 Input Format Register
CSIC_PRS_CH3_OUTPUT_HSIZE_REG	0x0328	CSIC Parser Channel_3 Output Horizontal Size Register
CSIC_PRS_CH3_OUTPUT_VSIZE_REG	0x032C	CSIC Parser Channel_3 Output Vertical Size Register
CSIC_PRS_CH3_INPUT_PARAO_REG	0x0330	CSIC Parser Channel_3 Input Parameter0 Register
CSIC_PRS_CH3_INPUT_PARA1_REG	0x0334	CSIC Parser Channel_3 Input Parameter1 Register
CSIC_PRS_CH3_INPUT_PARA2_REG	0x0338	CSIC Parser Channel_3 Input Parameter2 Register
CSIC_PRS_CH3_INPUT_PARA3_REG	0x033C	CSIC Parser Channel_3 Input Parameter3 Register
CSIC_PRS_CH3_INT_EN_REG	0x0340	CSIC Parser Channel_3 Interrupt Enable Register
CSIC_PRS_CH3_INT_STA_REG	0x0344	CSIC Parser Channel_3 Interrupt Status Register
CSIC_PRS_CH3_LINE_TIME_REG	0x0348	CSIC Parser Channel_3 Line Time Register
CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	CSIC Parser NCSIC RX Signal0 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	CSIC Parser NCSIC RX Signal5 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	CSIC Parser NCSIC RX Signal6 Delay Adjust Register
CSIC_PRS_SYNC_EN_REG	0x0520	CSIC Parser SYNC EN Register
CSIC_PRS_SYNC_CFG_REG	0x0524	CSIC Parser SYNC CFG Register
SIC_PRS_VS_WAIT_N_REG	0x0528	CSIC Parser VS WAIT N Register
CSIC_PRS_VS_WAIT_M_REG	0x052C	CSIC Parser VS WAIT M Register
CSIC_PRS_XSYNC_ENABLE_REG	0x0540	CSIC Parser XSYNC ENABLE Register
CSIC_PRS_XVS_PERIOD_REG	0x0544	CSIC Parser XVS Period Register
CSIC_PRS_XHS_PERIOD_REG	0x0548	CSIC Parser XHS Period Register
CSIC_PRS_XVS_LENGTH_REG	0x054C	CSIC Parser XVS LENGTH Register
CSIC_PRS_XHS_LENGTH_REG	0x0550	CSIC Parser XHS LENGTH Register
CSIC_PRS_SYNC_DLY_REG	0x0554	CSIC Parser SYNC DELAY Register
CSIC_DMA0		
CSIC_DMA_TOP_REG	0x0000	CSIC DMA TOP Register
CSIC_DMA_MUL_CH_CFG_REG	0x0004	CSIC DMA Multi-Channel Configuration Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0010	CSIC DMA Frame Rate Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0014	CSIC DMA Accumulated and Internal Clock Counter Register
CSIC_DMA_FS_FRM_CNT_REG	0x0020	CSIC DMA Fsync Frame Counter Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_VE_FRM_CNT_REG	0x0050	CSIC DMA VE Frame Counter Value Register
CSIC_DMA_VE_LINE_CNT_REG	0x0054	CSIC DMA VE Line Counter Value Register

Register Name	Offset	Description
CSIC_DMA_VE_CUR_FRM_ADDR_REG	0x0058	CSIC DMA VE Current Frame Address Register
CSIC_DMA_VE_LAST_FRM_ADDR_REG	0x005C	CSIC DMA VE Last Frame Address Register
CSIC_DMA_FIFO_STAT_REG	0x0080	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x0084	CSIC DMA FIFO Threshold Register
CSIC_DMA_TOP_INT_EN_REG	0x0100	CSIC DMA TOP Interrupt Enable Register
CSIC_DMA_TOP_INT_STA_REG	0x0104	CSIC DMA TOP Interrupt Status Register
CSIC_DMA_FEATURE_REG	0x01F4	CSIC DMA Feature List Register
CSIC_DMA_CH0_EN_REG	0x0200	CSIC DMA Channel0 Enable Register
CSIC_DMA_CH0_CFG_REG	0x0204	CSIC DMA Channel0 Configuration Register
CSIC_DMA_CH0_FRM_LOST_CNT_REG	0x0208	CSIC DMA Channel0 Frame Lost Counter Register
CSIC_DMA_CH0_HSIZE_REG	0x0210	CSIC DMA Channel0 Horizontal Size Register
CSIC_DMA_CH0_VSIZE_REG	0x0214	CSIC DMA Channel0 Vertical Size Register
CSIC_DMA_CH0_F0_BUFA_REG	0x0220	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH0_F0_BUFA_RESULT_REG	0x0224	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F1_BUFA_REG	0x0228	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH0_F1_BUFA_RESULT_REG	0x022C	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F2_BUFA_REG	0x0230	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH0_F2_BUFA_RESULT_REG	0x0234	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH0_BUF_LEN_REG	0x0238	CSIC DMA Channel0 Buffer Length Register
CSIC_DMA_CH0_FLIP_SIZE_REG	0x023C	CSIC DMA Channel0 Flip Size Register
CSIC_DMA_CH0_CAP_STA_REG	0x024C	CSIC DMA Channel0 Capture Status Register
CSIC_DMA_CH0_INT_EN_REG	0x0250	CSIC DMA Channel0 Interrupt Enable Register
CSIC_DMA_CH0_INT_STA_REG	0x0254	CSIC DMA Channel0 Interrupt Status Register
CSIC_DMA_CH0_LINE_CNT_REG	0x0258	CSIC DMA Channel0 Line Counter Register
CSIC_DMA_CH0_LINE_STAT_REG	0x0268	CSIC DMA Channel0 Line Statistic Register
CSIC_DMA_CH0_PCLK_STAT_REG	0x0270	CSIC DMA Channel0 PCLK Statistic Register
CSIC_LBC_CH0_CONFIG_REG	0x0300	CSIC LBC Channel0 Configure Register
CSIC_LBC_CH0_LINE_TAR_BIT0_REG	0x0304	CSIC LBC Channel0 Line Target Bit0 Register
CSIC_LBC_CH0_LINE_TAR_BIT1_REG	0x0308	CSIC LBC Channel0 Line Target Bit1 Register
CSIC_LBC_CH0_RC_ADV_REG	0x030C	CSIC LBC Channel0 RC ADV Register
CSIC_LBC_CH0_MB_MIN_REG	0x0310	CSIC LBC Channel0 MB MIN Register
CSIC_DMA_CH1_EN_REG	0x0400	CSIC DMA Channel1 Enable Register

Register Name	Offset	Description
CSIC_DMA_CH1_CFG_REG	0x0404	CSIC DMA Channel1 Configuration Register
CSIC_DMA_CH1_FRM_LOST_CNT_REG	0x0408	CSIC DMA Channel1 Frame Lost Counter Register
CSIC_DMA_CH1_HSIZE_REG	0x0410	CSIC DMA Channel1 Horizontal Size Register
CSIC_DMA_CH1_VSIZE_REG	0x0414	CSIC DMA Channel1 Vertical Size Register
CSIC_DMA_CH1_F0_BUFA_REG	0x0420	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH1_F0_BUFA_RESULT_REG	0x0424	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F1_BUFA_REG	0x0428	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH1_F1_BUFA_RESULT_REG	0x042C	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F2_BUFA_REG	0x0430	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH1_F2_BUFA_RESULT_REG	0x0434	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH1_BUF_LEN_REG	0x0438	CSIC DMA Channel1 Buffer Length Register
CSIC_DMA_CH1_FLIP_SIZE_REG	0x043C	CSIC DMA Channel1 Flip Size Register
CSIC_DMA_CH1_CAP_STA_REG	0x044C	CSIC DMA Channel1 Capture Status Register
CSIC_DMA_CH1_INT_EN_REG	0x0450	CSIC DMA Channel1 Interrupt Enable Register
CSIC_DMA_CH1_INT_STA_REG	0x0454	CSIC DMA Channel1 Interrupt Status Register
CSIC_DMA_CH1_LINE_CNT_REG	0x0458	CSIC DMA Channel1 Line Counter Register
CSIC_DMA_CH1_LINE_STAT_REG	0x0468	CSIC DMA Channel1 Line Statistic Register
CSIC_DMA_CH1_PCLK_STAT_REG	0x0470	CSIC DMA Channel1 PCLK Statistic Register
CSIC_LBC_CH1_CONFIG_REG	0x0500	CSIC LBC Channel1 Configure Register
CSIC_LBC_CH1_LINE_TAR_BIT0_REG	0x0504	CSIC LBC Channel1 Line Target Bit0 Register
CSIC_LBC_CH1_LINE_TAR_BIT1_REG	0x0508	CSIC LBC Channel1 Line Target Bit1 Register
CSIC_LBC_CH1_RC_ADV_REG	0x050C	CSIC LBC Channel1 RC ADV Register
CSIC_LBC_CH1_MB_MIN_REG	0x0510	CSIC LBC Channel1 MB MIN Register
CSIC_DMA_CH2_EN_REG	0x0600	CSIC DMA Channel2 Enable Register
CSIC_DMA_CH2_CFG_REG	0x0604	CSIC DMA Channel2 Configuration Register
CSIC_DMA_CH2_FRM_LOST_CNT_REG	0x0608	CSIC DMA Channel2 Frame Lost Counter Register
CSIC_DMA_CH2_HSIZE_REG	0x0610	CSIC DMA Channel2 Horizontal Size Register
CSIC_DMA_CH2_VSIZE_REG	0x0614	CSIC DMA Channel2 Vertical Size Register
CSIC_DMA_CH2_F0_BUFA_REG	0x0620	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH2_F0_BUFA_RESULT_REG	0x0624	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register

Register Name	Offset	Description
CSIC_DMA_CH2_F1_BUFA_REG	0x0628	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH2_F1_BUFA_RESULT_REG	0x062C	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F2_BUFA_REG	0x0630	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH2_F2_BUFA_RESULT_REG	0x0634	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH2_BUF_LEN_REG	0x0638	CSIC DMA Channel2 Buffer Length Register
CSIC_DMA_CH2_FLIP_SIZE_REG	0x063C	CSIC DMA Channel2 Flip Size Register
CSIC_DMA_CH2_CAP_STA_REG	0x064C	CSIC DMA Channel2 Capture Status Register
CSIC_DMA_CH2_INT_EN_REG	0x0650	CSIC DMA Channel2 Interrupt Enable Register
CSIC_DMA_CH2_INT_STA_REG	0x0654	CSIC DMA Channel2 Interrupt Status Register
CSIC_DMA_CH2_LINE_CNT_REG	0x0658	CSIC DMA Channel2 Line Counter Register
CSIC_DMA_CH2_LINE_STAT_REG	0x0668	CSIC DMA Channel2 Line Statistic Register
CSIC_DMA_CH2_PCLK_STAT_REG	0x0670	CSIC DMA Channel2 PCLK Statistic Register
CSIC_LBC_CH2_CONFIG_REG	0x0700	CSIC LBC Channel2 Configure Register
CSIC_LBC_CH2_LINE_TAR_BIT0_REG	0x0704	CSIC LBC Channel2 Line Target Bit0 Register
CSIC_LBC_CH2_LINE_TAR_BIT1_REG	0x0708	CSIC LBC Channel2 Line Target Bit1 Register
CSIC_LBC_CH2_RC_ADV_REG	0x070C	CSIC LBC Channel2 RC ADV Register
CSIC_LBC_CH2_MB_MIN_REG	0x0710	CSIC LBC Channel2 MB MIN Register
CSIC_DMA_CH3_EN_REG	0x0800	CSIC DMA Channel3 Enable Register
CSIC_DMA_CH3_CFG_REG	0x0804	CSIC DMA Channel3 Configuration Register
CSIC_DMA_CH3_FRM_LOST_CNT_REG	0x0808	CSIC DMA Channel3 Frame Lost Counter Register
CSIC_DMA_CH3_HSIZE_REG	0x0810	CSIC DMA Channel3 Horizontal Size Register
CSIC_DMA_CH3_VSIZE_REG	0x0814	CSIC DMA Channel3 Vertical Size Register
CSIC_DMA_CH3_F0_BUFA_REG	0x0820	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH3_F0_BUFA_RESULT_REG	0x0824	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F1_BUFA_REG	0x0828	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH3_F1_BUFA_RESULT_REG	0x082C	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F2_BUFA_REG	0x0830	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH3_F2_BUFA_RESULT_REG	0x0834	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH3_BUF_LEN_REG	0x0838	CSIC DMA Channel3 Buffer Length Register
CSIC_DMA_CH3_FLIP_SIZE_REG	0x083C	CSIC DMA Channel3 Flip Size Register

Register Name	Offset	Description
CSIC_DMA_CH3_CAP_STA_REG	0x084C	CSIC DMA Channel3 Capture Status Register
CSIC_DMA_CH3_INT_EN_REG	0x0850	CSIC DMA Channel3 Interrupt Enable Register
CSIC_DMA_CH3_INT_STA_REG	0x0854	CSIC DMA Channel3 Interrupt Status Register
CSIC_DMA_CH3_LINE_CNT_REG	0x0858	CSIC DMA Channel3 Line Counter Register
CSIC_DMA_CH3_LINE_STAT_REG	0x0868	CSIC DMA Channel3 Line Statistic Register
CSIC_DMA_CH3_PCLK_STAT_REG	0x0870	CSIC DMA Channel3 PCLK Statistic Register
CSIC_LBC_CH3_CONFIG_REG	0x0900	CSIC LBC Channel3 Configure Register
CSIC_LBC_CH3_LINE_TAR_BIT0_REG	0x0904	CSIC LBC Channel3 Line Target Bit0 Register
CSIC_LBC_CH3_LINE_TAR_BIT1_REG	0x0908	CSIC LBC Channel3 Line Target Bit1 Register
CSIC_LBC_CH3_RC_ADV_REG	0x090C	CSIC LBC Channel3 RC ADV Register
CSIC_LBC_CH3_MB_MIN_REG	0x0910	CSIC LBC Channel3 MB MIN Register

6.1.5 CSIC CCU Register Description

6.1.5.1 0x0000 CSIC CCU Clock Mode Register (Default Value:0x8000_0000)

Offset: 0x0000			Register Name: CSIC_CCU_CLK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CSIC_CCU_CLK_GATING_DISABLE Disable All CSIC CCU Clock Gating 0: CCU Clock Gating Registers(0x0004~0x0010) effect 1:CCU Clock Gating Registers(0x0004~0x0010) not effect
30:0	/	/	/

6.1.5.2 0x0004 CSIC CCU Parser Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE 0: Combo0 clock disable 1: Combo0 clock enable
7:3	/	/	/
2	R/W	0x0	MCSI_PARSER2_CLK_ENABLE 0: CSI Parser2 clock disable 1: CSI Parser2 clock enable
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE Parser0 clock gating 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

6.1.5.3 0x000C CSIC CCU Post0 Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE Post0 clock gating 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0: VIPP1 clock disable 1: VIPP1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPPO_CLK_ENABLE 0: VIPPO clock disable 1: VIPPO clock enable, when MCSI_POST0_CLK_ENABLE is 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE 0: BK3 clock disable 1: BK3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE BK1 clock gating 0: BK1 clock disable 1: BK1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BKO_CLK_ENABLE BKO clock gating 0: BKO clock disable 1: BKO clock enable, when MCSI_POST0_CLK_ENABLE is 1

6.1.6 CSIC TOP Register Description

6.1.6.1 0x0000 CSIC TOP Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_EN CSIC Version Register Read Enable: 0: Disable 1: Enable
30:3	/	/	/
2	R/W	0x0	BIST_MODE_EN CSIC Memory BIST Enable 0: Closed 1: EN BIST TEST
1	/	/	/
0	R/W	0x0	CSIC_TOP_EN CSIC TOP Module Enable 0: Reset and disable the CSIC module 1: Enable the CSIC module

6.1.6.2 0x0004 CSIC Pattern Generation Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:9	/	/	/
7:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software write this bit to "1" to start pattern generating from DRAM. When finished, the hardware will clear this bit to "0" automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

6.1.6.3 0x0008 CSIC Pattern Control Register (Default Value:0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	<p>PTN_PORT_SEL Pattern Generator output port selection</p> <p>010: NCSICO 011: NCSIC1 100: NCSIC2 101: NCSIC3 110: Combo others: reserved</p>
23:22	/	/	/
21:20	R/W	0x0	<p>PTN_GEN_DATA_WIDTH Pattern Generator output data width</p> <p>00:8bit 01:10bit 10:12bit 11:reserved</p>
19:16	R/W	0x0	<p>PTN_MODE Pattern mode selection</p> <p>0000: MIPI 1-lane 0001: MIPI 2-lane 0010: MIPI 3-lane 0011: MIPI 4-lane 0100:NCSIC with max 12-bit data ({field, VSYN, HSYN, 1'b0, data[11:0]}) 0101:NCSIC with max 16-bit data ({12'h0, field, VSYN, HSYN, 1'b0, data[15:0]}) 0110:NCSIC with max 24-bit data ({field, VSYN, HSYN, 5'h0, data[23:0]}) 0111: reserved 1000:BT656 8 bits' width 1001:BT656 16 bits' width 1010:BT656 24 bits' width 1011: reserved 1100: BAYER 12 bits for ISPFE 1101: UYVY422 12 bits for ISPFE 1110: UYVY420 12 bits for ISPFE 1111:reserved</p>
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

6.1.6.4 0x0020 CSIC Pattern Generation Length Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

6.1.6.5 0x0024 CSIC Pattern Generation Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

6.1.6.6 0x0028 CSIC Pattern ISP Size Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

6.1.6.7 0X0030 CSIC ISPO Input0 Select Register (Default Value:0x0000_0000)

Offset :0X0030			Register Name: CSIC_ISPO_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	ISPO Input0 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.8 0X0034 CSIC ISP0 Input1 Select Register (Default Value:0x0000_0001)

Offset :0X0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x1	ISPO Input1 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.9 0X0038 CSIC ISP0 Input2 Select Register (Default Value:0x0000_0002)

Offset :0X0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x2	ISPO Input2 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.10 0X003C CSIC ISP0 Input3 Select Register (Default Value:0x0000_0003)

Offset :0X003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	ISPO Input3 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.11 0X0040 CSIC ISP1 Input0 Select Register (Default Value:0x0000_0004)

Offset :0X0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x4	ISP1 Input0 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.12 0X0044 CSIC ISP1 Input1 Select Register (Default Value:0x0000_0005)

Offset :0X0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x5	ISP1 Input1 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.13 0X0048 CSIC ISP1 Input2 Select Register (Default Value:0x0000_0006)

Offset :0X0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x6	ISP1 Input2 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.14 0X004C CSIC ISP1 Input3 Select Register (Default Value:0x0000_0007)

Offset :0X004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x7	ISP1 Input3 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.1.6.15 0X00A0 CSIC DMA0 Input Select Register (Default Value:0x0000_0000)

Offset :0X00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA0 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.1.6.16 0X00A4 CSIC DMA1 Input Select Register (Default Value:0x0000_0000)

Offset :0X00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA1 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.1.6.17 0X00A8 CSIC DMA2 Input Select Register (Default Value:0x0000_0000)

Offset :0X00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	DMA2 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.1.6.18 0X00AC CSIC DMA3 Input Select Register (Default Value:0x0000_0000)

Offset :0X00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA3 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.1.6.19 0x00E0 CSIC BIST Control Register (Default Value:0x0000_0200)

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0: NO effect 1: Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
9	R	0x1	BIST_STOP BIST STOP 0: running 1:STOP
8	R	0x0	BIST_BUSY BIST Busy 0: idle 1:busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select
4	R/W	0x0	BIST_ADDR_Mode_SEL BIST Address mode select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write data Pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x0OFF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST Enable. A positive will trigger the BIST to start.

6.1.6.20 0x00E4 CSIC BIST Start Address Register (Default Value:0x0000_0000)

Offset:0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST Start Address BIST Start Address. It is 32-bit aligned.

6.1.6.21 0x00E8 CSIC BIST End Address Register (Default Value:0x0000_0000)

Offset:0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST END Address BIST END Address. It is 32-bit aligned.

6.1.6.22 0x00EC CSIC BIST Data Mask Register (Default Value:0x0000_0000)

Offset:0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0: Unmask 1:Mask

6.1.6.23 0x00F0 CSIC MBUS REQ MAX Register (Default Value:0x000f_0f0f)

Offset:0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:21	R	0x000	Reserved
20:16	R/W	0x0f	MISP_MEM_REQ_MAX Maximum of request commands for the master granted in MISP_MEM arbiter is N+1.
15:5	/	0x078	/
4:0	R/W	0x0f	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

6.1.6.24 0x0100 CSIC Multi-Frame Mode Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	MULF_STATUS Multi-Frame Mode Status indicates each DMA in frame done pending or not
23:16	/	/	/
15:8	R/W	0x0	MULF_CS Chip Selection for Multi-Frame Mode indicates which DMA is selected
7:1	/	/	/
0	R/W	0x0	MULF_EN Multi-Frame Mode Enable

6.1.6.25 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	MULF_ERR_PD Multi-Frame Mode Frame Error Interrupt Pending
16	R/W1C	0x0	MULF_DONE_PD Multi-Frame Mode Frame Done Interrupt Pending
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN Multi-Frame Mode Frame Error Interrupt Enable
0	R/W	0x0	MULF_DONE_EN Multi-Frame Mode Frame Done Interrupt Enable

6.1.6.26 0x01F0 CSIC Feature List Register (Default Value:0x3211_4400)

Offset: 0x01F0			Register Name: CSIC_FEATURE_LIST_REG
Bit	Read/Write	Default/Hex	Description
31:28	R	0x3	PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x2	MCSI_NUM Only can be read when version register read enable is on.
23:20	R	0x1	NCSI_NUM Only can be read when version register read enable is on.
19:16	R	0x1	ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x4	DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

6.1.7 CSIC Parser Register

6.1.7.1 0x0000 CSIC Parser Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	NCSIC_EN NCSI Controller Enable 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN NCSI Pixel Clock Gating 0:Gate pclk input 1:Enable pclk input
14:4	/	/	/
3:2	R/W	0x0	PRS_CH_MODE Parser channel mode 00: Parser output channel 0~3 corresponding from input channel 0~3 01: Parser output channel 0~3 all from input channel 0 10:Parser output channel0 and 2 from input channel 0, output channel1 and 3 from input channel 1 11: Reserved
1	R/W	0x0	PRS_MODE Parser Mode 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN Parser Enable 0: Reset and disable the parser module 1: Enable the parser module

6.1.7.2 0x0004 CSIC Parser NCSIC Interface Configuration Register (Default Value:0x0105_0080)

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER YUV420 Input Line Order 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30	/	/	/
29	R/W	0x0	YUV422_SEP When input format is YUV422 16bit or Bt1120, set this bit to transfer YU,YV(2 components for each clock cycle) to Y,U,Y,V(1 component for each clock cycle)
28	/	/	/

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0x1	<p>FIELD_DT_PCLK_SHIFT</p> <p>Only for vsync detected field mode, the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT</p>
23:20	R/W	0x0	<p>SRC_TYPE</p> <p>Bit 20~23 corresponding to the Source types for channel0~3</p> <p>0: Progressed</p> <p>1: Interlaced</p>
19	R/W	0x0	<p>FIELD</p> <p>For YUV HV timing, Field polarity</p> <p>0: negative(field=0 indicate odd, field=1 indicate even)</p> <p>1: positive(field=1 indicate odd, field=0 indicate even)</p> <p>For BT656 timing, Field sequence</p> <p>0: Normal sequence (field 0 first)</p> <p>1: Inverse sequence (field 1 first)</p>
18	R/W	0x1	<p>VREF_POL</p> <p>Vref polarity</p> <p>0: negative</p> <p>1: positive</p> <p>This register is not apply to CCIR656 interface.</p>
17	R/W	0x0	<p>HREF_POL</p> <p>Href polarity</p> <p>0: negative</p> <p>1: positive</p> <p>This register is not apply to CCIR656 interface.</p>
16	R/W	0x1	<p>CLK_POL</p> <p>Data clock type</p> <p>0: active in rising edge</p> <p>1: active in falling edge</p>
15:14	R/W	0x0	<p>Field_DT_MODE</p> <p>only valid when CSI_IF is YUV and source type is interlaced</p> <p>00:by both field and vsync</p> <p>01:by field</p> <p>10:by vsync</p> <p>11:reserved</p>
13	R/W	0x0	<p>DDR_SAMPLE_MODE_EN</p> <p>Dual Data Rate Sample mode Enable</p> <p>0:disable</p> <p>1:enable</p>

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
12:11	R/W	0x0	<p>SEQ_8PLUS2</p> <p>When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual CSI data bus according to these sequences:</p> <ul style="list-style-type: none"> 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	<p>IF_DATA_WIDTH</p> <p>Input Data Width</p> <ul style="list-style-type: none"> 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100: 2x8/16bit data bus 101: 14 bit data bus 110: 20 bit data bus,only for packet generator 111: 24 bit data bus,only for packet generator
7:6	R/W	0x2	<p>INPUT_SEQ</p> <p>Input data sequence, only valid for YUV422 and YUV420 input format.</p> <p>All data interleaved in one channel:</p> <ul style="list-style-type: none"> 00: YUYV 01: YVYU 10: UYVY 11: VYUY <p>Y and UV in separated channel:</p> <ul style="list-style-type: none"> x0: UV x1: VU
5	/	/	/

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	<p>CSI_IF YUV(separate syncs): 00000: YUYV422/YUV420 or RAW (All data in one data bus) 00001: 2x8 bit YUYV422 00010: Reserved 00011: Reserved</p> <p>CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16bit BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved</p> <p>01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16bit BT656(BT1120 like) 2 channels(All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16bit BT656(BT1120 like) 4 channels(All data interleaved in one data bus)</p> <p>Others: Reserved</p>

6.1.7.3 0x0008 CSIC Parser MCSIC Interface Configuration Register (Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order</p>
30:8	/	/	/
7:6	R/W	0X2	<p>INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format.</p> <p>All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY</p> <p>Y and UV in separated channel: x0: UV x1: VU</p>

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	/	/	/

6.1.7.4 0x000C CSIC Parser Capture Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames 15: 1/16 fps, only receives the first frame every 16 frames
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/WAC	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
23:22	/	/	/

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
21:18	R/W	0x0	<p>CH2_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames 15: 1/16 fps, only receives the first frame every 16 frames</p>
17	R/W	0x0	<p>CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.</p>
16	R/WAC	0x0	<p>CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.</p>
15:14	/	/	/
13:10	R/W	0x0	<p>CH1_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames 15: 1/16 fps, only receives the first frame every 16 frames</p>

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	<p>CH1_VCAP_ON</p> <p>Video capture control: Capture the video image data stream on channel 1.</p> <p>0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO.</p> <p>1: Enable video capture The CSI starts capturing image data at the start of the next frame.</p>
8	R/WAC	0x0	<p>CH1_SCAP_ON</p> <p>Still capture control: Capture a single still image frame on channel 1.</p> <p>0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.</p>
7:6	/	/	/
5:2	R/W	0x0	<p>CHO_FPS_DS</p> <p>Fps down sample</p> <p>0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames 15: 1/16 fps, only receives the first frame every 16 frames</p>
1	R/W	0x0	<p>CHO_VCAP_ON</p> <p>Video capture control: Capture the video image data stream on channel 0.</p> <p>0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO.</p> <p>1: Enable video capture The CSI starts capturing image data at the start of the next frame.</p>

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	<p>CHO_SCAP_ON Still capture control: Capture a single still image frame on channel 0.</p> <p>0: Disable still capture. 1: Enable still capture</p> <p>The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.</p>

6.1.7.5 0x0010 SIC Parser Signal Status Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	<p>FIFO_FULL Indicates the NCSI IN Async FIFO FULL</p> <p>0:Not Full 1:Full</p>
30:28	R	0x0	<p>PCLK_CNT Indicates the NCSI Pclk is toggle or not</p>
27	R	0x0	<p>VSYNC_STA Indicates the NCSI Vsync Signal status</p> <p>0:low 1:high</p>
26	R	0x0	<p>HSYNC_STA Indicates the NCSI Hsync Signal status</p> <p>0:low 1:high</p>
25	R	0x0	<p>FIELD_STA Indicates the NCSI Field Signal status</p> <p>0:low 1:high</p>
24	R	0x0	<p>DATA_VALID_STA Indicates the NCSI Data Valid Signal status(n=0~15),MSB for D15,LSB for D0</p> <p>0:low 1:high</p>
23:0	R	0x0	<p>DATA_STA Indicates the NCSI Data Signal status(n=0~15),MSB for D15,LSB for D0</p> <p>0:low 1:high</p>

6.1.7.6 0x0014 CSIC Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

6.1.7.7 0x0024 CSIC Parser Channel_0 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0024			Register Name: CSIC_PRS_CHO_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.8 0x0028 CSIC Parser Channel_0 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0028			Register Name: CSIC_PRS_CH0_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.9 0x002C CSIC Parser Channel_0 Output Vertical Size Register Default Value:0x02d0_0000)

Offset: 0x002C			Register Name: CSIC_PRS_CH0_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.7.10 0x0030 CSIC Parser Channel_0 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_PRS_CH0_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 0 0:Progress 1:Interlace

6.1.7.11 0x0034. CSIC Parser Channel_0 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_PRS_CH0_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.1.7.12 0x0038 CSIC Parser Channel_0 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: CSIC_PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.1.7.13 0x003C. CSIC Parser Channel_0 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: CSIC_PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.1.7.14 0x0040 CSIC Parser Channel_0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.1.7.15 0x0044 CSIC Parser Channel_0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PDO When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.1.7.16 0x0048 CSIC Parser Channel_0 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_PRS_CH0_LINE_TIME_REG
Bit	Read/Writ e	Default/Hex	Description
31:16	R	0x0	PRS_CHO_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CHO_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.1.7.17 0x0124 CSIC Parser Channel_1 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0124			Register Name: CSIC_PRS_CH1_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.18 0x0128 CSIC Parser Channel_1 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0128			Register Name: CSIC_PRS_CH1_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.19 0x012C CSIC Parser Channel_1 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x012C			Register Name: CSIC_PRS_CH1_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.7.20 0x0130 CSIC Parser Channel_1 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0130			Register Name: CSIC_PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 1 0:Progress 1:Interlace

6.1.7.21 0x0134 CSIC Parser Channel_1 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0134			Register Name: CSIC_PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.1.7.22 0x0138 CSIC Parser Channel_1 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0138			Register Name: CSIC_PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.1.7.23 0x013C CSIC Parser Channel_1 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.1.7.24 0x0140 CSIC Parser Channel_1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.1.7.25 0x0144 CSIC Parser Channel_1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0144			Register Name: CSIC_PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC PDO When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.1.7.26 0x0148 CSIC Parser Channel_1 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0148			Register Name: CSIC_PRS_CH1_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.1.7.27 0x0224 CSIC Parser Channel_2 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0224			Register Name: CSIC_PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.28 0x0228 CSIC Parser Channel_2 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0228			Register Name: CSIC_PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.29 0x022C CSIC Parser Channel_2 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.7.30 0x0230 CSIC Parser Channel_2 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_PRS_CH2_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 2 0:Progress 1:Interlace

6.1.7.31 0x0234 CSIC Parser Channel_2 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_PRS_CH2_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total $INPUT_VT = INPUT_VB + INPUT_Y$
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total $INPUT_HT = INPUT_HB + INPUT_X$

6.1.7.32 0x0238 CSIC Parser Channel_2 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.1.7.33 0x023C CSIC Parser Channel_2 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x023C			Register Name: CSIC_PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.1.7.34 0x0240 CSIC Parser Channel_2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0240			Register Name: CSIC_PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.1.7.35 0x0244 CSIC Parser Channel_2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC PDO When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.1.7.36 0x0248 CSIC Parser Channel_2 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0248			Register Name: CSIC_PRS_CH2_LINE_TIME_REG
Bit	Read/Writ e	Default/Hex	Description
31:16	R	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.1.7.37 0x0324 CSIC Parser Channel_3 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0324			Register Name: CSIC_PRS_CH3_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.1.7.38 0x0328 CSIC Parser Channel_3 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0328			Register Name: CSIC_PRS_CH3_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.7.39 0x032C CSIC Parser Channel_3 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x032C			Register Name: CSIC_PRS_CH3_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.7.40 0x0330 CSIC Parser Channel_3 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0330			Register Name: CSIC_PRS_CH3_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 3 0:Progress 1:Interlace

6.1.7.41 0x0334. CSIC Parser Channel_3 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0334			Register Name: CSIC_PRS_CH3_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.1.7.42 0x0338 CSIC Parser Channel_3 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0338			Register Name: CSIC_PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.1.7.43 0x033C CSIC Parser Channel_3 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x033C			Register Name: CSIC_PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.1.7.44 0x0340 CSIC Parser Channel_3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.1.7.45 0x0344 CSIC Parser Channel_3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0344			Register Name: CSIC_PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PDO When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.1.7.46 0x0348 CSIC Parser Channel_3 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0348			Register Name: CSIC_PRS_CH3_LINE_TIME_REG
Bit	Read/Writ e	Default/Hex	Description
31:16	R	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.1.7.47 0x0500 CSIC Parser NCSIC RX Signal0 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	Filed_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2ns

6.1.7.48 0x050C CSIC Parser NCSIC RX Signal3 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

6.1.7.49 0x0510 CSIC Parser NCSIC RX Signal4 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

6.1.7.50 0x0514 CSIC Parser NCSIC RX Signal5 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

6.1.7.51 0x0518 CSIC Parser NCSIC RX Signal6 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

6.1.7.52 0X0520 CSIC Parser SYNC EN Register (Default Value:0x0000_0000)

Offset :0X0520			Register Name: CSIC_PRS_SYNC_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
19:16	R/W	0x0	VSYNC_MODE Input vsync singal Source select 0: Vsync signals all from 1 parser 1: Vsync signals from 2 parser 2: Vsync signals from 4 parser others:reserved
15:12	/	/	/
11:8	R/W	0x0	VSYNC_SEL Generate sync singal Benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	VSYNC_USED Parser input vsync singal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	FSYNC_OUT_SEL Parser sent sync singal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	FSYNC_MODE Parser sync singal source select 0: From outside 1: Generate by self
0	R/W	0x0	FSYNC_FUN_EN Enable Parser sent sync singal 0: Disable 1: Enable

6.1.7.53 0X0524 CSIC Parser SYNC CFG Register (Default Value:0x0000_0000)

Offset :0X0524			Register Name: CSIC_PRS_SYNC_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	FSYNC_PUL_WID Sync singal pulse width $N*T_{24M}$, $N*T_{24M} \geq 4*T_{pclk}$
15:0	R/W	0x0	FYSNC_DISTANCE The interval of two sync signal

6.1.7.54 0X0528 CSIC Parser VS WAIT N Register (Default Value:0x0000_0000)

Offset :0X0528			Register Name: CSIC_PRS_VS_WAIT_N_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come,the max wait time.

6.1.7.55 0X052C CSIC Parser VS WAIT M Register (Default Value:0x0000_0000)

Offset :0X052C			Register Name: CSIC_PRS_VS_WAIT_M_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode,vsync comes at the different time,these bits indicate the max wait time.

6.1.7.56 0X0540. CSIC Parser XSYNC ENABLE Register (Default Value:0x0000_0000)

Offset:0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0x0	XVS_TO_XHS_T The period of XHS delay to XVS, \${XVS_TO_XHS_T}+1 master clock cycles, no more than XHS_LEN
7:5	/	/	/
4	R/W	0x0	XVS_XHS_OUT_SEL When sensor works in slave mode ,this bit select XVS and XHS to output. 0: XHS0,XVS0 1: XHS1,XVS1

Offset:0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	XVS_POL When sensor works in slave mode ,this bit set polarity of XVS. 0: Negative 1: Positive
2	R/W	0x0	XHS_POL When sensor works in slave mode ,this bit set polarity of XHS. 0: Negative 1: Positive
1	R/W	0x0	XVS_OUT_EN When sensor works in slave mode ,this bit enable output XVS to sensor 0: Disable 1: Enable
0	R/W	0x0	XHS_OUT_EN When sensor works in slave mode ,this bit enable output XHS to sensor 0: Disable 1: Enable

6.1.7.57 0X0544 CSIC Parser XVS Period Register (Default Value:0x0000_0000)

Offset:0X0544			Register Name: CSIC_PRS_XVS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_T The period of XVS signal, \${XVS_T}+2 master clock cycles

6.1.7.58 0X0548 CSIC Parser XHS Period Register (Default Value:0x0000_0000)

Offset:0X0548			Register Name: CSIC_PRS_XHS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_T The period of XHS signal, \${XHS_T}+2 master clock cycles

6.1.7.59 0X054C CSIC Parser XVS LENGTH Register (Default Value:0x0000_0000)

Offset:0X054C			Register Name: CSIC_PRS_XVS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_LEN The valid length of XVS signal, \${XVS_LEN}+1 master clock cycles

6.1.7.60 0X0550 CSIC Parser XHS LENGTH Register (Default Value:0x0000_0000)

Offset:0X0550			Register Name: CSIC_PRS_XHS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_LEN The valid length of XHS signal, \${XHS_LEN}+1 master clock cycles

6.1.7.61 0X0554 CSIC Parser SYNC DELAY Register (Default Value:0x0000_0000)

Offset:0X0554			Register Name: CSIC_PRS_SYNC_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SYNC_DLY The XHS/XVS will sent after, \${SYNC_DLY}+1 master clock cycles, no more than XVS_LEN

6.1.8 CSIC DMA Register Description

6.1.8.1 0x0000 CSIC DMA TOP Register (Default Value:0x7000_0000)

Offset:0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_EN CSIC DMA Version Register Read Enable: 0: Disable 1: Enable
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE VFLIP buffer address set by software or calculated by hardware 0: hardware 1: software
29	R/W	0x1	BUF_LENGTH_CFG_MODE buffer length set by software or calculated by hardware 0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:17	/	/	/
16	R/W	0x0	FRM_END_FOR_FRM_DONE_SEL Select BK frame end for frame done interrupt generation 0: Frame end from BK input 1: Frame end generated by self

Offset:0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
15	/	/	/
14:13	R/W	0x0	VE_ONLINE_CH_SEL Select BK Channel for VE Online handshake
12	R/W	0x0	VE_ONLINE_HANDSHAKE_EN Set this bit to Enable frame and line counter for VE online handshake
11:10	/	/	/
9:8	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if HFLIP is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes(not Support For DMA1\2\3)
7	/	/	/
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FS_FRM_CNT_EN When BK_TOP_EN enable, this bit set 1 indicate the Frame counter start to add. 0: Disable 1: Enable
4:3	/	/	/
2	R/W	0x0	FRM_RATE_CNT_SPL Sampling time for CLK counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every VSYNC
1	R/W	0x0	FRM_RATE_CNT_EN CLK count per frame enable
0	R/W	0x0	BK_TOP_EN Module Enable 0: Disable 1: Enable

6.1.8.2 0x0004 CSIC DMA Multi-Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
21:20	R	0x0	CUR_OUT_CH When Multi-Channel enable, this field indicates the Current Output Channel ID
19:18	/	/	/
17:16	R	0x0	CUR_IN_CH When Multi-Channel enable, this field indicates the Current Input Channel ID
15:1	/	/	/
0	R/W	0x0	MUL_CH_EN DMA off-line multi-channel enable 0: disable 1: enable

6.1.8.3 0x0010 CSIC DMA Frame Rate Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	FRM_RATE_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

6.1.8.4 0x0014 CSIC DMA Accumulated and Internal Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or VSYNC comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.1.8.5 0x0020 CSIC DMA Fsync Frame Counter Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	FS_FRM_CNT_CLR When the bit set to 1, Frame CNT clear to 0
30:16	R/W	0x0	FS_FRM_CNT_CLR_DISTANCE Frame CNT clear cycle $N \cdot T_{SYNC}$
15	/	/	/
14:0	R	0x0	FS_FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the REG full, it cleared to 0 . When parser sent a sync signal, it clear to 0

6.1.8.6 0x0040 CSIC DMA Video Input Timeout Threshold0 Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH0 Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , Time Unit is a 12M clock period.

6.1.8.7 0x0044 CSIC DMA Video Input Timeout Threshold1 Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH1 Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

6.1.8.8 0x0048 CSIC DMA Video Input Timeout Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	VI_TCNT_VAL Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

6.1.8.9 0x0050 CSIC DMA VE Frame Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_VE_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	FRM_DONE_CNT Indicates How Many Frame which Stored in DDR
15:8	/	/	/
7:0	R	0x0	FRM_ST_CNT Indicates the Frame Number which is Storing

6.1.8.10 0x0054 CSIC DMA VE Line Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_VE_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_DONE_CNT Indicates How Many Line which Stored in DDR
15:14	/	/	/
13:0	R	0x0	LINE_ST_CNT Indicates the Line Number which is Storing

6.1.8.11 0x0058 CSIC DMA VE Current Frame Address Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_VE_CUR_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_FRM_ADDR Indicates the FIFO0 Address Which Current Frame is Storing

6.1.8.12 0x005C CSIC DMA VE Last Frame Address Register (Default Value:0x0000_0000)

Offset: 0x005C			Register Name: CSIC_DMA_VE_LAST_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LAST_FRM_ADDR Indicates the FIFO0 Address Which Last Frame is Stored

6.1.8.13 0x0080 CSIC DMA FIFO Statistic Register(Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every VSYNC or framedone. Unit is byte.

6.1.8.14 0x0084 CSIC DMA FIFO Threshold Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change. Unit is byte.

6.1.8.15 0x0100 CSIC DMA TOP Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_DMA_TOP_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
1	R/W	0x0	CLR_FS_FRM_CNT_INT_EN Set a INT When Clear FS Frame CNT.
0	R/W	0x0	FS_PUL_INT_EN Set an INT when a FSYNC signal received

6.1.8.16 0x0104 CSIC DMA TOP Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_DMA_TOP_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time
1	R/W1C	0x0	CLR_FRAME_CNT_INT_PD Set a INT When Clear FS Frame cnt.
0	R/W1C	0x0	FS_PUL_INT_PD Set an INT when a Fsync signal received

6.1.8.17 0x01F4 CSIC DMA Feature List Register (Default Value:0x0000_0002)

Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x1	DMA0_EMBEDDED_LBC LBC Feature Existence 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC FBC Feature Existence 0: No Embedded DMA 1: Embedded FBC

6.1.8.18 0x0200 CSIC DMA Channel0 Enable Register (Default Value:0x0000_0000)

Offset:0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when VSYNC comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable

Offset:0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.1.8.19 0x0204 CSIC DMA Channel0 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

			OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved
19:16	R/W	0x0	When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence)

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.1.8.20 0x0208 CSIC DMA Channel0 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.1.8.21 0x0210 CSIC DMA Channel0 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0210			Register Name: CSIC_DMA_CH0_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.8.22 0x0214 CSIC DMA Channel0 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0214			Register Name: CSIC_DMA_CH0_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.8.23 0x0220 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: CSIC_DMA_CH0_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.1.8.24 0x0224 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0224			Register Name: CSIC_DMA_CH0_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.25 0x0228 CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0228			Register Name: CSIC_DMA_CH0_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

6.1.8.26 0x022C CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x022C			Register Name: CSIC_DMA_CH0_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.27 0x0230 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_DMA_CH0_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.1.8.28 0x0234 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_DMA_CH0_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.29 0x0238 CSIC DMA Channel0 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0238			Register Name: CSIC_DMA_CH0_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.1.8.30 0x023C CSIC DMA Channel0 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x023C			Register Name: CSIC_DMA_CH0_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.1.8.31 0x024C CSIC DMA Channel0 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.1.8.32 0x0250 CSIC DMA Channel0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO_OF_INT_EN FIFO overflow The bit is set when the FIFO become overflow.

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	<p>FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.</p>
0	R/W	0x0	<p>CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.</p>

6.1.8.33 0x0254 CSIC DMA Channel0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	<p>BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used</p>
17	R/W1C	0x0	<p>BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready</p>
16	R/W1C	0x0	<p>LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode</p>
15	R/W1C	0x0	<p>FRM_LOST_INT_PD Set an INT once frame is in when last frame processing</p>
14	R/W1C	0x0	<p>STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE</p>
13	R/W1C	0x0	<p>BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE</p>
12:8	/	/	/

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO_OF_PD FIFO overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.8.34 0x0258 CSIC DMA Channel0 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0258			Register Name: CSIC_DMA_CH0_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.1.8.35 0x0268 CSIC DMA Channel0 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0268			Register Name: CSIC_DMA_CH0_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.1.8.36 0x0270 CSIC DMA Channel0 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.1.8.37 0x0300 CSIC LBC Channel0 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0300			Register Name: CSIC_LBC_CH0_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.1.8.38 0x0304 CSIC LBC Channel0 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0304			Register Name: CSIC_LBC_CH0_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.1.8.39 0x0308 CSIC LBC Channel0 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0308			Register Name: CSIC_LBC_CH0_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.1.8.40 0x030C CSIC LBC Channel0 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x030C			Register Name: CSIC_LBC_CH0_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

6.1.8.41 0x0310 CSIC LBC Channel0 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0310			Register Name: CSIC_LBC_CH0_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

6.1.8.42 0x0400 CSIC DMA Channel1 Enable Register (Default Value:0x0000_0000)

Offset:0x0400			Register Name: CSIC_DMA_CH1_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.1.8.43 0x0404 CSIC DMA Channel1 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

			OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved
19:16	R/W	0x0	When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.1.8.44 0x0408 CSIC DMA Channel1 Frame Lost Counter Register (Default Value:0x0001_0000)

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.1.8.45 0x0410 CSIC DMA Channel1 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0410			Register Name: CSIC_DMA_CH1_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.8.46 0x0414 CSIC DMA Channel1 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0414			Register Name: CSIC_DMA_CH1_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.8.47 0x0420 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0420			Register Name: CSIC_DMA_CH1_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.1.8.48 0x0424 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0424			Register Name: CSIC_DMA_CH1_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.49 0x0428 CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0428			Register Name: CSIC_DMA_CH1_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

6.1.8.50 0x042C CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x042C			Register Name: CSIC_DMA_CH1_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.51 0x0430 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0430			Register Name: CSIC_DMA_CH1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.1.8.52 0x0434 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0434			Register Name: CSIC_DMA_CH1_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.53 0x0438 CSIC DMA Channel1 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0438			Register Name: CSIC_DMA_CH1_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.1.8.54 0x043C CSIC DMA Channel1 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x043C			Register Name: CSIC_DMA_CH1_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.1.8.55 0x044C CSIC DMA Channel1 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.1.8.56 0x0450 CSIC DMA Channel1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.8.57 0x0454 CSIC DMA Channel1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.8.58 0x0458 CSIC DMA Channel1 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0458			Register Name: CSIC_DMA_CH1_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.1.8.59 0x0468 CSIC DMA Channel1 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0468			Register Name: CSIC_DMA_CH1_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x0468			Register Name: CSIC_DMA_CH1_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.1.8.60 0x0470 CSIC DMA Channel1 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0470			Register Name: CSIC_DMA_CH1_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.1.8.61 0x0500 CSIC LBC Channel1 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0500			Register Name: CSIC_LBC_CH1_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.1.8.62 0x0504 CSIC LBC Channel1 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0504			Register Name: CSIC_LBC_CH1_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.1.8.63 0x0508 CSIC LBC Channel1 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0508			Register Name: CSIC_LBC_CH1_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.1.8.64 0x050C CSIC LBC Channel1 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x050C			Register Name: CSIC_LBC_CH1_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

6.1.8.65 0x0510 CSIC LBC Channel1 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0510			Register Name: CSIC_LBC_CH1_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

6.1.8.66 0x0600 CSIC DMA Channel2 Enable Register (Default Value:0x0000_0000)

Offset:0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable

Offset:0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.1.8.67 0x0604 CSIC DMA Channel2 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

			OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved
			When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
19:16	R/W	0x0	When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.1.8.68 0x0608 CSIC DMA Channel2 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.1.8.69 0x0610 CSIC DMA Channel2 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0610			Register Name: CSIC_DMA_CH2_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.8.70 0x0614 CSIC DMA Channel2 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.8.71 0x0620 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0620			Register Name: CSIC_DMA_CH2_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.1.8.72 0x0624 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0624			Register Name: CSIC_DMA_CH2_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.73 0x0628 CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0628			Register Name: CSIC_DMA_CH2_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

6.1.8.74 0x062C CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x062C			Register Name: CSIC_DMA_CH2_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.75 0x0630 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0630			Register Name: CSIC_DMA_CH2_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.1.8.76 0x0634 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0634			Register Name: CSIC_DMA_CH2_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.77 0x0638 CSIC DMA Channel2 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0638			Register Name: CSIC_DMA_CH2_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.1.8.78 0x063C CSIC DMA Channel2 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x063C			Register Name: CSIC_DMA_CH2_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.1.8.79 0x064C CSIC DMA Channel2 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x064C			Register Name: CSIC_DMA_CH2_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.1.8.80 0x0650 CSIC DMA Channel2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.8.81 0x0654 CSIC DMA Channel2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.8.82 0x0658 CSIC DMA Channel2 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0658			Register Name: CSIC_DMA_CH2_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.1.8.83 0x0668 CSIC DMA Channel2 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0668			Register Name: CSIC_DMA_CH2_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x0668			Register Name: CSIC_DMA_CH2_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.1.8.84 0x0670 CSIC DMA Channel2 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0670			Register Name: CSIC_DMA_CH2_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.1.8.85 0x0700 CSIC LBC Channel2 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0700			Register Name: CSIC_LBC_CH2_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.1.8.86 0x0704 CSIC LBC Channel2 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0704			Register Name: CSIC_LBC_CH2_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.1.8.87 0x0708 CSIC LBC Channel2 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0708			Register Name: CSIC_LBC_CH2_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.1.8.88 0x070C CSIC LBC Channel2 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x070C			Register Name: CSIC_LBC_CH2_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

6.1.8.89 0x0710 CSIC LBC Channel2 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0710			Register Name: CSIC_LBC_CH2_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

6.1.8.90 0x0800 CSIC DMA Channel3 Enable Register (Default Value:0x0000_0000)

Offset:0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable

Offset:0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.1.8.91 0x0804 CSIC DMA Channel3 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

			OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved
			When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
19:16	R/W	0x0	When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.1.8.92 0x0808 CSIC DMA Channel3 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.1.8.93 0x0810 CSIC DMA Channel3 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0810			Register Name: CSIC_DMA_CH3_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.8.94 0x0814 CSIC DMA Channel3 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0814			Register Name: CSIC_DMA_CH3_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.8.95 0x0820 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0820			Register Name: CSIC_DMA_CH3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.1.8.96 0x0824 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0824			Register Name: CSIC_DMA_CH3_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.97 0x0828 CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0828			Register Name: CSIC_DMA_CH3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address in DMA mode.

6.1.8.98 0x082C CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x082C			Register Name: CSIC_DMA_CH3_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.99 0x0830 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0830			Register Name: CSIC_DMA_CH3_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.1.8.100 0x0834 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0834			Register Name: CSIC_DMA_CH3_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.1.8.101 0x0838 CSIC DMA Channel3 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0838			Register Name: CSIC_DMA_CH3_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.1.8.102 0x083C CSIC DMA Channel3 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x083C			Register Name: CSIC_DMA_CH3_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.1.8.103 0x084C CSIC DMA Channel3 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.1.8.104 0x0850 CSIC DMA Channel3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.8.105 0x0854 CSIC DMA Channel3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.8.106 0x0858 CSIC DMA Channel3 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0858			Register Name: CSIC_DMA_CH3_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.1.8.107 0x0868 CSIC DMA Channel3 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0868			Register Name: CSIC_DMA_CH3_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x0868			Register Name: CSIC_DMA_CH3_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.1.8.108 0x0870 CSIC DMA Channel3 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0870			Register Name: CSIC_DMA_CH3_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.1.8.109 0x0900 CSIC LBC Channel3 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0900			Register Name: CSIC_LBC_CH3_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.1.8.110 0x0904 CSIC LBC Channel3 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0904			Register Name: CSIC_LBC_CH3_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.1.8.111 0x0908 CSIC LBC Channel3 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0908			Register Name: CSIC_LBC_CH3_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.1.8.112 0x090C CSIC LBC Channel3 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x090C			Register Name: CSIC_LBC_CH3_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control adventure 3
23:16	R/W	0x10	Rate control adventure 2
15:8	R/W	0x10	Rate control adventure 1
7:0	R/W	0x10	Rate control adventure 0

6.1.8.113 0x0910 CSIC LBC Channel3 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0910			Register Name: CSIC_LBC_CH3_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

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7 Video Output Interfaces

7.1 TCON LCD

7.1.1 Overview

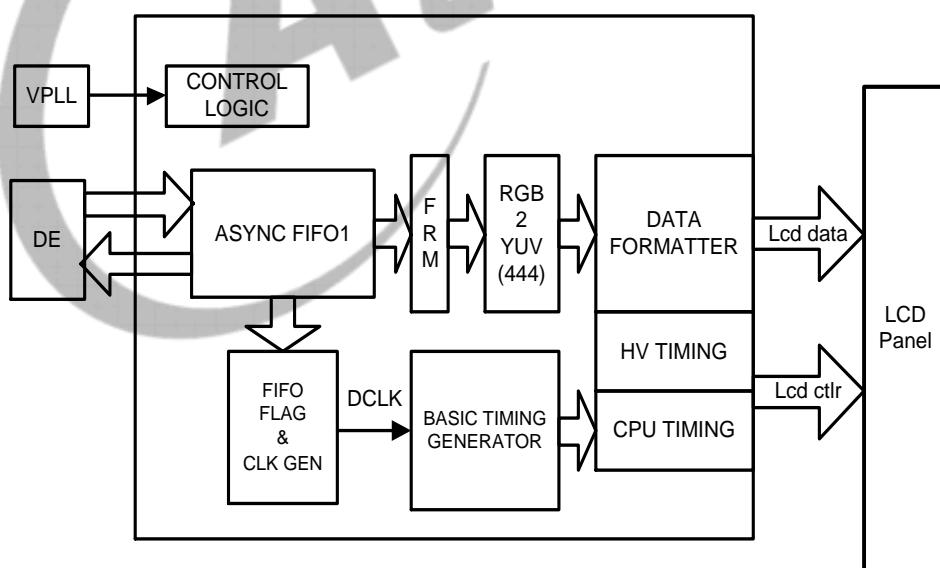
The Timing Controller LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Fsync (Frame Sync.) for camera sensor

7.1.2 Block Diagram

Figure 7-1 TCON_LCD Block Diagram



7.1.3 Functional Description

7.1.3.1 External Signals

The following table describes the external I/O signals of TCONLCD

Table 7-1 LCD External Signals

Signal	Description	Type
LCD0_CLK	LCD clock, pixel data are sync by this clock	O
LCD0_VSYNC	LCD Vertical sync, indicates one new frame	O
LCD0_HSYNC	LCD Horizontal sync, indicate one new scan line	O
LCD0_DE	LCD data output enable	O
TCON-TRIG	LCD Sync (TCON outputs to LCD for sync)	O
LCD0_D23	LCD data[23] output or input	O/I
LCD0_D22	LCD data[22] output or input	O/I
LCD0_D21	LCD data[21] output or input	O/I
LCD0_D20	LCD data[20] output or input	O/I
LCD0_D19	LCD data[19] output or input	O/I
LCD0_D18	LCD data[18] output or input	O/I
LCD0_D17	LCD data[17] output or input	O/I
LCD0_D16	LCD data[16] output or input	O/I
LCD0_D15	LCD data[15] output or input	O/I
LCD0_D14	LCD data[14] output or input	O/I
LCD0_D13	LCD data[13] output or input	O/I
LCD0_D12	LCD data[12] output or input	O/I
LCD0_D11	LCD data[11] output or input	O/I
LCD0_D10	LCD data[10] output or input	O/I
LCD0_D9	LCD data[9] output or input	O/I
LCD0_D8	LCD data[8] output or input	O/I
LCD0_D7	LCD data[7] output or input	O/I
LCD0_D6	LCD data[6] output or input	O/I
LCD0_D5	LCD data[5] output or input	O/I
LCD0_D4	LCD data[4] output or input	O/I
LCD0_D3	LCD data[3] output or input	O/I
LCD0_D2	LCD data[2] output or input	O/I
LCD0_D1	LCD data[1] output or input	O/I
LCD0_D0	LCD data[0] output or input	O/I

7.1.3.2 Control Signal and Data Port Mapping

		SYNC RGB			DC	CPU Cmd	CPU 18-bit	CPU 16bit						CPU 8bit			CPU 9bit			
External I/O	Internal pin	Para RGB	Serial RGB		CCIR 656	YUV422	25-6K	256K						65K	256K			65K		
		1 st	2 nd	3 rd				1 st	2 nd	3 rd	1 st	2 nd	1 st	2 nd	1 st	2 nd	3 rd	1 st	2 nd	
LCD0_VSYNC	IO0	VSYNC			VSYNC	CS														
LCD0_HSYNC	IO1	HSYNC				RD														
LCD0_CLK	IO2	DCLK			DCLK	WR														
LCD0_DE	IO3	DE			HSYNC	RS														
LCD0_D23	D23	R7				D23	R5	R5	B5	G5	R5		R5	B5	R4					
LCD0_D22	D22	R6				D22	R4	R4	B4	G4	R4		R4	B4	R3					
LCD0_D21	D21	R5				D21	R3	R3	B3	G3	R3		R3	B3	R2					
LCD0_D20	D20	R4				D20	R2	R2	B2	G2	R2		R2	B2	R1					
LCD0_D19	D19	R3				D19	R1	R1	B1	G1	R1		R1	B1	R0					
LCD0_D18	D18	R2				D18	R0	R0	B0	G0	R0		R0	B0	G5					
LCD0_D17	D17	R1				D17														
LCD0_D16	D16	R0				D16														
LCD0_D15	D15	G7				D15	G5								G4					
LCD0_D14	D14	G6				D14	G4								G3					
LCD0_D13	D13	G5				D13	G3													
LCD0_D12	D12	G4	D71	D72	D73	D7	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5
LCD0_D11	D11	G3	D61	D62	D63	D6	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4
LCD0_D10	D10	G2	D51	D52	D53	D5	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3
LCD0_D9	D9	G1				D9														
LCD0_D8	D8	G0				D8														
LCD0_D7	D7	B7	D41	D42	D43	D4	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2
LCD0_D6	D6	B6	D31	D32	D33	D3	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1
LCD0_D5	D5	B5	D21	D22	D23	D2	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0
LCD0_D4	D4	B4	D11	D12	D13	D1	D1	D4	B2								B1		G4	B1
LCD0_D3	D3	B3	D01	D02	D03	D0	D0	D3	B1								B0		G3	B0
LCD0_D2	D2	B2						D2	B0										G3	B0
LCD0_D1	D1	B1						D1												
LCD0_D0	D0	B0						D0												

7.1.3.3 Clock Sources

Module	Module Clock	Sources	Description
TCONLCD	LCD0_CLK DE_CLK	CCU	Refer to section 3.4 Clock Controller Unit (CCU) for detailed information.

7.1.3.4 Interface mode

HV interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are defined as:

Table 7-2 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync to this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO to panel	O

The timing diagram of HV interface is as follows.

Figure 7-2 HV Interface Vertical Timing

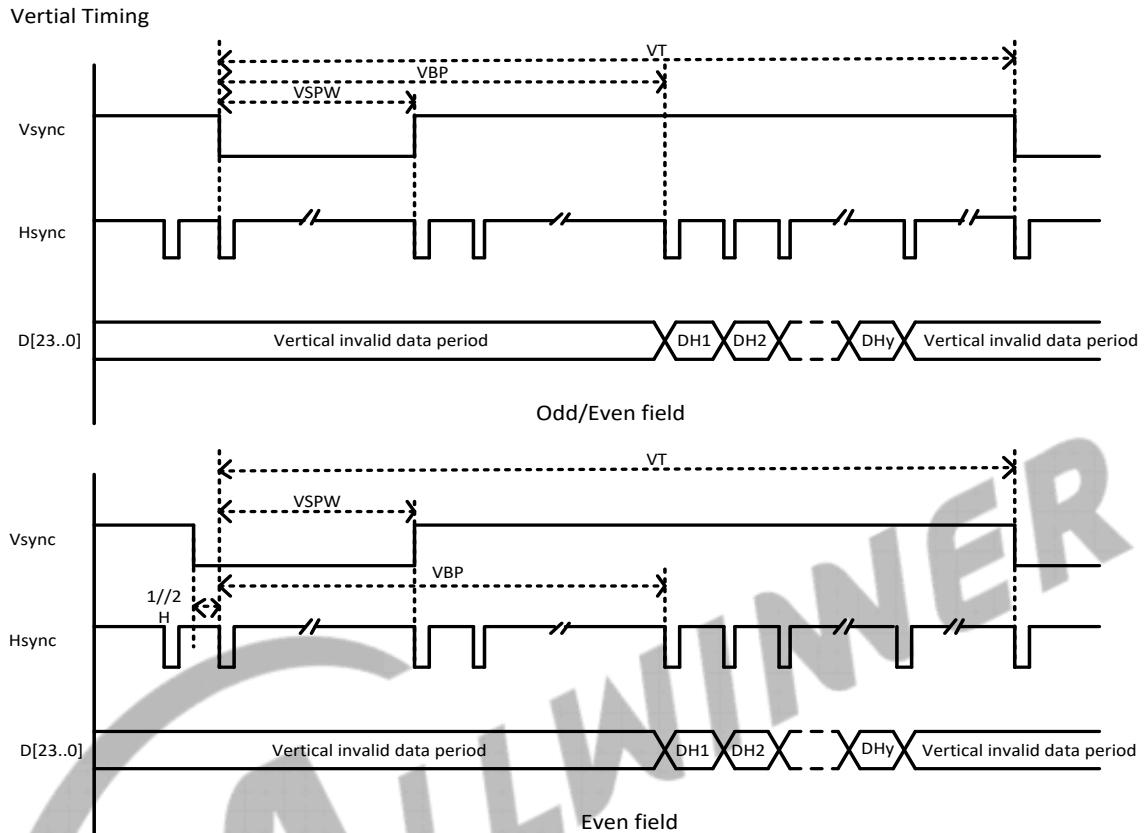
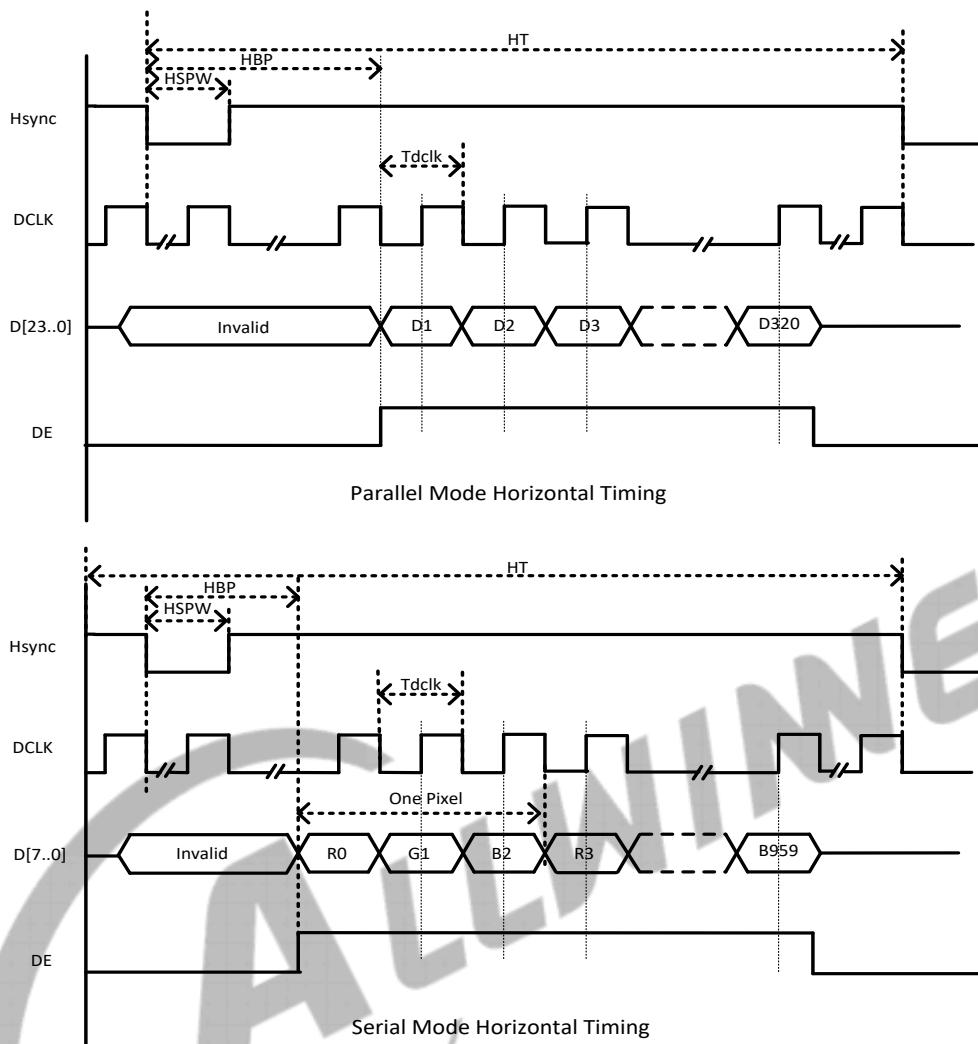


Figure 7-3 HV Interface Horizontal Timing



BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 7-3 BT656 Panel Signals

Signal Name	Description	Type
DCLK	Clock signal	O
DATA[7:0]	Data signal	O

Its logic is:

F = "0" for Field 1 F = "1" for Field 2

V = "1" during vertical blanking

H = "0" at SAV H = "1" at EAV

P3-P0 = protection bits

$$P3 = V \oplus H$$

$$P2 = F \oplus H$$

$$P1 = F \oplus V$$

$$P0 = F \oplus V \oplus H$$

Where \oplus represents the exclusive-OR function.

The 4 byte SAV/EAV sequence is as follows.

Figure 7-4 EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

i8080 Interface

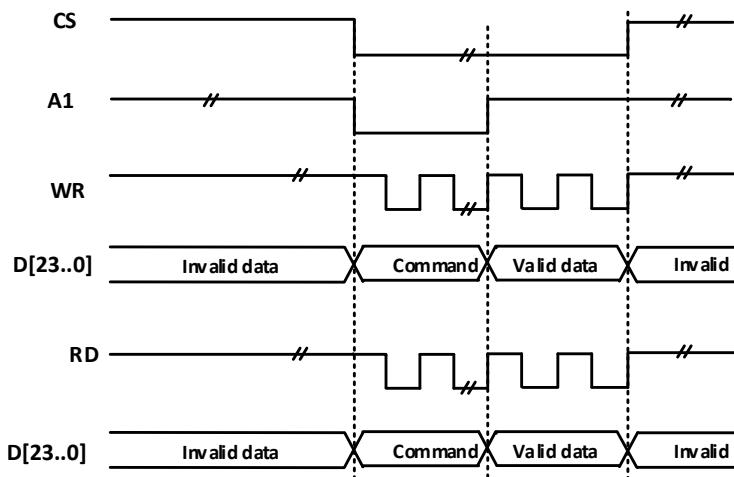
The i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. The CPU control signals are active low.

Table 7-4 CPU Panel Signals

Main Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPU1/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure shows the relationship between basic timing and CPU timing. WR is 180° delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

Figure 7-5 i8080 Interface Timing



When CPU I/F is in IDLE state, it can generate WR/RD timing by setting “Lcd_CPUI/F”. The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

7.1.3.5 CEU Module

This module enhances color data from DE .

$$R' = Rr * R + Rg * G + Rb * B + Rc$$

$$G' = Gr * R + Gg * G + Gb * B + Gc$$

$$B' = Br * R + Bg * G + Bb * B + Bc$$



NOTE

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb s13 (-16, 16)

Rc, Gc, Bc s19 (-16384, 16384)

R, G, B u8 [0-255]

R' has the range of [Rmin ,Rmax]

G' has the range of [Rmin ,Rmax]

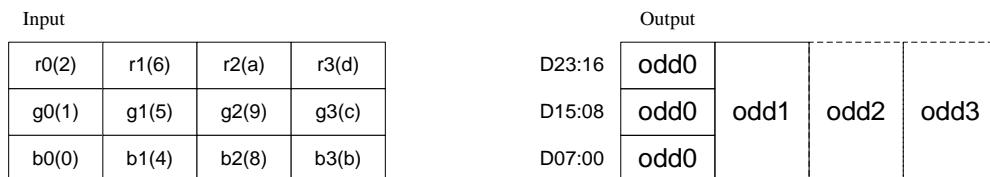
B' has the range of [Rmin ,Rmax]

7.1.3.6 CMAP Module

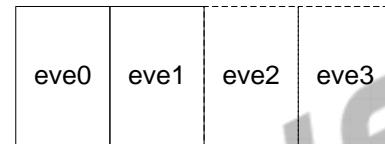
Function: This module map color data from DE.

Every 4 input pixels are as a unit. A unit is divided into 12 bytes. Output byte can select one of those 12 bytes. Note that even line and odd line can be different, and output can be 12 bytes (4 pixels) or reduce to 6 bytes (2 pixels).

Figure 7-6 CMAP Module

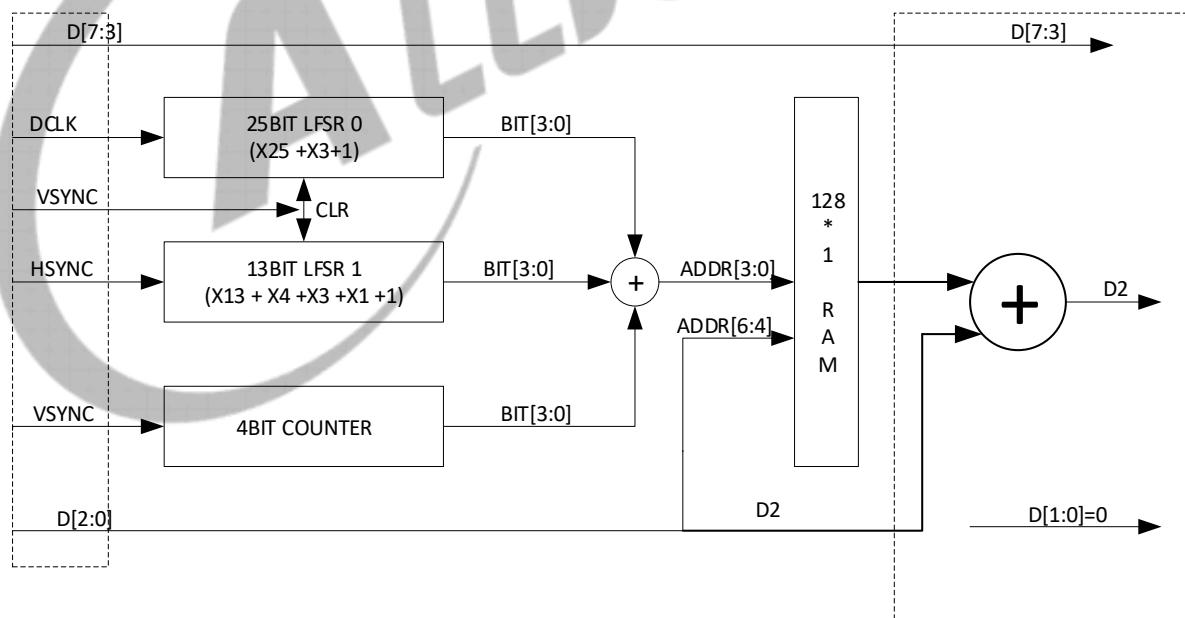


In mode: 4 pixels
Out mode: 4 pixels/2 pixels



7.1.3.7 FRM Module

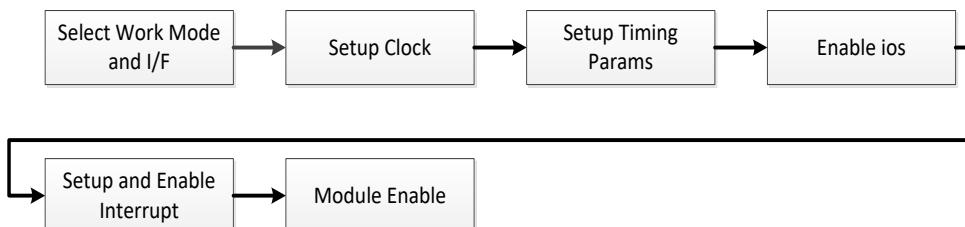
Figure 7-7 FRM Module



7.1.4 Programming Guidelines

7.1.4.1 HV Mode Configuration Process

Figure 7-8 HV Mode Initial Process



- Parallel RGB

1. Select HV interface type

LCD_CTL_REG[LCD_IF] (reg0x40) to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE] (reg0x58) to 0 to select 24bit/1cycle parallel mode.

```
lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);
```

```
lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...
```

```
lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24bit/1cycle parallel mode;
```

2. Clock configuration



NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0–2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

```
lcd_dev[sel]->lcd_dclk.dclk_en = en;
```

```
lcd_dev[sel]->lcd_dclk.dclk_div = div;
```

3. Set sequence parameters

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASE2_REG.VT needs be set to the twice of the actual value.

```
lcd_dev[sel]->lcd_basic0.x = x-1;  
lcd_dev[sel]->lcd_basic0.y = y-1;  
lcd_dev[sel]->lcd_basic1.ht = ht-1;  
lcd_dev[sel]->lcd_basic1.hbp = hbp-1;  
lcd_dev[sel]->lcd_basic2.vt = vt*2;  
lcd_dev[sel]->lcd_basic2.vbp = vbp-1;  
lcd_dev[sel]->lcd_basic3.hspw = hspw-1;  
lcd_dev[sel]->lcd_basic3.vspw = vspw-1;
```

4. Open IO output

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0~3_INV (reg0x88).

5. Set and open interrupt function

The LCD_GINT0_REG (reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG (reg0x8) sets the interrupt line position of Line interrupt mode.

V interrupt:

```
lcd_dev[sel]->lcd_gint0.vb_en = 1;
```

Line interrupt:

```
lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;
```

```
lcd_dev[sel]->lcd_gint0.line_en = 1;
```

6. Open module enable

Enable LCD_CTL_REG.LCD_EN (reg0x40) and LCD_GCTL_REG.LCD_EN (reg0x00).

```
lcd_dev[sel]->lcd_ctl.lcd_en = 1;
```

```
lcd_dev[sel]->lcd_gctl.lcd_en = 1;
```

• Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

1. Select HV interface type

Set LCD_CTL_REG.LCD_IF (reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE (reg0x58) to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

```
lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);
lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...
lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;
```

2. Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASE2_REG.VT needs not to be set to the twice of the actual value.

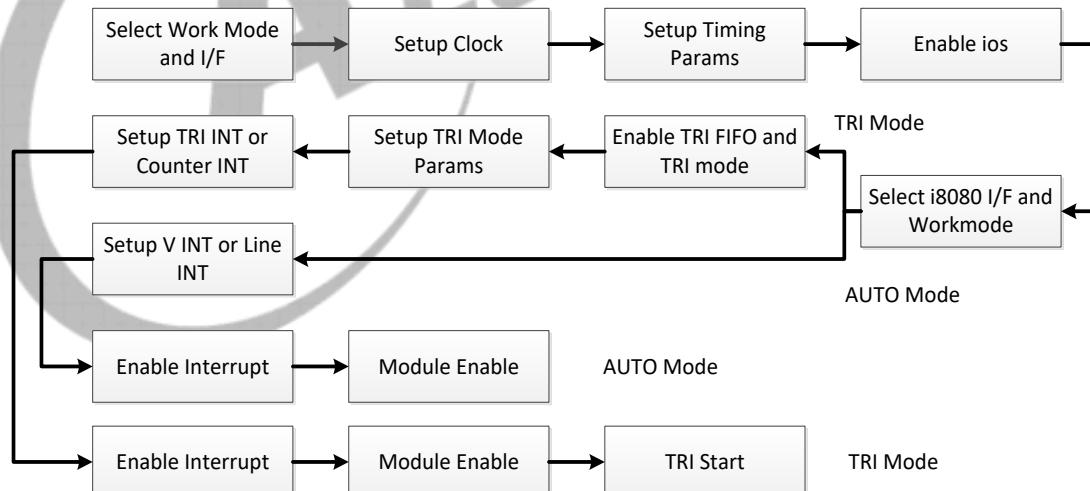
```
lcd_dev[sel]->lcd_basic2.vt = vt;
```

Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

```
lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;
lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;
```

7.1.4.2 i8080 Mode Configuration Process

Figure 7-9 i8080 Mode Initial Process



1. Select i8080 interface type.
2. The step is the same as HV mode, but pulse adjustment function is invalid.
3. The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.
4. The step is the same as HV mode.

5. Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

-----For TRI mode-----

6. Open TRI FIFO switch, and TRI mode function.
7. Set parameters of TRI mode, including block size, block space and block number.



NOTE

When output interface is parallel mode, then the setting value of block space parameter is not less than 20.

When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.

When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.

When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

8. Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to "1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.
9. Open the total switch of interrupt.
10. Open the total enable of interrupt.
11. Operate "tri start" operation (the bit1 of LCD_CPU_IF_REG is set to "1").

-----For Auto mode-----

6. Set and open V interrupt or Line interrupt, the step is the same as HV mode.
7. Open module total enable.

7.1.5 Register List

Module Name	Base Address
TCONLCD0	0x0546 1000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register

Register Name	Offset	Description
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x014+N*0x04(N=0~5)	LCD FRM Seed Register
LCD_FRM_TAB_REG	0x02C+N*0x04(N=0~3)	LCD FRM Table Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD Hv Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RDO_REG	0x0068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x0110+N*0x04(N=0~10)	LCD CEU Coefficient Register0
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10(N=0~2)	LCD CEU Coefficient Register1
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04(N=0~2)	LCD CEU Coefficient Register2
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x0180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x0190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x0194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x0198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x019C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
FSYNC_GEN_CTRL_REG	0x0228	LCD FSYNC Generate Control Register
FSYNC_GEN_DLY_REG	0x022C	LCD FSYNC Generate Delay Register
LCD_SYNC_CTL_REG	0x0230	LCD Sync Control Register
LCD_SYNC_POS_REG	0x0234	LCD Sync Position Register
LCD_SLAVE_STOP_POS_REG	0x0238	LCD Slave Stop Position Register

7.1.6 Register Description

7.1.6.1 0x0000 LCD Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN When it is disabled, the module will be reset to idle state. 0: Disable 1: Enable
30:0	/	/	/

7.1.6.2 0x0004 LCD Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_VB_INT_EN Enable the Vb interrupt 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN Enable the line interrupt 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN Enable the trigger finish interrupt 0: Disable 1: Enable
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN Enable the trigger counter interrupt 0: Disable 1: Enable
25:16	/	/	/
15	R/WOC	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame Write 0 to clear it.
14	/	/	/
13	R/WOC	0x0	LCD_LINE_INT_FLAG Trigger when SY0 match the current LCD scan line Write 0 to clear it.
12	/	/	/

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
11	R/WOC	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when CPU trigger mode finished Write 0 to clear it.
10	R/WOC	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/WOC	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when sync by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/WOC	0x0	FSYNC_INT_INV Enable the fsync interrupt to set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/WOC	0x0	DE_INT_FLAG Asserted at the first valid line in every frame Write 0 to clear it.
0	R/WOC	0x0	FSYNC_INT_FLAG Asserted at the FSYNC signal in every frame Write 0 to clear it.

7.1.6.3 0x0008 LCD Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger (including inactive lines). Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 is disabled.
15:0	/	/	/

7.1.6.4 0x0010 LCD FRM Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_FRM_EN Enable the dither function 0: Disable 1: Enable
30:7	/	/	/

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	LCD_FRM_MODE_R The R component output bits in dither function 0: 6-bit FRM output 1: 5-bit FRM output
5	R/W	0x0	LCD_FRM_MODE_G The G component output bits in dither function 0: 6-bit FRM output 1: 5-bit FRM output
4	R/W	0x0	LCD_FRM_MODE_B The B component output bits in dither function 0: 6-bit FRM output 1: 5-bit FRM output
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST Set the test mode of dither function 00: FRM 01: Half 5-/6-bit, half FRM 10: Half 8-bit, half FRM 11: Half 8-bit, half 5-/6-bit

7.1.6.5 0x0014+ N*0x04 (N=0~5) LCD FRM Seed Register (Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04 (N=0~5)			Register Name:
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE Set the seed used in dither function N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Note: Avoid setting it to 0.

7.1.6.6 0x002C+ N*0x04 (N=0~3) LCD FRM Table Register (Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04 (N=0~3)			Register Name: LCD_FRM_TAB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	<p>FRM_TABLE_VALUE Set the data used in dither function Usually set as follows: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777</p>

7.1.6.7 0x0040 LCD Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>LCD_EN It executes at the beginning of the first blank line of LCD timing. 0: Disable 1: Enable</p>
30:26	/	/	/
25:24	R/W	0x0	<p>LCD_IF Set the interface type of LCD controller. 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved</p>
23	R/W	0x0	<p>LCD_RB_SWAP Enable the function to swap red data and blue data in fifo1. 0: Default 1: Swap RED and BLUE data at FIFO1</p>
22	/	/	/
21	R/W	0x0	<p>LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK</p>
20	R/W	0x0	<p>LCD_INTERLACE_EN This flag is valid only when LCD_EN == 1 0: Disable 1: Enable</p>
19:9	/	/	/
8:4	R/W	0x0	<p>LCD_START_DLY The unit of delay is T_line. Note: Valid only when LCD_EN == 1</p>
3	/	/	/

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	<p>LCD_SRC_SEL LCD Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reversed 111: Gridding Check</p>

7.1.6.8 0x0044 LCD Data Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	<p>LCD_DCLK_EN LCD clock enable 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others: Reversed</p>
27:7	/	/	/
6:0	R/W	0x0	<p>LCD_DCLK_DIV Tdclk = Tsclk/DCLKDIV Note: 1.If dclk1&dclk2 are used, DCLKDIV >=6 2.If only dclk is used, DCLKDIV >=1</p>

7.1.6.9 0x0048 LCD Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	WIDTH_X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_Y Panel height is Y+1

7.1.6.10 0x004C LCD Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT $\text{Thcycle} = (\text{HT}+1) * \text{Tdclk}$ Computation: 1) parallel: $\text{HT} = X + \text{BLANK}$ Limitation: 1) parallel: $\text{HT} \geq (\text{HBP}+1) + (X+1) + 2$ 2) serial 1: $\text{HT} \geq (\text{HBP}+1) + (X+1) * 3 + 2$ 3) serial 2: $\text{HT} \geq (\text{HBP}+1) + (X+1) * 3/2 + 2$
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch (in dclk) $\text{Thbp} = (\text{HBP}+1) * \text{Tdclk}$

7.1.6.11 0x0050 LCD Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	VT $\text{TVT} = (\text{VT})/2 * \text{Thsync}$ $\text{VT}/2 \geq (\text{VBP}+1) + (\text{Y}+1) + 2$
15:12	/	/	/
11:0	R/W	0x0	VBP $\text{Tvbp} = (\text{VBP}+1) * \text{Thsync}$

7.1.6.12 0x0054 LCD Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	HSPW $\text{Thspw} = (\text{HSPW}+1) * \text{Tdclk}$ $\text{HT} > (\text{HSPW}+1)$
15:10	/	/	/
9:0	R/W	0x0	VSPW $\text{Tvspw} = (\text{VSPW}+1) * \text{Thsync}$ $\text{VT}/2 > (\text{VSPW}+1)$

7.1.6.13 0x0058 LCD HV Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	<p>HV_MODE Set the HV mode of LCD controller 0000: 24-bit/1-cycle parallel mode 1000: 8-bit/3-cycle RGB serial mode (RGB888) 1010: 8-bit/4-cycle Dummy RGB (DRGB) 1011: 8-bit/4-cycle RGB Dummy (RGBD) 1100: 8-bit/2-cycle YUV serial mode (CCIR656)</p>
27:26	R/W	0x0	<p>RGB888_ODD_ORDER Serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7...). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B</p>
25:24	R/W	0x0	<p>RGB888_EVEN_ORDER Serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8...). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B</p>
23:22	R/W	0x0	<p>YUV_SM Serial YUV mode Output sequence 2-pixel-pair of every scan line. 00: YUYV 01: YYUU 10: UYYV 11: VYUY</p>
21:20	R/W	0x0	<p>YUV_EAV_SAV_F_LINE_DLW Set the delay line mode. 00: F toggle right after active video line 01: delay 2 line (CCIR PAL) 10: delay 3 line (CCIR NTSC) 11: reserved</p>
19	R/W	0x0	<p>CCIR_CSC_DIS LCD convert source from RGB to YUV. 0: Enable 1: Disable Only valid when HV mode is "1100".</p>
18:0	/	/	/

7.1.6.14 0x0060 LCD CPU Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	CPU_MODE Set the CPU interface work mode 0000: 18-bit/256K mode 0010: 16-bit mode0 0100: 16-bit mode1 0110: 16-bit mode2 1000: 16-bit mode3 1010: 9-bit mode 1100: 8-bit 256K mode 1110: 8-bit 65K mode xxx1: 24-bit for DSI
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG The status of write operation. 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG The status of read operation. 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto transfer mode If it is 1, all the valid data during this frame are written to panel. Note: This bit is sampled by Vsync.
16	R/W	0x0	FLUSH Direct transfer mode If it is enabled, FIFO1 is regardless of the HV timing, the pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRI_FIFO_BIST_EN Entry address is 0xFF8 0: Disable 1: Enable

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	TRI_FIFO_EN Enable the trigger FIFO 0: Disable 1: Enable
1	R/W1S	0x0	TRI_START Software must make sure that write '1' only when this flag is '0'. Writing '1' starts a frame flush and writing '0' has no effect. This flag indicates the frame flush is running.
0	R/W	0x0	TRI_EN Enable trigger mode 0: Trigger mode disable 1: Trigger mode enable

7.1.6.15 0x0064 LCD CPU Panel Write Data Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus.

7.1.6.16 0x0068 LCD CPU Panel Read Data Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus.

7.1.6.17 0x006C LCD CPU Panel Read Data Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus.

7.1.6.18 0x0088 LCD IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	<p>IO_OUTPUT_SEL When it is set as '1', the d[23:0], io0, io1, io3 are sync to dclk. 0: Normal output 1: Register output</p>
30:28	R/W	0x0	<p>DCLK_SEL Set the phase offset of clock and data in hv mode. 000: Used DCLK0 (normal phase offset) 001: Used DCLK1 (1/3 phase offset) 010: Used DCLK2 (2/3 phase offset) 100: DCLK0/2 phase 0 101: DCLK0/2 phase 90 Others: Reserved</p>
27	R/W	0x0	<p>IO3_INV Enable invert function of IO3 0: Not invert 1: Invert</p>
26	R/W	0x0	<p>IO2_INV Enable invert function of IO2 0: Not invert 1: Invert</p>
25	R/W	0x0	<p>IO1_INV Enable invert function of IO1 0: Not invert 1: Invert</p>
24	R/W	0x0	<p>IO0_INV Enable invert function of IO0 0: Not invert 1: Invert</p>
23:0	R/W	0x0	<p>Data_INV LCD output port D[23:0] polarity control, with independent bit control. 0: Normal polarity 1: Invert the specify output</p>

7.1.6.19 0x008C LCD IO Control Register (Default Value: 0xFFFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	RGB_ENDIAN Set the endian of data bits 0: Normal 1: Bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN Enable the output of IO3 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN Enable the output of IO2 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN Enable the output of IO1 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN Enable the output of IO0 1: Disable 0: Enable
23:0	R/W	0xFFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D[23:0] output enable, with independent bit control. 1: Disable 0: Enable

7.1.6.20 0x00FC LCD Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	LCD_FIFO_UNDERFLOW The flag shows whether the fifos in underflow status 0: Not underflow 1: Underflow
30	/	/	/
29	R	0x0	LCD_FIELD_POL The flag indicates the current field polarity 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
15:0	/	/	/

7.1.6.21 0x0100 LCD CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CEU_EN Enable CEU function 0: Bypass 1: Enable
30	R/W	0x0	BT656_F_MASK BT656 F Mask 0: Disable 1: Enable
29	R/W	0x0	BT656_F_MASK_VALUE BT656 F Mask Value
28:0	/	/	/

7.1.6.22 0x0110+N*0x04 (N=0~10) LCD CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0~10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13-bit value, range of (-16,16). N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

7.1.6.23 0x011C+N*0x10 (N=0~2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10 (N=0~2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

Offset: 0x011C+N*0x10 (N=0~2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19-bit value, range of (-16384, 16384). N=0: Rc N=1: Gc N=2: Bc

7.1.6.24 0x0140+N*0x04 (N=0~2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0~2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0, 255].
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0, 255].

7.1.6.25 0x0160 LCD CPU Panel Trigger Register0 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set >20*pixel.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

7.1.6.26 0x0164 LCD CPU Panel Trigger Register1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

7.1.6.27 0x0168 LCD CPU Panel Trigger Register2 (Default Value: 0x0020_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x20	START_DLY $T_{dly} = (\text{Start_Delay} + 1) * \text{be_clk} * 8.$
15	R/W	0x0	TRANS_START_MODE Select the FIFOs used in CPU mode. 0: ECC_FIFO+TRI_FIFO 1: TRI_FIFO
14:13	R/W	0x0	SYNC_MODE Set the sync mode in CPU interface. 0x: Auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

7.1.6.28 0x016C LCD CPU Panel Trigger Register3 (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE When set as 01, the Tri_Counter_Int occurs in cycle of (Count_N+1)×(Count_M+1)×4 dclk. When set as 10 or 11, the io0 is map as TE input. 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor
7:0	R/W	0x0	COUNTER_M The value of counter factor

7.1.6.29 0x0170 LCD CPU Panel Trigger Register4 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/