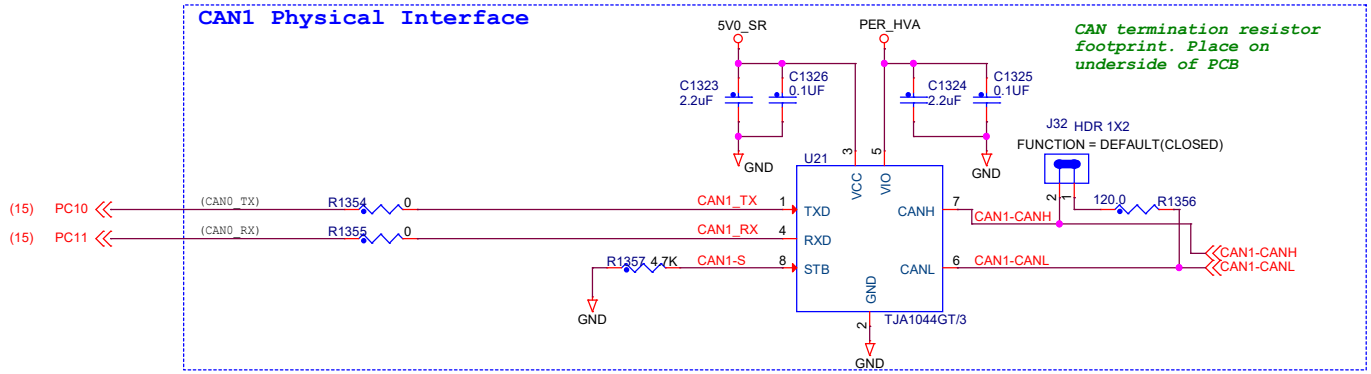
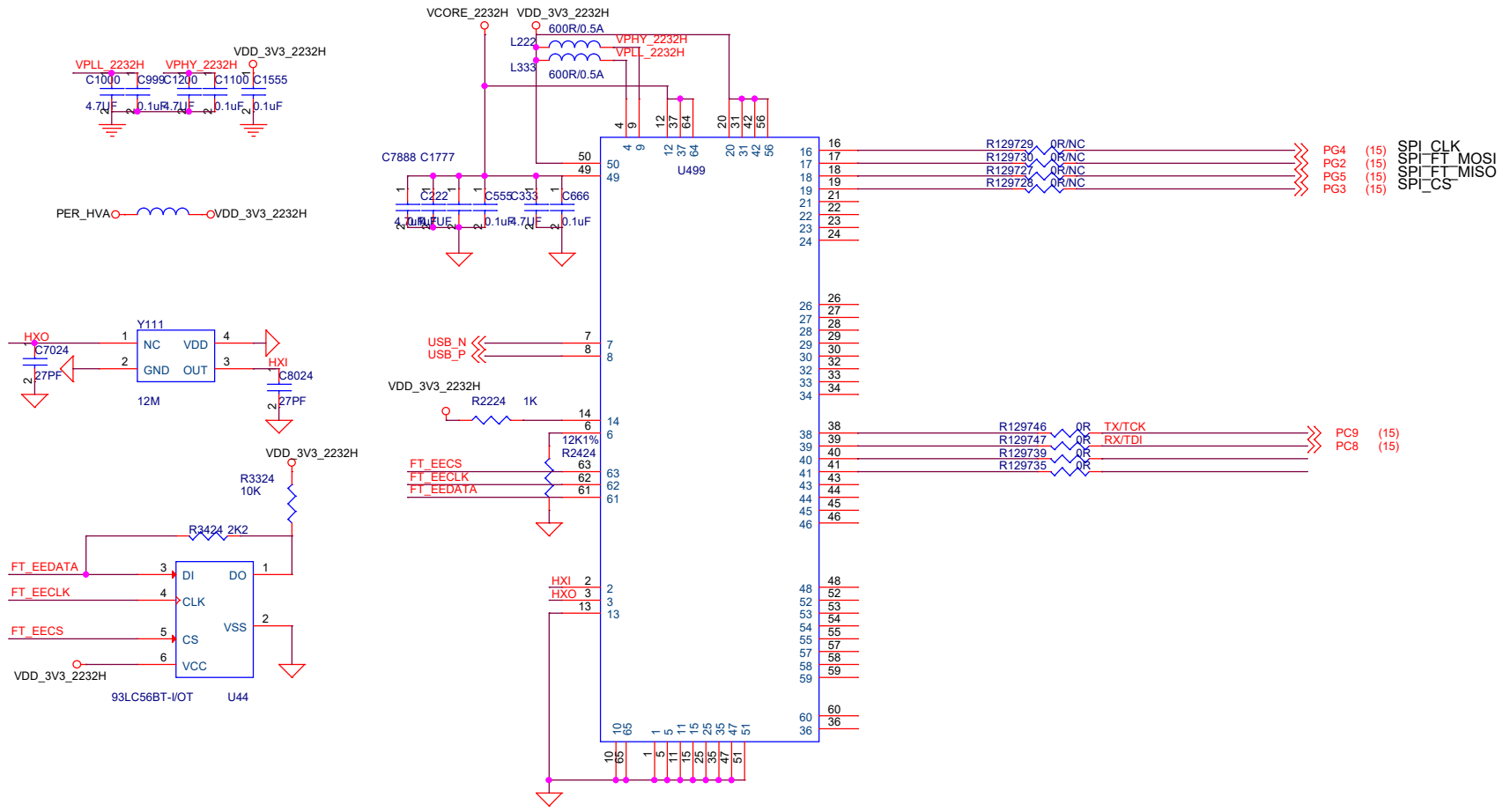

CAN1 Physical Interface
5V0_SR
PER_HVA
CAN termination resistor footprint. Place on underside of PCB
C1323 2.2uF
C1326 0.1UF
C1324 2.2uF
C1325 0.1UF
GND
GND
J32 HDR 1X2
FUNCTION = DEFAULT(CLOSED)
U21
VCC
VIO
(15) PC10
(15) PC11
(CAN0_TX)
(CAN0_RX)
R1354 0
R1355 0
CAN1_TX
CAN1_RX
TXD
RXD
STB
CANH
CANL
CAN1-CANH
CAN1-CANL
120.0 R1356
R1357 4.7K
CAN1-S
GND
GND
TJA1044GT/3


VDD_3V3_2232H
VPLL_2232H
VPHY_2232H
C1000
C999
C1200
C1100
C1555
4.7UF
0.1uF
4.7UF
0.1uF
0.1uF
PER_HVA
VDD_3V3_2232H
VCORE_2232H
VDD_3V3_2232H
600R/0.5A
L222
VPHY_2232H
VPLL_2232H
L333
600R/0.5A
C7888 C1777
C222
C555
C333
C666
4.7UF
0.1uF
4.7UF
0.1uF
U499
R129729 0R/NC
R129730 0R/NC
R129727 0R/NC
R129728 0R/NC
PG4 (15) SPI_CLK
PG2 (15) SPI_FT_MOSI
PG5 (15) SPI_FT_MISO
PG3 (15) SPI_CS
Y111
HXO
C7024
27PF
NC
VDD
GND
OUT
12M
HXI
C8024
27PF
USB_N
USB_P
VDD_3V3_2232H
R2224 1K
12K1%
R2424
FT_EECS
FT_EECLK
FT_EEDATA
R129746 0R TX/TCK
R129747 0R RX/TDI
R129739 0R
R129735 0R
PC9 (15)
PC8 (15)
VDD_3V3_2232H
R3324
10K
R3424 2K2
FT_EEDATA
FT_EECLK
FT_EECS
VDD_3V3_2232H
DI
DO
CLK
CS
VSS
VCC
93LC56BT-I/OT
U44
HXI
HXO

FlexRay V1 2023.02.13

Table Of Contents:

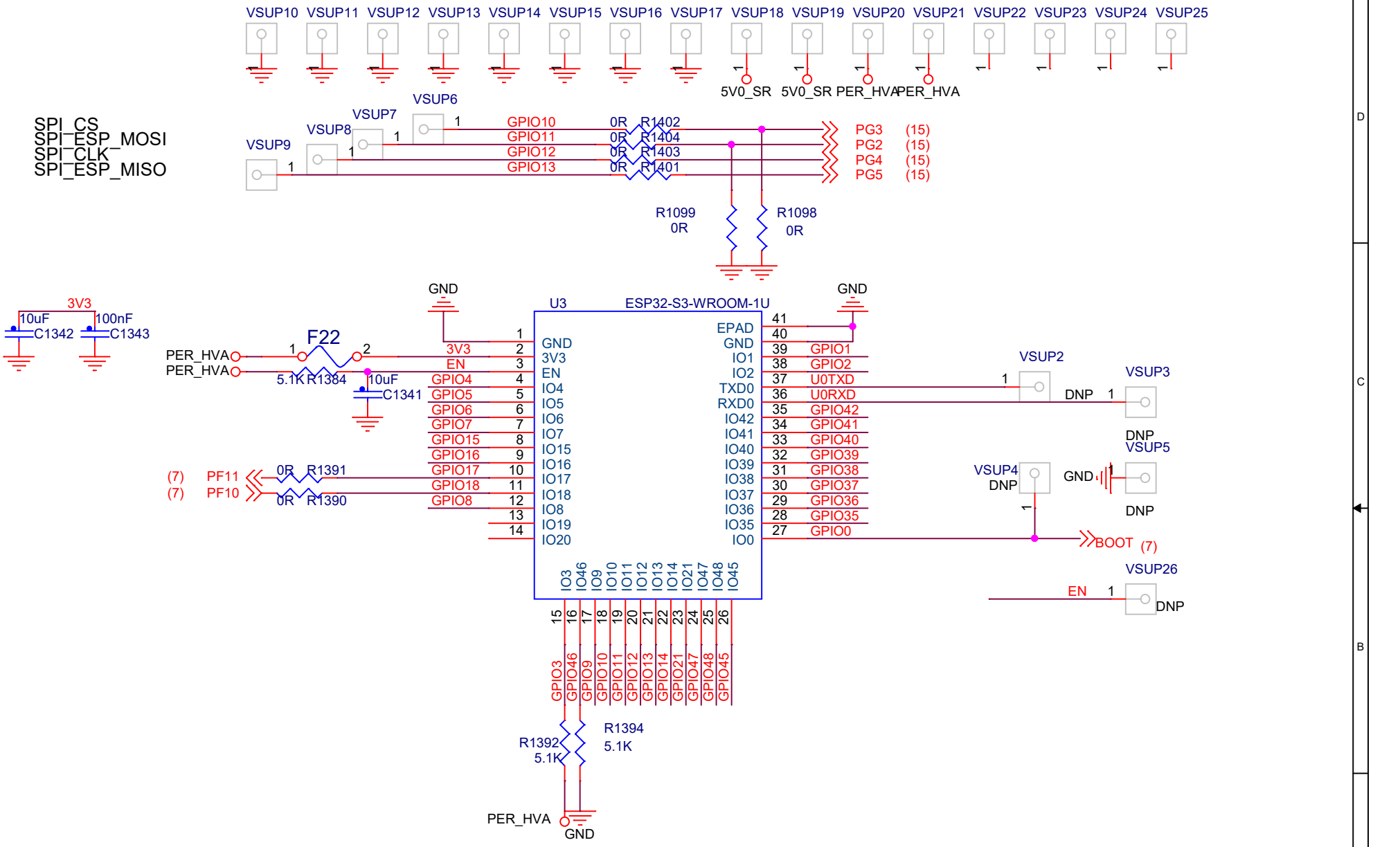
Revision Information

Rev	Date	Designer	Comments
A1	13 Jan 2023	Mingming Wan	

Automotive Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: C Neacsu	Drawing Title: DEVKIT-MPC5748G	
Drawn by: C Neacsu	Page Title: Index and Title Page	
Approved: Pesses Philip	Size B / Document Number SCH-29030 PDF: SPF-29030	Rev D1
	Date: Monday, April 03, 2023	Sheet 1 of 15



ESP32-S3-WROOM-1U(pin-out)
Note: This is not another chip, it is module pinout.

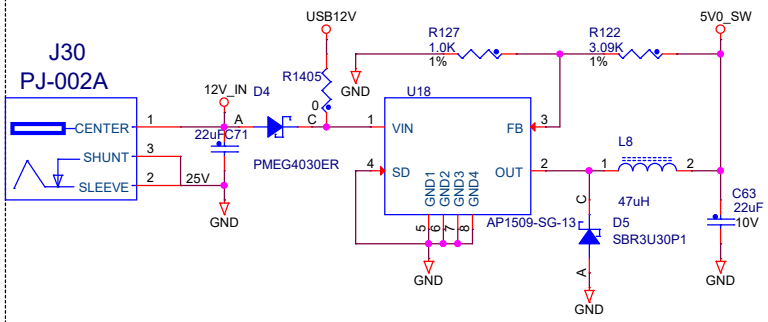
Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Saturday, July 29, 2023	Sheet 1 of 1	

Power Input and Voltage Regulators

12V Power Supply Input

5V Switching Regulator

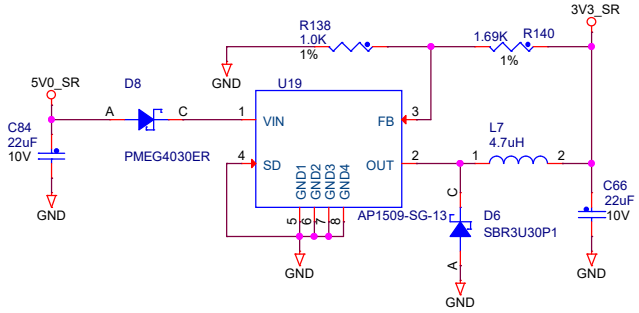
Input Voltage 12V, Output 5V at 1800mA



Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

3.3V Switching Regulator

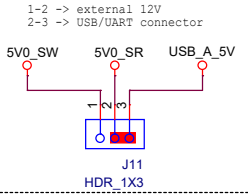
Input Voltage 5V, Output 3.3V at 1600mA



Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

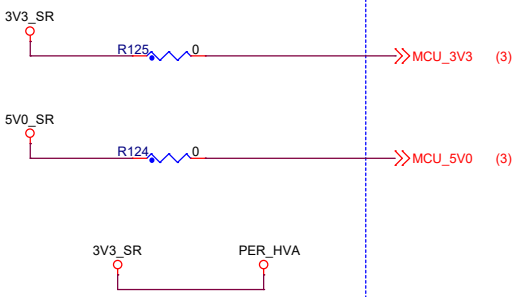
Board supply selection

Select between USB and external 12V



Power Control

Jumpers can be fitted to facilitate power measurements



Test and reference points

GND Test Points, Top Side

ICAP Classification: CP: ___ IUO: X PUBI: ___			
Drawing Title: DEVKIT-MPC5748G			
Page Title: Power Input, 5V, 3.3V Reg			
Size B	Document Number SCH-29030 PDF: SPF-29030		Rev D1
Date: Monday, April 03, 2023		Sheet 2 of 15	

Calypso MCU Power Connections

Power Supply Contraints:

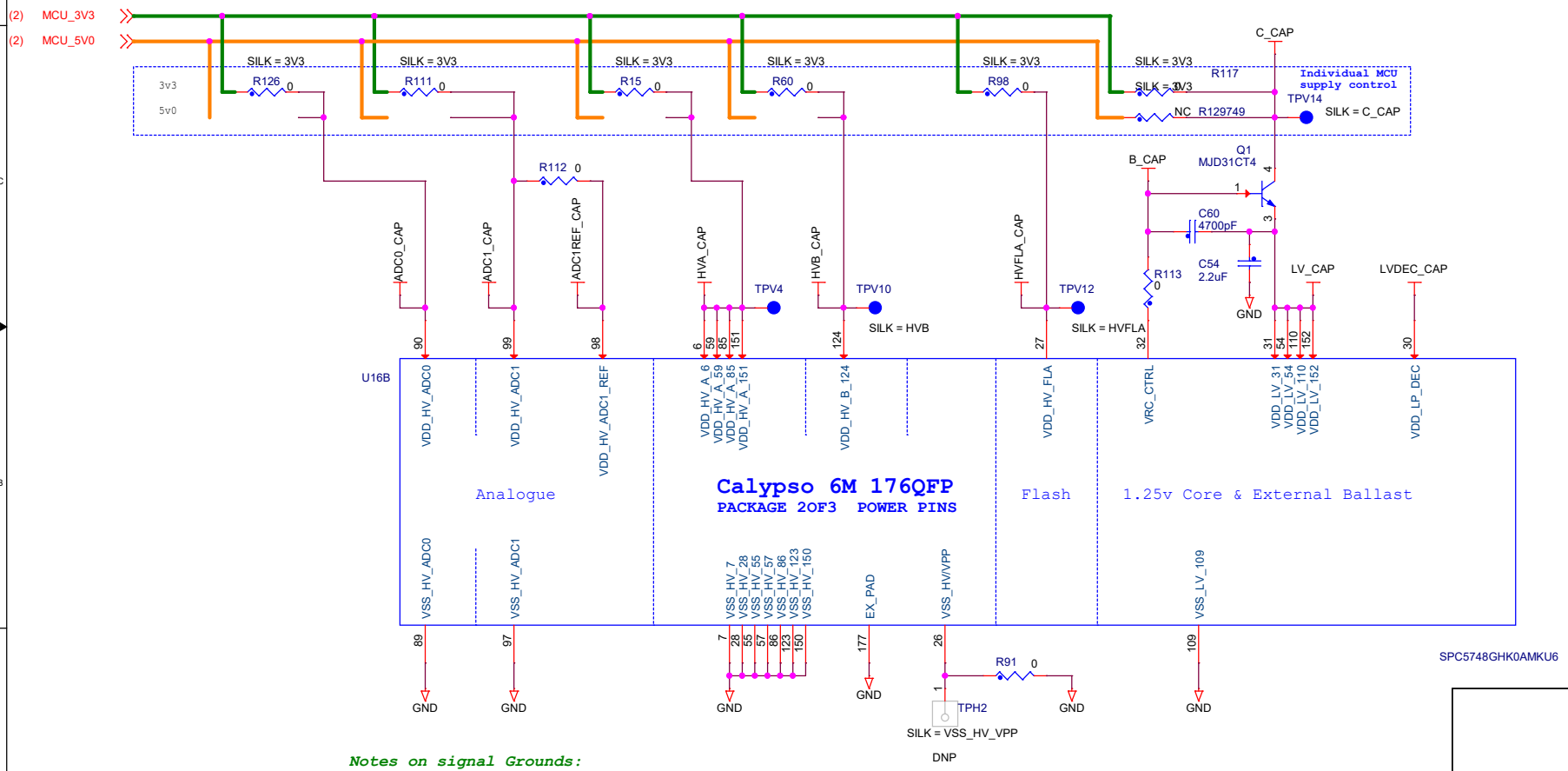
- If VDD_HV_A is driven from 3.3V, VDD_HV_FLA must also be supplied from 3.3V
- If VDD_HV_A is driven from 5V, the VDD_HV_FLA pin must be disconnected from 3.3V

- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuration:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FLA = External 3.3V supplied (jumper fitted)

The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



Notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **DEVKIT-MPC5748G**

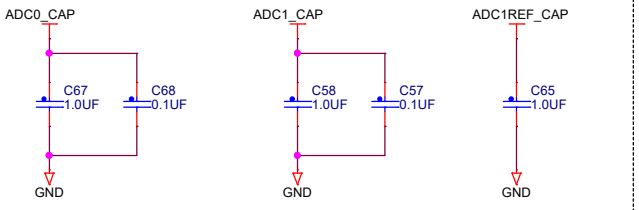
Page Title: **Calypso MCU Power**

Size	Document Number	Rev
B	SCH-29030 PDF: SPF-29030	D1

Date: Thursday, April 06, 2023 Sheet 3 of 15

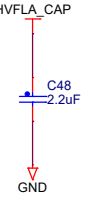
Calypso MCU Decoupling and bulk storage

ADC

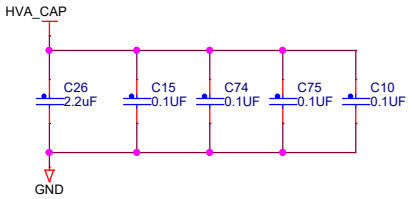


Place small Caps as close as possible to MCU pins

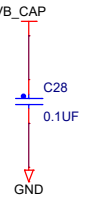
Flash



VDD_HVA

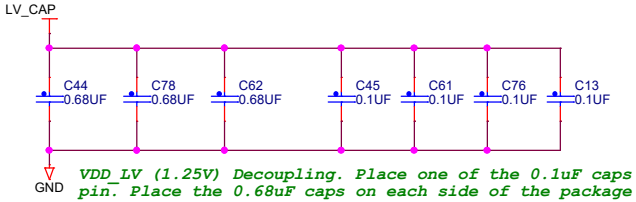


VDD_HVB



One 0.1uF cap per VDD_HV_x pin. Place as close as possible to pin

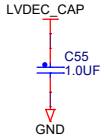
VDD_LV



VDD_LV (1.25V) Decoupling. Place one of the 0.1uF caps close to each VDD_LV pin. Place the 0.68uF caps on each side of the package such that there is no cap on the side with the ballast transistor

(For regulator stability the total capacitance should be around 2.2uF).

LP Internal Reg Cap



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Drawing Title: DEVKIT-MPC5748G		
Page Title: Calypso MCU Decoupling		
Size B	Document Number SCH-29030 PDF: SPF-29030	Rev D1
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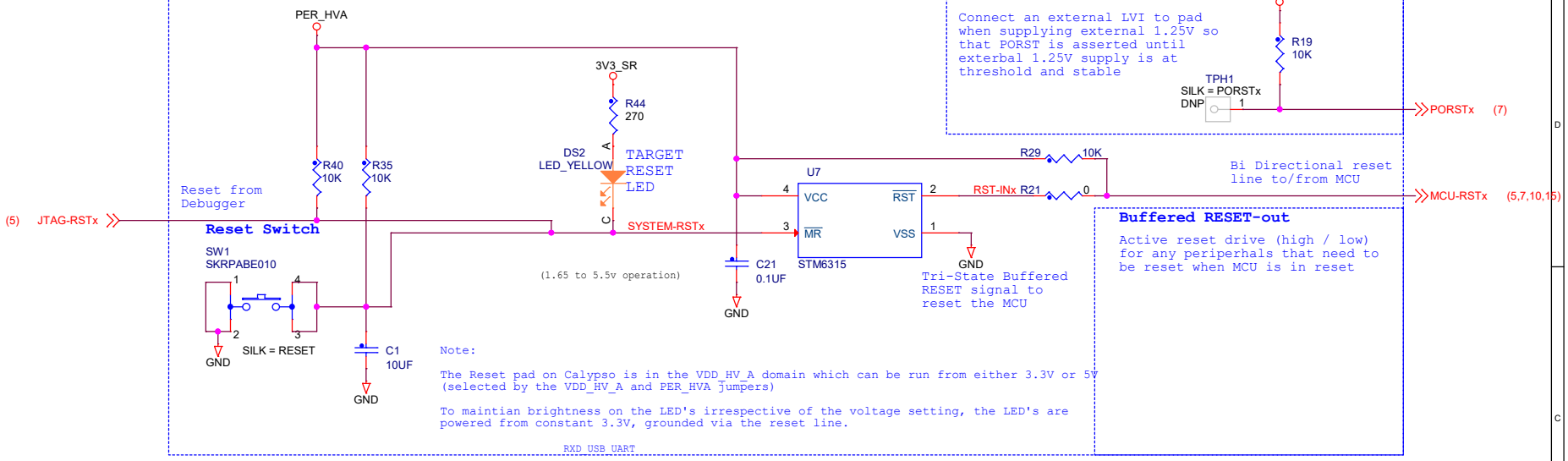
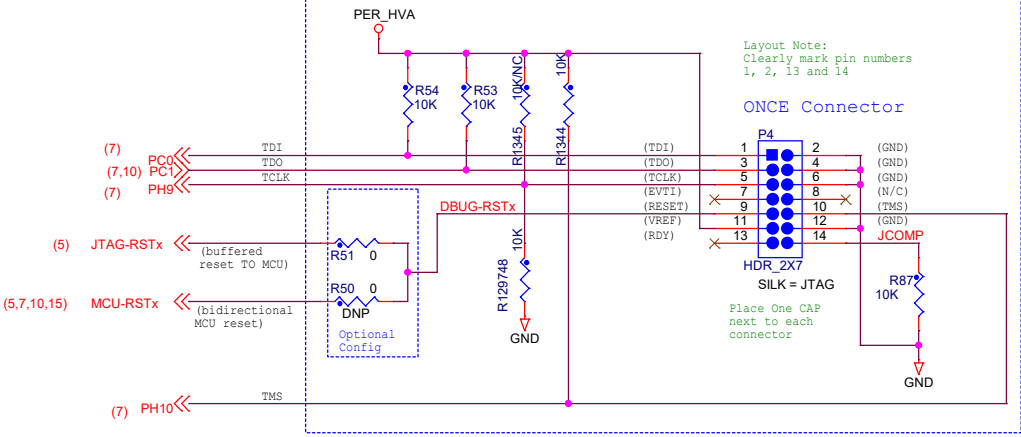
Reset and External Clock In

Reset is in the VDD_HVA domain.

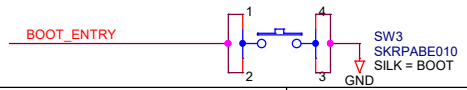
Reset Input / Output



JTAG Standard 14-pin Connector



OpenSDA INTERFACE



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Drawing Title:	DEVKIT-MPC5748G		
Page Title:	Reset Circuitry & External Clock In, JTAG		
Size B	Document Number SCH-29030 PDF: SPF-29030		Rev D1
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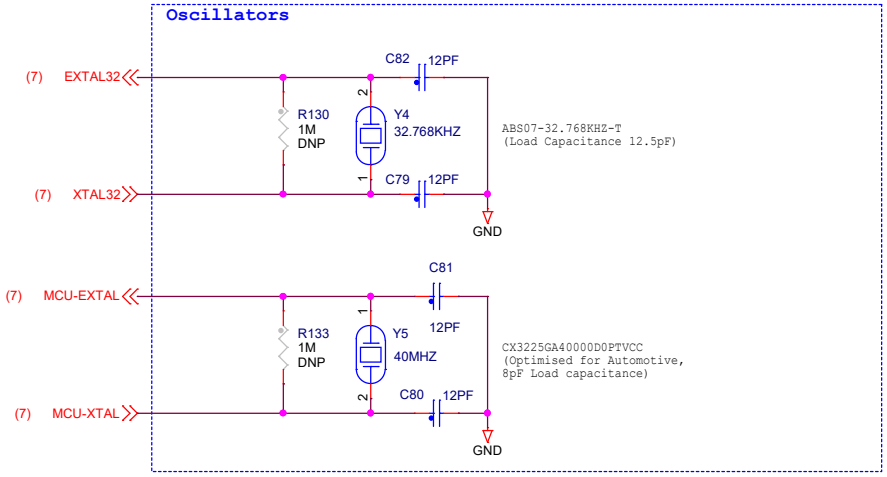
Clocks



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Page Title:	Clocks		
Size: B	Document Number: SCH-29030 PDF: SPF-29030		Rev: D1
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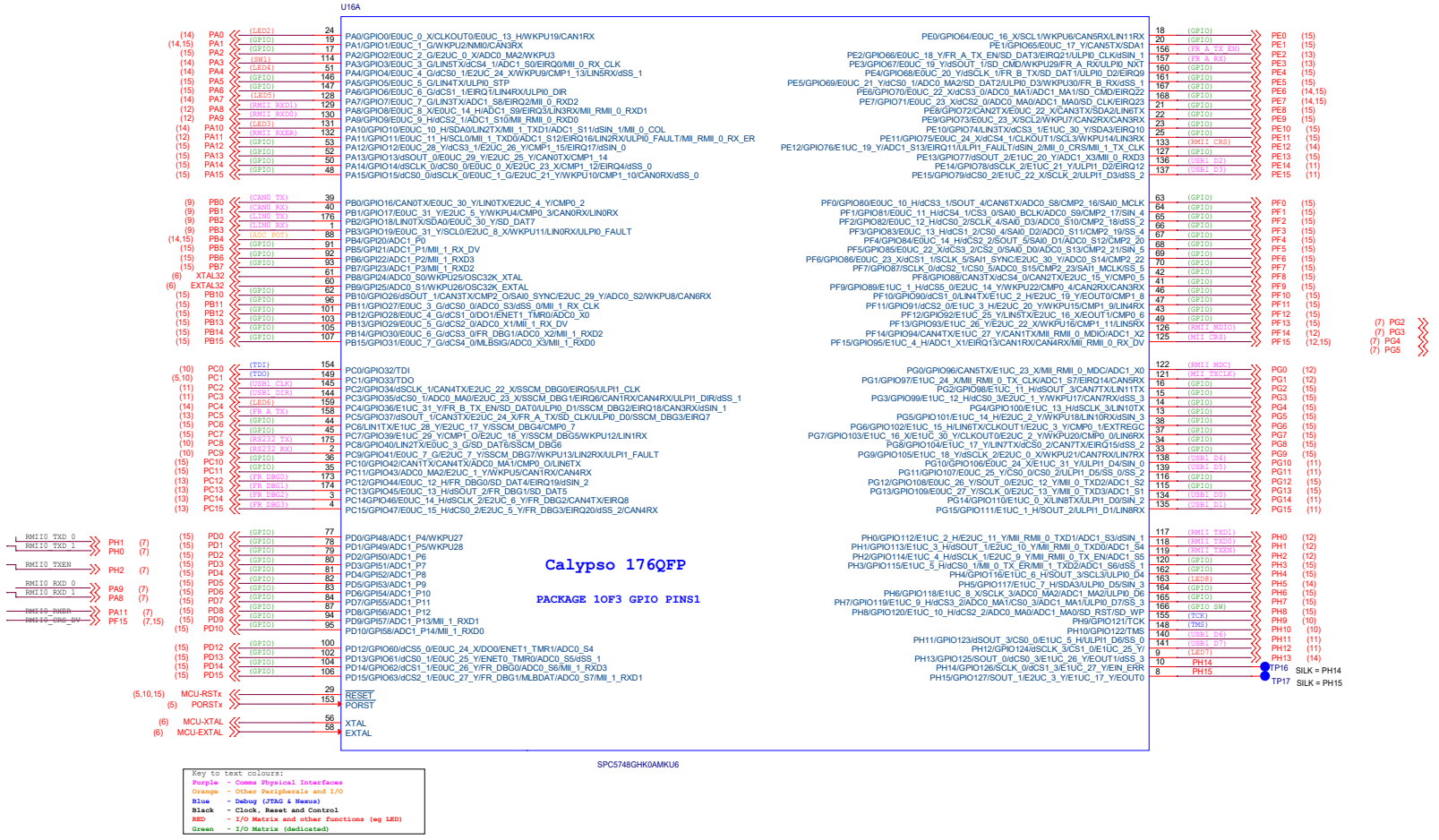
Calypso GPIO 1 of 2



Key to text colours:

- Purple – Comms Physical Interfaces
- Orange – Other Peripherals and I/O
- Blue – Debug (JTAG & Nexus)
- Black – Clock, Reset and Control
- RED – I/O Matrix and other functions (eg LED)
- Green – I/O Matrix (dedicated)

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **DEVKIT-MPC5748G**

Page Title: **Calypso GPIO 1of2**

Size	Document Number	Rev
C	SCH-29030 PDF: SPF-29030	D

Date: Tuesday, April 04, 2023 Sheet 7 of 15

Calypso GPIO 2 of 2

Key to text colours:
Purple - Comms Physical Interfaces
Orange - Other Peripherals and I/O
Blue - Debug (JTAG & Nexus)
Black - Clock, Reset and Control
RED - I/O Matrix and other functions (eg LED)
Green - I/O Matrix (dedicated)

U16C

Calypso 176QFP

PACKAGE 3OF3 GPIO PINS2

(14,15)	PI0	(GPIO)	PI0	172	PI0/GPIO128/E0UC_28_Y/LIN8TX/SDA1/SD_DAT3
(14,15)	PI1	(GPIO)	PI1	171	PI1/GPIO129/E0UC_29_Y/SCL1/SD_DAT2/WKPU24/LIN8RX
(14,15)	PI2	(GPIO)	PI2	170	PI2/GPIO130/E0UC_30_Y/LIN9TX/SDA2/SD_DAT1
(14,15)	PI3	(GPIO)	PI3	169	PI3/GPIO131/E0UC_31_Y/SCL2/SD_DAT0/WKPU23/LIN9RX
(11)	PI4	(USB1_STP)	PI4	143	PI4/GPIO132/E1UC_28_Y/SOUT_0/ULPI1_STP
(11)	PI5	(USB1_NXT)	PI5	142	PI5/GPIO133/E1UC_29_Y/SCLK_0/CS2_1/CS2_2/ULPI1_NXT
(15)	PI6	(GPIO)	PI6	11	PI6/GPIO134/E1UC_30_Y/CS0_0/CS0_1/CS0_2/DO0/SS_0/SS_1/SS_2
(11,15)	PI7	(USB1_RST)	PI7	12	PI7/GPIO135/E1UC_31_Y/CS1_0/CS1_1/CS1_2/DO1
(15)	PI8	(GPIO)	PI8	108	PI8/GPIO136/E2UC_15_Y/ADC0_S16/MLBCLK/MII_1_RX_CLK
(12,15)	PI11	(ENET_RST)	PI11	111	PI11/GPIO139/E2UC_14_Y/ENET0_TMR1/ADC0_S19/dSIN_3
(15)	PI12	(GPIO)	PI12	112	PI12/GPIO140/dCS0_3/dCS0_2/MII_1_TX_EN/ADC0_S20/dSS_2/dSS_3
(15)	PI13	(GPIO)	PI13	113	PI13/GPIO141/dCS1_3/dCS1_2/MII_1_TXD3/ADC0_S21
(15)	PI14	(GPIO)	PI14	76	PI14/GPIO142/SAI2_D0/ADC0_S22/SIN_0
(15)	PI15	(GPIO)	PI15	75	PI15/GPIO143/CS0_0/dCS2_2/SAI2_MCLK/ADC0_S23/SS_0
(15)	PJ0	(GPIO)		74	PJ0/GPIO144/CS1_0/dCS3_2/SAI2_SYNC/E2UC_19_Y/ADC0_S24
(15)	PJ1	(GPIO)		73	PJ1/GPIO145/SOUT_0/SAI2_BCLK/ADC0_S25/SIN_1
(15)	PJ2	(GPIO)		72	PJ2/GPIO146/CS0_1/CS0_2/CS0_3/SAI1_D0/ADC0_S26/SS_1/SS_2/SS_3
(15)	PJ3	(GPIO)		71	PJ3/GPIO147/CS1_1/CS1_2/CS1_3/SAI1_BCLK/ADC0_S27
(14)	PJ4	(LED1)		5	PJ4/GPIO148/SCLK_1/E1UC_18_Y/E2UC_4_Y/EIN_ERR

SPC5748GHK0AMKU6

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **DEVKIT-MPC5748G**

Page Title: **Calypso GPIO 2of2**

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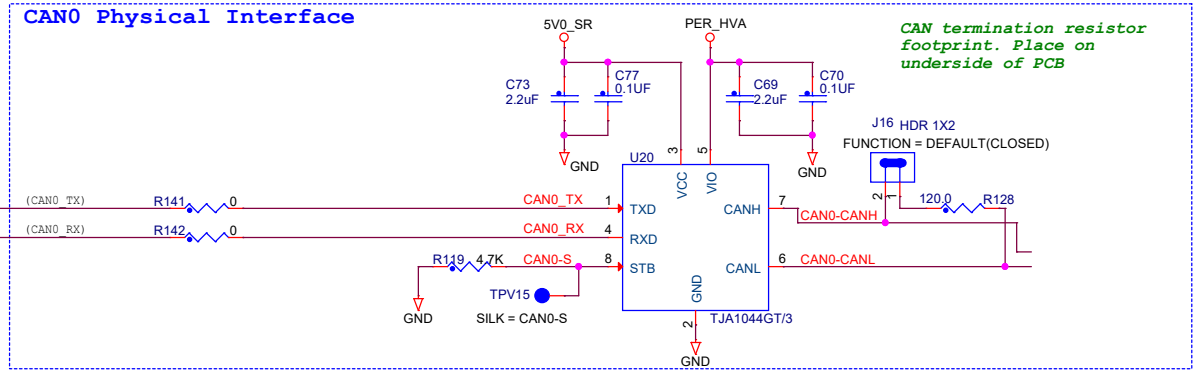
All CAN and LIN signals are in power domain VDD_HV_A.

All interfaces will work at 3.3V or 5.0V (PER_HVA)

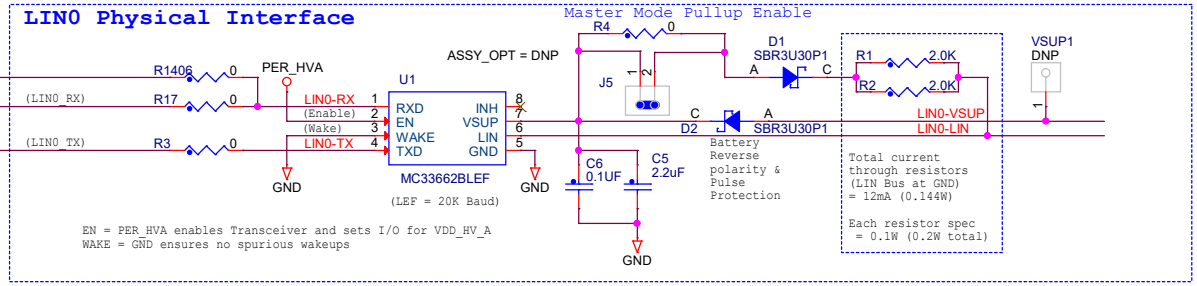
CAN & LIN

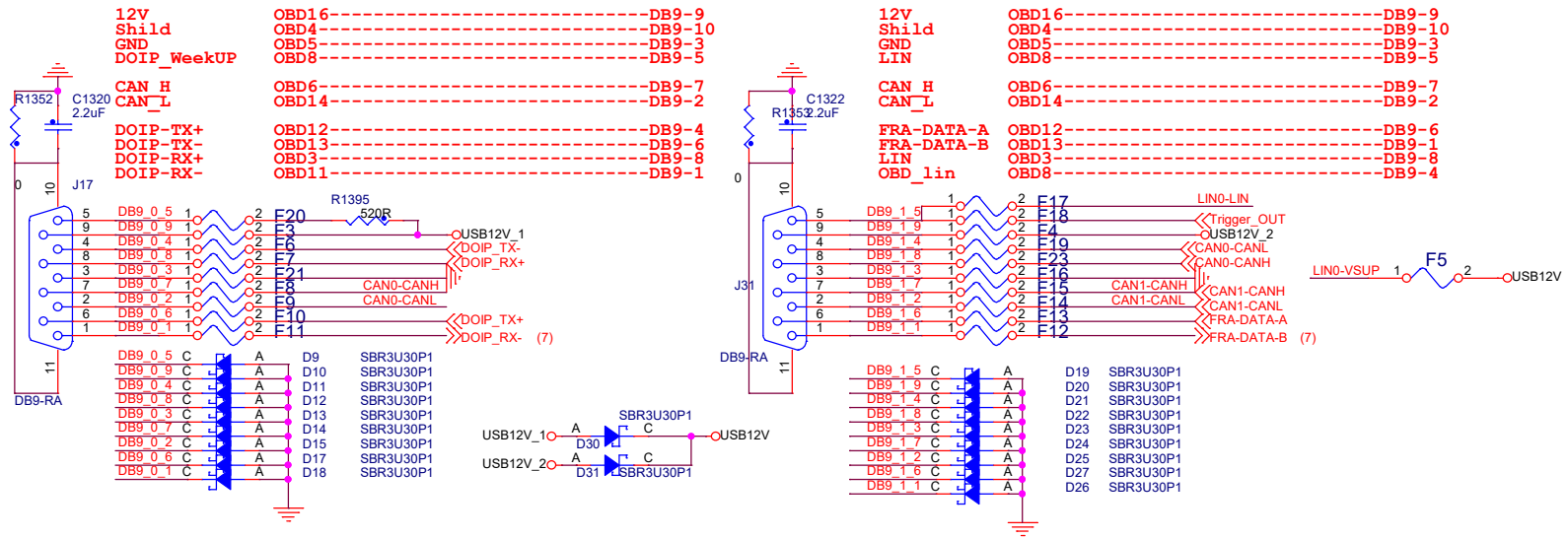
VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)
VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V
STB - High for Standby mode, pulled low for normal mode.

CAN0 Physical Interface



LIN0 Physical Interface

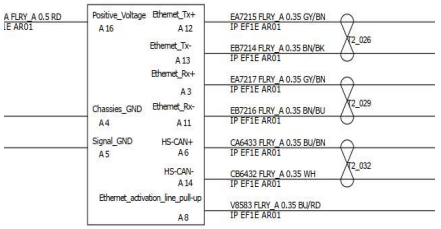




OBD/M	对应接线	DB9/F
11	----------	1
14	----------	2
5	----------	3
8	----------	4
1	----------	5
空	----------	6
6	----------	7
3	----------	8
16	----------	9

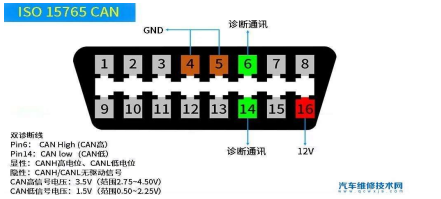
接线定义一

线总长度：1米



17/13

DIAGNOSTIC SOCKET OBD II



ICAP Classification:		CP: ___	IUO: X	PUBI: ___	
Drawing Title:	DEVKIT-MPC5748G				
Page Title:	CAN and LIN				
Size B	Document Number	SCH-29030	PDF: SPF-29030		Rev D1
Date:	Friday, July 28, 2023	Sheet	9	of	15

USB (Type A Host and Type AB OTG)

General Layout Note. Recommendation is to keep all tracks between MCU and USB PHI less than 3"

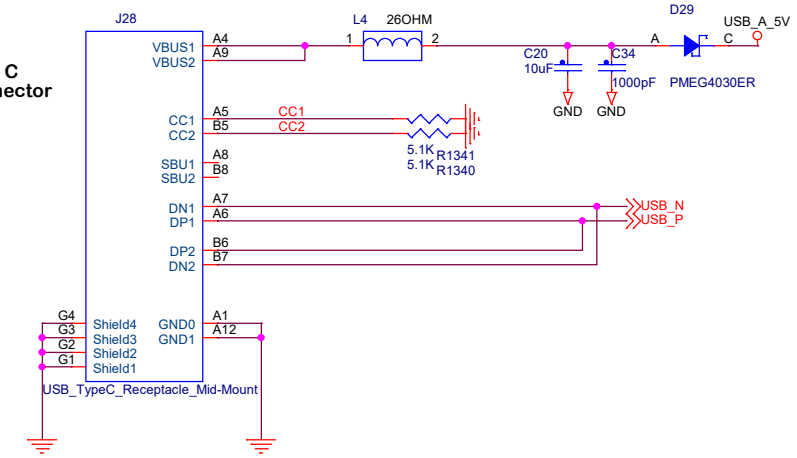
USB Signals are in power domain VDD_HV_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups or series resistors to be removed

(Layout Note: Place Series Termination resistor (30 Ohm) close to USB IC)

211-78945 -
CON 5 USB_MICRO_AB_RECEPTACLE RA SKT SMT 0.65MM SP 122H AU
Changed to
211-75297-USB_TYPE_A
CON 4 SKT RA SMT -- AU USB A

Type C Connector



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **DEVKIT-MPC5748G**

Page Title: **USB Type A / Type AB**

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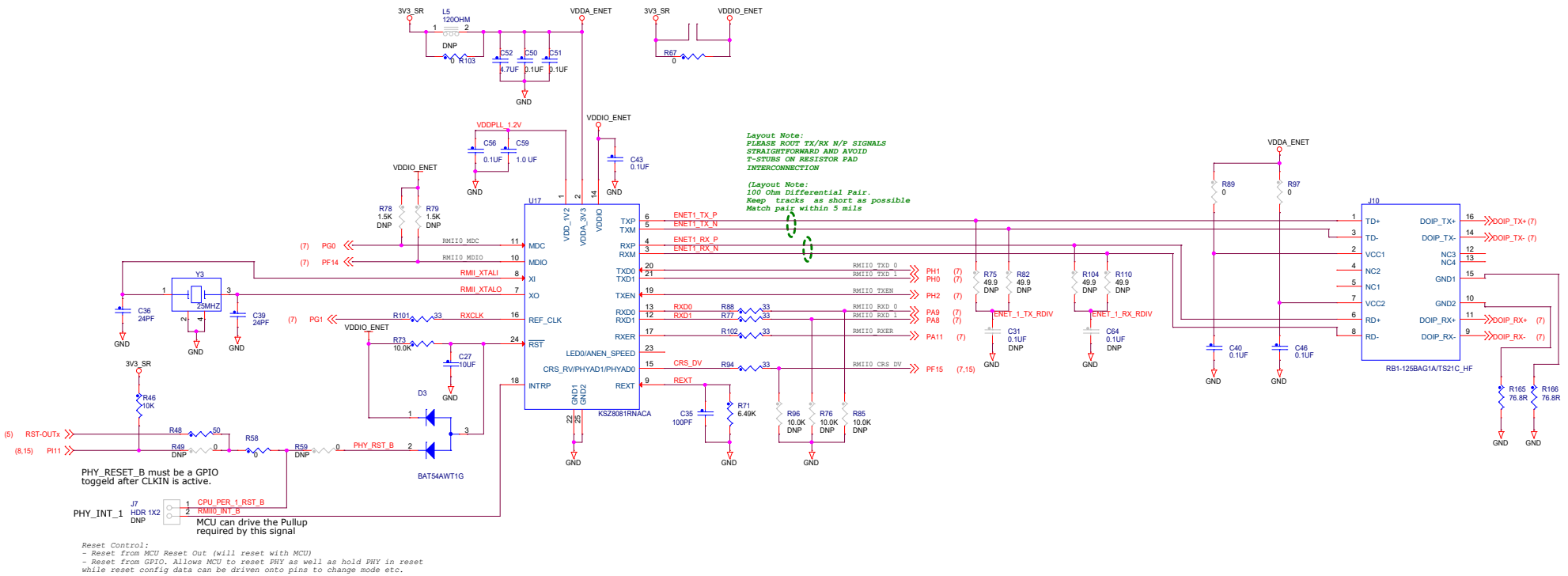
Ethernet Physical Interface & DOIP



ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title:	DEVKIT-MPC5748G		
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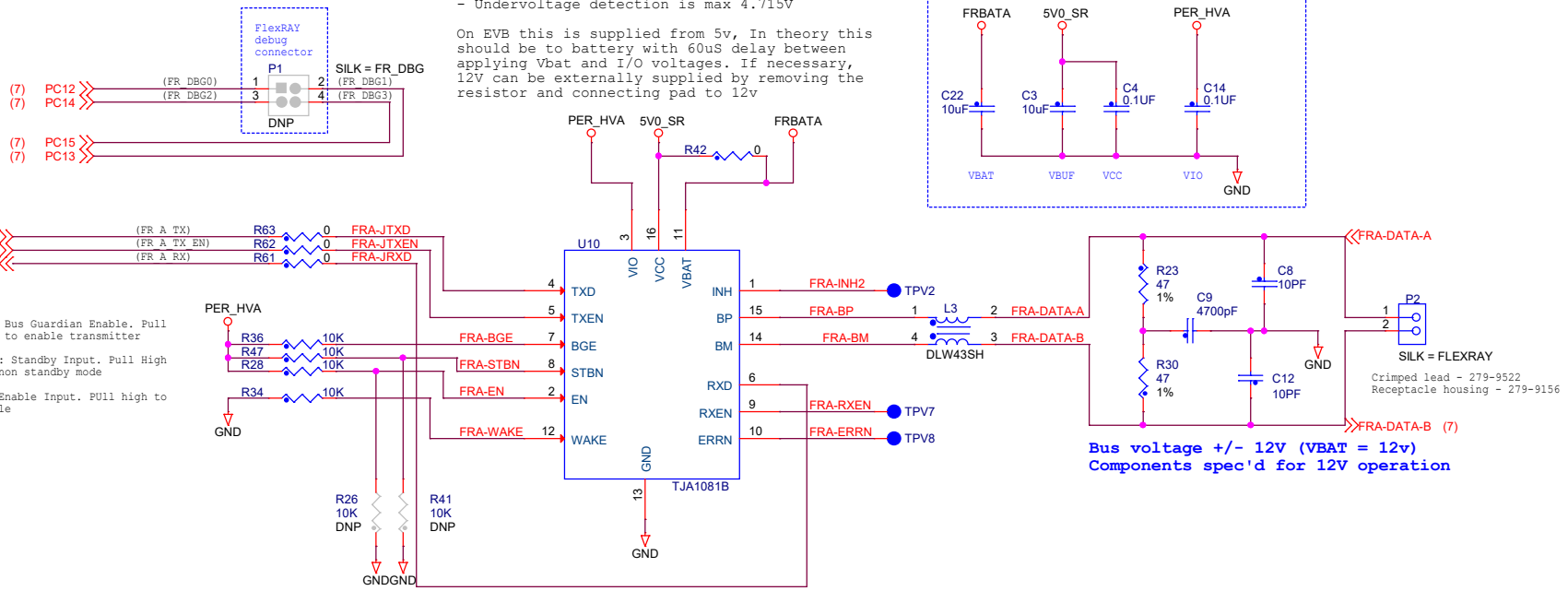
FlexRAY Physical Interface

All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)



MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

BGE: Bus Guardian Enable. Pull high to enable transmitter

STBN: Standby Input. Pull High for non standby mode

EN: Enable Input. PUll high to enable

ICAP Classification: CP: ___ IUO: X PUBI: ___

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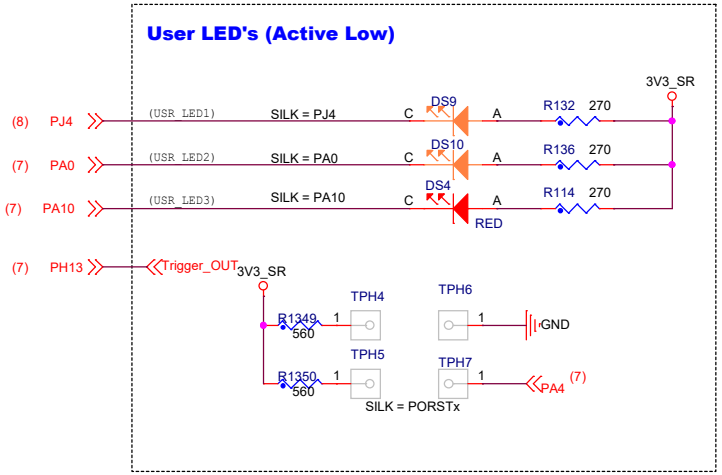
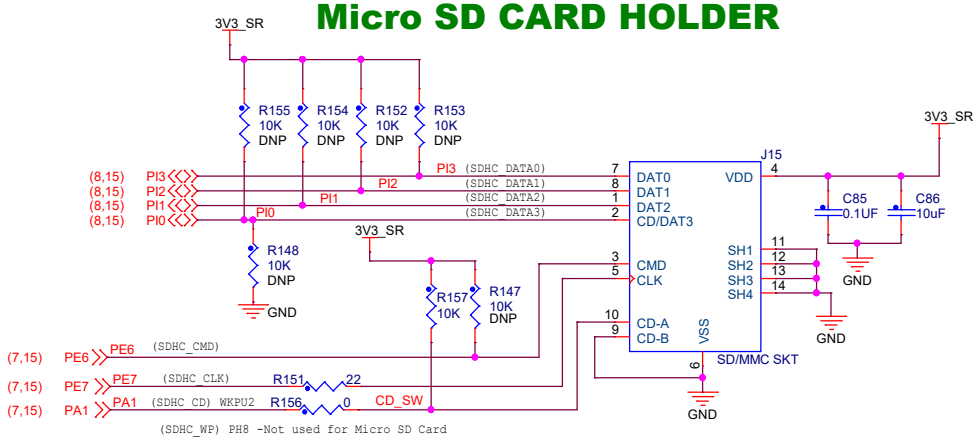
User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage





ICAP Classification:	CP: ___	IUO: X	PUBI: ___
Drawing Title: DEVKIT-MPC5748G			
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