

2.3ghz i5 4200u (dual core, hyperthreading)
4ghz DDR3L (soldered)
Sandisk U100 16GB SSD
HP NC365T quad port GBE NIC
1x USB3.0, 1x USB2.0, 1x Micro-HDMI

Mobo: From Lenovo Yoga 2 13"

- Remove power button protrusion from motherboard (scissors! X) and solder a jumper for power switch
- Solder jumper for Power LED from unpopulated HDD connector 5v
- Solder USB header to USB lines normally going to SD card/USB/audio daughterboard
 - Two more USB ports available: card reader USB lines, and another port on M.2 (LAN)
 - Not populated because should never need them, and may run power budget over
 - Removed the inductor from the USB lines to solder to the pads.
 - Power pulled from daughterboard USB power (hoping it may have USB overpower protection)
- NIC
 - HP NC365T (intel I340 T4)
 - Intel 82580 controller
 - Claims to operate at PCI-E 2.0, 1x, unlike the PRO/1000 adapters
 - Both HP data sheet and 82580 datasheet say it ought to
 - ~5 watts (quad port)
 - Confirmed: will operate at PCI-E 2.0, 1x, without issues!
 - May throttle due to bandwidth if all 4 ports were slinging max rates
 - PCI-E 2.0: ~500MiB/s per lane
 - 1GBE: ~110MiB/s per port
 - Created replacement bracket model & printed
 - Card has 3 supports: Two on top of ports, one screw. Fine in normal casing, maybe not in mine, so printed an additional support and welded to it bracket.
- Fans
 - 13.5k RPM 40x28 delta server fans
 - These babies sing!
 - Claim .6A peak, actually .45A (@12v)
 - Best I can tell, these fans run their drivers directly off the PWM signal, so 7 mA drive strength is required (@5v).
 - Also, the tach signal is a hot mess (seems to have PWM mixed in??)
 - Minimum PWM voltage is 4.2v, any lower and they won't run.
 - Attiny85 fan driver
 - 5v, gnd, pwm from fan header
 - Level conversion (3.3v in, 5v out) as fans need 5v (or more) logic with a decent amount of drive strength
 - 32khz PWM, as 8khz is horribly noisy with these fans
 - Mobo would also turn off fans, this prevents that.
 - Spin up fans, then...
 - PWM out = constrain(PWM in + 20, 40, 100)
- Modify bios to remove Wifi module whitelisting
 - Dump bios with test clip and ch341a programmer
 - Use UEFIttool to find the error message, and extract just that module
 - Load module in IDA64, find error message, backtrack to find unique call to that function
 - hex edit to module file, nop'ing out the call to that function
 - Reassemble bios via uefity and flash
 - Tested with a wifi module I knew wouldn't work previously- works!

- Unlocked the BIOS secret menus while I was at it. Nothing terribly applicable, but neat all the same. This one [I had to look up](#), rather than derive it myself.
- Pentium heatsink
 - Bent paperclips to hold it down! Woo!
 - 50 deg C peak load temp (non-AVX)
- Fabricate a sata cable from spare parts
 - The unit came with a slim hdd with a proprietary connector, originally, and I didn't even have that cable to work with, so had to reverse engineer it.
 - Turns out SATA is super sensitive to noise, would not work reliably until sata pairs were twisted.
 - Seems I might have been able to buy one...? Oh well!
- Sony Laptop 45W PSU used instead of original due to size constraints
 - Absolute worst case loading on every single part would put it right at 45W or a little over
 - However, these PSUs are good for 50W (at least; short duration), and will be actively cooled
 - Practical load power is <15W
 - Delta, 2.3A, 19.5V, green power LED
 - ABS casing! YAY!
 - Welded mounting tabs to side and rear
- Casing
 - Printed in 2 parts, due to build area size
 - Printed rear/front faces against bed: bottom down had severe cracking.
 - There was some cracking printing upright, but I was able to repair it with ABS goop.
 - [Heatserts used for all threaded parts](#)
 - These standoffs are stupid strong. How HP manages to screw these up is beyond me.
 - Oh, wait, no it isn't: HP is stupid cheap, and uses the bare minimum amount of plastic
 - No wonder they break off so often.
 - 38 screws used, total
 - Some parts printed separately and welded on due to interior layout being somewhat in flux, and/or would be difficult to print adequately in that orientation
 - Cable management hooks
 - M.2 standoff
 - SSD standoffs
 - Ethernet support
 - DC-DC module mount
- [12V DC-DC](#)
 - Nifty! 12\$ for 6.
 - You probably aren't getting 3A out of one of these without heatsinking/airflow. But, for my worst-case 1.5A or so, they are enough.
 - Adequate efficiency: 86% going 19v to 12v.
 - Super bright blue power LED: sigh.
 - I really should have got some small power connectors for the 12v bus, so it could be disassembled.
- M.2 to PCI-E
 - What a mess!
 - [A pre-made adapter is \\$150](#) (marked up horribly at bplus), as it was a low demand item and the various chinese places that made them no longer make them. Also, terrible form factor for what I'm doing.
 - A M.2 breakout board is \$80 - thanks but no thanks.
 - Could get my own made at oshpark (0.8mm PCB!), but 2-3 week turnaround time, plus it would need to be designed.
 - Soldering directly - yeah no
 - [BCM94360CS2/BCM943224 12+6 Pin Wireless Card To NGFF Key A/E Adapter For Mac OS](#)
 - Used for adapting mac wifi modules to M.2, for hackintoshes.

- The mac header is 18 pins and has every single pin I need, at a much more friendly spacing for hand soldering
- Pull the mac connector off and cut it to length, then solder a hand-made PCIE riser to it.
 - Port off a dead mobo, with end dremeled off to allow larger cards
 - IDE 32 gauge ribbon wire
- Relay off 3.3v to switch 12v on/off. Probably not required, but just in case...
- \$19, all told
- Except shipping has been terrible: still waiting as of 3/31 (ordered 3/8).
- Should have made my own PCB....
- Received adapter...finally.... on 4/5/17. Assembled, it works!
- SSD
 - Sandisk Extreme
 - Actually a sandisk pSSD/u100 behind a sata to usb bridge
 - Was going to adapt to sata, however, was not able to get a stable link at SATA III speeds. May have been caused by removing decoupling capacitors.
 - Interestingly, have to poke a USB data line for the sata bridge to bring the SSD portion online. Must be an enable pin somewhere.
 - HP 689057-001 / Apacer 16GB MLC module
 - Used in thin clients.
 - More a flash drive than an SSD: no trim, barely any SMART, etc.
 - Pretty terrible: 75mb/s seq read, 20mb/s seq write.
 - 4k random read IOPS: ~4k (only redeeming factor), 263 4k random write.
 - Nice and small, however, and suitable for this task
 - Unfortunately, does not seem to handle reboots at all: module would stop responding on reboot or shortly thereafter and not work until entire machine powered off.
 - Sandisk U100 16GB
 - SSD removed from casing - originally a sandisk u100 2.5", but they use the server format half-sata drive in a plastic box.
 - 10TBW endurance

http://www.ridetheclown.com/downloads/20170331_114513.jpg
http://www.ridetheclown.com/downloads/20170331_120345.jpg
http://www.ridetheclown.com/downloads/20170405_180856.jpg
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http://www.ridetheclown.com/downloads/20170405_180900.jpg
http://www.ridetheclown.com/downloads/20170405_181742.jpg

Enclosure Stuff:

4 parts, two top, two bottom

3d print separate fan grills and mount the fans internally to the case front

Fans min 4mm above board level

Board thickness: 1mm

Case bottom standoffs: 3.5mm

.5mm from sides of case to mobo

Print with supports everywhere

Network card support from side of case

Fans:PWM info

500ohms at 12v to reliably power on

~5v logic high

4.2 absolute min high

15ma @ ~5v

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PCI-E Stuff

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset
Key notch			
12	CLKREQ#	Ground	Request running clock
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK-	
15	HSOn(0)	Ground	Lane 0 transmit data, + and -
16	Ground	HSIp(0)	Lane 0 receive data, + and -
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	

Apple PIN#	Function
P1	3.3V (Wi-Fi)
P2	LED_WLAN#
P3	GND
P4	PETp0
P5	PETn0
P6	GND
P7	REFCLK+
P8	REFCLK-
P9	GND
P10	PERp0
P11	PERn0
P12	GND
Mechanical Key	
P13	WAKE#
P14	PERST#
P15	CLKREQ#
P16	USB_D-
P17	USB_D+
P18	3.3V (Bluetooth)

© Skvo

2+6PIN



Side B			Side A		
1	+12v		1	N/C	
2	+12v		2	+12v	
3	+12v		3	+12v	
4	GND		4	GND	
5	N/C		5	N/C	
6	N/C		6	N/C	
7	GND		7	N/C	
8	+3.3v		8	N/C	
9	N/C		9	+3.3v	
10	+3.3v		10	+3.3v	
11	WAKE#		11	PERST#	
KEY			KEY		
12	CLKREQ#		12	GND	
13	GND		13	REFCLK+	
14	PETp0	TX	14	REFCLK-	
15	PETn0	TX	15	GND	
16	GND		16	PER0	RX
17	N/C		17	PERn0	RX
18	GND		18	GND	

(Figure M2-A, the key in the pin8-pin15. With PCIe x2, NFC, Display Port and USB 2.0 channel)

		GND	75
74	3.3Vaux	REFCLKN1	73
72	3.3Vaux	REFCLKP1	71
70	PEWake1# (IO)(0/3.3V)	GND	69
68	CLKREQ1# (IO)(0/3.3V)	PERn1	67
66	PERST1# (O)(0/3.3V)	PERp1	65
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	GND	63
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	PETn1	61
60	NFC I2C SM CLK (O)(0/3.3)	PETp1	59
58	NFC I2C SM DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(0/3.3V)	REFCLKN0	49
48	COEX1(?)(0/1.8V)	REFCLKP0	47
46	COEX2(?)(0/1.8V)	GND	45
44	COEX3(?)(0/1.8V)	PERn0	43
42	CLink CLK	PERp0	41
40	CLink DATA	GND	39
38	CLink RESET (O)(0/3.3V)	PETn0	37
36	GND	PETp0	35
34	DP_ML0p	GND	33
32	DP_ML0n	DP_HPD (O)(0/3.3V)	31
30	GND	GND	29
28	DP_ML1p	DP_ML2p	27
26	DP_ML1n	DP_ML2n	25
24	GND	GND	23
22	DP_AUXp	DP_ML3p	21
20	DP_AUXn	DP_ML3n	19
18	GND	GND	17
16	LED#2 (I)(OD)	Key	
	Key	Key	
	Key	Key	
	Key	Key	
		GND	7
6	LED#1 (I)(OD)	USB_D-	5
4	3.3Vaux	USB_D+	3
2	3.3Vaux	GND	1

#911165

(Figure M2-B, the key in the pin12-pin19. With SIM card, audio, PCIe 2.0, SATA and USB 3.0 channel multiplexing channel, etc.)

		USB3.0 IND (OC-USB3.0/GND-Other)	75
74	3.3Vaux	GND	73
72	3.3Vaux	GND	71
70	3.3Vaux	PEDET (OC-PCIe/GND-SATA)	69
68	SUSCLK(32kHz) (O)(0/3.3V)	Reset# (O)(0/1.8V)	67
66	SIM Detect (O)	ANTCTL3 (I)(0/1.8V)	65
64	COEX1 (?) (0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
62	COEX2 (?) (0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
60	COEX3 (?) (0/1.8V)	ANTCTL0 (I)(0/1.8V)	59
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWake# (IO)(0/3.3V)	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V)	GND	51
50	PERST# (O)(0/3.3V)	PERp0/SATA-A+	49
48	GNSS4(0/1.8V)	PERn0/SATA-A-	47
46	GNSS3(0/1.8V)	GND	45
44	GNSS2(0/1.8V)	PETp0/SATA-B-	43
42	GNSS1(0/1.8V)	PETn0/SATA-B+	41
40	GNSS0(0/1.8V)	GND	39
38	DEVSLP (O)(0/3.3V)	PERp1/USB3.0-Rx+/SSIC-RxP	37
36	UIM-PWR (I)	PERn1/USB3.0-Rx-/SSIC-RxN	35
34	UIM-DATA (IO)	GND	33
32	UIM-CLK (I)	PETp1/USB3.0-Tx+/SSIC-TxP	31
30	UIM-RESET (I)	PETn1/USB3.0-Tx-/SSIC-TxN	29
28	UIM-RFU (I/O)	GND	27
26	Audio3(0/1.8V)	Reserved (Future Expansion)	25
24	Audio2(0/1.8V)	Reserved (Future Expansion)	23
22	Audio1(0/1.8V)	WWAN/SSD IND (GND-WWAN/OC-SSD)	21
20	Audio0(0/1.8V)	Key	
	Key	Key	
	Key	Key	
	Key	Key	
		GND	11
10	LED#1/DAS/DSS# (I)(OD)	USB_D-	9
8	W_DISABLE#1 (O)(0/3.3V)	USB_D+	7
6	Full_Card_Power_Off# (O)(0/1.8V)	GND	5
4	3.3Vaux	GND	3
2	3.3Vaux	Presence IND (GND)	#911165

(Figure M2-E, the key in the pin24-pin31. With PCIe x2, NFC, SDIO, PCM, USB 2.0 channel, etc.)

		GND	75
74	3.3Vaux	RESERVED	73
72	3.3Vaux	RESERVED	71
70	RESERVED	GND	69
68	RESERVED	Reserved/2nd Lane PERn1	67
66	RESERVED	Reserved/2nd Lane PERp1	65
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	GND	63
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	Reserved/2nd Lane PETn1	61
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETp1	59
58	NFC I2C SM DATA (IO)(0/3.3)	GND	57
56	W_DISABLE#1 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(0/3.3V)	REFCLKNO	49
48	COEX1 (?) (0/1.8V)	REFCLKPO	47
46	COEX2 (?) (0/1.8V)	GND	45
44	COEX3 (?) (0/1.8V)	PERn0	43
42	CLink CLK	PERp0	41
40	CLink DATA	GND	39
38	CLink RESET (O)(0/3.3V)	PETn0	37
36	UART CTS (O)(0/1.8V)	PETp0	35
34	UART RTS (I)(0/1.8V)	GND	33
32	UART Tx (O)(0/1.8V)	Key	
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(0/1.8V)	SDIO Reset(O)(0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake(I)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (OI)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (OI)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	#911165

(Figure M2-M, the key in the pin59-pin66. With PCIe x4 and SATA multiplex channel)

		GND	75
74	3.3Vaux	GND	73
72	3.3Vaux	GND	71
70	3.3Vaux	PEDET (OC-PCIe/GND-SATA)	69
68	SUSCLK(32kHz) (O)(0/3.3V)	N/C	67
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWake# (IO)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PERp0/SATA-A+	49
48	N/C	PERn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PETp0/SATA-B-	43
42	N/C	PETn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)(0/3.3V)	PERp1	37
36	N/C	PERn1	35
34	N/C	GND	33
32	N/C	PETp1	31
30	N/C	PETn1	29
28	N/C	GND	27
26	N/C	PERp2	25
24	N/C	PERn2	23
22	N/C	GND	21
20	N/C	PETn2	19
18	3.3Vaux	PETp2	17
16	3.3Vaux	GND	15
14	3.3Vaux	PERp3	13
12	3.3Vaux	PERn3	11
10	DAS/DSS# (I)(OD)	GND	9
8	N/C	PETn3	7
6	N/C	PETp3	5
4	3.3Vaux	GND	3
2	3.3Vaux	GND	#911465