Design an 8 to 1 MUX using case statement in Verilog HDL

by

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Problem Statement

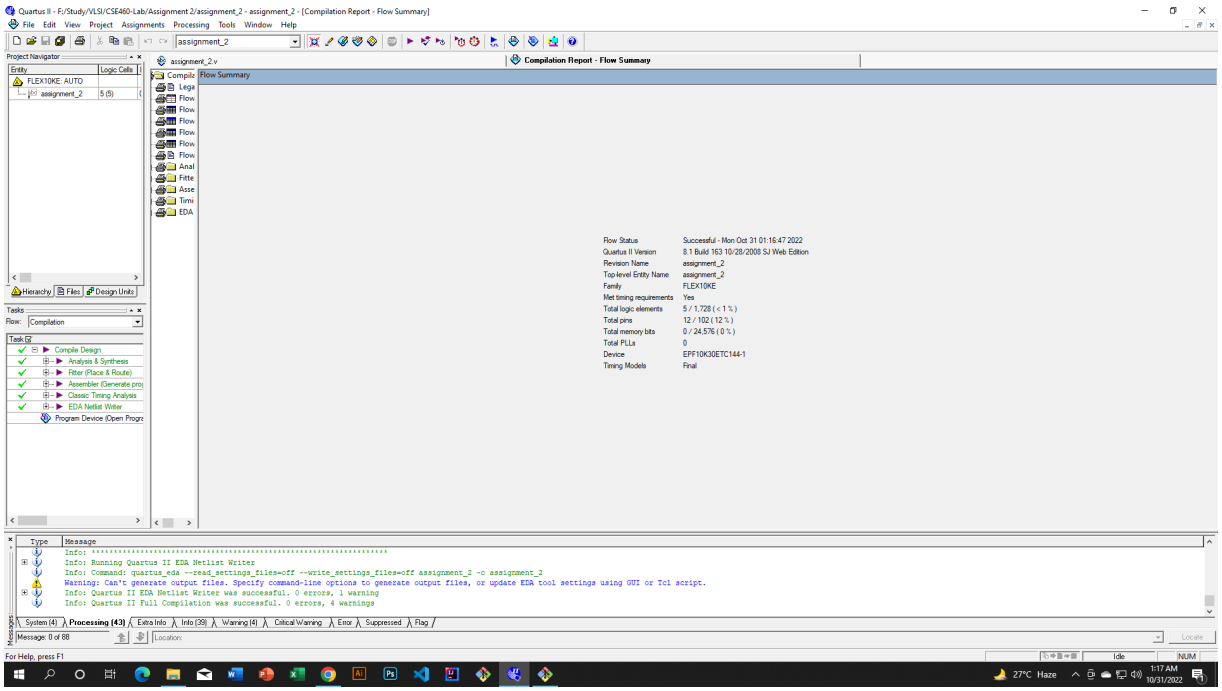
Design an 8 to 1 MUX using case statement in Verilog HDL

Code

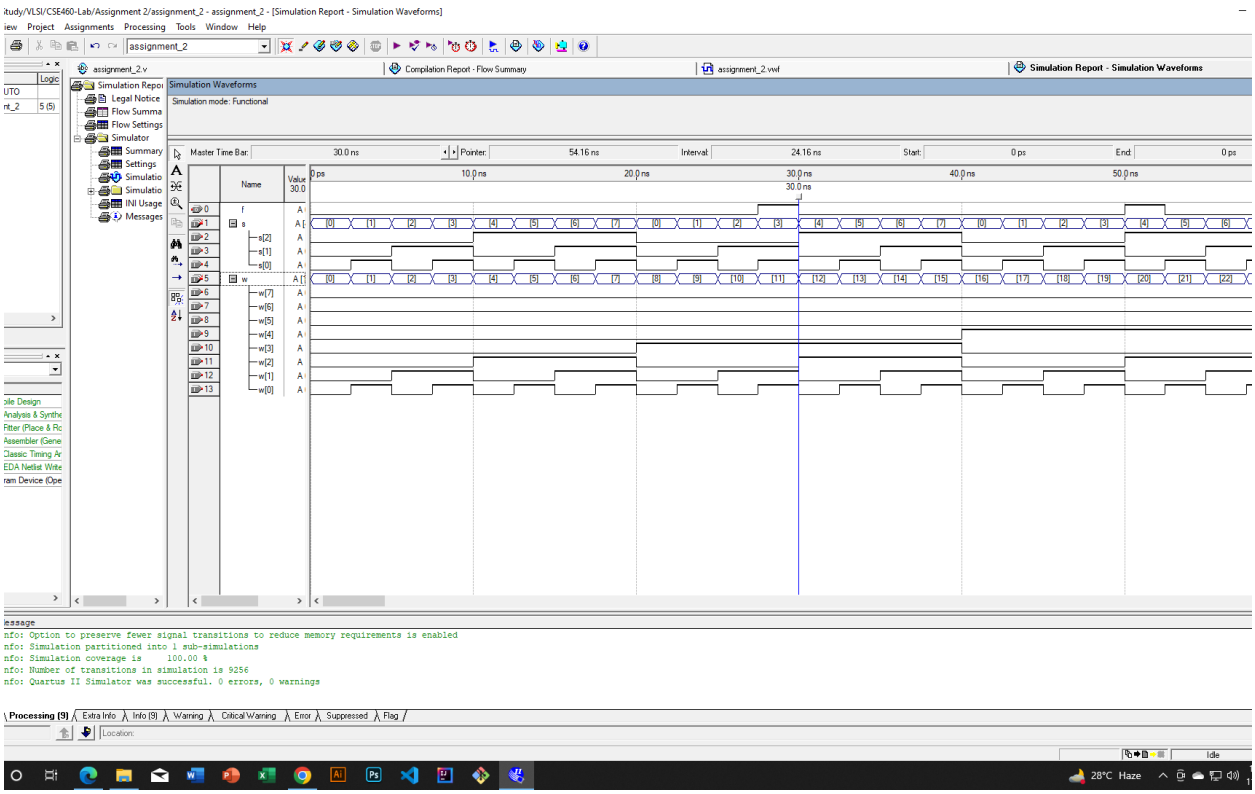
```
module assignment_2(w,s,f);
	input [7:0]w;
	input [2:0]s;
	output reg f;

	always @(w,s)
	begin
		case(s)
			3'b000: f=w[0];
			3'b001: f=w[1];
			3'b010: f=w[2];
			3'b011: f=w[3];
			3'b100: f=w[4];
			3'b101: f=w[5];
			3'b110: f=w[6];
			3'b111: f=w[7];
			default: f=1'b0;
		endcase
	end
endmodule
```

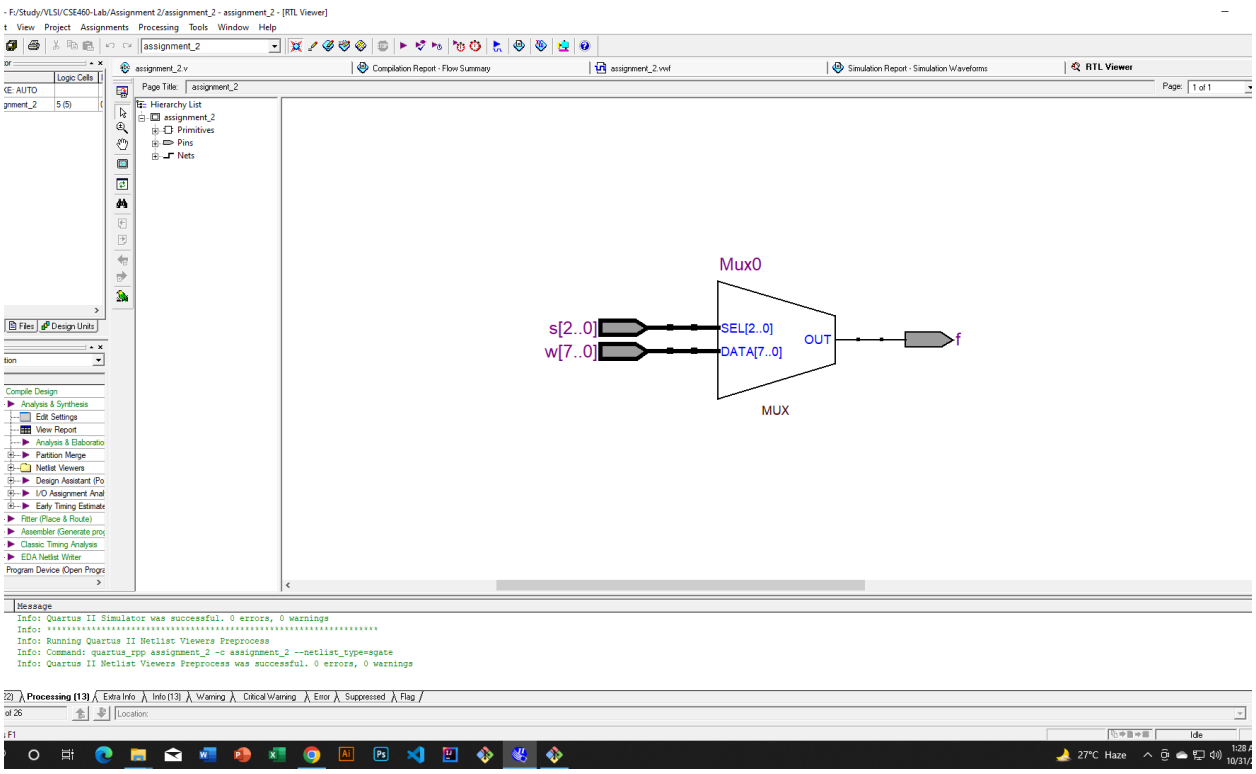
Compilation Report



Simulation Report



RTL View



Discussion about the input output from the timing diagram

Here we have 8 input and our system is 8 to 1 MUX. To select the input combination we have 3 pin selection inputs pin which are denoted by s and the main 8 inputs are denoted by w. At the time of 30 ns we get our output high and our chip selection pin is at 0 1 0 . So that means the outpin pin got high at this chip selection combination. There are few other combinations for get the output high.