A sequential circuit has two inputs, w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If w1 = w2 during any four consecutive clock cycles, the circuit produces z = 1; otherwise, z = 0

by

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Problem Statement

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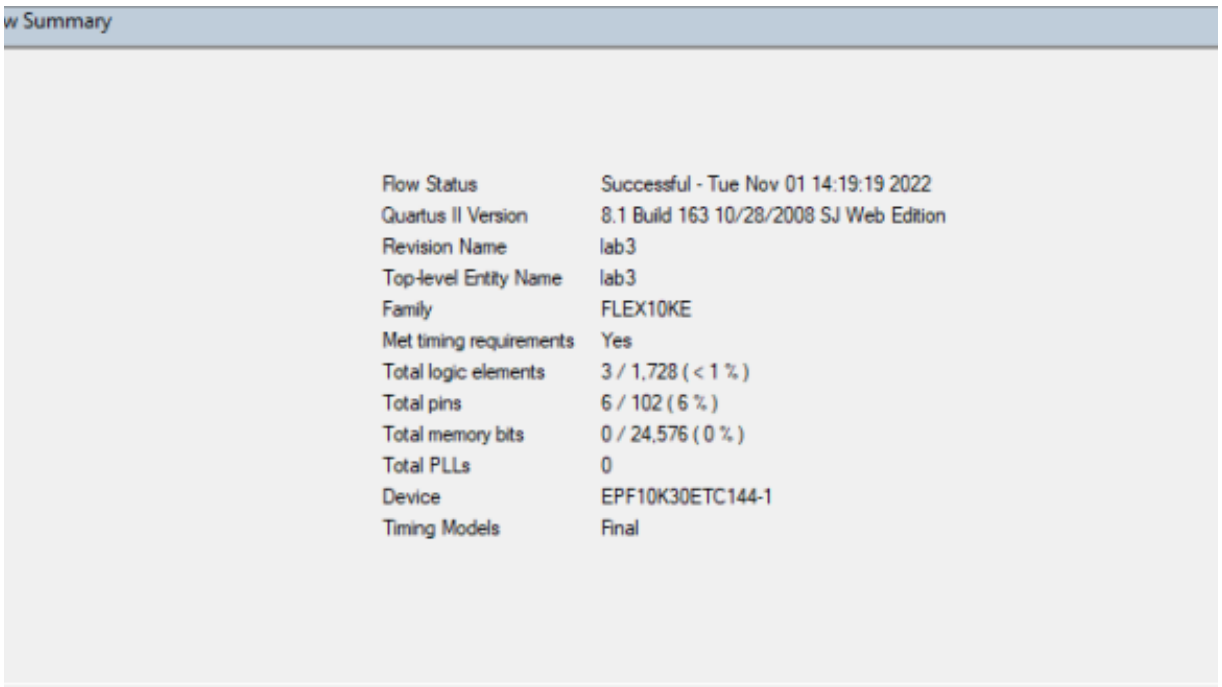
Code

```
module assignment_3(clk, reset, w, z, current_state, next_state);
	input clk, reset, w;
	output reg z, current_state, next_state;
	parameter A = 1'b0, B = 1'b1;
	always @(posedge clk, posedge reset)
	begin
		if(reset == 1)
		begin
			current_state = A;
			next_state = B;
			z = 0;
		end
		else
		begin
			current_state = next_state;
			case(current_state)
				A: if(w == 0)
				begin
					next_state = A;
					z = 0;
				end
				else
```

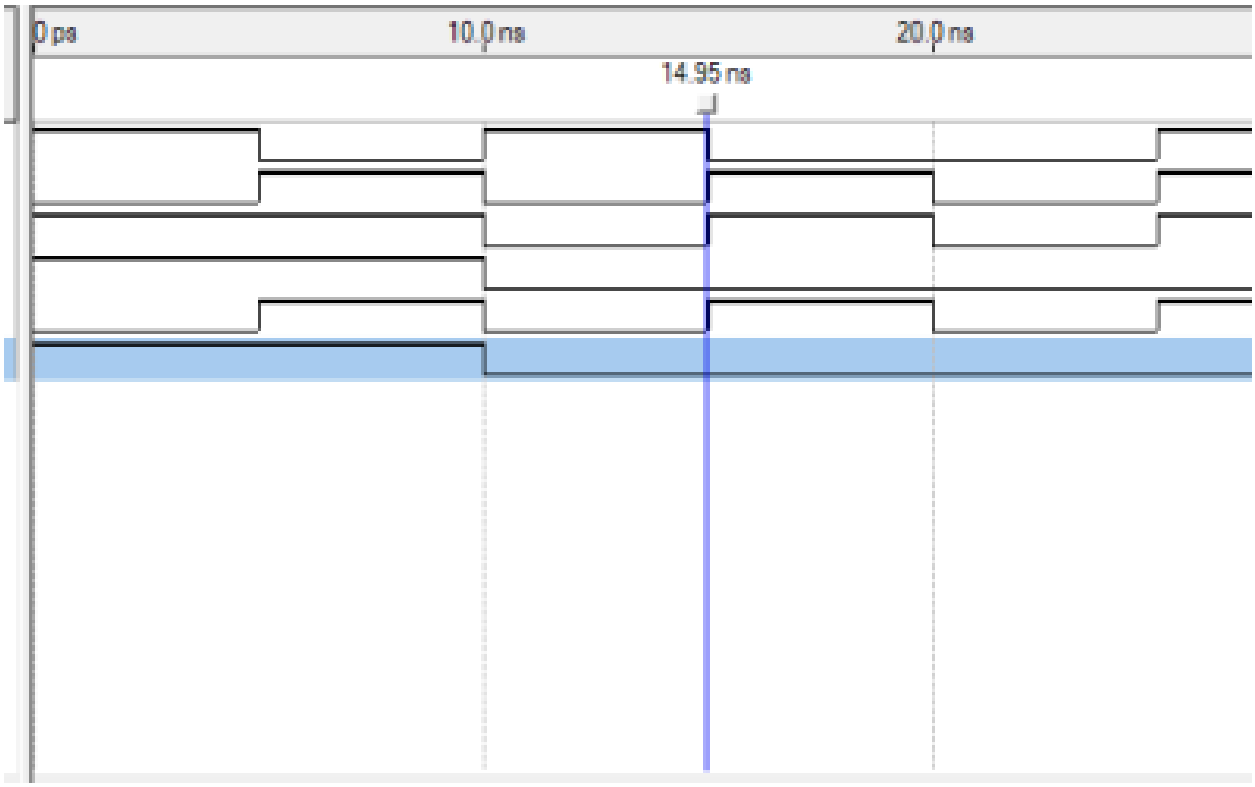
```
                    begin
                        next_state = B;
                        z = 0;
                    end

                    B: if(w == 0)
                    begin
                        next_state = A;
                        z = 0;
                    end
                    else
                    begin
                        next_state = B;
                        z = 1;
                    end
                endcase
            end
        end
endmodule
```

Compilation Report



Simulation Report



Discussion about the input output from the timing diagram

Here the machine is mealy type machine. It tells us when the two inputs are same in consecutive four clock cycle the output z will be high. As, it is a mealy type machine so input and transition state both will be needed. If we observe the timing diagram we can see that input w1 and input w2 are same for consecutive four clock cyle and that's why we get high in the output otherwise, when it doesn't match the output is low.