

A sequential circuit has two inputs, w_1 and w_2 , and an output, z . Its function is to compare the input sequences on the two inputs. If $w_1 = w_2$ during any four consecutive clock cycles, the circuit produces $z = 1$; otherwise, $z = 0$

by

**Ishraq Ahmed Esha
19301261**

**A Lab Report 3 submitted to the CSE460 VLSI Design
Course of Sec: 5**

**Brac University
November 1, 2022**

Problem Statement

A sequential circuit has two inputs, w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If $w1 = w2$ during any four consecutive clock cycles, the circuit produces $z = 1$; otherwise, $z = 0$

Code

```
module assignment_3(clk, reset, w, z, current_state, next_state);
    input clk, reset, w;
    output reg z, current_state, next_state;
    parameter A = 1'b0, B = 1'b1;
    always @(posedge clk, posedge reset)
    begin
        if(reset == 1)
        begin
            current_state = A;
            next_state = B;
            z = 0;
        end
        else
        begin
            current_state = next_state;
            case(current_state)
                A: if(w == 0)
                begin
                    next_state = A;
                    z = 0;
                end
                else
            end
        end
    end
end
```

```

begin
    next_state = B;
    z = 0;
end

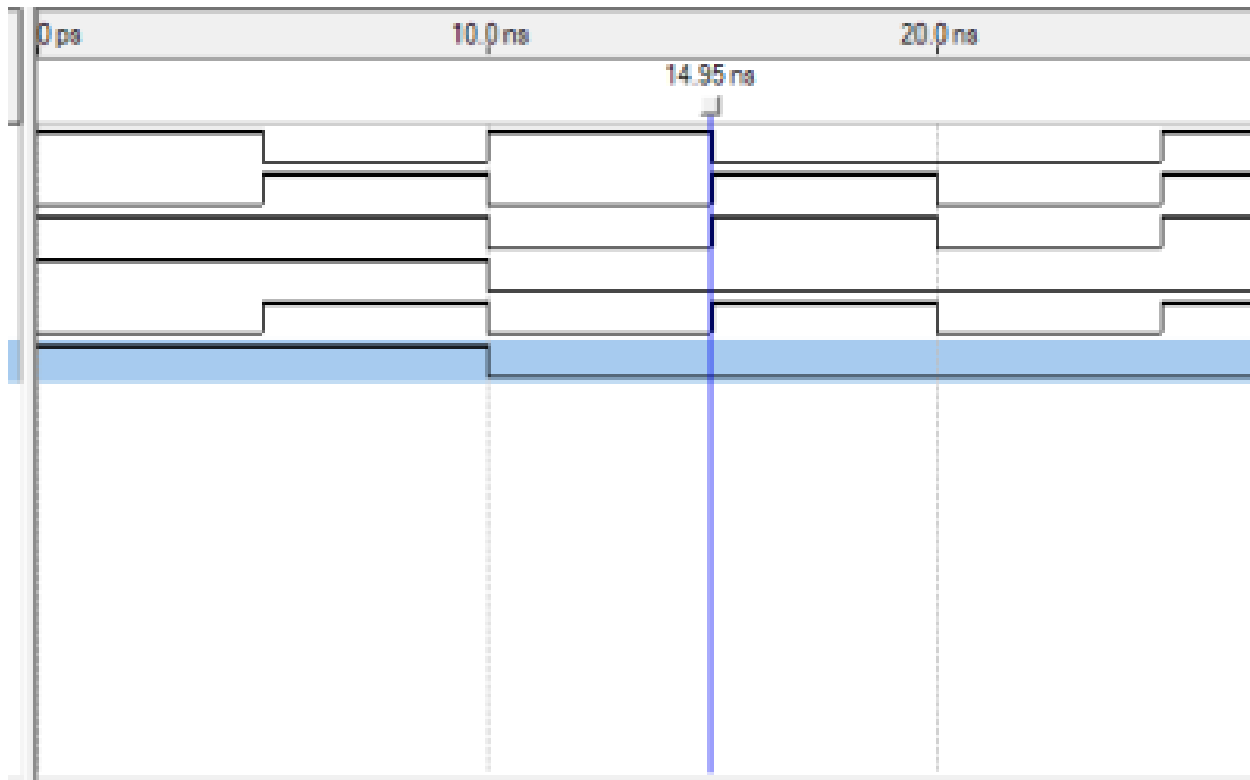
B: if(w == 0)
begin
    next_state = A;
    z = 0;
end
else
begin
    next_state = B;
    z = 1;
end
endcase
end
end
endmodule

```

Compilation Report

Summary	
Flow Status	Successful - Tue Nov 01 14:19:19 2022
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	lab3
Top-level Entity Name	lab3
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	3 / 1,728 (< 1 %)
Total pins	6 / 102 (6 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Simulation Report



Discussion about the input output from the timing diagram

Here the machine is mealy type machine. It tells us when the two inputs are same in consecutive four clock cycle the output z will be high. As, it is a mealy type machine so input and transition state both will be needed. If we observe the timing diagram we can see that input w1 and input w2 are same for consecutive four clock cycle and that's why we get high in the output otherwise, when it doesn't match the output is low.