# Draw the layout of AND3 and verify it with the timing diagram

**by**

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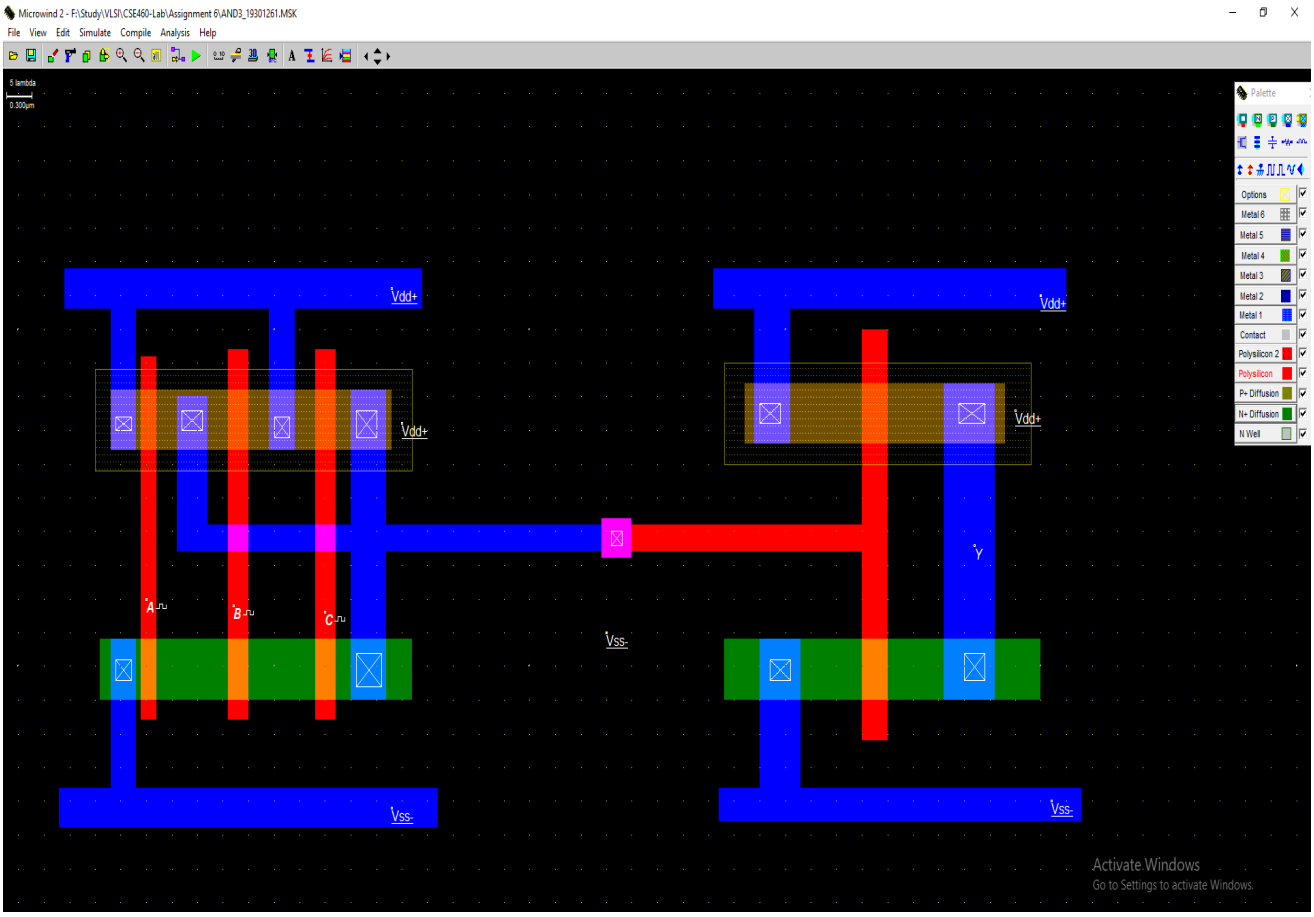
**A Lab Report 6 submitted to the CSE460 VLSI Design**
**Course of Sec: 5**

**Brac University**
**December 2, 2022**

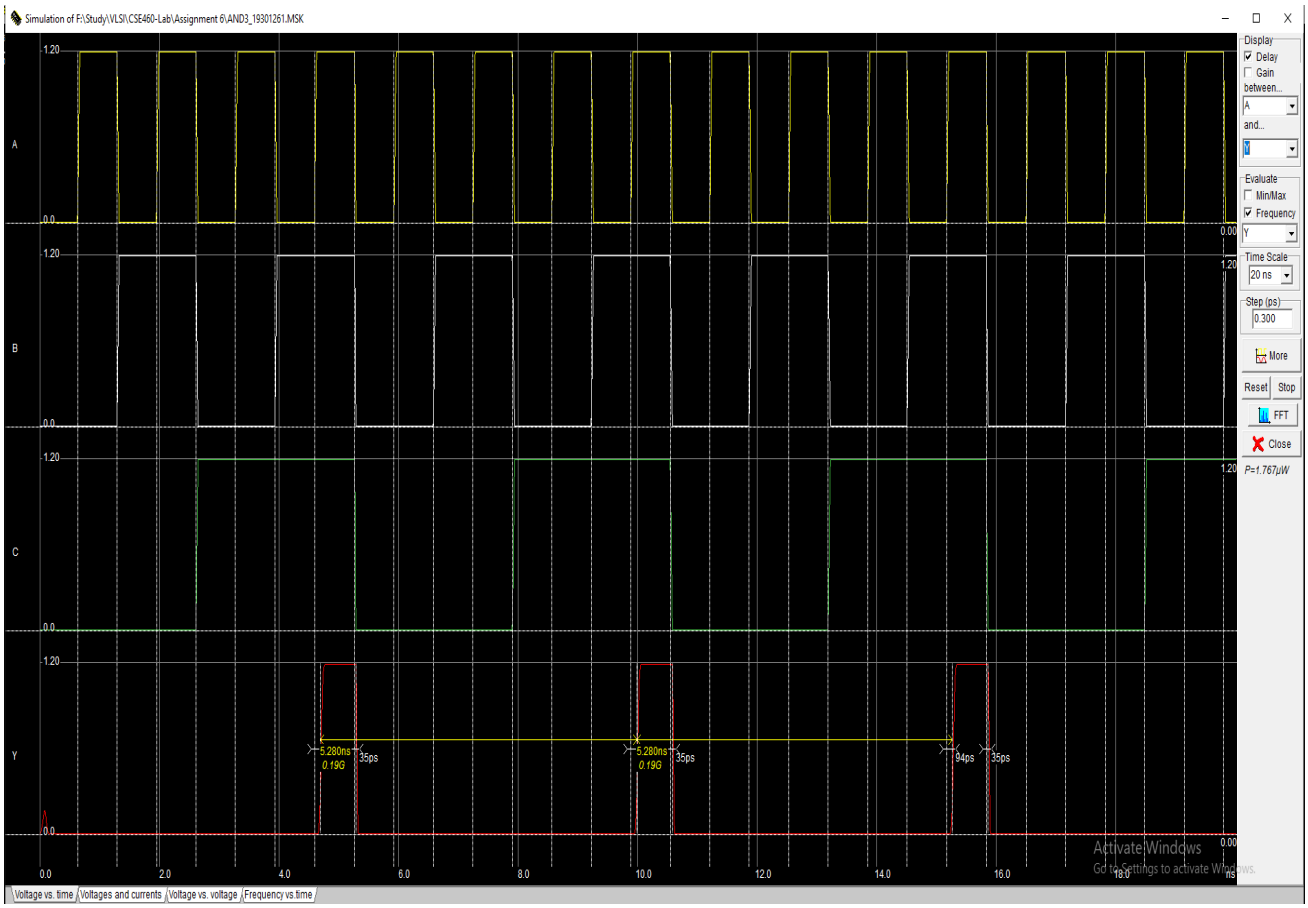
## Problem Statement

Draw the layout of AND3 and verify it with the timing diagram

## A) Layout Design File



## B) Timing Diagram




## Discussion

I have designed a layout of an AND3 circuit. First of all, I made the NAND3 circuit then connected it with the inverter and made the AND3 circuit. Now to verify the circuit timing diagram which I have generated via Microwind software will use the below truth table of the AND3 circuit.

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Now if we observe the timing diagram and the truth table of the AND3 circuit, consider the third combination from the truth table 010 as input of A,B,C respectively for this combination we should get the output value in off state means 0. From the timing diagram we can see that when the inputs are in 010 state respectively then the output Y is in 0 that means in off state. Now consider the last combination which is 111 as input of A,B,C respectively for this combination we should get the output value in on state means 1. From the timing diagram we can see that when all the inputs are in high or state means 111 at that time we get the output Y as 1 means in on state. The AND3 truth table shows us when all the inputs are high at that time the output Y will be high otherwise all the time it will remain low which is clearly visible in the timing diagram. So from the above discussion we can state that the layout design, timing diagram is verified with the AND3 circuit truth table.