A Circuit Design with the Dsch2 software

by

Ishraq Ahmed Esha
19301261

A Lab Report 5 submitted to the CSE460 VLSI Design
Course of Sec: 5

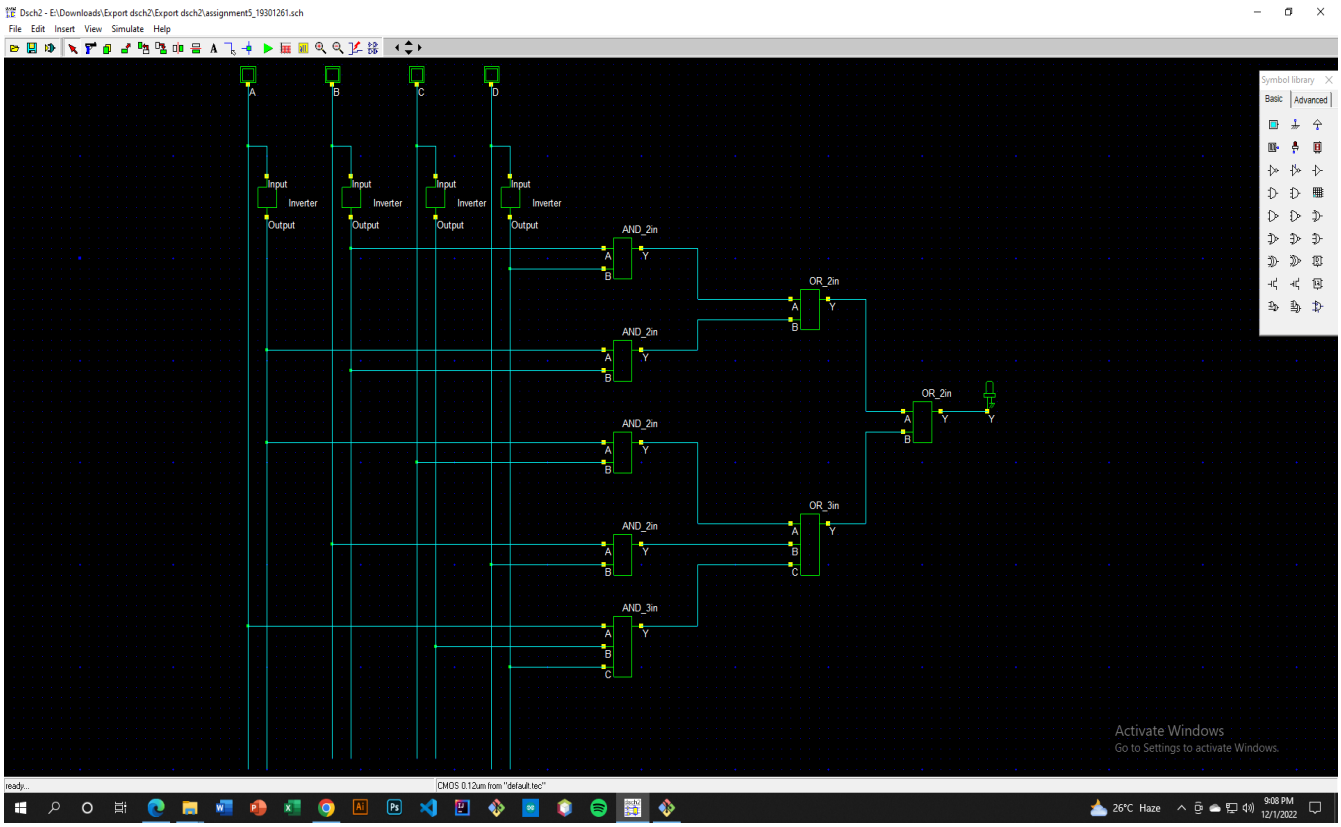
Brac University
December 1, 2022

Problem Statement

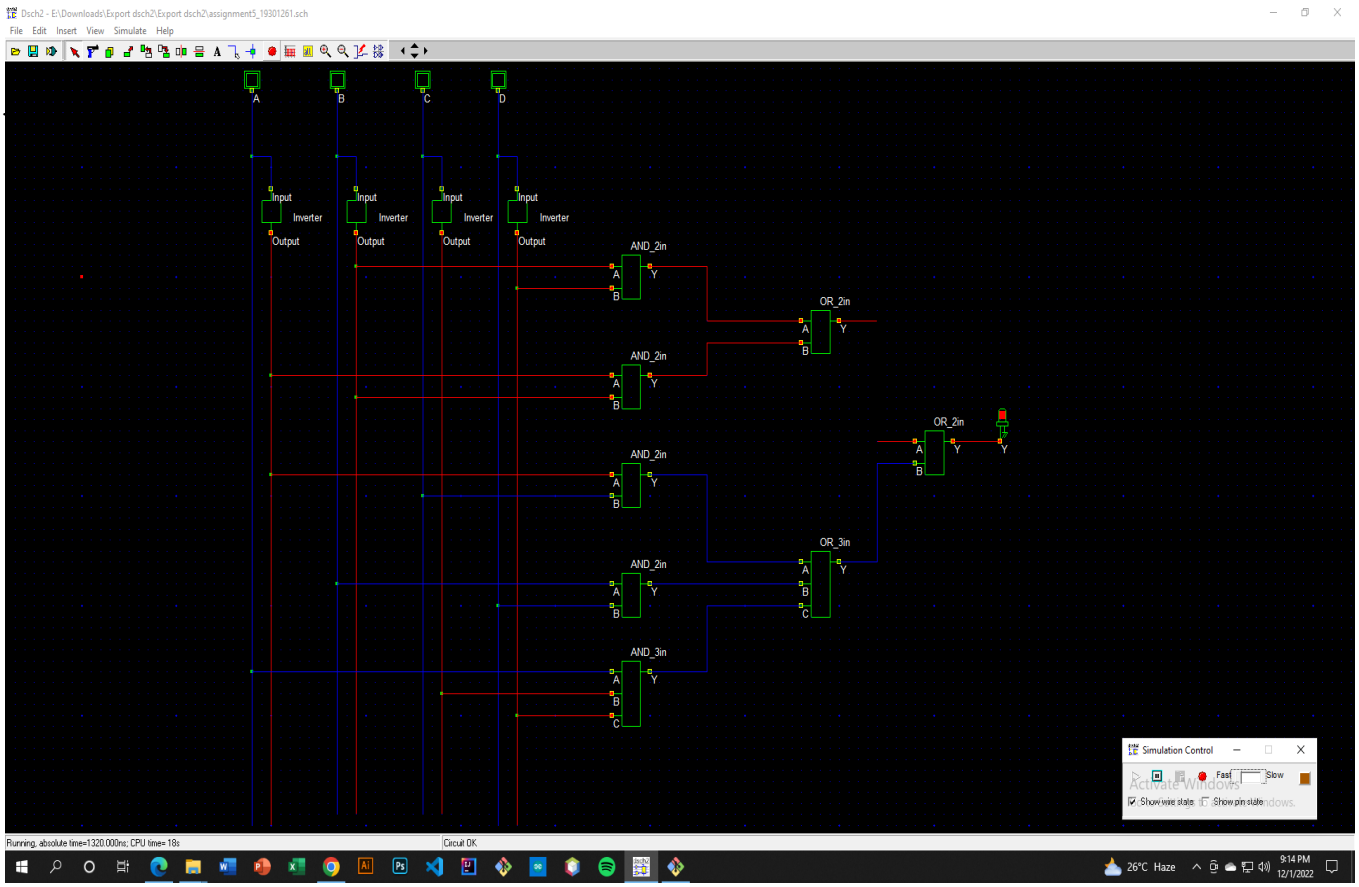
Derive the Boolean logic expression from the following K-Map and implement the logic function using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but cannot use readily available logic gates.

CD \ AB	00	01	11	10
00	1	0	1	1
01	1	d	d	0
11	d	d	1	0
10	1	1	0	1

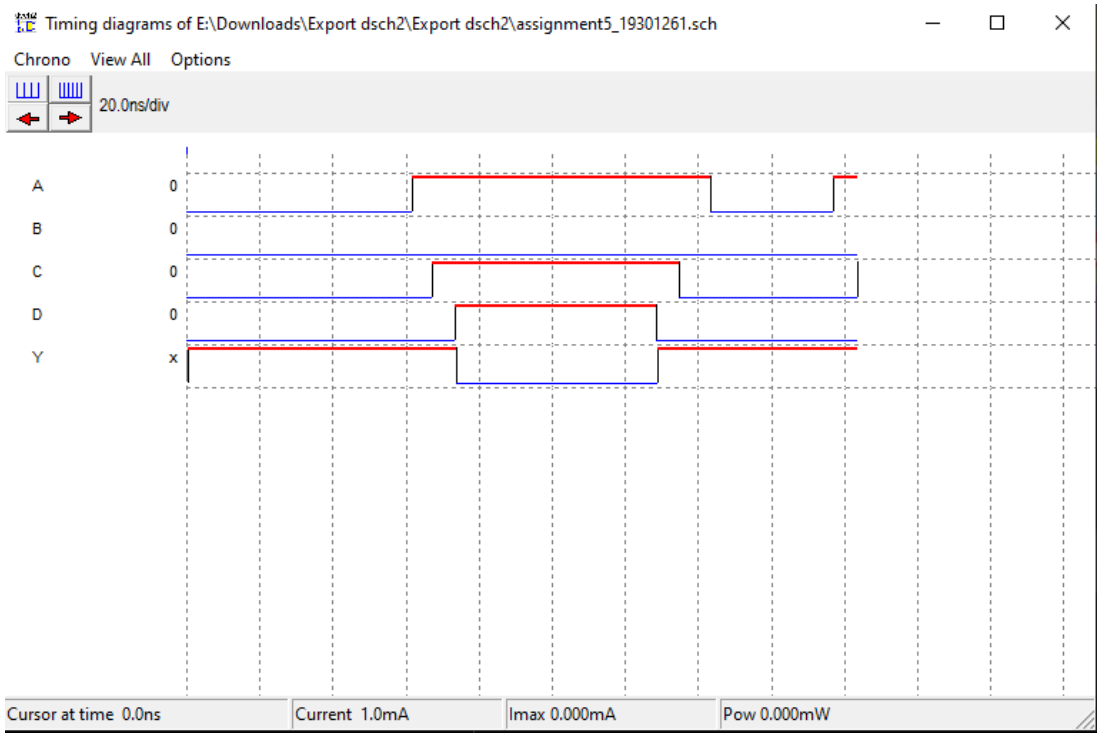
A) Design File



B) Simulation File



C) Timing Diagram



Discussion

From the K-map I have derive the boolean logic expression which is

$Y = \overline{A}\overline{B}C + \overline{B}\overline{D} + \overline{C}\overline{D} + A\overline{C} + BD$

Now to verify the circuit timing diagram in Dsch2 I have generate a truth table

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	X
1	1	0	1	X
1	1	1	0	0
1	1	1	1	1

In Dsch2 I have taken the button as input and made an inverter with cmos for each gate. Then make the blocks of AND gate and OR gate then connect the wire and after compiling when run the simulation with different combinations get the timing diagram. Lastly, I verify the circuit

design with the timing diagram and truth table. For explanation of the timing diagram with the truth table, consider the first combination as “0000”. All the input is in off state and the output is showing on state as 1. If we see the truth table for the first combination then we can see that the output will be 1 and our circuit is working. In addition, from the timing diagram we can observe that when all the input is 0 the output Y is 1. Secondly if we consider “1011” combination then we can see that the output is in off state and from the truth table we get the output 0 for the mentioned combination and if we look at the timing diagram when the A, B, C, D get 1,0,1,1 respectively then the output Y is showing as 0 means off state. So, we can see that the circuit output truth table and timing diagram all are working with the same logic that means we verified our circuit design with the Dsch2 software.