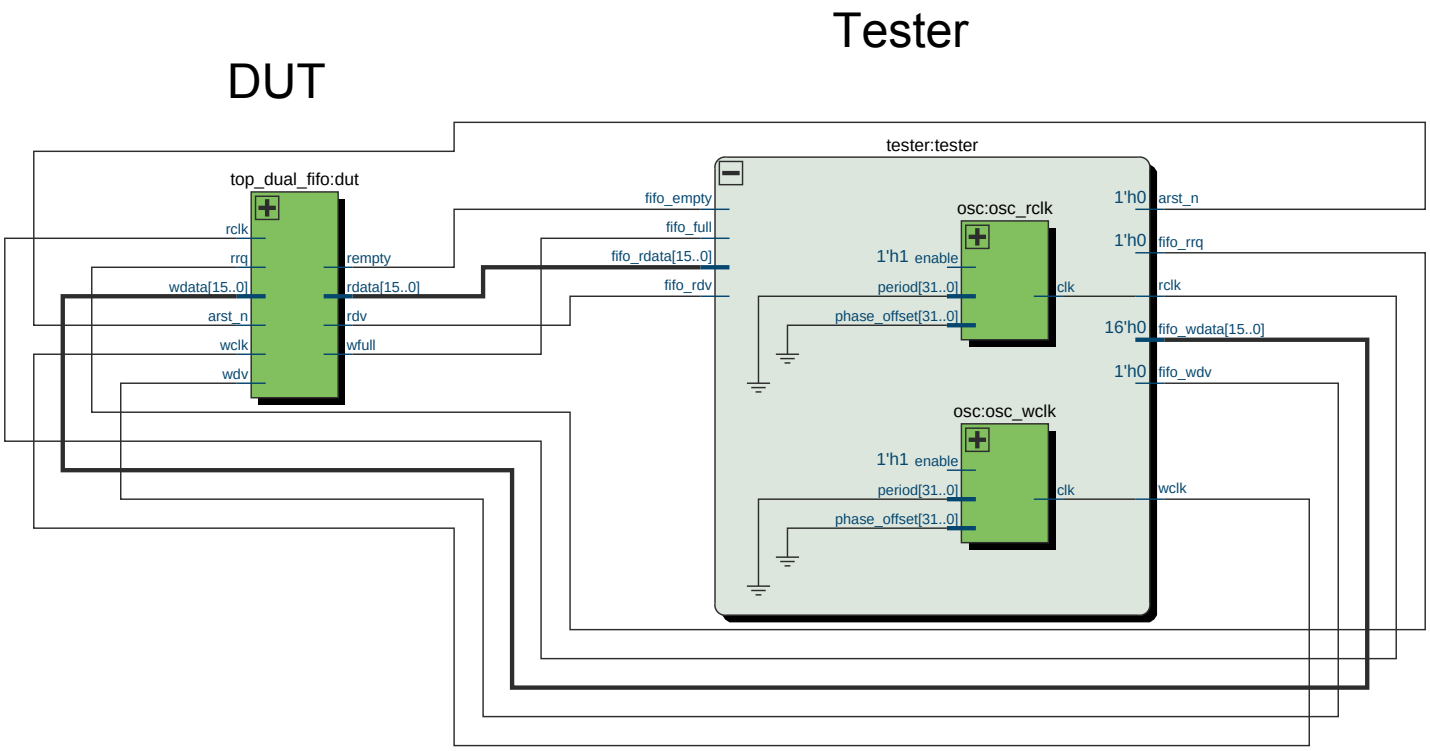
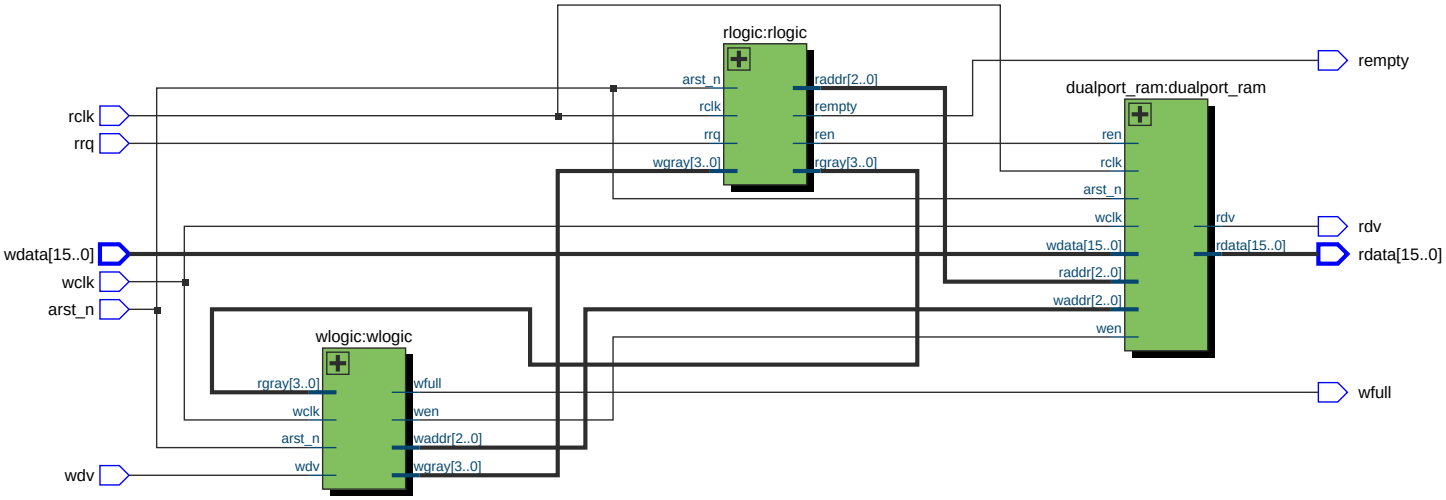
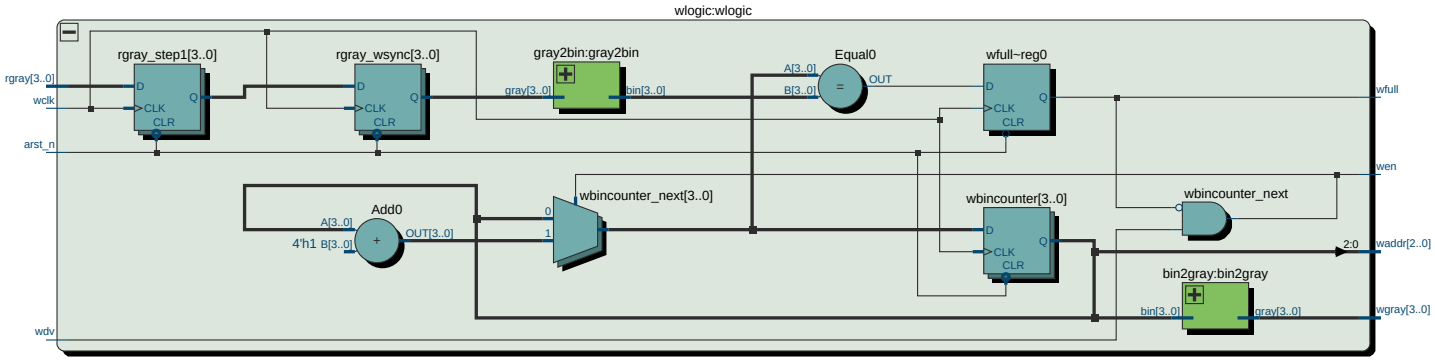
Testbench


DUT
Tester
top_dual_fifo:dut
rclk
rrq
wdata[15..0]
arst_n
wclk
wdv
rempty
rdata[15..0]
rdv
wfull
tester:tester
fifo_empty
fifo_full
fifo_rdata[15..0]
fifo_rdv
osc:osc_rclk
1'h1 enable
period[31..0]
phase_offset[31..0]
clk
osc:osc_wclk
1'h1 enable
period[31..0]
phase_offset[31..0]
clk
1'h0 arst_n
1'h0 fifo_rrq
rclk
16'h0 fifo_wdata[15..0]
1'h0 fifo_wdv
wclk

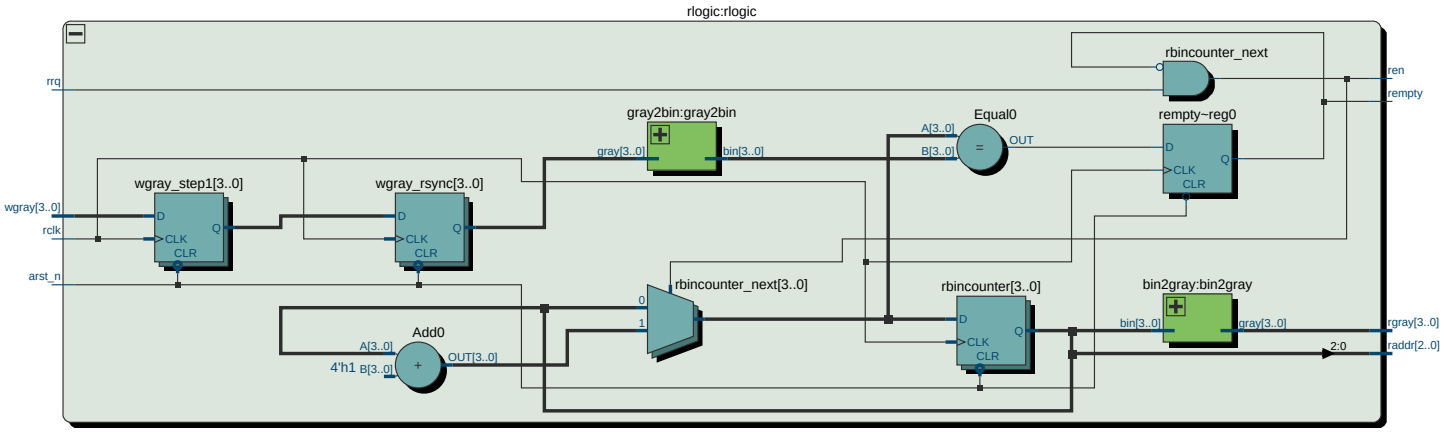
top_dual_fifo



WRITE LOGIC


wlogic:wlogic
rgray_step1[3..0]
rgray_wsync[3..0]
gray2bin:gray2bin
Equal0
wfull~reg0
rgray[3..0]
wclk
arst_n
wdv
wfull
wen
waddr[2..0]
wgray[3..0]
Add0
4'h1
wbincounter_next[3..0]
wbincounter[3..0]
wbincounter_next
bin2gray:bin2gray
D
CLK
CLR
Q
A[3..0]
B[3..0]
OUT
OUT[3..0]
gray[3..0]
bin[3..0]
2:0

READ LOGIC


rlogic:rlogic
rrq
rclk
arst_n
wgray[3..0]
wgray_step1[3..0]
wgray_rsync[3..0]
gray2bin:gray2bin
gray[3..0]
bin[3..0]
Equal0
A[3..0]
B[3..0]
OUT
rbincounter_next
rempty~reg0
rbincounter_next[3..0]
rbincounter[3..0]
Add0
4'h1
OUT[3..0]
bin2gray:bin2gray
rgray[3..0]
raddr[2..0]
2:0
ren
rempty
D
Q
CLK
CLR

Dual-port block RAM