SystemC Assignment 1
Weightage: 10 marks **Deadline: 9th Nov, 2022**

On the System C assignment --> We can have the trivial instruction set as an example and the following to be implemented...
a> implement the ISA model in plain C and run the application as in (c) below.
b> implement the ISA in SystemC with full clock visibility and run the application as in (c) below.
The following to be noted

- It takes one clock cycle for a RAM or ROM model. i.e, if the address is given on the rising edge of clock '0', data will come out on clock '1' read cycle. For a write cycle, it takes one clock to actually complete the write.
- It takes one clock cycle for a Register Bank similar to RAM.
- It takes one clock cycle to add, subtract numbers
- Students can add JNZ (Jump on Not Zero) as a new instruction of their own to simplify the application sw.

c> Application sw is to do an addition of 10 numbers. say a0, a1, ... a9. Each number is 8bits wide.

Figure 2.6: A simple (trivial) instruction set.

Assembly instruct.	First byte		Second byte		Operation
MOV Rn, direct	0000	Rn	direct		Rn = M(direct)
MOV direct, Rn	0001	Rn	direct		M(direct) = Rn
MOV @Rn, Rm	0010		Rn	Rm	M(Rn) = Rm
MOV Rn, #immed.	0011	Rn	immediate		Rn = immediate
ADD Rn, Rm	0100		Rn	Rm	Rn = Rn + Rm
SUB Rn, Rm	0101		Rn	Rm	Rn = Rn - Rm
JZ Rn, relative	1000	Rn	relative		PC = PC+ relative (only if Rn is 0)