

[illegible]

FRAMOS FSA interface

To Wire to Board connector

J1
DF40C-60DS-0.4V(51)

To Wire to Board connector

3V8_CAM
3V8_CAM
1V8_CAM
CAM_SCL_1V8
CSI_CAM_XVS
CAM_SDA_1V8
CSI_CAM_XTRIG
1V8_CAM
CSI_CAM_EN
CSI_CAM_CLK
CSI_D0_N
CSI_D0_P
CSI_D2_P
CSI_D2_N

AUX_ANA
AUX_IF
XCLR
XMASTER
XCE
XHS
PW_EN_0
SLAMODE1
INCK
MCLK1

AUX_DIG
AUX_V
SDO
TENABLE
TOUT
PW_EN_1
SLAMODE2

1V8_CAM
1V8_CAM
CSI_CAM_EN
CSI_D3_P
CSI_D3_N
CSI_D1_N
CSI_D1_P
CSI_CLK_P
CSI_CLK_N

R1 100k
R2 10k
R3 100k
R4 10k DNP
R5 100k
R6 10k
R7 12k DNP
R8 12k
R9
R10 DNP OR

TP4
TP1
TP3
TP5
TP7
TP9
TP10
TP11 1V2
TP12
TP13
TP8
TP14

GND

FRAMOS CSI interposer connector

J2
MSAK24025P30
STM

CSI_D3_N
CSI_D3_P
CSI_D2_N
CSI_D2_P
CSI_D1_N
CSI_D1_P
CSI_D0_N
CSI_D0_P
CSI_CLK_N
CSI_CLK_P
CAM_SDA_3V3
CAM_SCL_3V3
CSI_CAM_EN
CSI_CAM_XVS
CSI_CAM_CLK
CSI_CAM_XTRIG

3V3FFC
TP20
5V0_SYS
TP21

C8 100n
C12 100n
C15 100n
C16 100n

GND

Matching socket: STE-I-PEX-20455-030E-12
Matching cable: KAB-I-PEX-20453-030T-0500-111-ROUND

I2C logic level translator

JNB can have I2C configured as 1V8

1V8_CAM

CAM_SCL_1V8

CAM_SDA_1V8

GND

U1 NTS0102GT

VCC_A VCC_B

A1 B1

A2 B2

OE GND

3V3FFC

CAM_SCL_3V3

CAM_SDA_3V3

GND GND

I2C logic level translator bypass

CAM_SCL_1V8

CAM_SDA_1V8

R16 DNP

R17 DNP

CAM_SCL_3V3

CAM_SDA_3V3

Pull-up resistors from 3V3 side are placed on JNB

Mount holes

- MP1 PCB_Mount_Hole_2.2_4.5
- MP2 PCB_Mount_Hole_2.2_4.5
- MP3 PCB_Mount_Hole_2.2_4.5
- MP4 PCB_Mount_Hole_2.2_4.5

I2C logic level translator

JNB can have I2C configured as 1V8

1V8_CAM

CAM_SCL_1V8

CAM_SDA_1V8

GND

U1 NTS0102GT

VCC_A VCC_B

A1 B1

A2 B2

OE GND

3V3FFC

CAM_SCL_3V3

CAM_SDA_3V3

GND GND

I2C logic level translator bypass

CAM_SCL_1V8

CAM_SDA_1V8

R16 DNP

R17 DNP

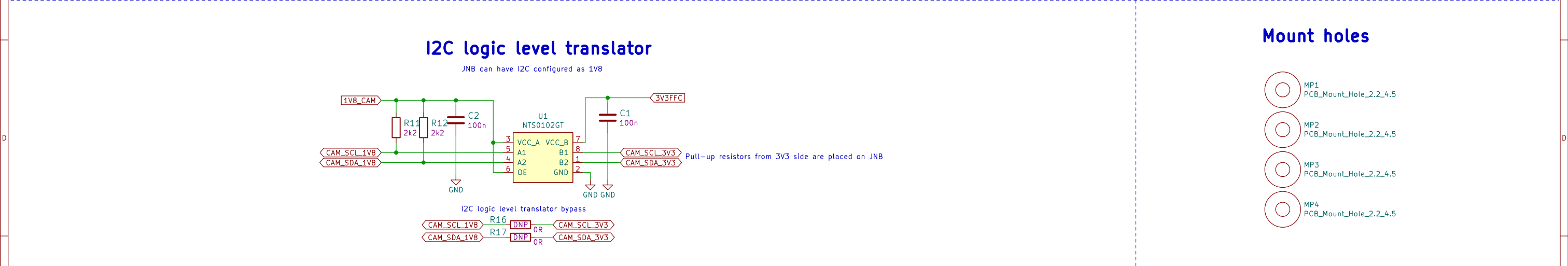
CAM_SCL_3V3

CAM_SDA_3V3

Pull-up resistors from 3V3 side are placed on JNB

Mount holes

- MP1 PCB_Mount_Hole_2.2_4.5
- MP2 PCB_Mount_Hole_2.2_4.5
- MP3 PCB_Mount_Hole_2.2_4.5
- MP4 PCB_Mount_Hole_2.2_4.5



I2C logic level translator

JNB can have I2C configured as 1V8

1V8_CAM

CAM_SCL_1V8

CAM_SDA_1V8

GND

U1 NTS0102GT

VCC_A VCC_B

A1 B1

A2 B2

OE GND

3V3FFC

C1 100n

CAM_SCL_3V3

CAM_SDA_3V3

GND GND

Pull-up resistors from 3V3 side are placed on JNB

I2C logic level translator bypass

CAM_SCL_1V8 R16 DNP OR CAM_SCL_3V3

CAM_SDA_1V8 R17 DNP OR CAM_SDA_3V3

- ### I2C logic level translator

JNB can have I2C configured as 1V8

1V8_CAM

CAM_SCL_1V8

CAM_SDA_1V8

GND

U1 NTS0102GT

VCC_A VCC_B

A1 B1

A2 B2

OE GND

3V3FFC

C1 100n

CAM_SCL_3V3

CAM_SDA_3V3

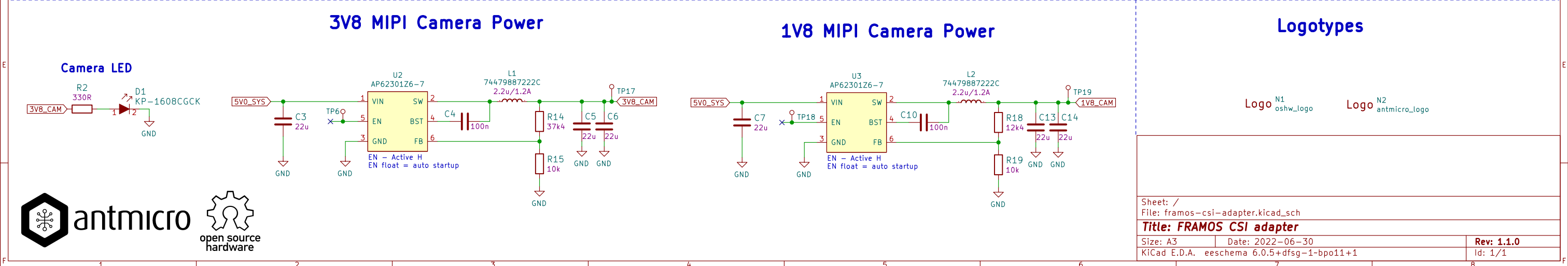
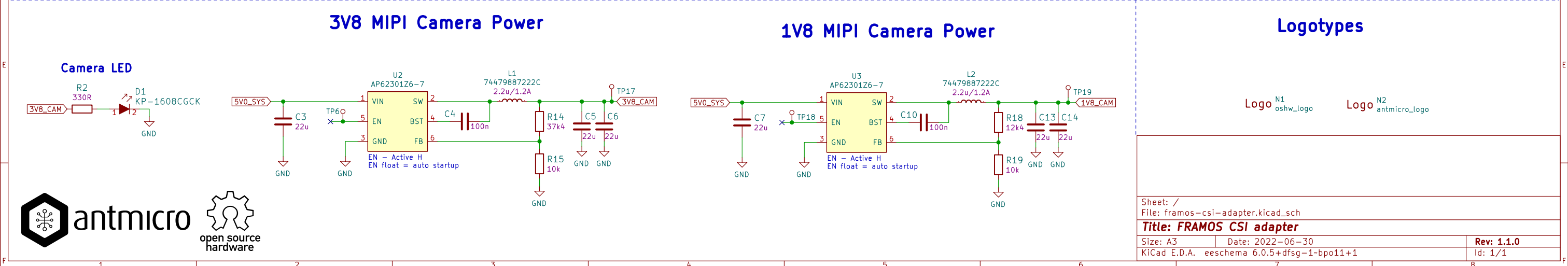
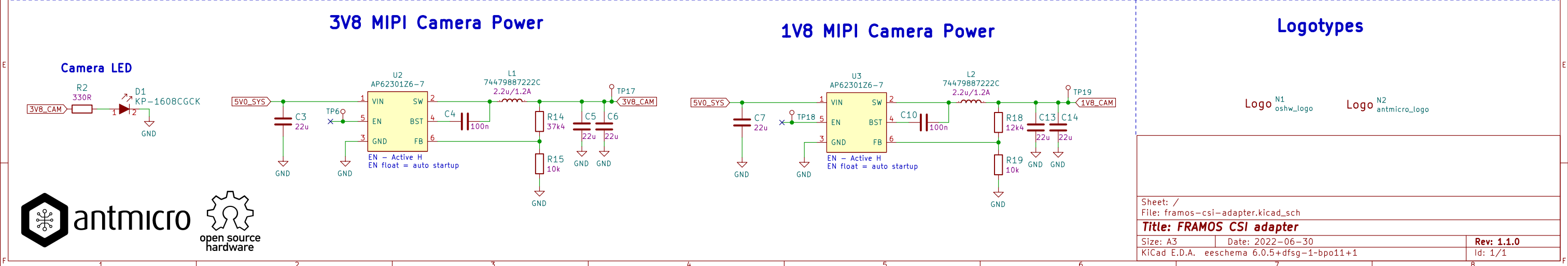
GND GND

Pull-up resistors from 3V3 side are placed on JNB

I2C logic level translator bypass

CAM_SCL_1V8 R16 DNP OR CAM_SCL_3V3

CAM_SDA_1V8 R17 DNP OR CAM_SDA_3V3

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The schematic illustrates the power management for a camera module, divided into four main sections:

- Camera LED:** A simple circuit where the 3V8_CAM supply passes through a resistor R2 (330R) to drive an LED D1 (KP-1608CGCK).
- 3V8 MIPI Camera Power:** This section shows a voltage regulator U2 (AP62301Z6-7) converting 5V0_SYS to 3V8. The EN pin is active-high and floats for auto-startup. Input/output capacitors C3 and C4 are 22uF. An output capacitor C5 is 22uF. A feedback network consists of resistors R14 (37k4) and R15 (10k). Inductor L1 is 2.2uH/1.2A.
- 1V8 MIPI Camera Power:** Similar to the 3V8 section, it uses a voltage regulator U3 (AP62301Z6-7) to convert 5V0_SYS to 1V8. It includes input/output capacitors C7 and C10 (22uF), an output capacitor C13 (22uF), a feedback network with R18 (12k4) and R19 (10k), and inductor L2 (2.2uH/1.2A).
- Logotypes:** Two logos are present: Logo N1 (oshw_logo) and Logo N2 (antmicro_logo).

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