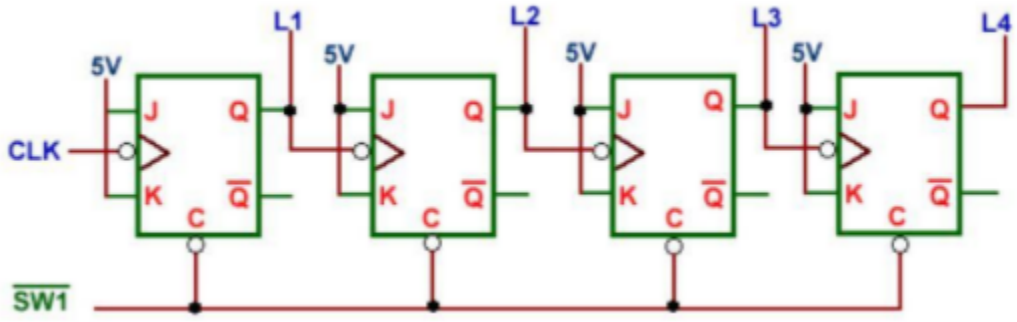
Experiment-9 **Digital Circuits** **2022**

To be implemented on TinkerCad

PART: A **Binary Ripple Counter**

A binary counter is required to count in the binary number sequence – either in the increasing order (UP counting) or in the decreasing order (DOWN counting). A ripple counter consists of T flip-flops with T = 1 connected in cascade. As T flip-flops are not available as of now, one has to either use J-K flip-flops with J = K = 1 or use D flip-flops with D = Q'. In this experiment, we will set up and test a 4-bit binary ripple counter using four J-K flip-flops available in the tinkercad.



4-Bit Binary Ripple Counter

Truth Table

Decimal	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0

7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Steps to be followed

1. Use two dual JK flip-flop ICs (74HC73) in tinker cad. Give logic '1' for J and K inputs of all the four flip-flops. Use a function generator from tinker cad to give the clock input of frequency of 1 Hz, amplitude 5V and DC offset 2.5 V.

2. Connect all the Reset inputs together to one Input Switch and the outputs Q_0, Q_1, Q_2, Q_3 to four LED Displays. Set up a Binary Ripple Counter by making clock connections as follows: CK_0 = External Clock from an Input Switch, $CK_1 = Q_0$, $CK_2 = Q_1$, $CK_3 = Q_2$.

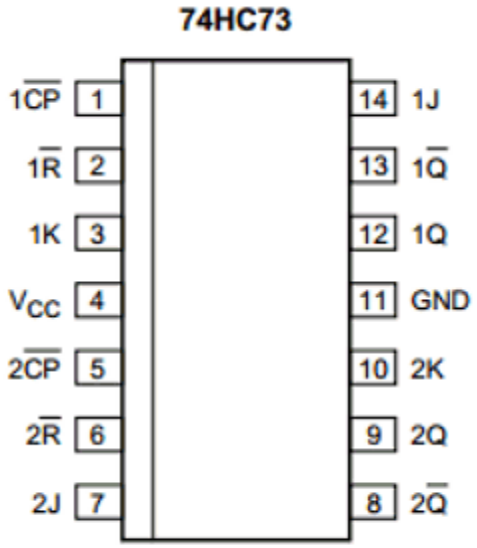
3. Apply a few Clock pulses to CK_0 and note whether the count sequence is UP or DOWN. Apply Reset input so as to initialize the counter to the appropriate starting state (0000).

4. Now make Reset = 1 so that counting is enabled. Apply Clock pulses to CK_0 and tabulate the state sequence for the different cycles.

5. Change the clock connections to $CK_1 = Q_0'$, $CK_2 = Q_1'$, $CK_3 = Q_2'$, with the other connections unchanged. Repeat steps 3 and 4. and observe the sequence.

Note: In the figure, L_1, L_2, L_3 and L_4 represent Q_0, Q_1, Q_2 and Q_3 respectively.

IC Diagram

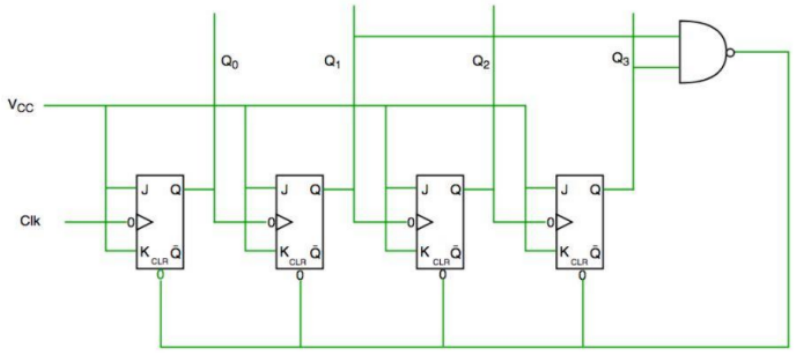


PART: B <u>Decade Ripple Counter</u>

A decade counter has the count sequence 0→1→2→.....→8→9→0.., which can be achieved by making Reset = (Q3·Q1)' for all the flip-flops in a 4-bit binary counter. This forces the state to become 0000 as soon as the counter makes the transition to the state1010 from the state 1001 according to the normal UP counting sequence.

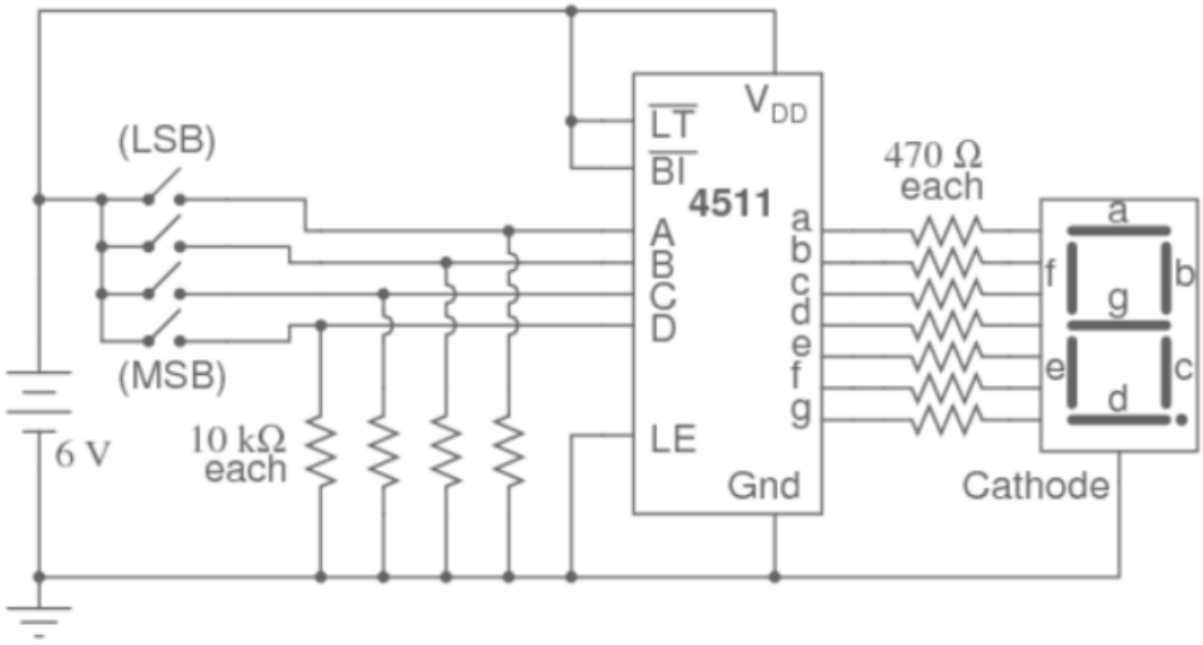
<u>Decade Counter Circuit Diagram</u>

Count	Output			
	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1



Steps to be followed:

1. Disconnect the Input Switch connected to Reset. Use one NAND gate from the 74HC00 IC chip to implement the logic for Reset. Make Clock connections as required for UP counting.
2. Apply Clock pulses to CK0 and tabulate the state sequence for different cycles of the clock.
3. Place the decoder 4511 IC on the breadboard. Make the connections to the 7 segment display.
4. Connect the decoder outputs a, b, c, d, e, f, and g to the corresponding alphabets on the 7 segment display through resistors.
5. Follow the steps we did in Lab 5 here to display the counter values on 7 segment display.



Note:

Take the outputs from the output pins of J-K flip-flops and connect it directly to the 4511 IC. Use 1K ohm resistors in place of 470 ohm resistors while connecting to the & segment display.

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Deliverables

1) Tinker-Cad Link
2) Screenshot of the Tinker-Cad Circuit
3) Pin Diagram
4) Characteristic equation (K-map also)
5) Observations and justifications
6) Applications (at least two)