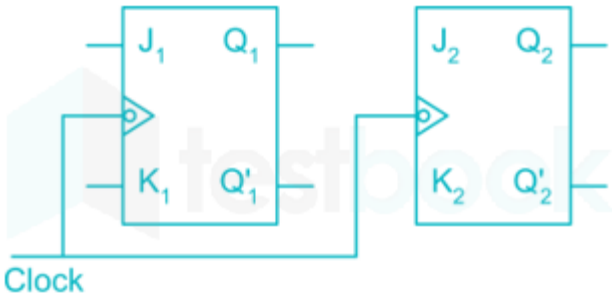
TUTORIAL 9

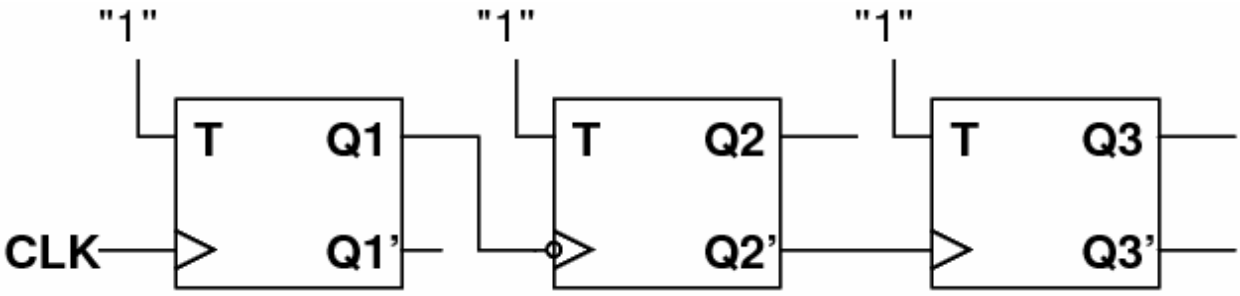
Q1. Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with

A 4 bit data 1011 is applied to the shift register 1. Find the minimum number of clock pulses required to get the same output data as the input data with the same clock pulses.

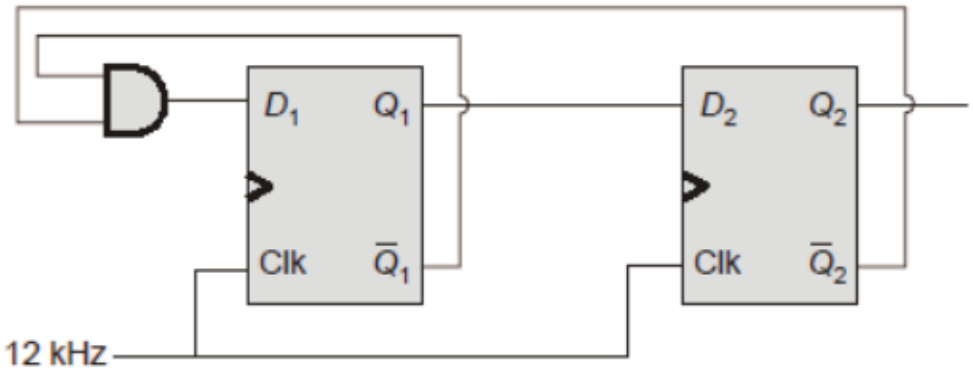
Q2. A synchronous counter using two J-K flip flops that goes through the sequence of states: Q1Q2 = 00->10->01->11->00 is required. To achieve this, find the inputs of the flip flops?



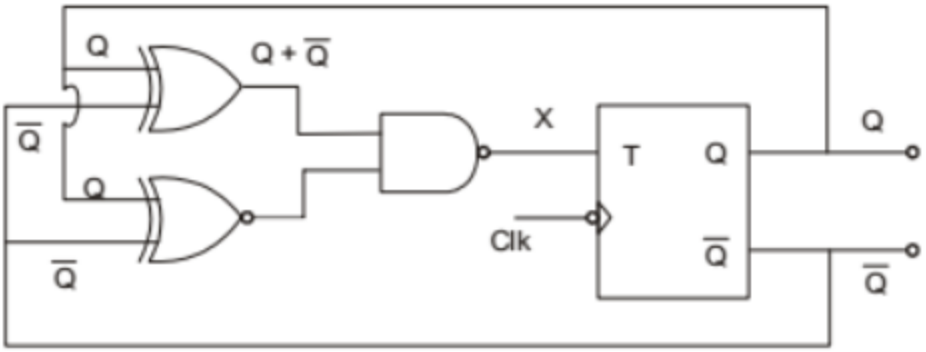
Q3.Draw output waveforms (Q1, Q2, Q3) of the given T FFs along with the CLK signal for 5 Clock cycles. Consider the initial states of Q1=Q2=Q3=0.



Q4.In the circuit shown the frequency of the clock signal is 12 KHz. The frequency of the signal at Q2 will be ?



Q5 The clock frequency for the following circuit is 2kHz. If the initial state of the output Q of FF is '0', then the frequency of the output Q in kHz.



Q6. Design serial n-bit adder using 1-bit adder and shift registers.

Q7. Design a counter, which counts the sequence 4-5-6-7-8-9-4…. Using active low clear and active low preset.

Q8. Assume that you have an oscillator which provides clock signal with frequency 8 Hz. Design modulo-6 counter which increments its output count every second. Design a modulo 7 ripple counter.