Rubrics:

Q1.

Set A:

Inst. Number in which hazard is present	Register in which hazard is present	Inst. Number due to which hazard is present
5	R4	4

Set B:

Inst. Number in which hazard is present	Register in which hazard is present	Inst. Number due to which hazard is present
4	R4	2

Set C:

Inst. Number in which hazard is present	Register in which hazard is present	Inst. Number due to which hazard is present
4	R5	2

Q2.

Set A:
Minimum clock period = max (3,5,7, 10,6) = 10 ns (**1 mark**)

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
add r1, r2, r3	F	D	E	M	W													
add r4, r1, r3		F	D	D	D	D	E	M	W									
add r5, r4, r1			F	F	F	F	D	D	D	D	E	M	W					
add r6, r7, r8							F	F	F	F	D	E	M	W				
add r2, r6, r7											F	D	D	D	D	E	M	W

(**0.5 + 1.5 + 1.5 + 1 + 1.5** = **6 marks** for correct pipeline diagram)
Time needed = 18 *10 = 180 ns (**1 mark**)

Set B:
Minimum clock period = max (10,13,7, 15,10) = 15 ns (**1 mark**)

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
add r1, r2, r3	F	D	E	M	W													
add r4, r2, r3		F	D	E	M	W												
add r5, r4, r1			F	D	D	D	D	E	M	W								
add r6, r5, r8				F	F	F	F	D	D	D	D	E	M	W				
add r2, r6, r7								F	F	F	F	D	D	D	D	E	M	W

(**0.5 + 1 + 1.5 + 1.5 + 1.5** = **6 marks** for correct pipeline diagram)
Time needed = 18 *15 = 270 ns (**1 mark**)

Set C:
Minimum clock period = max (1,3,2, 8,5) = 8 ns (**1 mark**)

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14
add r3, r4, r5	F	D	E	M	W									
sub r1, r0, r2		F	D	E	M	W								
add r6, r7, r3			F	D	D	D	E	M	W					
add r8, r3, r10				F	F	F	D	E	M	W				
sub r11, r8, r6							F	D	D	D	D	E	M	W

(**0.5 + 1 + 2 + 1 + 1.5** = **6 marks** for correct pipeline diagram)
Time needed = 14 *8 = 112 ns (**1 mark**)

Q3.

Set A:

Instruction	1	2	3	4	5	6	7	8	9
add r1, r2, r3	S1	S2	S3	S4	S5				
add r4, r5, r6		S1	S2	S3	S4	S5			
add r2, r15, r3			S1	S2	S3	S4	S5		
sub r5, r7, r8				S1	S2	S3	S4	S5	
sub r9, r10, r11					S1	S2	S3	S4	S5

(**1.2 * 5 = 6 marks** for correct pipeline diagram)
Implementation time for processor A = 5 cycles *10 μs/cycle = 50 μs (**1 mark**)
Implementation time for processor B = 9 cycles* 4 μs/cycle = 36 μs (**1 mark**)

Set B:

Instruction	1	2	3	4	5	6	7	8	9
add r1, r2, r3	S1	S2	S3						
sub r4, r5, r6		S1	S2	S3					
add r2, r15, r3			S1	S2	S3				
Exsub r5, r7, r8				S1	S2	S3			
add r6, r3, r9					S1	S2	S3		
add r10, r11, r12						S1	S2	S3	
add r13, r11, r12							S1	S2	S3

(0.8 *7 ~ **6 Marks** for correct pipeline diagram)
Implementation time for processor A = 7 cycles *10 μs/cycle = 70 μs (**1 mark**)
Implementation time for processor B = 9 cycles *6 μs/cycle = 54 μs (**1 mark**)

Set C:

Instruction	1	2	3	4	5	6	7	8	9
add r1, r2, r3	S1	S2	S3	S4					
sub r4, r5, r6		S1	S2	S3	S4				
add r2, r15, r3			S1	S2	S3	S4			
sub r5, r7, r8				S1	S2	S3	S4		
add r6, r3, r9					S1	S2	S3	S4	
add r10, r11, r12						S1	S2	S3	S4

(1*6 = **6 marks** for correct pipeline diagram)
Implementation time for processor A = 6 cycles*10 μs/cycle = 60 μs (**1 mark**)
Implementation time for processor B = 9 cycles *5 μs/cycle = 45 μs (**1 mark**)
