

Quiz 2
CSE 112 Computer Organization

Dt: 12/07/2022

Total Marks = 60

Time Duration = 80 minutes

INSTRUCTIONS:

1. The duration of the quiz is 80 mins. No further extension of time will be given regarding this.
2. Write any assumption clearly, if any. Only reasonable assumptions will be considered if any ambiguity is found in the question.
3. Do not use question paper for rough work, please show rough work (*if any*) in the answer sheet itself.
4. Calculators are NOT allowed during exam time. ONLY use pen and paper for writing the exam.

GOOD LUCK !!

For All the questions, please use the following ISA. You are not allowed to use any instructions which are not part of the ISA, unless specified otherwise.

The instructions supported by the ISA are mentioned in the table below. The ISA has 16 General purpose registers: r0 to r15

Name	Semantics	Syntax
Add	Performs $\text{reg1} = \text{reg2} + \text{reg3}$	add reg1 reg2 reg3
Sub	Performs $\text{reg1} = \text{reg2} - \text{reg3}$	sub reg1 reg2 reg3
Mov imm	Performs $\text{reg1} = \text{Imm}$	mov reg1 \$Imm
Mov	Performs $\text{reg1} = \text{reg2}$	mov reg1 reg2
Branch to label if Equal to immediate value	Branch to label if $\text{reg1} == \text{imm}$	beq reg1 \$imm label
Branch to label if Equal to register value	Branch to label if $\text{reg1} == \text{reg2}$	beq reg1 reg2 label
Branch to address if Equal	Branch to address stored in reg3 if $\text{reg1} == \text{reg2}$	beq reg1 reg2 reg3
Branch unconditional	Branch to label unconditionally	b label
Increment by 1	Performs $\text{reg1} = \text{reg1} + 1$	inc reg1
Decrement by 1	Performs $\text{reg1} = \text{reg1} - 1$	dec reg1

Apart from the above instructions, the following subroutines are also valid and can be used in assembly code:

Name	Semantics	Syntax
Input	Reads immediate data from the user into register rg	in rg
Output	Prints str on the console	out "str"

Note: For Questions, Q1 and Q2, assume the initial value of all the registers r0 to r15 is equal to 0 unless specified otherwise.

Q3.[CO3] Consider a hypothetical three-stage pipeline - Fetch (F), Decode (D), and Execute (E). In the fetch stage, the instructions are fetched from the instruction memory. In the decode stage, the fetched instructions are decoded and the values of the input registers are read. In the execution stage, ALU performs the computation on values read from the decode stage and updates the value of the output register.

For the instructions given below, write the pipeline diagram. Assume all register values to be zero. **[3x5 = 15 marks]**

1. mov r0, r2
2. mov r1, r3
3. add r4, r8, r9
4. add r5, r2, r3
5. beq r4, r5, r7

Note: Pipeline Diagram is used to tell in what stage the instructions are n. An example of a pipeline diagram is given below. **No marks shall be given if the answer is not in this form.**

add r0, r2, r3	F	D	E		
add r1, r2, r3		F	D	E	
beq r2, r2, r7			F	D	E

Q4.[CO2] Consider a stack that starts from memory location 0x400. In addition to the instructions defined in **Q1**, consider the two instructions below for stack operations.

Semantics	Syntax
Pushes the value in register reg1 into stack	PUSH reg1
Pops the last value in the stack into register reg1	POP reg1

Whenever a value is put into the stack via PUSH instruction, the value of Stack Pointer (SP) decrements by one. Whenever a value is moved out of the stack via POP instruction, the value of SP increments by one. For the given program, determine the value of SP for each instruction.

[1.5x10 = 15 marks]

1. PUSH r1
2. PUSH r2
3. POP r1
4. PUSH r1
5. PUSH r5
6. PUSH r4
7. POP r2
8. PUSH r3
9. POP r5
10. PUSH r7