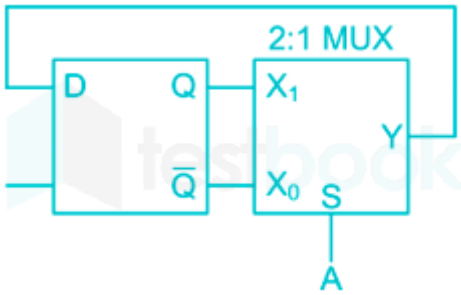
INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

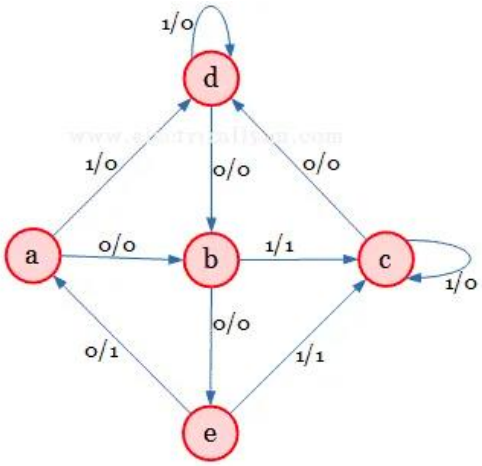
PRACTICE PROBLEM X

ECE 111 DIGITAL CIRCUITS

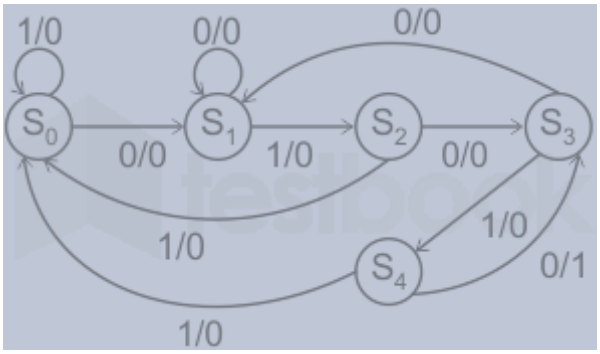
1. Draw the state transition diagram for the given circuit:



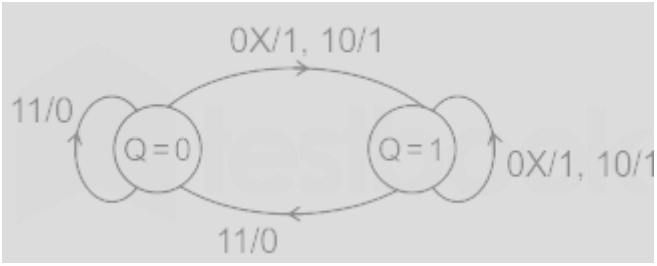
2. Determine the reduced state diagram for the given state diagram.



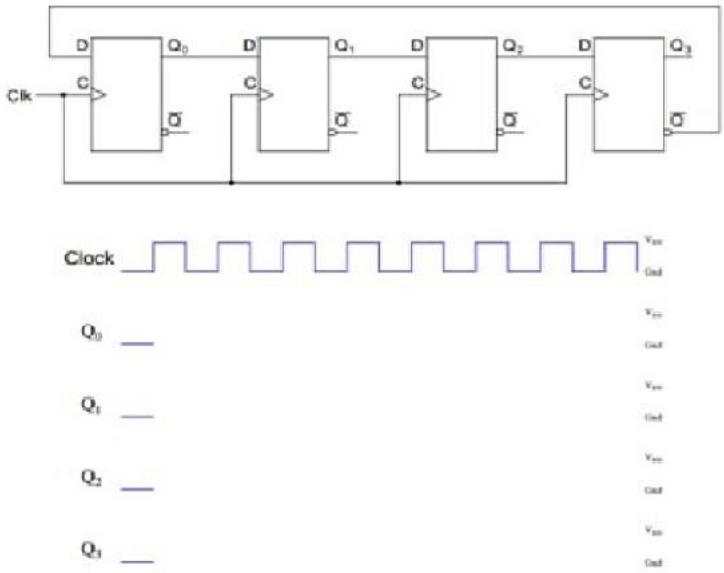
3. The state diagram of a sequence detector is shown below, State So is the initial state of the sequence detector, if the output is 1, then what is the sequence detected



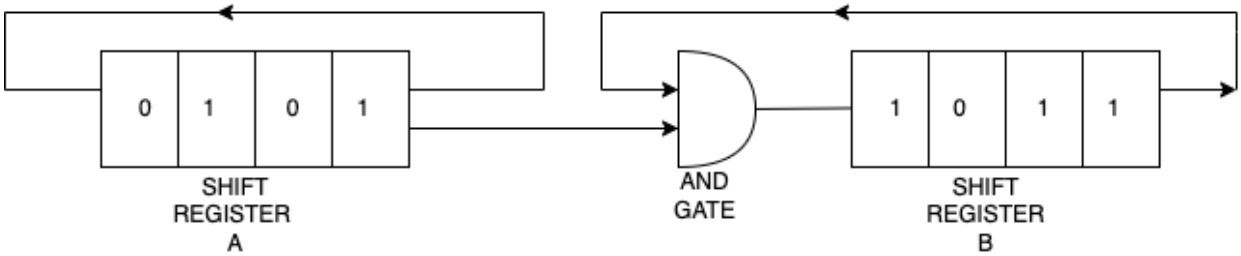
4. A state diagram of a logic gate which exhibits delay in the output is shown in the figure, where X is don't care condition and Q is the output representing the state. Which logic gate is represented by this state diagram?



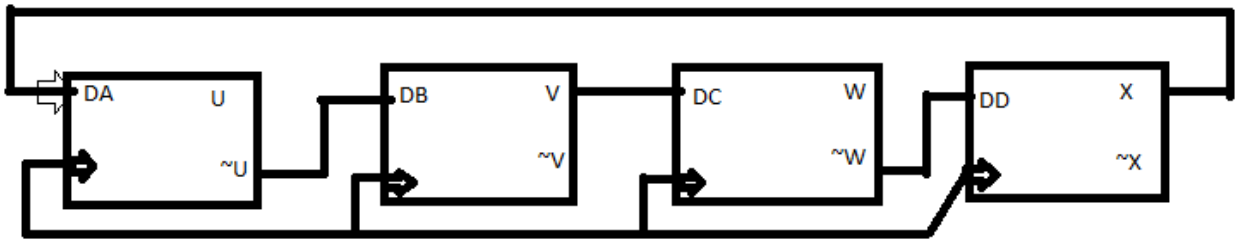
5. Design a Mealy FSM using D flip-flops to detect an overlapping sequence of 1101.
6. Design a Moore FSM using T flip-flops to detect a non-overlapping sequence of 111
7. Give the State Machine for Serial 2's complementer. Start from LSB onwards.
8. Draw the outputs of all flip-flops and identify the function of this circuit.



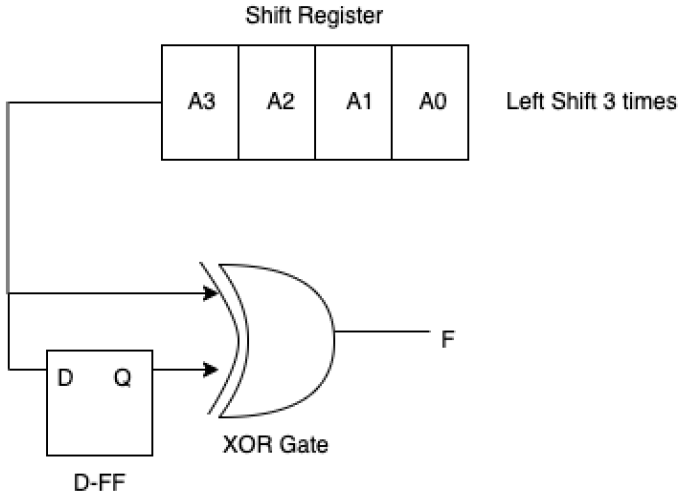
9. Design a synchronous counter with D flip flop that goes through states 0, 1, 2, 4, 0, … The unused state must always go to zero state on the next clock pulse.
10. If A=0101 and B=1011, then what will be the content of register A and B after 4 right shifts.



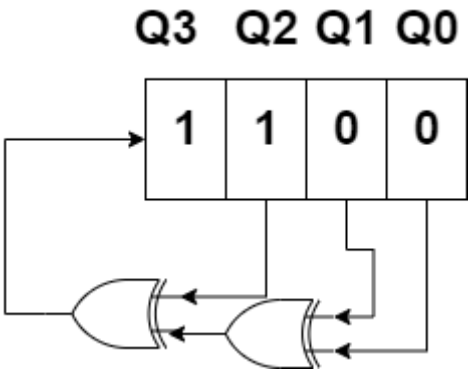
11. Initial value of UVWX=0000, then what are the sequence of numbers the given circuit is counting?



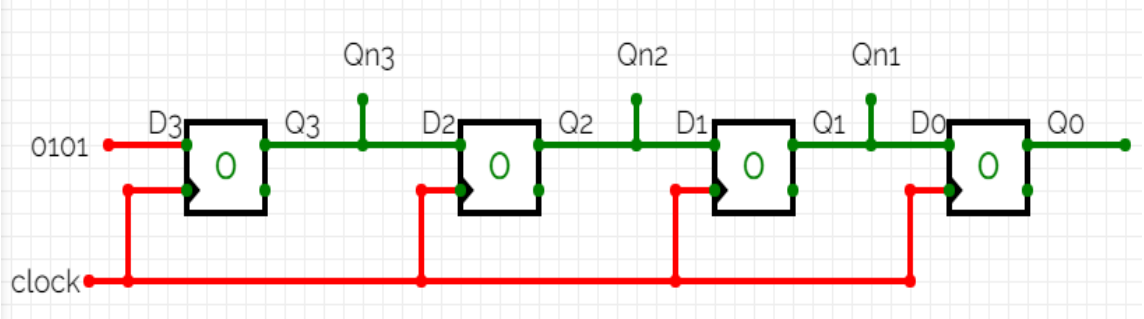
12. What will be output at F at CLK=0, CLK=1, CLK=2, CLK=3 (write equations). Given that Input bits are left shifted at each CLK and Initially Q=0.



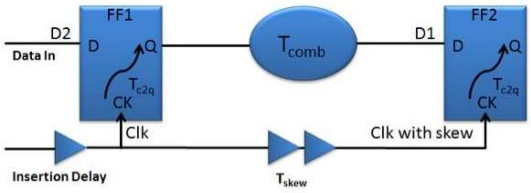
13. In the figure, right shift register is given along with two xor gates. Determine the number of clocks required to bring it to the initial state of '1100'?



14. You are given with a SIPO (Serial input parallel output) shift register. If the input to this register is given as 0101 at D3, and previous values stored at FFs output are Qn3, Qn2, Qn1, Qn0 respectively. Find the number of clocks cycles needed to display the data at the output,



15. Suppose you are given a counter which is at initial value as 8. Assume that counter to be 4-bit twisted ring counter. Write down sequence of all states it will show (until it reaches to its highest value) after giving clock input with proper explanation.
16. A 14 bit timer is loaded with the counter value of 07D0 H. The timer input is connected to a clock with the frequency of 800 kHz. The timer is programmed to produce a continuous square wave output. What will be the frequency of square wave output?
17. A 15 MHz clock frequency is applied to a cascade of modulus 2 counter, modulus 3 counter and modulus 5 counter. What will be the lowest output frequency and the overall modulus?
18. Describe briefly about Clock non idealities like clock Skew and Jitter. Do they effect the effective cycle time?
19. How does Clock Skew affect timing (i.e Setup and Hold Time) of the Flip-flop/Pipeline? Explain and give the modified equations of Setup and Hold Calculations.
20. How clock skew affects the circuits considering setup and hold time?
21. Observe the given figure.



What is the maximum clock frequency if tclk_q =1ns ,Tsetup=1.5ns Tcomb=3ns , Tskew= 2ns to avoid setup violation?

22. Derive a minimal state table for a single-input and single-output Moore-type FSM that produces an output of 1 if in the input sequence it detects either 110 or 101 patterns. Overlapping sequences should be detected.
23. Repeat Problem 22 for a Mealy-type FSM.
24. A sequential circuit has two inputs, w1 and w2, and an output, z. Its function is to compare the input sequences on the two inputs. If w1 = w2 during any four consecutive clock cycles, the circuit produces z = 1; otherwise, z = 0. For example

    w1 : 0110111000110

    w2 : 1110101000111

    z : 0000100001110

    Derive a suitable circuit.

25. Derive the circuits that implement the state tables in Figures a and b. What is the effect of state minimization on the cost of implementation?

Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

Figure a

Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	B	C	1
B	A	F	1
C	F	C	0
F	C	A	0

Figure b

26. A given FSM has an input, w, and an output, z. During four consecutive clock pulses, a sequence of four values of the w signal is applied. Derive a state table for the FSM that produces $z = 1$ when it detects that either the sequence w : 0010 or w : 1110 has been applied; otherwise, $z = 0$. After the fourth clock pulse, the machine has to be again in the reset state, ready for the next sequence. Minimize the number of states needed.

27. Derive a minimal state table for an FSM that acts as a three-bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit $p = 1$ if and only if the number of 1s in the three-bit sequence is odd.