ECE111: Digital Circuits

Practice Problem IX

1. Show how to build a J K Flip Flop using T FF with enable and combinational circuits.
2. Show how to build a SR latch using a single 7474 IC chip, which is positive edge triggered D FF and no other components.
3. Analyse the circuit shown in Fig. 1. Define the output Q1, Q2 and Output of OR gates for different input X = 0 or 1.

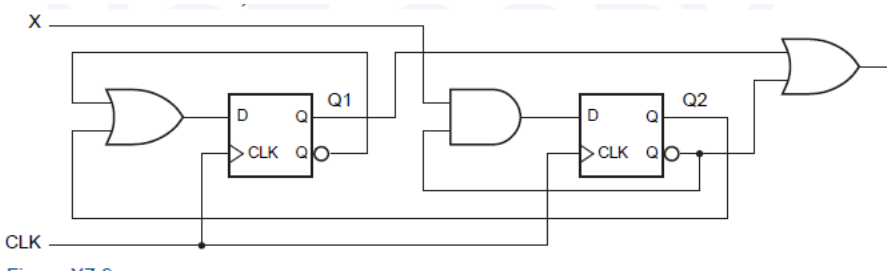

Figure 1

4. Compare the circuit shown in Fig. 2a with that of Fig. 2b. Show that both circuit functions identically.

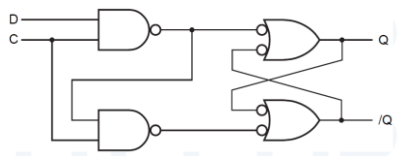

Figure 2a

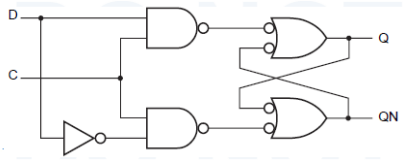

Figure 2b

5. An SR latch constructed from NAND gates is shown in Fig. 3. Determine the logic level at points a, b and c under the following conditions:
   a. S = R = Q = 0.
   b. As in (a) but S changes from 0 to 1.
   c. S = 0, R = 0 and Q = 1 and R changes from 0 to 1.

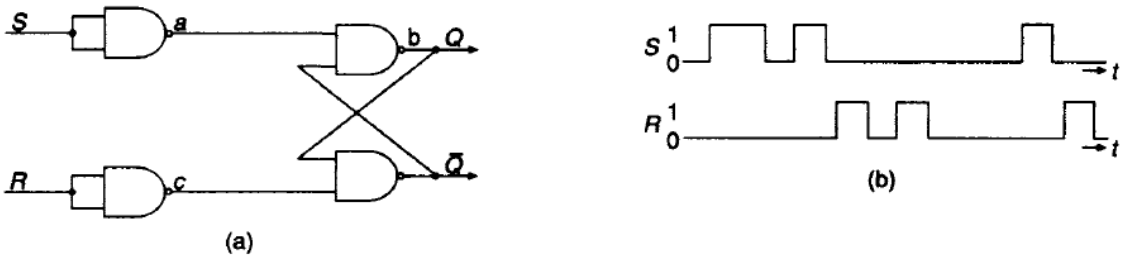

Figure 3

6. A Master/slave JK flip-flop is shown in Fig. 4. Assuming that, J = K = Q_m = Q_s = 0, trace the logic levels through the diagram for the following changes. (Assume that J and K changes during the positive clock period.)

a. J = 0 to 1, K = 0 to 0, during first positive clock period.
b. J = 1 to 1, K = 0 to 1, during second positive clock period.
c. J = 1 to 0, K = 1 to 0, during third positive clock period.
d. J = 0 to 1, K = 0 to 0, during fourth positive clock period.

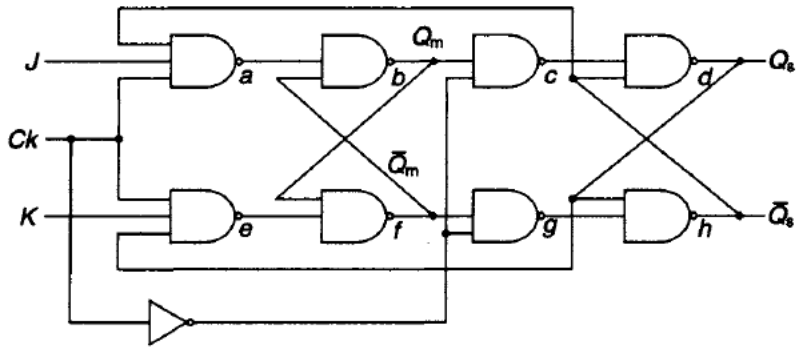

Figure 4

7. The waveform shown in Fig. 5a are to be applied to the circuit shown in Fig. 5b; assuming that the initial value of Q = 0, determine the Q output.

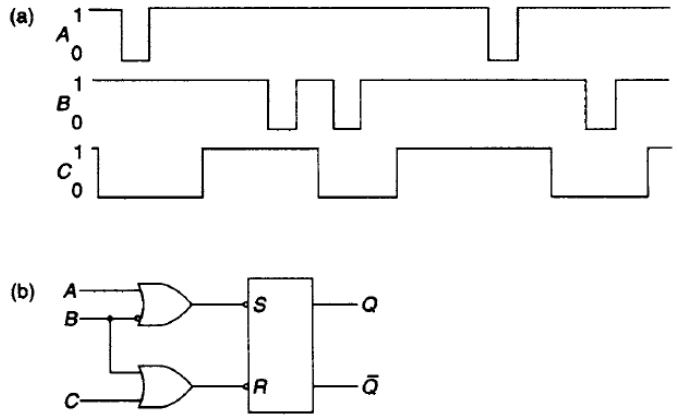

Figure 5

8. Given the S and R waveforms for an SR latch shown in Fig. 6 and assuming the initial value Q = 0, plot the time variations of Q output of the latch. How does the Q output vary if the latch is controlled by the G waveform?

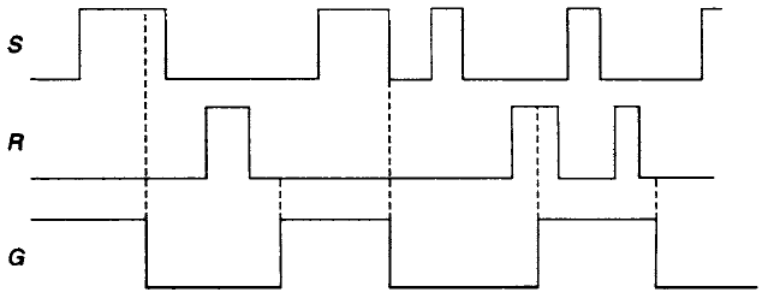

Figure 6

9. The circuit shown in Fig. 8 is a Flip Flop with X as input. Identify the flip flop type, i.e. S-R, J-K, D or T.

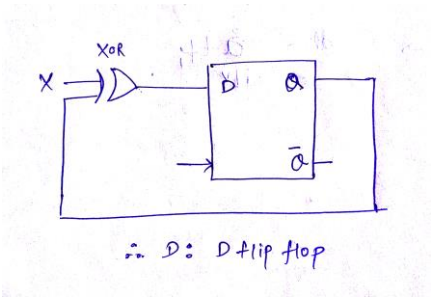

Figure 8

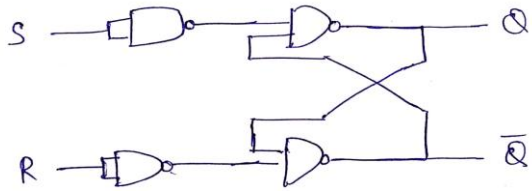

Figure 9

10. Derive the characteristic equation for T flip flop.
11. Derive the relation between T, J&K and between T, S&R by using k-map.
12. What combinational logic circuit (Fig. 10) is needed (In circular shape box) to generate sequence (Q_1 Q_0) : 10,00,01, ….? The input to circular box Q_0 and Q_1.

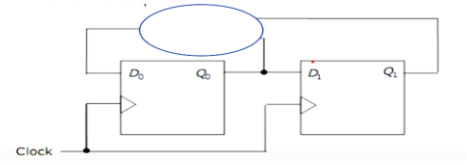

Figure 10

13. What would be the sequence (Q2Q1Q0) generated in Fig. 11? If Q2 is the output of last FF and Q0 is of first FF.

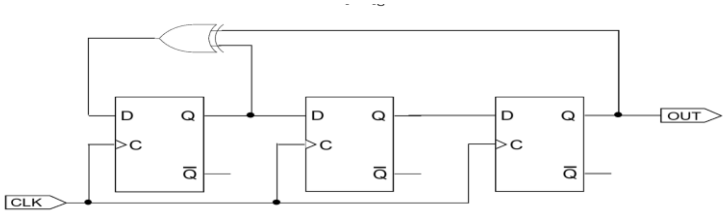

Figure 11