INDRAPRASTHA INSTITUTE OF INFORMATION TWCHNOLOGY DELHI

QUIZ 2

ECE 111 DIGITAL CIRCUITS

Date: March 7, 2022. Max. Marks: 10

ANSWER ALL QUESTIONS

1. Figure 1 shows the symbol of 74154 4 to 16 decoder. Using this decoder, give the logic circuit realization for the following logic functions using 74154 and minimum number of logic gates.

$$f_1(W,X,Y,Z) = \sum m(1,9,12,15)$$
$$f_2(W,X,Y,Z) = \sum m(0,1,2,3,4,5,7,8,10,11,12,13,14,15)$$

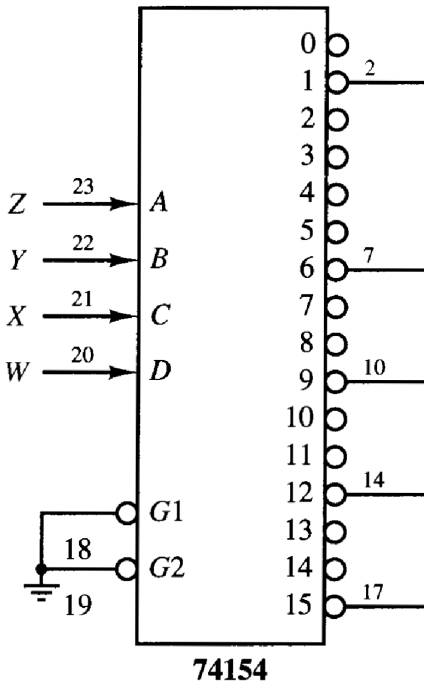


Figure 1

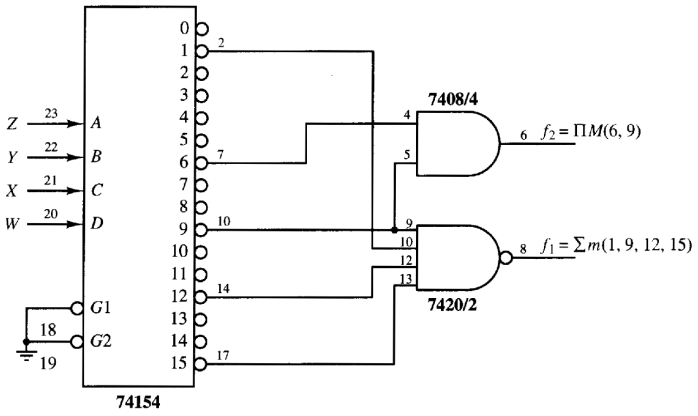
ANS:

We have f_1 = A'B'C'D + A'B'CD' + A'BC'D' +AB'C'D' = $\overline{\overline{m_1} + \overline{m_9} + \overline{m_{12}} + \overline{m_{15}}}$ and **1.5 marks**

f_2 = $\overline{m_6} + \overline{m_9}$ **1.5 marks**

For any other minimised expression one mark each.

The realisation is shown below:



2 Marks

2. Realise logic function F = ∑ (2, 3, 6, 7, 12, 13, 14, 15, 18, 19, 21, 23, 26, 27, 29, 31) using minimum number of two inputs 2:1 MUX.

ANS:
Karnaugh Map:

A = 0

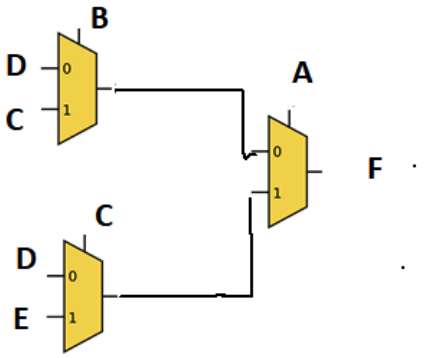
BC \ DE	00	01	11	10
00			1	1
01			1	1
11	1	1	1	1
10				

A = 1

BC \ DE	00	01	11	10
00			1	1
01			1	1
11			1	1
10			1	1

2 Mark

F = A [CE + C ' D] + A' [BC + B'D] By using Karnaugh map. The realization is shown below. **1 Mark**



2 Marks