INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY, DELHI

ECE111 DC

TUTORIAL 6 **(20 marks)**

Q1. A logic circuit implements the boolean function $F = \bar{X}.Y + X.\bar{Y}.\bar{Z}$. It is found that the input combination X = Y = 1 can never occur. Taking this into account, Find the simplified expression for F. (1.5 marks)

Q2. Simplify the given equation in part (i) and (ii):

(i) In terms of SOP and don't care conditions.

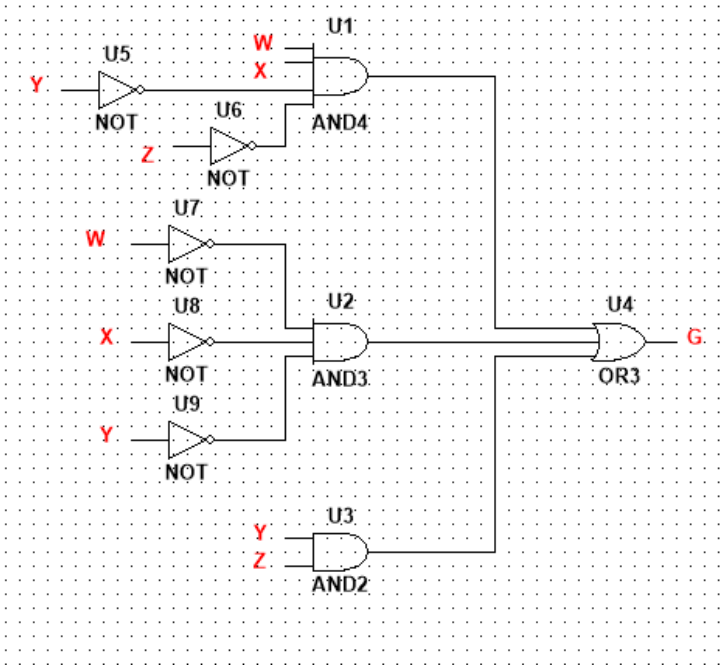
$$f(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$$ (1.5 marks)

(ii) In terms of POS and don't care conditions.

$$f(A,B,C,D) = \prod M(4,5,6,7,8,12).d(1,2,3,9,11,14)$$ (1.5 marks)

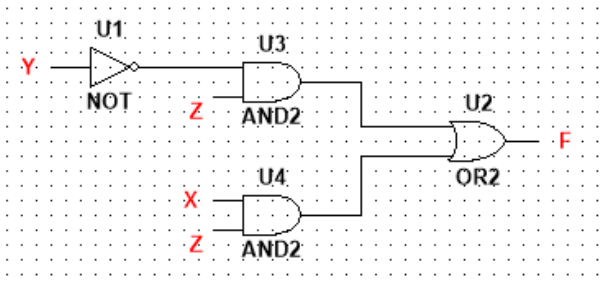
Q3.

i) Write the minterms of the circuit below.



(1.5 marks)

ii) Write the max terms of the circuit below.



(1.5 marks)

Q4. The even parity generator maintains the binary data in even number of 1's, for example, if the input data taken is in odd number of 1's, then even parity generator is going to maintain the data as even number of 1's by adding the extra 1 to the odd number of 1's. Whereas, odd parity generator will maintain the data as odd number of 1's by adding the extra 1 to the even number of 1's. Design a 4 bit odd and even parity generator. (Also show the Truth Table, KMAP).

(3 marks)

Q5) Implement f(A, B,C) = $\sum m(0,1,4,6,7)$ using 4×1 MUX. (2 marks)

Q6) Design a combinational circuit that accepts a 3-bit number as input and generates an output a 6-bit number of value equal to square of the input number. (3 marks)

Q7) Assuming that only X and Y logic inputs are available, and their complements X and Y are not available, then what is the minimum number of two-input NAND gates require to implement $X \oplus Y$? (2 marks)

Q8) The two number represented in signed 2`s complement form are, P = 11101101 and Q = 11100110. If Q is subtracted from P then find the value obtained in signed 2`s complement form.

(2.5 marks)