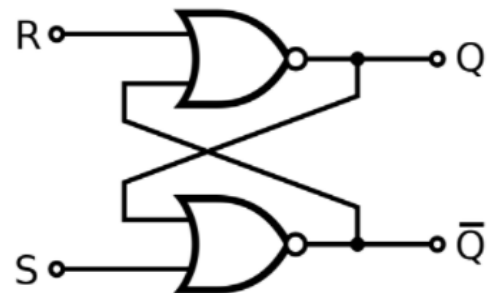
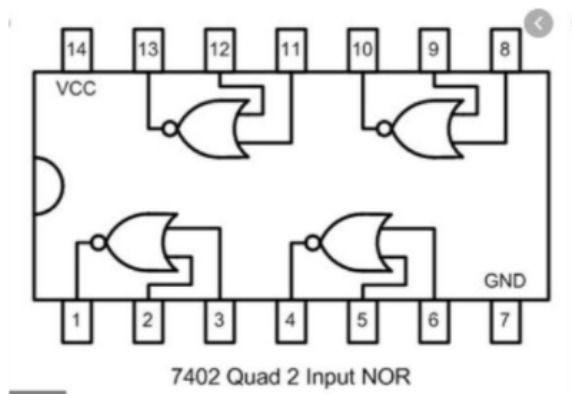


To be implemented on TinkerCad

## Latches

In this experiment, we will study about Latches. Latches have a feedback path and it can be a memory device. Latch can store one bit of data as long as the device is powered. It is an important element for sequential circuit design. Latches are asynchronous and do not operate on clocks, hence its state changes with the change in inputs. They can be implemented by cross-coupled NAND and NOR gates. All the ICs used in this experiment belong to the 74HCxx family.

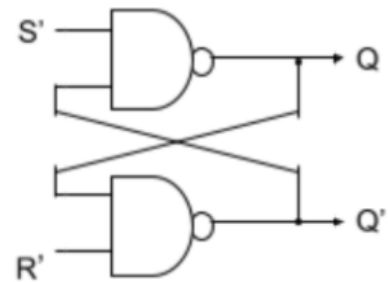
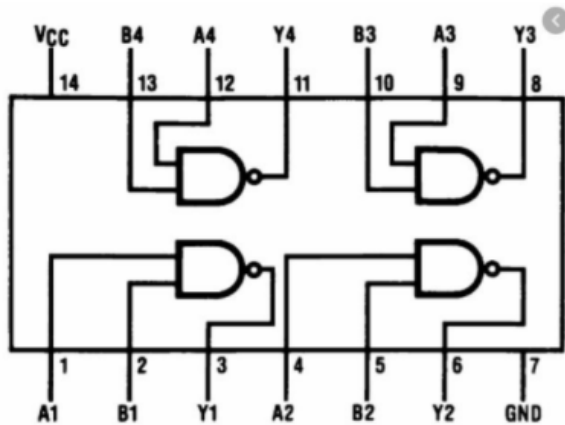
### A. NOR Latch



**Fig. NOR Latch using 74HC02 Quad 2- input NOR Gate**

1. Assemble a NOR latch using two NOR gates from the 74HC02 chip on TinkerCad, with the R and S inputs connected to two Input Switches and the Q and Q' outputs displayed on two LED Displays.
2. Observe and tabulate the sequence of Q and Q' in response to the following input sequence:  
S R = 01, 00, 10, 00, 01, 10, 01, 11, 00, 10, 11, 00.
3. Interpret the observed result and verify the latch operation.

## B. NAND Latch



**Fig. NAND Latch using 74HC00 Quad 2- input NAND**

Repeat the experiment with a NAND latch assembled using two gates in the 74HC00 chip, applying the following sequence of inputs through two Input switches:

$S' R' = 10, 11, 01, 11, 10, 01, 10, 00, 11, 01, 00, 11.$

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## **Deliverables & Rubrics (Total-10 marks)**

The TinkerCad link has to be shared with your lab TAs and your respective lab evaluator (mentioned on the shared sheet). Both A and B part to be made on the same workspace on different breadboards.

- 1) Aim
- 2) Components/ICs Used
- 3) Link of TINKERCAD Workspace (working project): 4 marks
- 4) Pin Diagram of the IC: 1 marks
- 5) Neat Circuit Diagram (Screenshot of TinkerCAD workspace): 0.5 marks
- 6) Characteristic equation, Characteristic Table and Excitation table : 1.5 marks
- 7) Observations/Results: 1 marks
- 8) Application(atleast two, with brief description of both): 2 marks

\*\*\*\*\*

## **Penalties**

- 1) TinkerCad link not accessible :- 0 grade
- 2) Faulty circuit :- 0 grade
- 3) Circuit is public :- 5 marks
- 4) Not labeled:- 2 marks

5) Late submission

- i) 0-10 min: No penalty
- ii) 10-30 min: 2 marks
- iii) More than 30 min: 5 marks

6) Plagiarized submission :- 0 grade

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