

ECE111: Digital Circuits

Practice Problem IX

1. Show how to build a J K Flip Flop using T FF with enable and combinational circuits.
2. Show how to build a SR latch using a single 7474 IC chip, which is positive edge triggered D FF and no other components.
3. Analyse the circuit shown in Fig. 1. Define the output Q1, Q2 and Output of OR gates for different input X = 0 or 1.

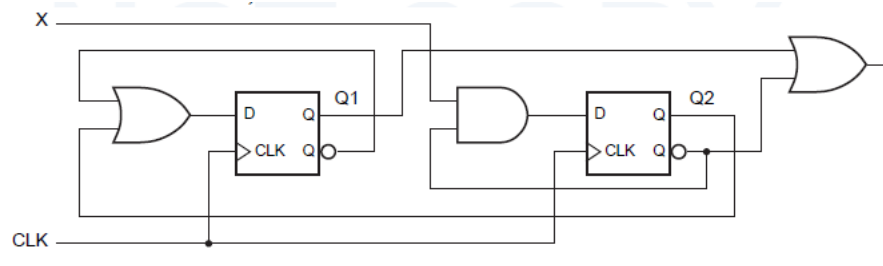


Figure 1

4. Compare the circuit shown in Fig. 2a with that of Fig. 2b. Show that both circuit functions identically.

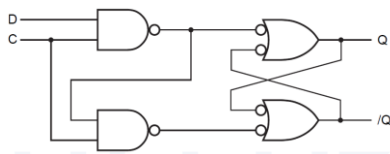


Figure 2a

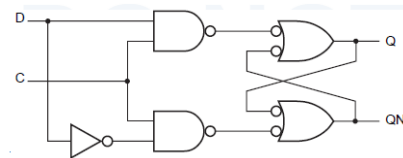


Figure 2b

5. An SR latch constructed from NAND gates is shown in Fig. 3. Determine the logic level at points a, b and c under the following conditions:
 - a. $S = R = Q = 0$.
 - b. As in (a) but S changes from 0 to 1.
 - c. $S = 0, R = 0$ and $Q = 1$ and R changes from 0 to 1.

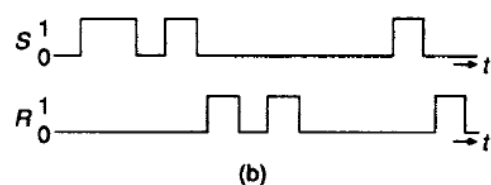
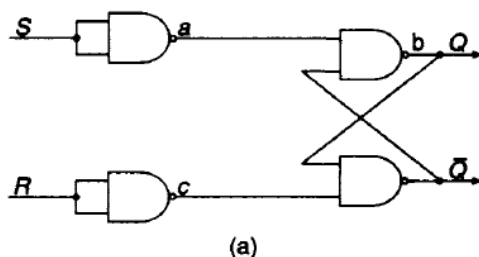
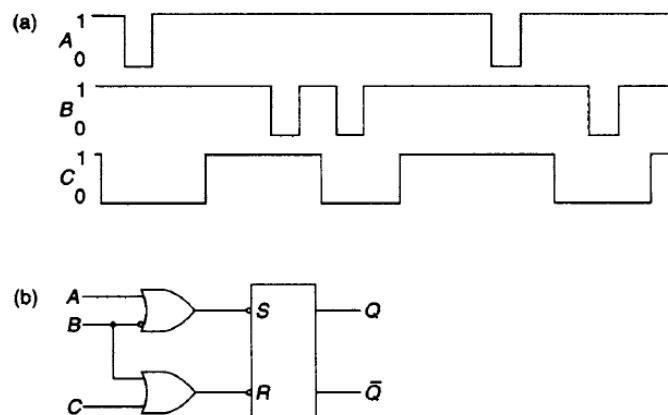


Figure 3

6. A Master/slave JK flip-flop is shown in Fig. 4. Assuming that, $J = K = Q_m = Q_s = 0$, trace the logic levels through the diagram for the following changes. (Assume that J and K changes during the positive clock period.)

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- The logic diagram shows a 4-bit shift register. It has three inputs: J , Ck (clock), and K . It has four outputs: Q_m , \bar{Q}_m , Q_s , and \bar{Q}_s . The circuit consists of eight 2-input AND gates and two inverters. The inputs J and K are connected to the first four AND gates (a, e, b, f) and the last two AND gates (g, h). The clock input Ck is connected to the first four AND gates (a, e, b, f). The outputs of the first four AND gates are a , b , c , and d . The outputs of the last two AND gates are g and h . The outputs Q_m and \bar{Q}_m are connected to the inputs of the last two AND gates (g, h). The outputs Q_s and \bar{Q}_s are connected to the inputs of the first four AND gates (a, e, b, f). The output of the first AND gate (a) is connected to the input of the second AND gate (b). The output of the second AND gate (b) is connected to the input of the third AND gate (c). The output of the third AND gate (c) is connected to the input of the fourth AND gate (d). The output of the fourth AND gate (d) is connected to the input of the fifth AND gate (e). The output of the fifth AND gate (e) is connected to the input of the sixth AND gate (f). The output of the sixth AND gate (f) is connected to the input of the seventh AND gate (g). The output of the seventh AND gate (g) is connected to the input of the eighth AND gate (h). The output of the eighth AND gate (h) is connected to the input of the first AND gate (a). The output of the first AND gate (a) is connected to the input of the second AND gate (b). The output of the second AND gate (b) is connected to the input of the third AND gate (c). The output of the third AND gate (c) is connected to the input of the fourth AND gate (d). The output of the fourth AND gate (d) is connected to the input of the fifth AND gate (e). The output of the fifth AND gate (e) is connected to the input of the sixth AND gate (f). The output of the sixth AND gate (f) is connected to the input of the seventh AND gate (g). The output of the seventh AND gate (g) is connected to the input of the eighth AND gate (h). The output of the eighth AND gate (h) is connected to the input of the first AND gate (a).

7. The waveform shown in Fig. 5a are to be applied to the circuit shown in Fig. 5b; assuming that the initial value of $Q = 0$, determine the Q output.



8. Given the S and R waveforms for an SR latch shown in Fig. 6 and assuming the initial value $Q = 0$, plot the time variations of Q output of the latch. How does the Q output vary if the latch is controlled by the G waveform?

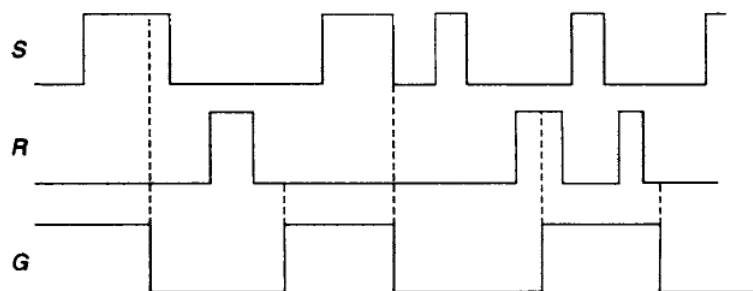


Figure 6

9. The circuit shown in Fig. 8 is a Flip Flop with X as input. Identify the flip flop type, i.e. S-R, J-K, D or T.

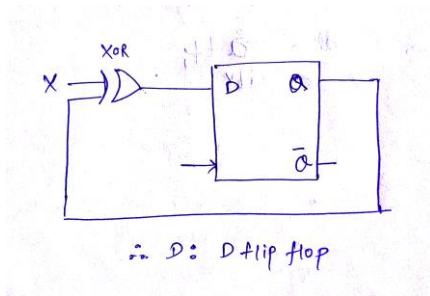


Figure 8

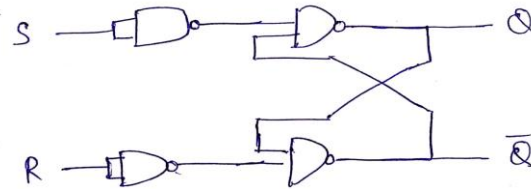


Figure 9

10. Derive the characteristic equation for T flip flop.
 11. Derive the relation between T, J&K and between T, S&R by using k-map.
 12. What combinational logic circuit (Fig. 10) is needed (In circular shape box) to generate sequence $(Q_1 Q_0) : 10, 00, 01, \dots$? The input to circular box Q_0 and Q_1 .

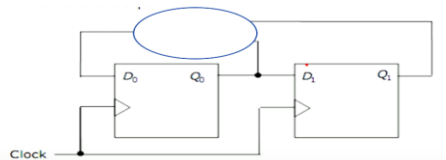


Figure 10

13. What would be the sequence $(Q_2 Q_1 Q_0)$ generated in Fig. 11? If Q_2 is the output of last FF and Q_0 is of first FF.

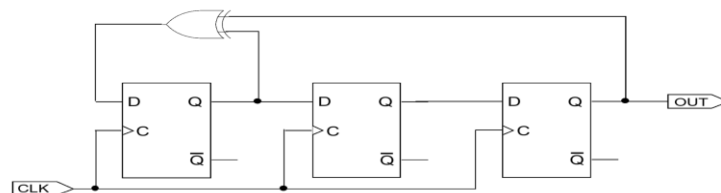


Figure 11