Q1. Find an equivalent expression with only one occurrence of A and one occurrence of $\bar{A}$ (Shannon's expansion) at most for the expression F = $A{\cdot}B + \bar{A}\cdot C + (A + D)\cdot E + (\bar{A} + F)\cdot G$

ANS:

$$F = A\cdot B + \bar{A}\cdot C + (A + D)\cdot E + (\bar{A} + F)\cdot G$$
$$= A\cdot B + A\cdot E + \bar{A}\cdot C + \bar{A}\cdot G + D\cdot E + F\cdot G$$
$$= A\cdot B + A\cdot E + \bar{A}\cdot C + \bar{A}\cdot G + A\cdot D\cdot E + \bar{A}\cdot D\cdot E + A\cdot F\cdot G + \bar{A}\cdot F\cdot G$$
$$= A\cdot (B + E + D\cdot E + F\cdot G) + \bar{A}\cdot (C + G + D\cdot E + F\cdot G)$$
$$= A\cdot (B + E + F\cdot G) + \bar{A}\cdot (C + G + D\cdot E)$$

---------- 4 Marks

You can give a maximum of 2 marks for partially correct answer. The TA in consultation with TF can decide whether to give 1 or 2.

Q2. An insurance company may issue Policy No. 22 only if the applicant

1. Has been issued Policy No. 19 and is a married male or
2. Has been issued Policy No. 19 and is married and under 25 or
3. Has not been issued Policy No. 19 and is a married female or
4. Is a male under 25 or
5. Is married and 25 or over.

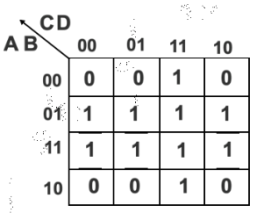
Give a logic expression to describe the condition for the issuance of the premium.

ANS:

Let A = Applicant has been issued Policy No. 19
B = Applicant is married
C = Applicant is male
D = Applicant is under 25

Policy N0. 22 may be issued only if following statements are TRUE:

1. ABC
2. ABD
3. $\bar{A}B\bar{C}$
4. CD
5. $B\bar{D}$



6. **F = ABC + ABD + $\bar{A}B\bar{C}$ + CD + B$\bar{D}$ is TRUE.**
   $F = B + CD$. **Minimized form is not needed in the solution as it has not been asked for in the question.**

Policy No. 22 may be issued if the applicant

1. Is married OR
2. Is a male under 25.

Since minimization was not asked for you can give 8 marks for the expressions shown in purple. The student loses 2 marks for each error. If only one term or none is correct, the student gets a zero for this question.

Q3. Express $F = A \cdot (B + \bar{C}) + D$ as:

(a) minimum sum of products.
(b) minimum product of sums.
(c) canonical sum of products.
(d) canonical product of sums.

ANS:

a. Minimum sum of products

F = AB+AC'+D

b. Minimum product of sums

Taking complement of F, we get

F' = ($\bar{A}$+$\bar{B}$)($\bar{A}$+C) $\bar{D}$
= $\bar{A}\bar{D}$+$\bar{A}$C$\bar{D}$+$\bar{A}\bar{B}\bar{D}$+$\bar{A}$C$\bar{D}$

Taking compliment of F', we obtain

F = (A+D) (A+$\bar{C}$+D) (A+B+D) (B+$\bar{C}$+D)
= (A+D) (B+$\bar{C}$+D)

c. Canonical sum of products

F = ABCD + ABC$\bar{D}$ + AB$\bar{C}\bar{D}$ + AB$\bar{C}$D + A$\bar{B}\bar{C}\bar{D}$ + $\bar{A}\bar{B}\bar{C}D$ + $\bar{A}\bar{B}$CD + $\bar{A}$B$\bar{C}$D + $\bar{A}$BCD + A$\bar{B}$CD + A$\bar{B}\bar{C}D$

d. Canonical product of sums

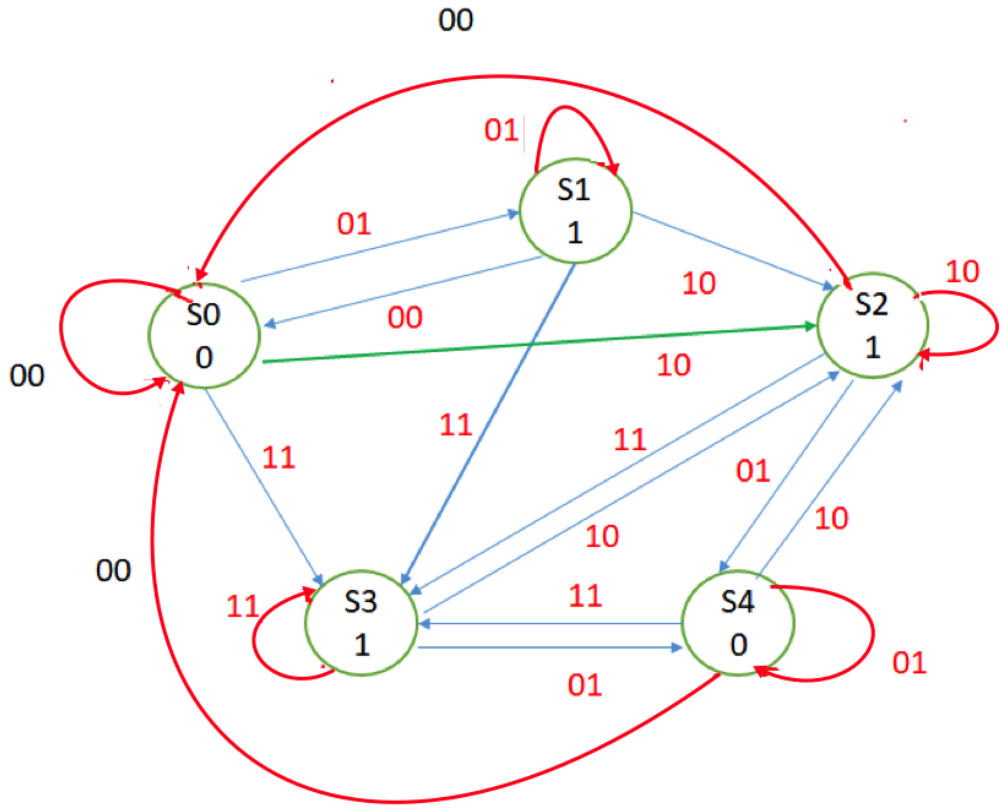
F = (A+B+C+D). (A+$\bar{B}$ + $\bar{C}$+D). (A+$\bar{B}$+C+D). (A+B+$\bar{C}$+D). ($\bar{A}$+B+$\bar{C}$+D).

Give 2 marks for each correct answer. No partial marking.

Q4. A sequential circuit is to have two inputs, x_1 and x_2, and one output, Z. The inputs represent, in binary, the numbers 0 to 3. If a change in input increases the represented number, the output is to turn on, if not already on. If a change in input decreases the represented number, the output is to turn off, if not already off. All input changes are possible except that both inputs will never change simultaneously. Draw the state diagram and then give the state transition table.

ANS:

We start with State S_0. The state transition diagram is shown in following figure:



Since there are five states, we require 3 flip-flops to design the circuit.
Let $S_0 = 000$, $S_1 = 001$, $S_2 = 010$, $S_3 = 011$, $S_4 = 100$
(There could be other alternate assignments as well.)
State transition table can be derived from state transition diagram as below.

Clock	Present State	Next State			
		x_1x_2 =00	01	11	10
1	S_0	S_0	S_1	S_3	S_2
2	S_1	S_0	S_1	S_3	S_2
3	S_2	S_0	S_4	S_3	S_2
4	S_3	-	S_4	S_3	S_2
5	S_4	S_0	S_4	S_3	S_2

Give 2 marks each foreach set of correct links at each state (a total of 10 marks for 5 states)
Give 1 mark each for correct row entry and give 6 if all rows are correct.

Q5. Design a counter to count in the sequence using TFFs, ensure that the counter does not get stuck in any illegal state.

The count sequence required is $001 \rightarrow 100 \rightarrow 010 \rightarrow 101 \rightarrow 110 \rightarrow 011 \rightarrow 001$,

CLOCK	PRESENT STATE	NEXT STATE			
	$Q_{An-1}\ Q_{Bn-1}\ Q_{Cn-1}$	$Q_{An}\ Q_{Bn}\ Q_{Cn}$	T_A	T_B	T_C
1	001	100	1	0	1
2	100	010	1	1	0
3	010	101	1	1	1
4	101	110	0	1	1
5	110	011	1	0	1
6	011	001	0	1	0
	000	001	0	0	1
	111	001	1	1	0

$Q_A\ Q_B$ \ Q_C	0	1
00	0	1
01	1	0
11	1	1
10	1	0

$$T_A = Q_B\overline{Q_C} + Q_A\overline{Q_C} + Q_AQ_B + \overline{Q_A}\ \overline{Q_B}\ Q_C$$

$Q_A\ Q_B$ \ Q_C	0	1
00	0	0
01	1	1
11	0	1
10	1	1

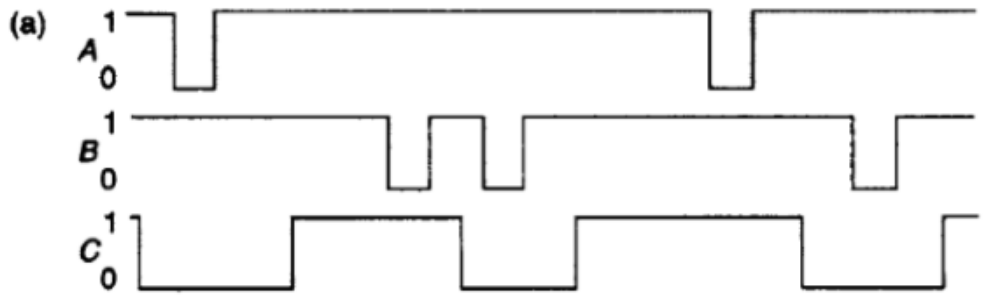
$$T_B = Q_BQ_C + Q_A\overline{Q_B} + \overline{Q_A}\ Q_B$$

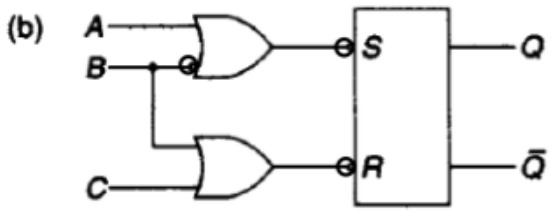
$Q_A\ Q_B$ \ Q_C	0	1
00	1	1
01	1	0
11	1	0
10	0	1

$$T_C = Q_B\overline{Q_C} + \overline{Q_B}Q_C + \overline{Q_A}\ \overline{Q_B}$$

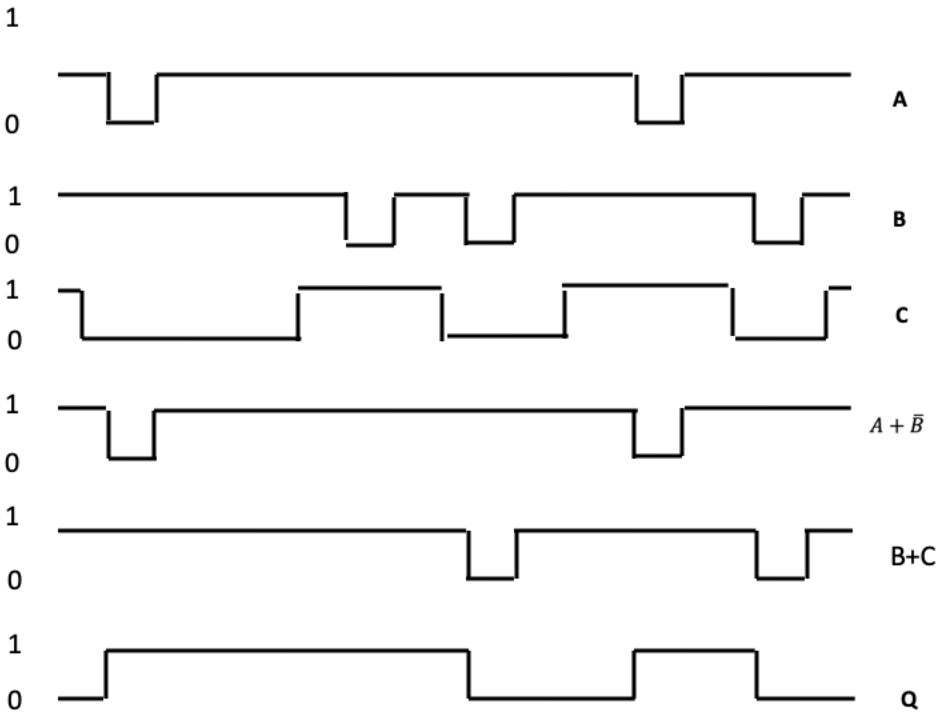
Give 4 marks for the STT with a legal transition from the illegal state (111). If the illegal state is not considered give only 2 marks.
For each correct value of Ts give 4 marks. If the student has used any landing state from 111 other than 001, check for the correctness and evaluate.
If the student does not consider the illegal state no marks to be awarded for evaluation of Ts.

Q6. The waveforms shown in Fig. 7(a) are applied to the circuit in Fig. 7(b); assuming initial value Q=0 plot the output.





ANS:



Give 5 marks each for the correct wave form for the three wave forms and additional 1 if all the three are correct.

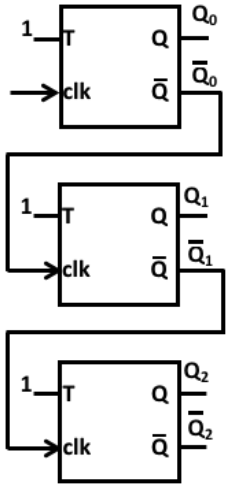
Q7. Design a counter with minimum number of flip-flops to give an output sequence, a binary equivalent of first 8 prime numbers. 1 is not counted as a prime number. The first prime number is decimal number 2.

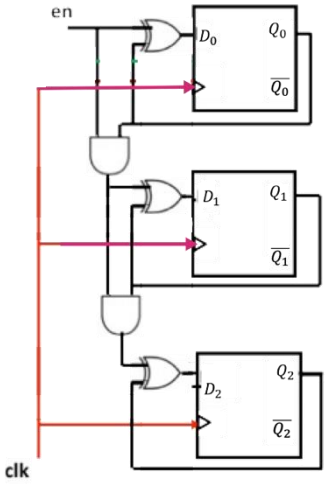
ANS:

First eight prime numbers are following:

2, 3, 5, 7, 11, 13, 17,19

Since there are eight numbers, so modulo 8 counter or 3-bit up counter will be needed, which will require 3 FFs.





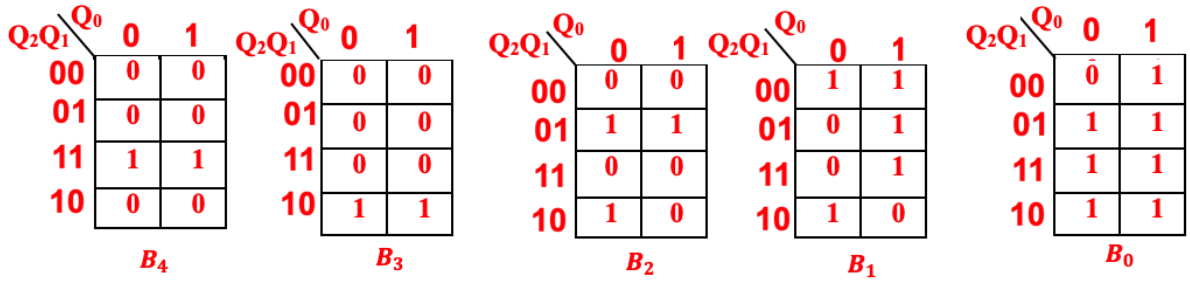
Award 2 marks for identifying that the minimum FFs needed is 3.

Award 4 marks for any correct 3-bit counter design. I have given one each of asynchronous and synchronous design. There are other designs available and if the design presented by the student is correct allot him 4 marks.

In order to get the required output, we will require 5 bits output.

P. STATE $Q_2Q_1Q_0$	N. STATE $Q_2Q_1Q_0$	PRESENT STATE OUTPUTS (MOORE)					
		B_4	B_3	B_2	B_1	B_0	
0 0 0	**0 0 1**	**0**	**0**	**0**	**1**	**1**	**3**
0 0 1	**0 1 0**	**0**	**0**	**1**	**0**	**1**	**5**
0 1 0	**0 1 1**	**0**	**0**	**1**	**1**	**1**	**7**
0 1 1	**1 0 0**	**0**	**1**	**0**	**1**	**1**	**11**
1 0 0	**1 0 1**	**0**	**1**	**1**	**0**	**1**	**13**
1 0 1	**1 1 0**	**1**	**0**	**0**	**0**	**1**	**17**
1 1 0	**1 1 1**	**1**	**0**	**0**	**1**	**1**	**19**
1 1 1	**0 0 0**	**0**	**0**	**0**	**1**	**0**	**2**

The circuit will be a 3 bit binary counter followed by the decoding circuits defining the outputs B_4 B_3 B_2 B_1 B_0.

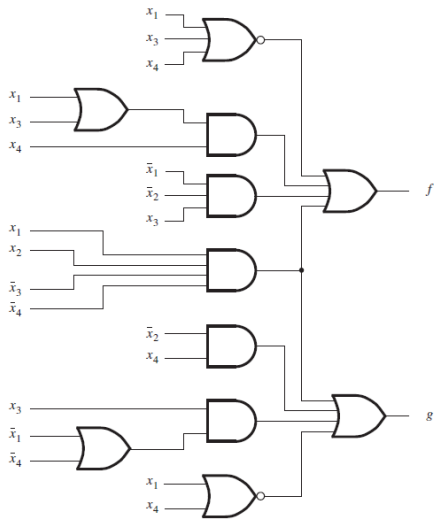


$B_4 = Q_2Q_1$; $B_3 = Q_2\overline{Q_1}$; $B_2 = \overline{Q_2}Q_1 + Q_2\overline{Q_1}\,\overline{Q_0}$; $B_1 = \overline{Q_2}\,\overline{Q_1} + Q_1Q_0 + Q_2\overline{Q_1}\,\overline{Q_0}$; $B_0 = Q_2 + Q_1 + Q_0$

Allot 10 marks for the correct expression for the 5 bits at the output. Give extra 2 marks for those who give the gate realization also. (These 2 marks is a bonus)

For those who have designed a 5 bit counter to generate the required sequence, award them 4 marks for effort.

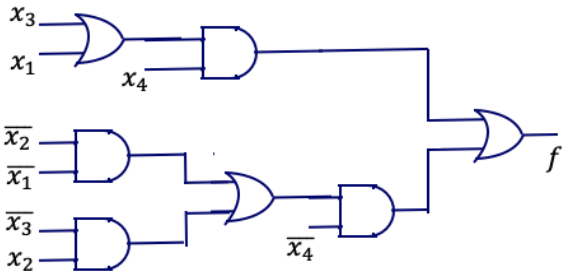
Q8. Consider the circuit in figure below, which implements functions f and g. Redesign the circuit to implement the same functions, but with minimum number of 2-input gates. Assume that variable and its complement are available.



ANS:

From the circuit given: $f = \overline{x_4}\,\overline{x_3}\,\overline{x_1} + (x_1 + x_3)\cdot x_4 + \overline{x_1}\,\overline{x_2}\,x_3 + x_1x_2\overline{x_3}\,\overline{x_4}$

x_4x_3 \ x_2x_1	00	01	11	10
00	1	0	1	1
01	1	0	0	0
11	1	1	1	1
10	0	1	1	0



$f = x_4x_3 + x_4x_1 + \overline{x_4}\,\overline{x_2}\,\overline{x_1} + \overline{x_4}\,\overline{x_3}x_2$

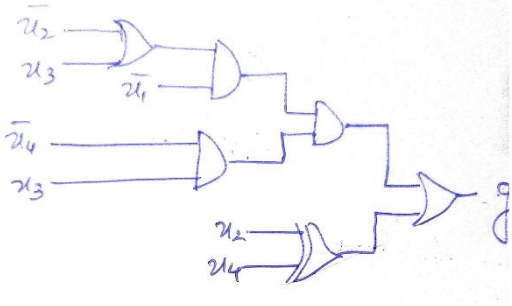
$= x_4\cdot(x_3 + x_1) + \overline{x_4}\cdot(\overline{x_2}\,\overline{x_1} + \overline{x_3}x_2)$

$g = x_1x_2\overline{x_3}\,\overline{x_4} + x_4\overline{x_2} + (\overline{x_4} + \overline{x_1})\cdot x_3 + \overline{x_4}\,\overline{x_1}$

$g = \overline{x_2}\,\overline{x_1} + \overline{x_4}x_3 + \overline{x_4}x_2 + x_4\overline{x_2} + x_3\overline{x_1}$

$= \overline{x_1}\cdot(\overline{x_2} + x_3) + \overline{x_4}x_3 + x_2 \oplus x_4$ or $= \overline{x_2}\cdot(\overline{x_1} + x_4) + \overline{x_4}\cdot(x_3 + x_2) + \overline{x_1}x_3$

x_4x_3 \ x_2x_1	00	01	11	10
00	1	0	1	1
01	1	1	1	1
11	1	1	0	1
10	1	1	0	0



Give 2 marks each for getting the original expressions for f and g. Give 3 marks each for getting the reduced expression for f and g. If in the case of f they only get the first expression below the K-map, still give 3 marks. Give 3 marks each for realizing with minimum gates for f and g. There are two reduced expression given for f, realizing the first expression gets no marks and realizing the second expression gets 3 marks.