QUIZ 6 Solution

ECE 111 DIGITAL CIRCUITS

1. Draw the output of gates A, B, C, D, E AND F for both LOW to HIGH and HIGH to LOW transitions of IN taking into account the propagation delays for the circuit shown on Fig, 1 with all labels. Determine the exact maximum propagation delay from IN to OUT using the timing information given in Table 1. What will be typical propagation delay for LOW to HIGH transition of IN.

Table 1

Part No,	Typical (ns)		Maximum (ns)	
	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
74LS00	9	10	12	15

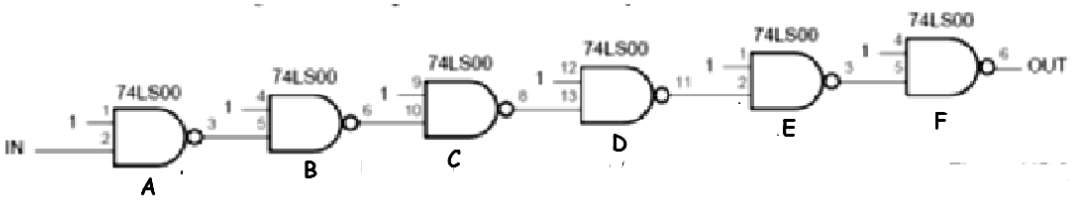
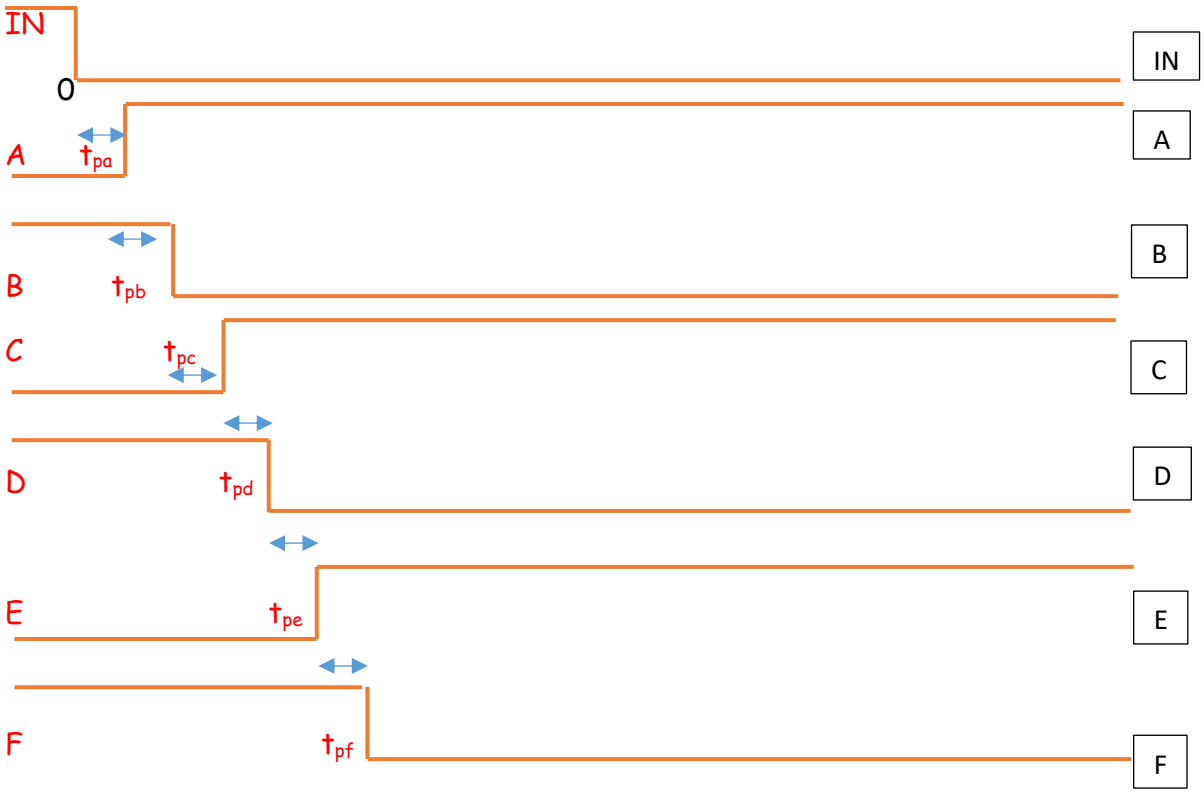


Fig. 1

Solution:

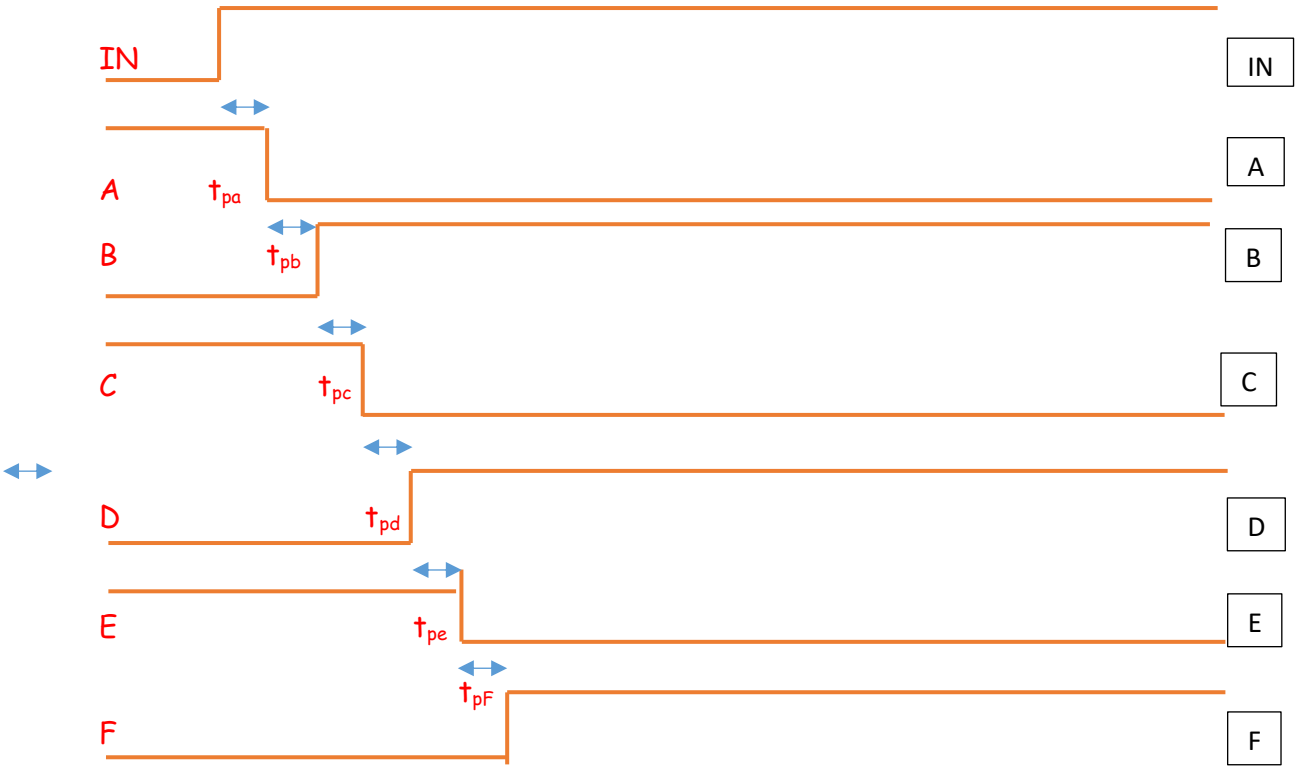
The output waveforms are shown below for HIGH to LOW transition at input:



Maximum Propagation Delay = tpamax+ tpbmax+ tpcmax+ tpdmax+ tpemax+ tpfmax

= (12+15+12+15+12+15) ns = 81 ns

For LOW to HIGH IN, the outputs will be following:



Maximum Propagation Delay = tpamax+ tpbmax+ tpcmax+ tpdmax+ tpemax+ tpfmax

= (15+12+15+12+15+12) ns = 81 ns

Typical propagation delay = 9+10+9+10+9+10 = 57 ns

Correct Wave forms with all details = 3.5 Marks

Waveforms with no details 1.5 marks each

Correct Delay calculation 0.5 marks each = 1.5 Marks

2. For the counter shown in Fig. 2, define the counting sequence and then identify the type of counter.

   Is it a synchronous or asynchronous counter? Give reason for your answer.

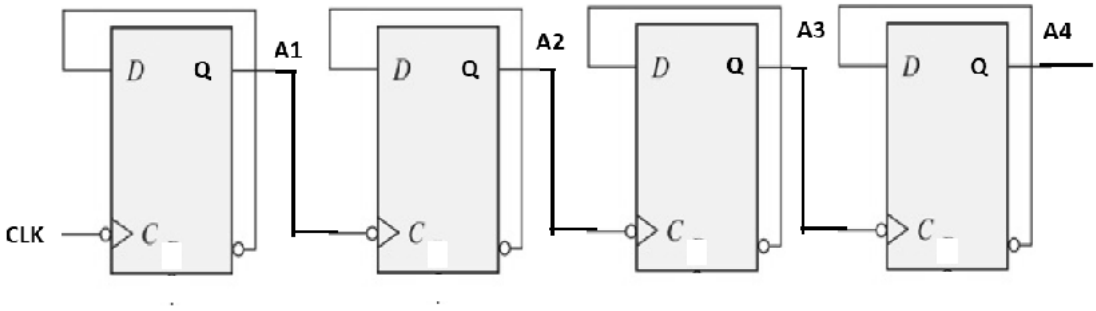


Fig. 2

Solution:

Let us assume that initially A1A2A3A4 is 0100. The counting sequence would be following:

Clock	A1	A2	A3	A4
0	0	1	0	0
1	1	1	0	0
2	0	0	1	0
3	1	0	1	0
4	0	1	1	0
5	1	1	1	0
6	0	0	0	1
7	1	0	0	1
8	0	1	0	1
9	1	1	0	1
10	0	0	1	1
11	1	0	1	1
12	0	1	1	1
13	1	1	1	1
14	0	0	0	0
15	1	0	0	0
16	0	1	0	0
17	1	1	0	0

We find that the sequence repeats after 16 counts. 3 MARKS

This a 4 bit Binary Ripple up counter. 1 MARKS

This is ASYNCHRONOUS COUNTER because all FFs are not driven by same CLOCK signal.

1 MARKS

[Note: Students can start with any initial value, but the order of sequence will be same]

ALTERNATIVE SOLUTION

The following answer should also be acceptable.

Let us assume that initially A1A2A3A4 is 0100. The counting sequence would be following:

Clock	A1	A2	A3	A4
0	0	1	0	0
1	1	1	0	0
2	0	0	1	0
3	1	0	1	0
4	0	1	1	0
5	1	1	1	0
6	0	0	0	1
7	1	0	0	1
8	0	1	0	1
9	1	1	0	1
10	0	0	1	1
11	1	0	1	1
12	0	1	1	1
13	1	1	1	1
14	0	0	0	0
15	1	0	0	0
16	0	1	0	0
17	1	1	0	0

We find that the sequence repeats after 16 counts. 3 MARKS

Each DFF has been connected as a TFF and the Q output of each TFF is connected to the clk input of the next TFF, hence it is an Asynchronous 4-bit binary counter.

1 MARKS

Since Q feeds the clock of negative edge triggered TFF, it is a 4-bit up counter. The counting sequence, with A_4 as MSB, is (we should accept even if MSB is not identified as it is the LSB which gets the clock input.)

$$0000 \rightarrow 0001 \rightarrow 0010 \rightarrow 0011 \rightarrow 0100 \rightarrow 0101 \rightarrow 0110 \rightarrow 0111 \rightarrow 1000$$

$$\rightarrow 1001 \rightarrow 1010 \rightarrow 1011 \rightarrow 1100 \rightarrow 1101 \rightarrow 1110 \rightarrow 1111 \rightarrow 0000$$

1 MARKS