Digital Circuits(ECE111)

Experiment 3 **Winter 2022**

Digital Multiplexer Design Using Basic Gates

Aim:-

In this experiment, we will design 2x1, 4x1 and 8x1 Multiplexers having Enable pin, using basic logic gates in TinkerCad and test its performance for various conditions.

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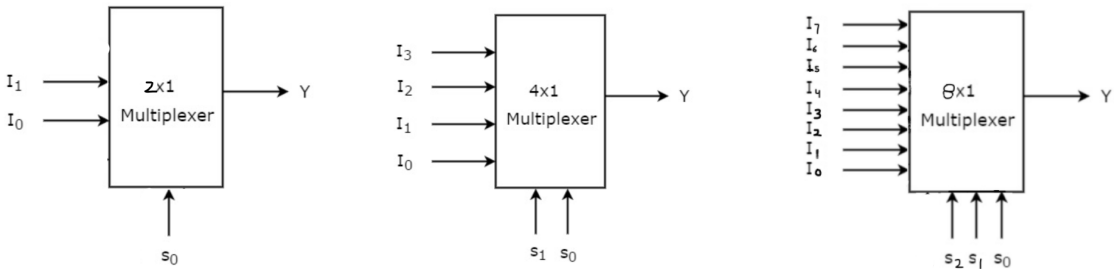
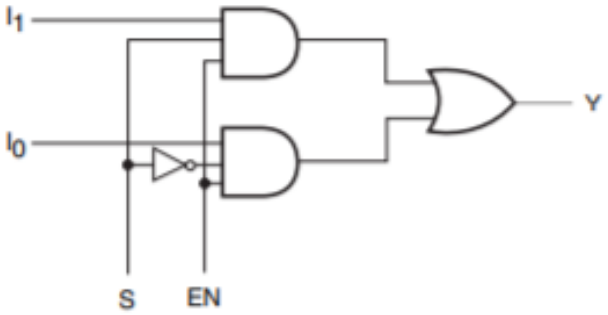
There are different types of multiplexers: 2x1, 4x1, 8x1, where 2, 4, 8 denotes the number of inputs and 1 denotes the output.

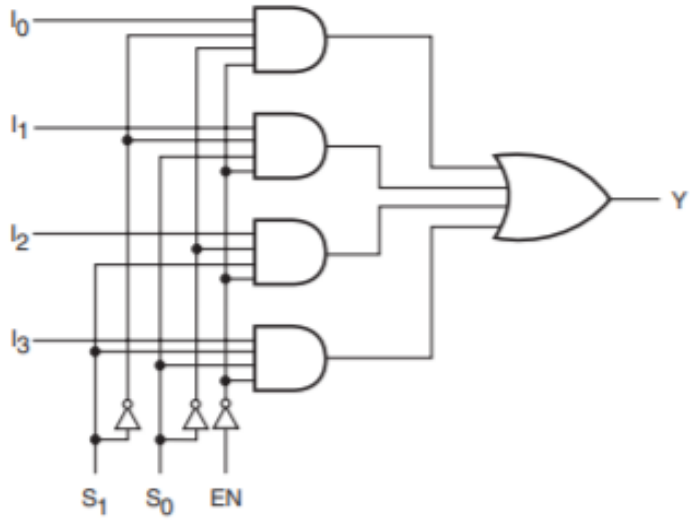


<u>Part A:</u> 2x1 MUX



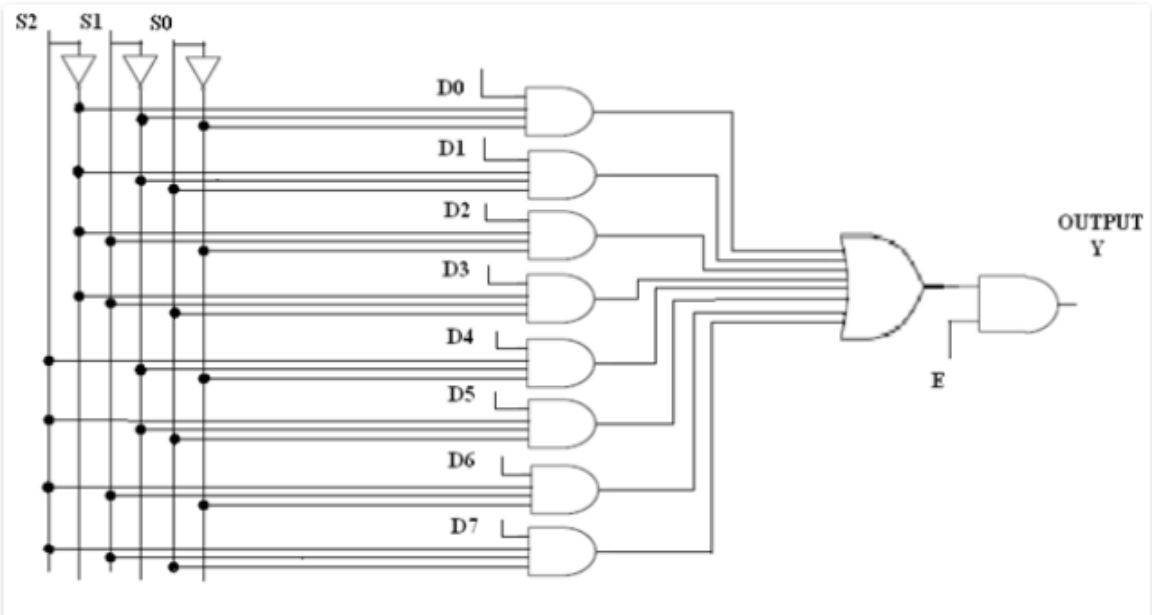
S	EN	Y
X	0	0
0	1	I_0
1	1	I_1

Part B: **4x1 MUX**



S_1	S_0	EN	Y
X	X	1	0
0	0	0	I_0
0	1	0	I_1
1	0	0	I_2
1	1	0	I_3

Part C: **8x1 MUX**



Select Data Inputs				Output
S_2	S_1	S_0	E	Y
X	X	X	0	0
0	0	0	1	D_0
0	0	1	1	D_1
0	1	0	1	D_2
0	1	1	1	D_3
1	0	0	1	D_4
1	0	1	1	D_5
1	1	0	1	D_6
1	1	1	1	D_7

Part D: Problem Statement

A pound lock is used to raise and lower boats on rivers and canals. They consist of a pair of gates creating a chamber (lock) in which the water level is varied using valves.

To go upstream, the boat enters the drained lock through the bottom gate and the gate is closed behind it. The lock is then filled with water by opening the filling valve. Once full, the top gate is opened and the boat leaves.

To go downstream, the boat enters the filled lock through the top gate and the gate is closed behind it. The lock is then drained by opening the drain valve. Once drained, the bottom gate is opened and the boat leaves.

In both cases, the gates are controlled manually by a single lever. When the lever is not pulled, both gates should be closed. When pulled, it must open only the correct gate for the current water level. Hence, the top gate must only

open if the lock is full, and the bottom gate must only open if the lock is drained.

Design the logic circuit required for the lock controller, modelling the gate lever, valve control and gates as follows:

→ Gate lever(input J):

0 – Closes both gates

1 – Opens one gate depending on water level

→ Valve control (input K):

0 – Lock drained (drain valve open)

1 – Lock filled (filler valve open)

→ Gates: 0 – Gate closed

(outputs X (bottom) and Y (top)) 1 – Gate opened

Deliverables & Rubrics (Total-10 marks)

Deliverables-

1) Aim
2) Components/ICs Used
3) Link of TINKERCAD Workspace (working project): 1 mark
4) Pin Diagram of the IC: 1.5 marks
5) Neat Circuit Diagram (Screenshot of TinkerCAD workspace): 2 marks
6) Truth Table: 1.5 marks
7) Observations/Results: 1 marks
8) Application: 1 marks (Applications of Multiplexers)
9) Problem statement solution, circuit implementation(design screenshot): 2 marks

Note- Keep the Aim(point 1) common, followed by point 2-7 for each part then a common application(point 8) and at last the Problem statement(point 9).

Penalties:- (-ve marking)

1) Circuit not working 0 grade
2) Plag case 0 grade
2) Late submission

0-10 min: no penalty
10-30 min: 2 marks
More than 30 min: 5 marks

3) Crosswires or wire crossing a component 2 marks
4) Component out of the board: 1 mark/component
5) Unnecessary use of a component or wires: 1 mark/component