INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

QUIZ 6

ECE 111 DIGITAL CIRCUITS

Date: 4th April, 2022 Time: 6:30 – 7:00 PM. Max. Marks: 10

ANSWER ALL QUESTIONS

1. Draw the output of gates A, B, C, D, E AND F for both LOW to HIGH and HIGH to LOW transitions of IN taking into account the propagation delays for the circuit shown on Fig, 1 with all labels. Determine the exact maximum propagation delay from IN to OUT using the timing information given in Table 1. What will be typical propagation delay for LOW to HIGH transition of IN.

Table 1

Part No,	Typical (ns)		Maximum (ns)	
	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
74LS00	9	10	12	15

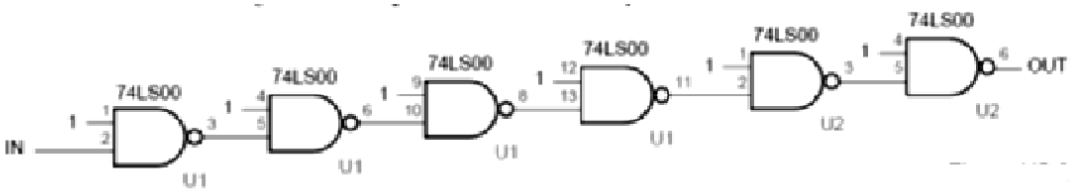

Fig. 1

2. For the counter shown in Fig. 2, define the counting sequence and then identify the type of counter.

   Is it a synchronous or asynchronous counter? Give reason for your answer.

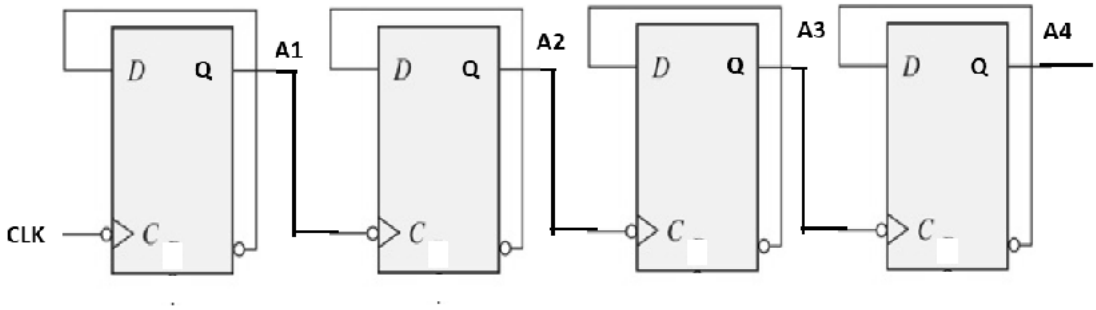

Fig. 2