INDRAPRASTHA INSTITUTE OF INFORMATION TECHNOLOGY DELHI

QUIZ 4

ECE 111 DIGITAL CIRCUITS

Date: March 21, 2022 Time: 8:00 – 8:20 PM. Max. Marks: 10

ANSWER ALL QUESTIONS

1. Sketch the output of an SR latch shown in Fig. 1 for the input waveform shown in Fig. 1b. Assume that the input and output rise and fall times are zero and propagation delay of NOR gate is 10 ns, and each time division shown in Fig. 1b is 10 ns.

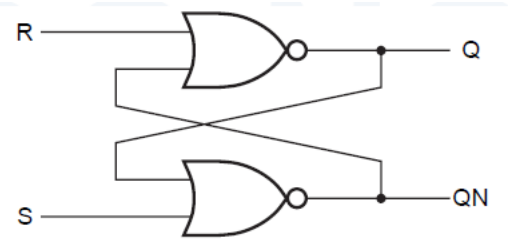

Figure 1a

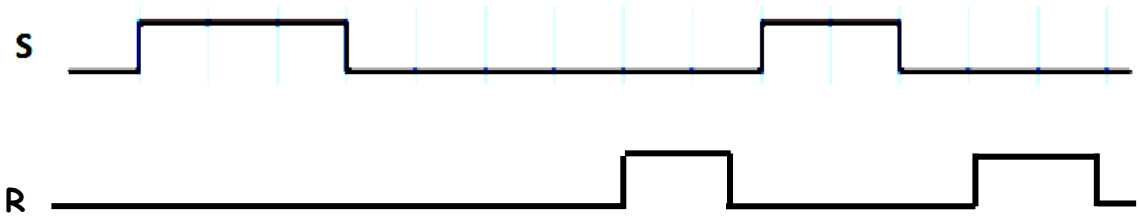

Figure 1b

2. Figures 2a and 2b shows two different types of Latches. Identify the Flip Flop by defining the characteristics tables. A and B are inputs and Q is output. Give the logical expression for present output Q in terms of inputs and the previous output.

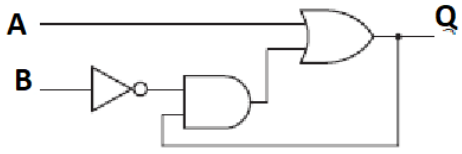

Figure 2a

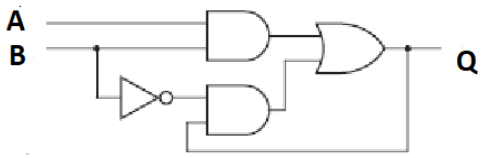

Figure 2b