Computer Organization & Assembly Language

Final Exam – 2009/1/14

Dept. of Engineering Science, National Cheng Kung University

1. [General Questions]

Answer *True* or *False* to the following statements. (36%)

F (A) The performance of an antilock brake system can be evaluated in terms of the real-time constraint.

F (B) CPU time includes the time spent for computing and time spent waiting for I/O.

T (C) Benchmarks are programs specifically chosen to measure performance of a computer.

(D) When designing the processor, the control signals RegRead and RegWrite are used for controlling the data access of register files.

(E) In the single-cycle design, all control signals except the PCSrc can be set based on the contents of the instruction to be executed.

F (F) In the multicycle design, more clock cycles are needed for executing a store word instruction than an R-type instruction.

(G) Designing the control is more complicated than designing the datapath since it requires an understanding of how all the components in the processor operate.

(H) In an instruction set like the 80x86, where instructions are not of the same length, pipelining is considerably easier.

(I) The CPI value of an ideal pipeline processor is the same as that of a single-cycle processor.

(J) Pipelining increases throughput and reduces individual instruction execution time.

(K) Pipeline bubbles cause loss of performance since that a number of pipeline stages are left empty.

(L) Data forwarding can help reducing the possible delay in data hazards.

2. [Performance]

Assume that Machine A's clock rate is 500MHz and Machine B's clock rate is 400MHz. Both machines have three classes of instructions. The cycle counts per instruction for the three classes are as follows:

	Machine A	Machine B
Class X	4	2
Class Y	3	4
Class Z	2	1

Two programs of interest that will be run on these machines require the following number of instructions (in billions, i.e., 10^9) for each instruction class:

	Program 1	Program 2
Class X	1	1
Class Y	2	2
Class Z	5	10

(A) Which program is faster on Machine A? Please calculate the average CPI for both programs. (6%)

(B) Which program is with a higher MIPS (million instructions per second) on Machine A? (4%)

(C) How much faster (or slower) is Machine A compared to Machine B if two programs were run successively on these two machines? (4%)

3. **[Single-Cycle & Multicycle Processors - I]**

(A) How many clock cycles does it take for the following codes to be executed on a single-cycle machine? and on a multicycle machine (according to our design)? (6%)

```
sub     $3, $4, $5
lw      $4, 10($6)
add     $7, $3, $4
sw      $7, 20($6)
add     $7, $2, $1
```

(B) Suppose that the function unit times are given as follows: (1 ns = 10^{-9} seconds)

2 ns for memory access,

1 ns for ALU operation, and

0.5 ns for register file read or write.

What is the desirable clock rate for the single-cycle machine and the multicycle machine, respectively? (6%)

What is the execution time for running the code in (A) on the single-cycle and the multicycle machine, respectively? (6%)

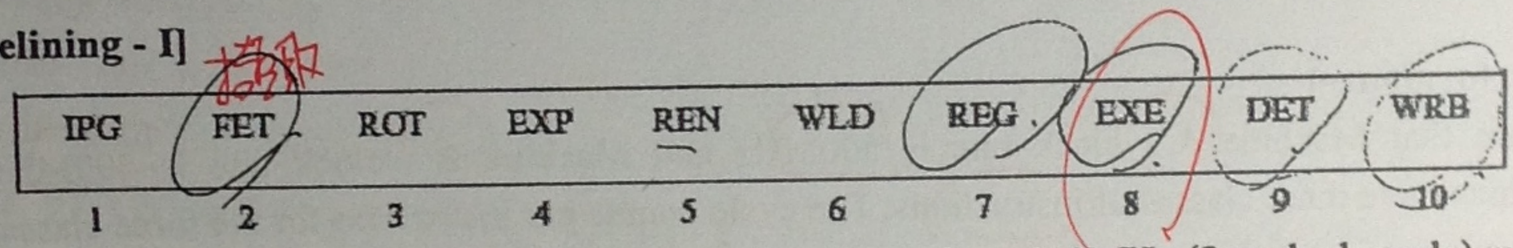
4. **[Single-Cycle & Multicycle Processors - II]**

An instruction set is composed of h different instruction classes, with the execution time of class-i instruction being $4+2i$ ns, $1 \le i \le h$. Consider a multi-cycle control implementation with a clock cycle of 2 ns and assume that class-i instructions can then be executed in $2+i$ clock cycles.

(A) Derive the performance advantage (speedup factor) of the multi-cycle machine relative to the single-cycle one, assuming that all instruction classes are used with the same frequency. (8%)

(B) Is any speedup factor possible for a suitably large h? Why or why not? (4%)

5. **[Pipelining - I]**



One CPU manufacturer proposed the 10-stage pipeline above for a 500MHz (2ns clock cycle) machine. Here are the correspondences between this and the MIPS pipeline:

- Instructions are fetched in the FET stage.
- Register reading is performed in the REG stage.
- ALU operations and memory access are both done in the EXE stage.
- Branches are resolved in the DET stage.
- WRB is the writeback stage.

(A) How much time is required to execute one million instructions on this processor, assuming there are no dependencies or branches in the code? (3%)

(B) Without forwarding, how many stall cycles are needed for the following codes? Assume that the register file could be written and read in the same clock cycle. (3%)

What is this data hazard called? (3%)

```
lw   $t0, 0($a0)
add  $v1, $t0, $t0
```

(C) If a branch is mispredicted, how many instructions should be flushed from the pipeline? (3%)

6. **[Pipelining - II]**

Explain why the pipelined design is with advantages of both the single-cycle and the multicycle designs. Justify your answers in terms of the CPI and the clock cycle time. (8%)