

2015/11/03

104 學年度第一學期

計算機概論 第一次期中考 詳解

I. (According to the Von Neumann architecture, Textbook: P.117)

1. Fetch instruction
2. Decode
3. Get data from Memory or put data into Register
4. Execute
5. Input / Output

(Need to describe them)

II.

1. (According to the Von Neumann architecture, Textbook: P.116, cpphtp7LOV_ch01 Introduction to Computers.ppt: P.7)
 - (a) ALU (Arithmetic and logic unit)
 - (b) CPU (Central processing unit)
 - (c) memory (or memory unit, main memory, primary memory)
 - (d) output (or output device)
 - (e) auxiliary storage device (or Secondary storage unit)
2.
 - (a) assembly language
 - (b) high-level language
3. (According to cpphtp7LOV_ch01 Introduction to Computers.ppt: P.16)
 - (a) compiler
 - (b) interpreter
4. Bits
5. OR
6. gate (Textbook: P.107)
7. bus (Textbook: P.117)
8. register (Textbook: P.116)
9. protocol (Textbook: P.144)
10. (ISO) OSI (Textbook: P.147)
11. ring (or loop, Textbook: P.150)
12. WAN (Textbook: P.149)

13. IP (Textbook: P.174)
14. router

III.

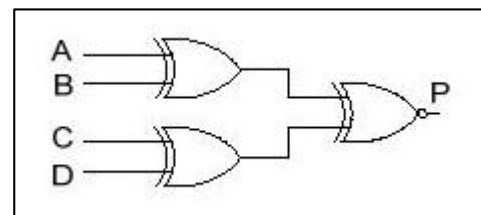
1. F (Integrated circuits are made of transistor)
2. T (Textbook: P.100)
3. T
4. F (It is, Textbook: P.116)
5. F (ROM does, Textbook: P.119)
6. T (Textbook: P.120)
7. F (weaken, Textbook: P.140)
8. T (Textbook: P.147)
9. T (Textbook: P.172)
10. F (IP is, Textbook: P.174)

IV.

X	Y	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

V. 4-bit ODD-parity generator

A	B	C	D	Odd Parity Bit (F)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



VI. Mux

s_1	s_0	x_3	x_2	x_1	x_0	y
0	0	x	x	x	0	0
0	0	x	x	x	1	1
0	1	x	x	0	x	0
0	1	x	x	1	x	1
1	0	x	0	x	x	0
1	0	x	1	x	x	1
1	1	0	x	x	x	0
1	1	1	x	x	x	1

VII. (Need to describe them)

- BIOS Basic Input/Output Systems (Textbook: P.119)
- DSL Digital Subscriber Line (Textbook: P.158)
- ADSL Asymmetric Digital Subscriber Line ([Wikipedia](#))
- XOR Exclusive OR gate (Textbook: P.110)
- FDM Frequency-Division Multiplexing
- TDM Time-Division Multiplexing (Textbook: P.158)
- LAN Wide Area Network (Textbook: P.149)

References:

- Textbook: Connecting With Computer Science 2nd Edition
- Slides: cpphttp7LOV_ch01 Introduction to Computers.ppt
(The download link of the slide as below)
- Wikipedia
- [A. Spielberg \(1954\) - US Patent 2,674,727 - Google Patents](#)
- [A. ANJANA \(2013\) - Even and Odd Parity Generator and Checker using the Reversible logic gates - ijcsec.scientistlink.org](#)

<http://140.116.39.106/eaglesource/C++/cpphttp7LOV.zip>



C++ How to Program, Late Objects Version 7/E
by Paul Deitel & Harvey Deitel

7. Pointers
8. Sequential-Access Files
9. Classes: A Deeper Look, Part 1
10. Classes: A Deeper Look, Part 2 ———> An Iterator Example, Rational

Exercise 10.10 and 10.11 header files <— The zip file now contains

11. Operator Overloading —> Example of converting between types.
12. Object-Oriented Programming: Inheritance
13. Object-Oriented Programming: Polymorphism —> An Example —> And

Exercise 12.10 header files <— The zip file now contains a main fun
for 13.10.

14. Templates
15. Stream Input/Output
16. Exception Handling —> Examples
17. Random-Access Files
18. Class String and String Stream Processing
19. Searching and Sorting
20. Data Structures —> InsertionOrder Example

Final Term Exercise 20.12/13 header files <— The zip file now conta
Ex21_12_ToBeFinished

Please download these files as soon as possible. In case the web s

21. Standard Template Library (STL)
Appendix A. Operator Precedence and Associativity
Appendix B. ASCII Character Set
Appendix C. Fundamental Types Index

Download all the original chapter slides here.