The 2nd mid-exam for Digital Logic Design course
7:00~8:40 PM, 2007-05-28

1. Implement the following Boolean function with an 8-to-1-line multiplexer and a single inverter: $F(A,B,C,D) = \sum m(2,3,5,6,8,9,12,14)$
2. Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, design a logic diagram whose output is equal to 1 when the inputs contain any one of the six unused bit combinations in the BCD code.
3. A majority function can be designed by a combinational circuit with the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority function.
4. Design a combinational circuit that accepts a 2-bit number and generates a 4-bit binary number output equal to the square of the input number. (Hint: you can use multiplexer logic)
5. Design a binary multiplier that multiplies two 3-bit numbers. Use AND gates and binary adders.

(20 points for each problem)

※ The detail procedures must be presented in your answer sheet! ※

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