Digital **L**ogic **D**esign

Final Exam. June/23/2004　　考試時間: 90 mins　　姓名:

注意:作弊一律以零分計

學號:

一. (40pts) Design a 4-bit counter with sequences 0,2,4,6,7,8,9,10,11,12,13,14

Note: Use the symbols in order of DCBA.

(a) Use D FFs.

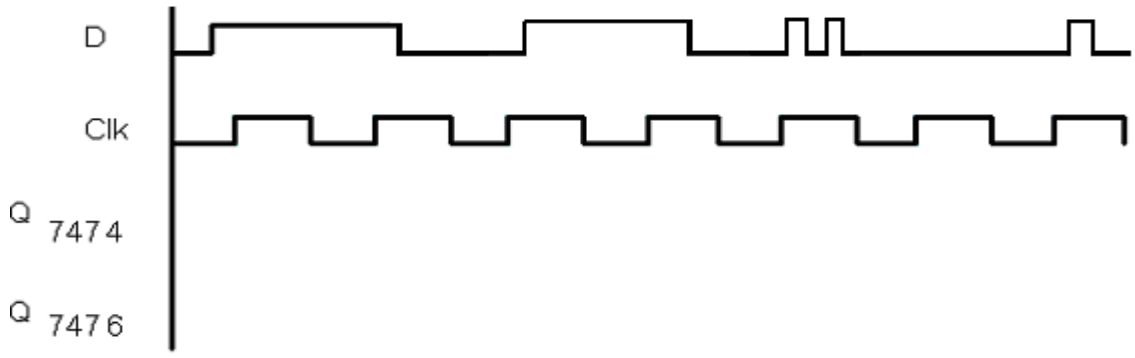
(b) Draw the state diagram of your circuit obtained in (a). Using the state diagram to explain how the circuit would react to the illegal states?

二. (20pts) Implement the logic function $F(A,B,C,D)=\sum m(0,1,2,3,12,15)+d(13,14)$

(a) using a 4: 1 Multiplexer

(b) using a 2: 1 Multiplexer

三. (15pts) Complete the waveforms of Q_{7474} and Q_{7476}



四. (15pts) Describe the special properties of FPGA. Describe what benefits it can bring when a complex system design is implemented using FPGA, i.e., SOC implemented with FPGA. Describe product families provided by Altera Company?

五. (10 pts) Compare the following two design strategies, **using the space shuttle example** given in Chap 7 of Feyman's book "The pleasure of finding things out".

(a) Bottom-up (b) Top-down