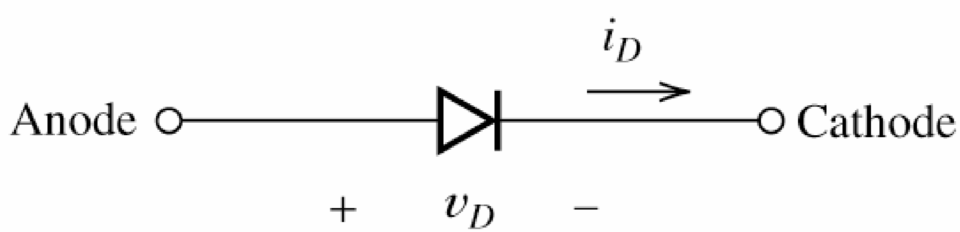
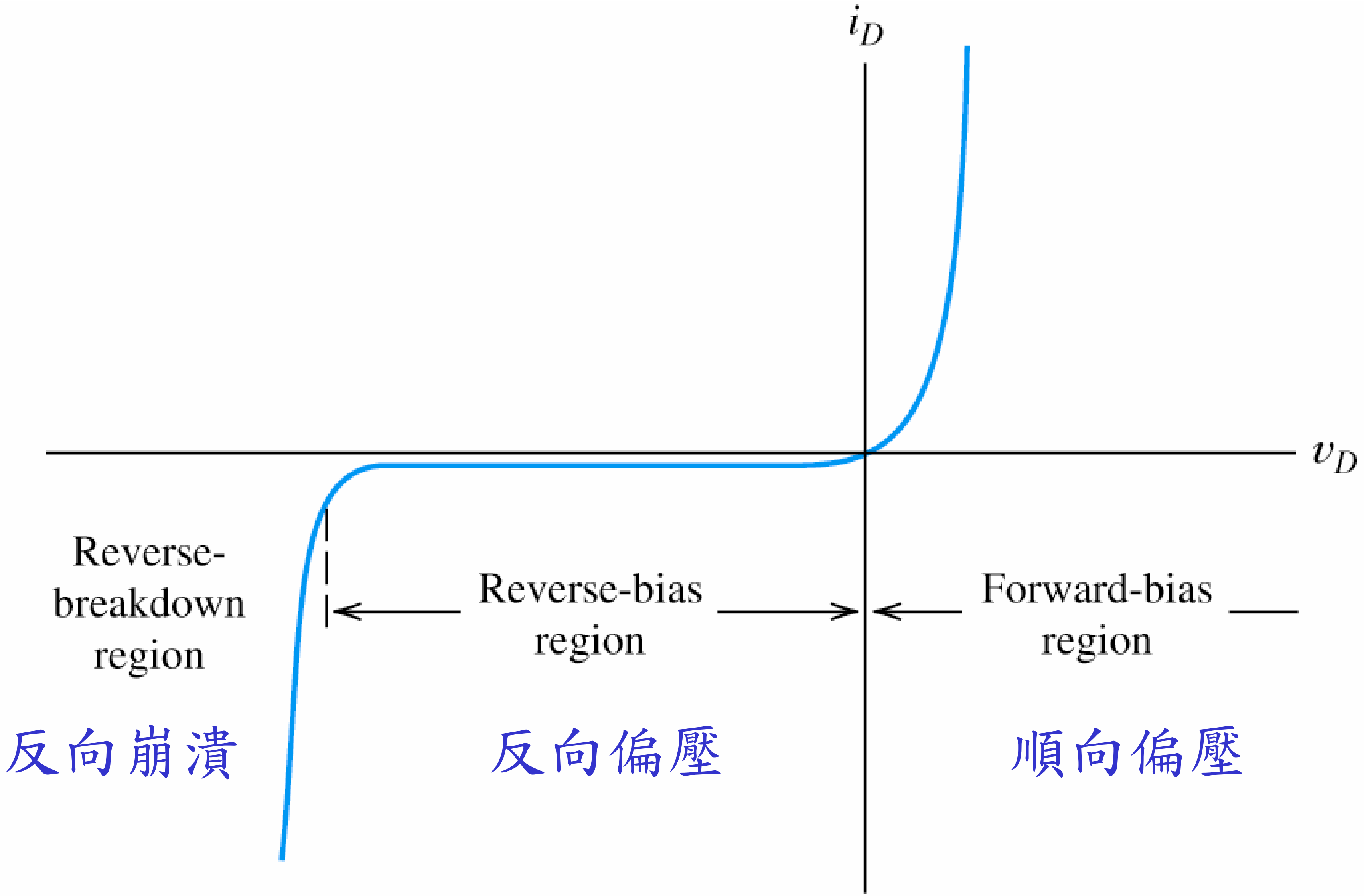
Chapter 10 Diodes (二極體)

10.1 Basic Diode Concept

- The diode has two terminals, the anode (正極) and the cathode (負極)。



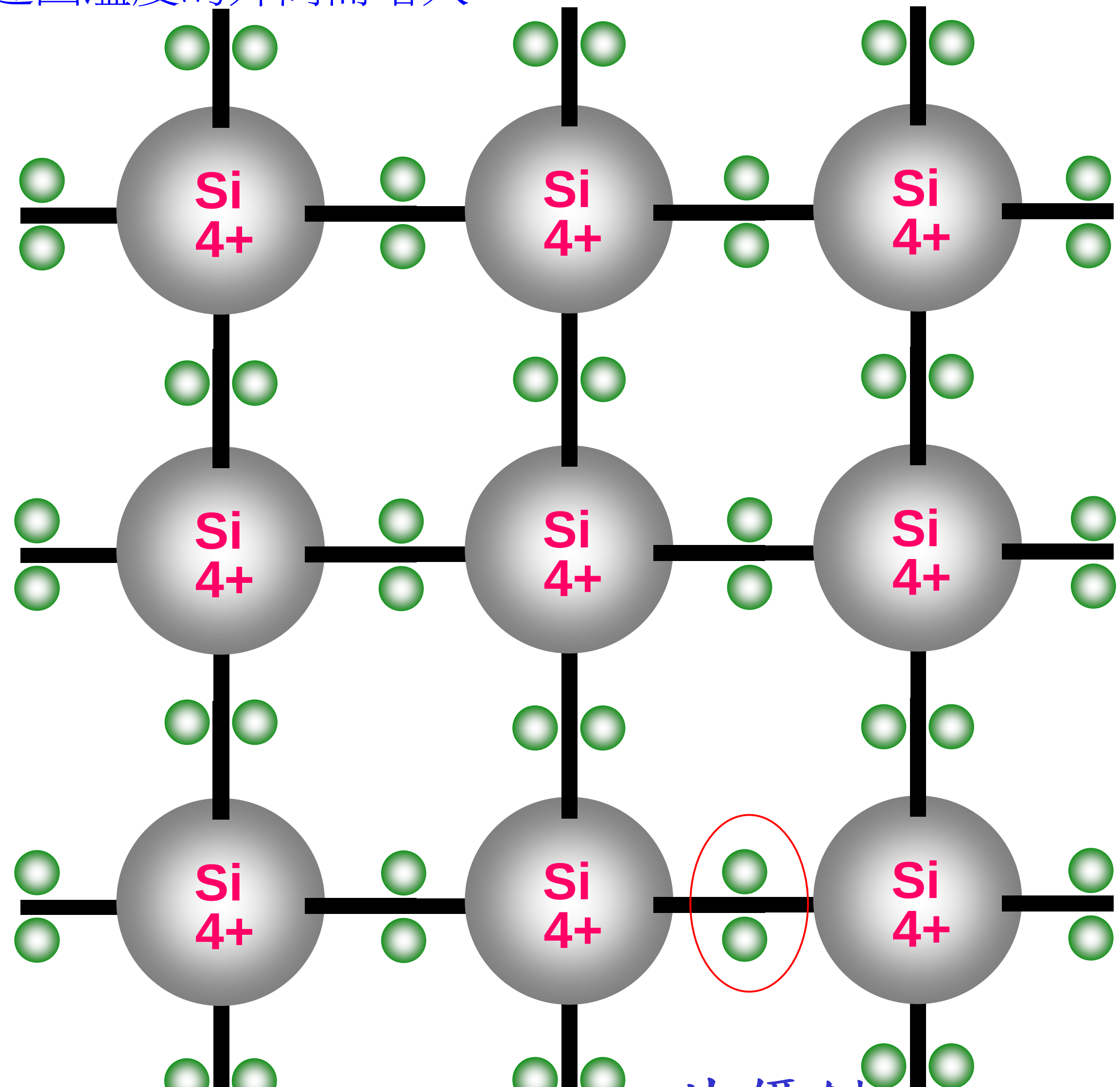
- 當二極體正極與負極間給一v_D>0, 稱為順向偏壓 (forward bias.)
- 當二極體正極與負極間給一v_D<0, 稱為反向偏壓 (reverse bias.)



i_D
v_D
Reverse-breakdown region
Reverse-bias region
Forward-bias region
反向崩潰
反向偏壓
順向偏壓

本質半導體 (intrinsic semiconductor)

溫度越高，被熱能釋放出來的電子和電洞的數量也越多。因此，本質半導體的導電性遂因溫度的升高而增大



共價鍵

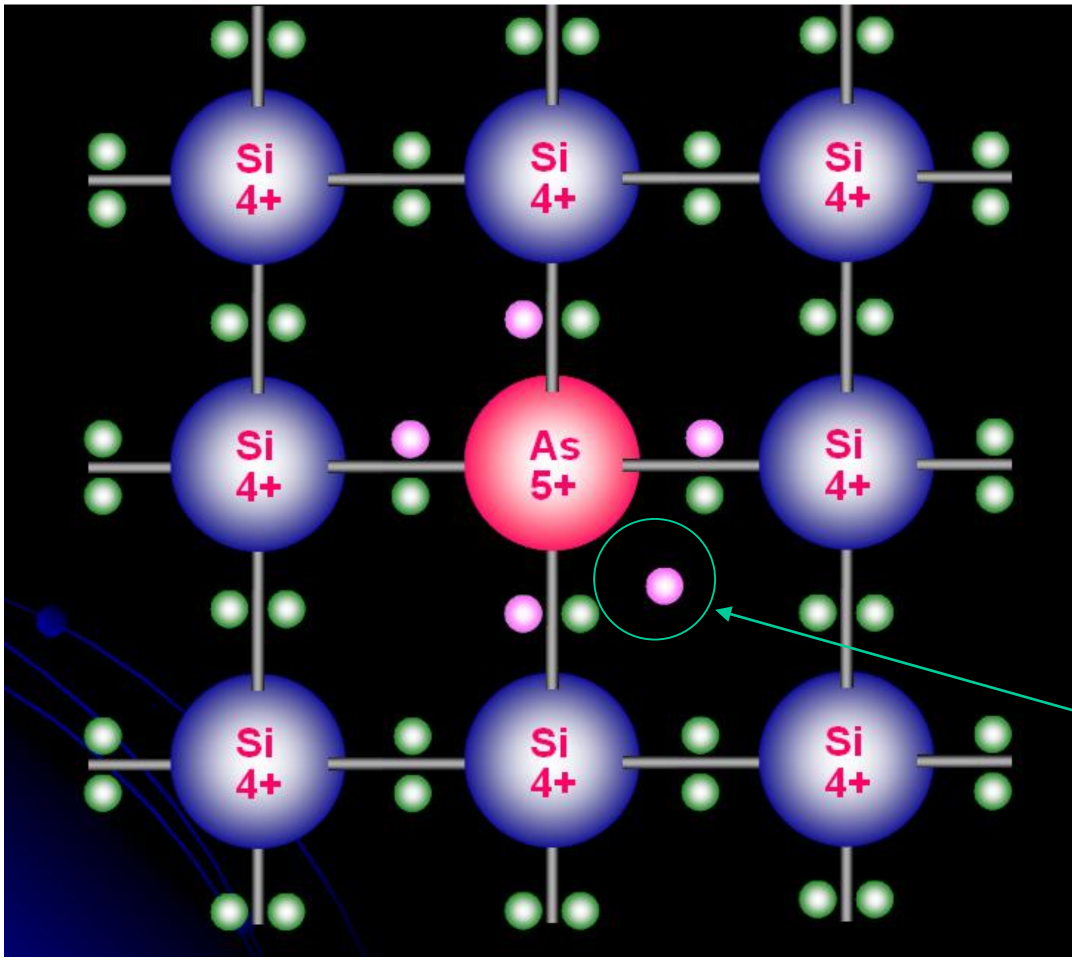
IIB	IIIA	IVA	VA	VIA
	B 硼	C 碳	N 氮	O 氧
	Al 鋁	Si 矽	P 磷	S 硫
Zn 鋅	Ga 鎵	Ge 鍺	As 砷	Se 硒
Cd 鎘	In 銦		Sb 銻	Te 碲
Hg 汞				

四價原子

非本質半導體(extrinsic semiconductor)

n-type

四價原子摻雜(doping)五價原子



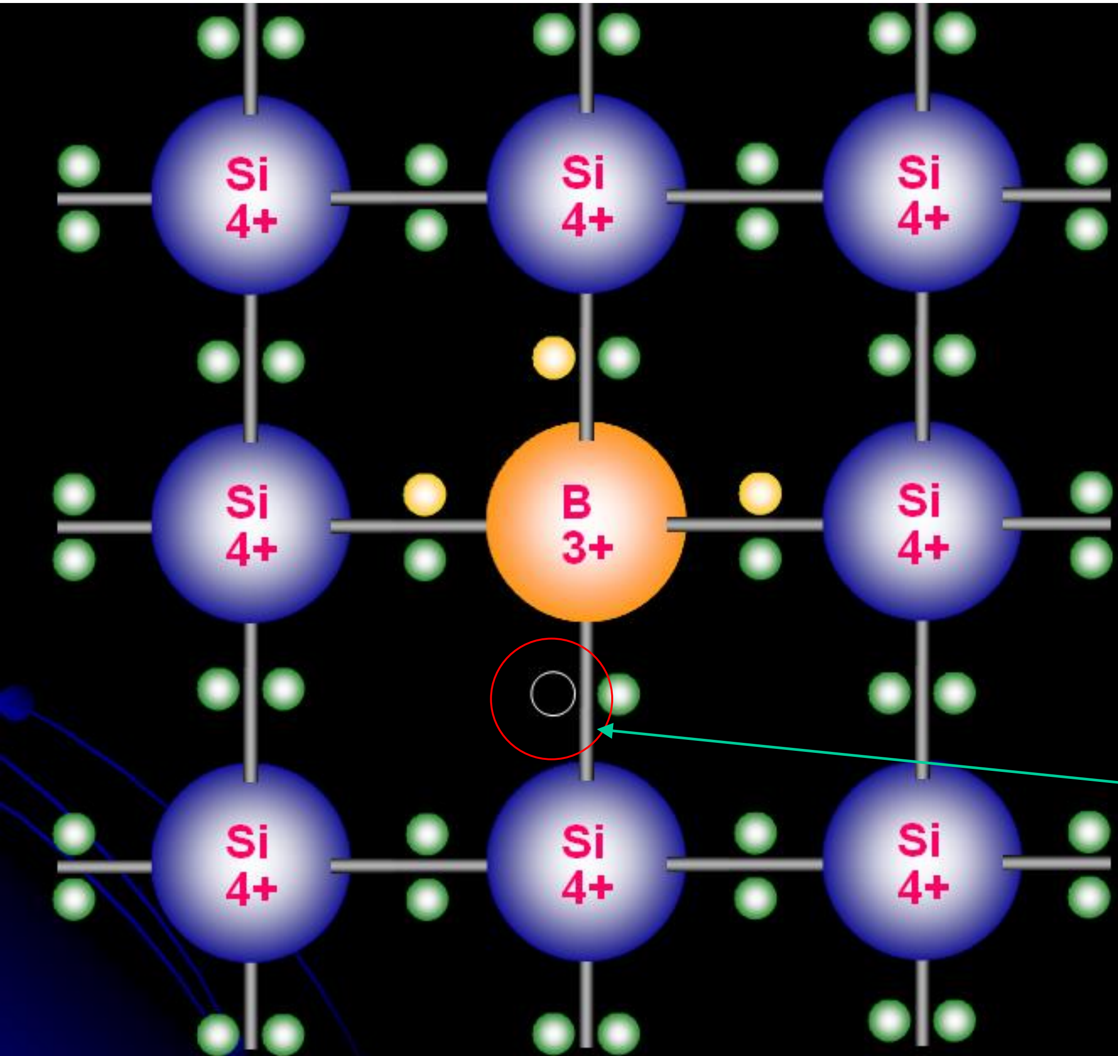
IIB	IIIA	IVA	VA	VIA
	B 硼	C 碳	N 氮	O 氧
	Al 鋁	Si 矽	P 磷	S 硫
Zn 鋅	Ga 鎵	Ge 鍺	As 砷	Se 硒
Cd 鎘	In 銦		Sb 銻	Te 碲
Hg 汞				

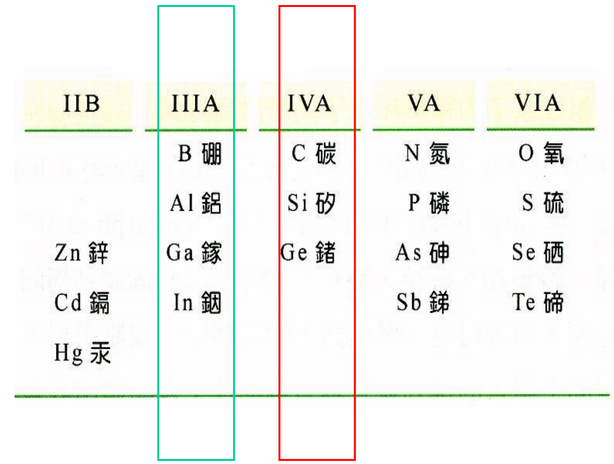
具帶負電荷的自由電子(由所摻雜的五價原子提供)

非本質半導體(extrinsic semiconductor)

p-type

四價原子摻雜(doping)三價原子





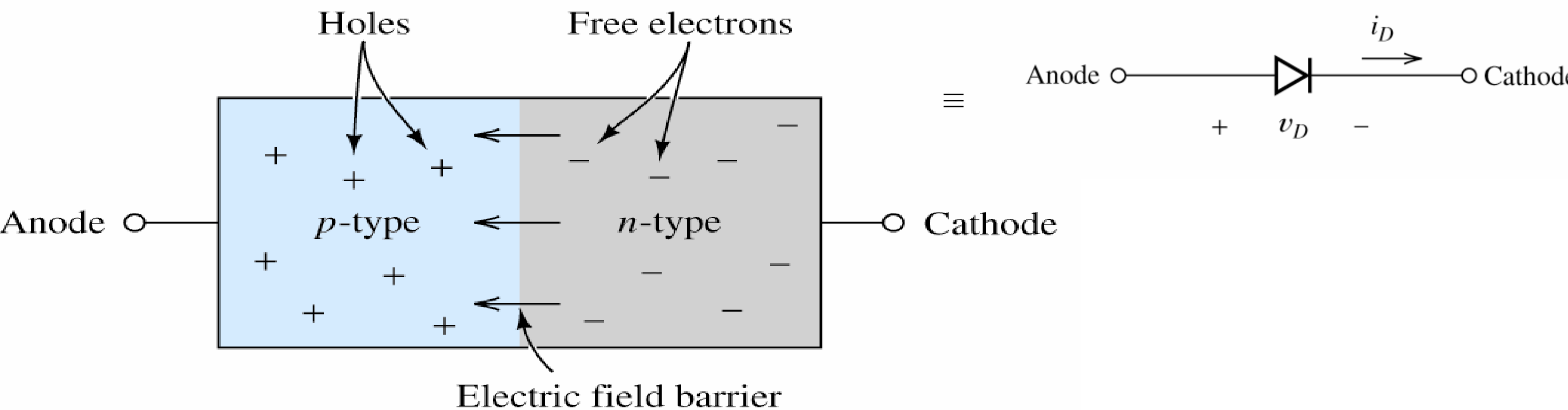
IIB	IIIA	IVA	VA	VIA
	B 硼	C 碳	N 氮	O 氧
	Al 鋁	Si 矽	P 磷	S 硫
Zn 鋅	Ga 鎵	Ge 鍺	As 砷	Se 硒
Cd 鎘	In 銦		Sb 銻	Te 碲
Hg 汞				

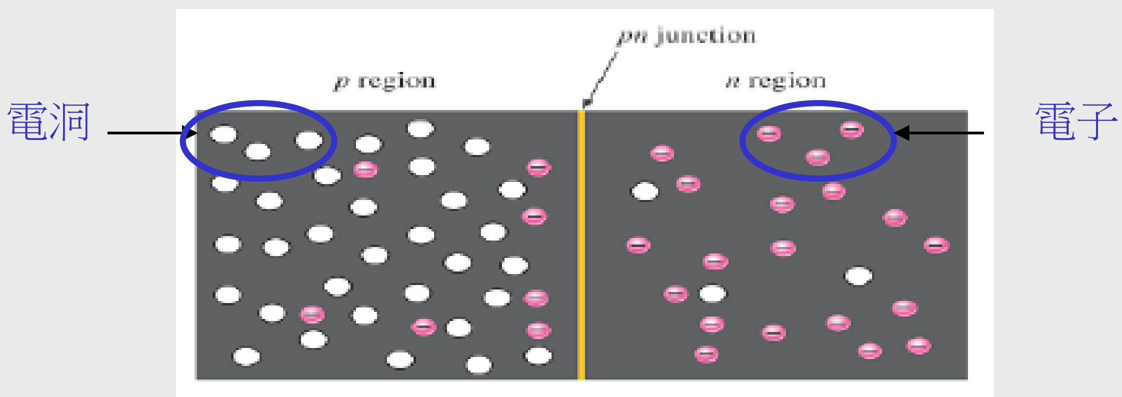
具帶正電荷的自由電洞(由所摻雜的三價原子提供)

Doping

- 摻雜(Doping)
  - 將定量雜質加入純質半導體中，就可大幅提升矽與鍺的導電性
  - 摻有雜質的半導體有兩種
    - N型: 加入五價的雜質原子，砷(As), 磷(P), 鉍(Bi), 銻(Sb)等
    - P型:加入三價的雜質原子，硼(B), 銦(In), 鎵(Ga)等

PN Junction (PN 接面)

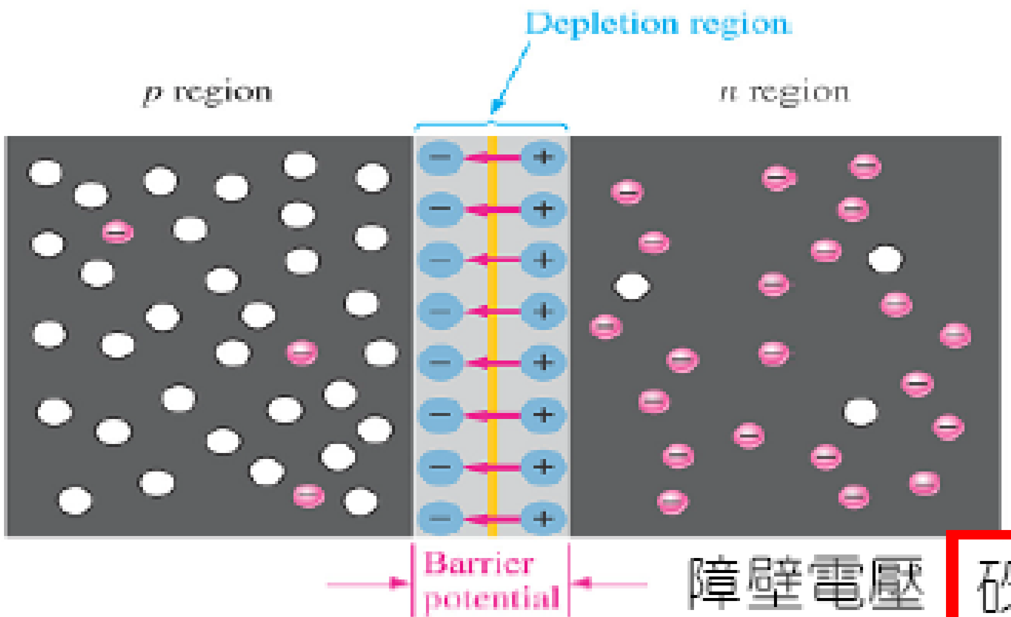




在*pn*接面形成的瞬間，在*n*型區接近*pn*接面的自由電子開始跨過接面擴散進入*p*型區靠近接面的電洞。

PN Junction (PN 接面)

Electric-field barrier



障壁電壓

矽：0.7V

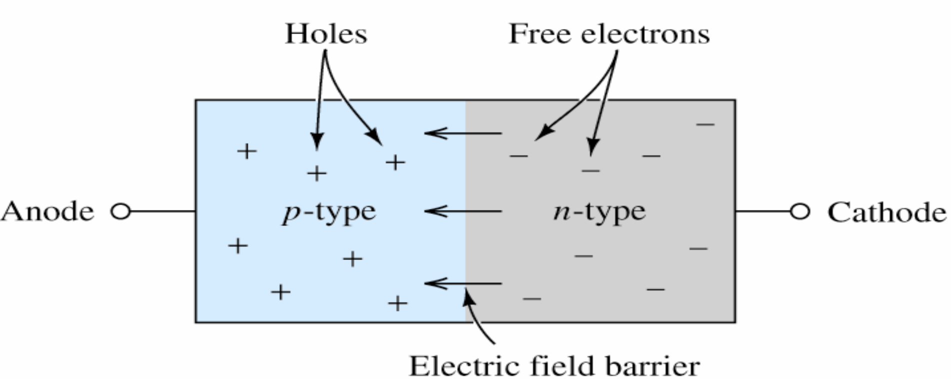
每一個擴散通過接面而與電洞結合的電子，就會在*n*型區留下一個正電荷，並且在*p*型區產生一個負電荷，這樣就形成障壁電壓。這種現象會一直持續，直到產生的障壁電壓大到能夠排斥進一步的擴散作用為止。

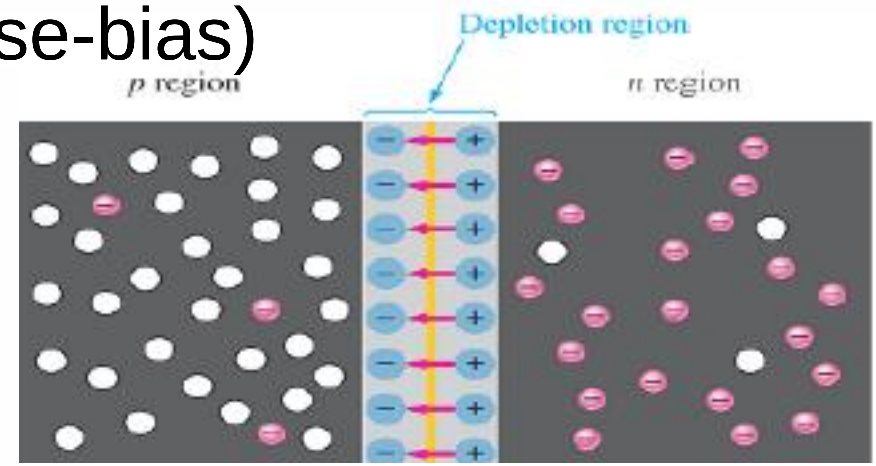
PN Junction (PN 接面)

- Electric-filed barrier (電場屏障，P端低, N端高)使得N端自由電子無法到達P 端，P端自由電洞無法到達N 端。此接面稱為Depletion region (空乏區)。

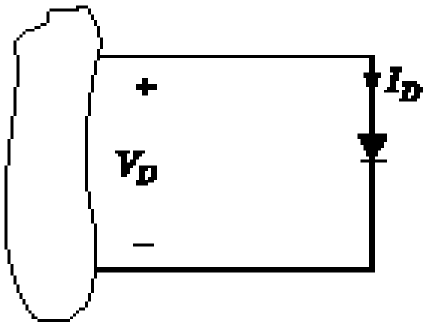
- 當v_D >*electric-field barrier(*順向偏壓, forward-bias)，則二極體導通，電子(N端)與電洞(P端)向另一端流動。

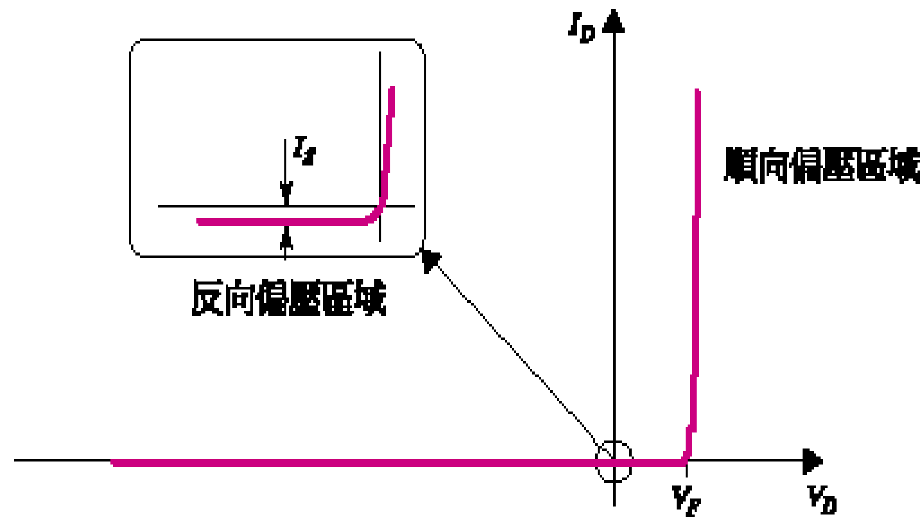
- 當二極體正v_D <*0(*反向偏壓)，則增強electric-filed barrier, 更不導通。(reverse-bias)





Shockley Equation





$$\boxed{i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]}$$

I_s: **(reverse) saturation current ((反向)飽和電流)**

$V_T = \frac{kT}{q} \cong 0.026\text{V(at } 300^\circ\text{K)}$ **: Termal voltage (熱電位)**

$k = 1.38 \times 10^{-23}$ (J/K) **波茲曼常數**

$q = 1.6 \times 10^{-19}$ C

T ($^\circ$K) **溫度**

n: ideality factor, **理想因子** $1 \leq n \leq 2$

在順向偏壓下，指數項為正指數特性；
在逆向偏壓下，v_D為負值，
i_D將逼近$-I_S$

二極體完整I-V曲線

順向偏壓時, 當 $v_D >> nV_T$ $\quad i_D \cong I_s \exp\left(\dfrac{v_D}{nV_T}\right)$

Breakdown voltage
崩潰電壓，一般
diode易燒毀

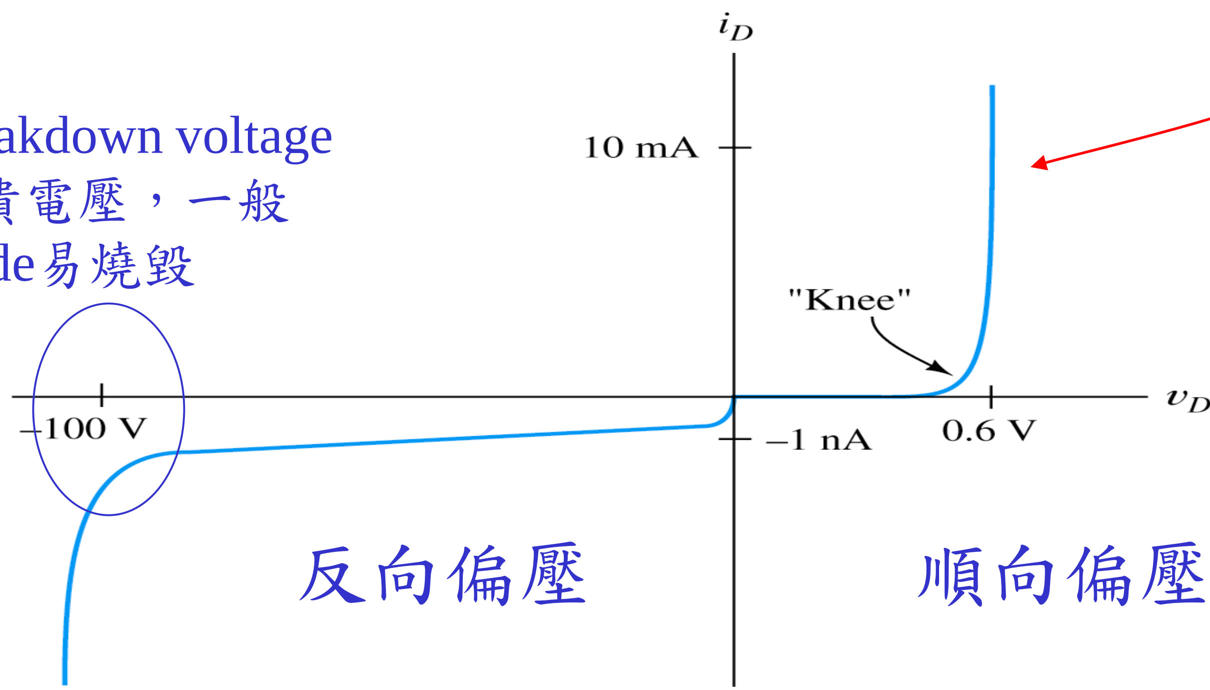
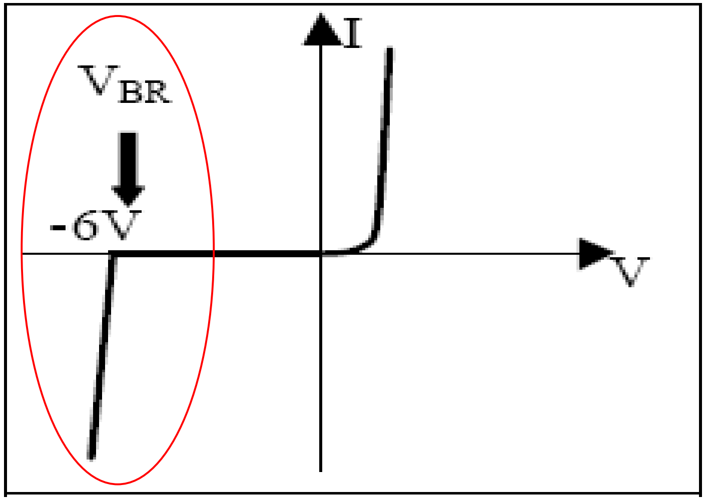
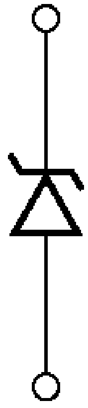


Figure 10.2 Volt–ampere characteristic for a typical small-signal silicon diode at a temperature of 300 K. Notice the change of scale for negative current and voltage.

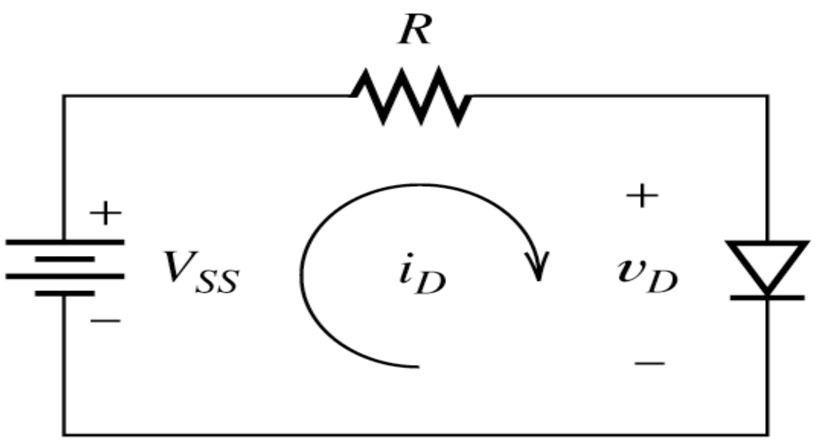
Zener Diodes (齊納二極體)

Diodes that are intended to operate in the breakdown region (崩潰區) are called **Zener diodes**. 其在正向偏壓時與一般diode 一樣。





10.2 LOAD-LINE ANALYSIS OF DIODE CIRCUITS



KVL

$$V_{SS} = Ri_D + v_D$$

Diode I-V equation

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

- 兩條方程式，可解兩個未知數 i_D&v_D。
- 將兩條方程式畫在同一張I-V圖上，交點即是解。
- 此成為負載線分析法(load-line analysis)。

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]$$

$$V_{SS} = Ri_D + v_D$$

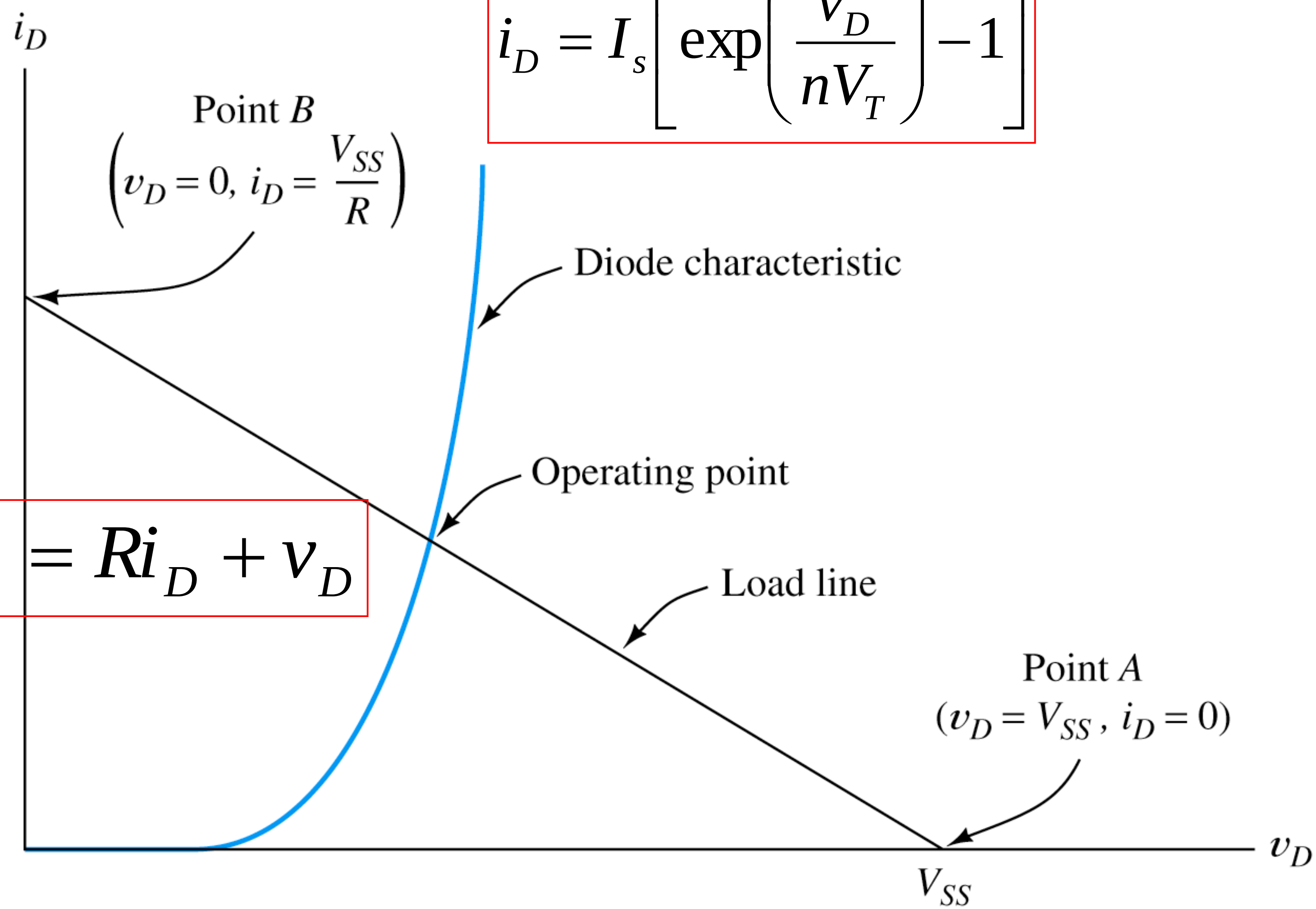
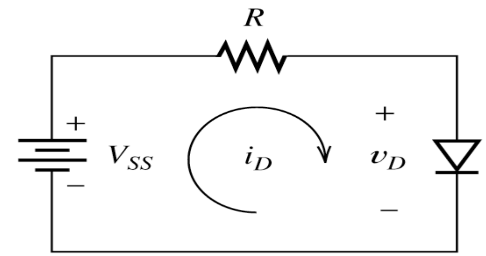


Figure 10.6 Load-line analysis of the circuit of Figure 10.5.

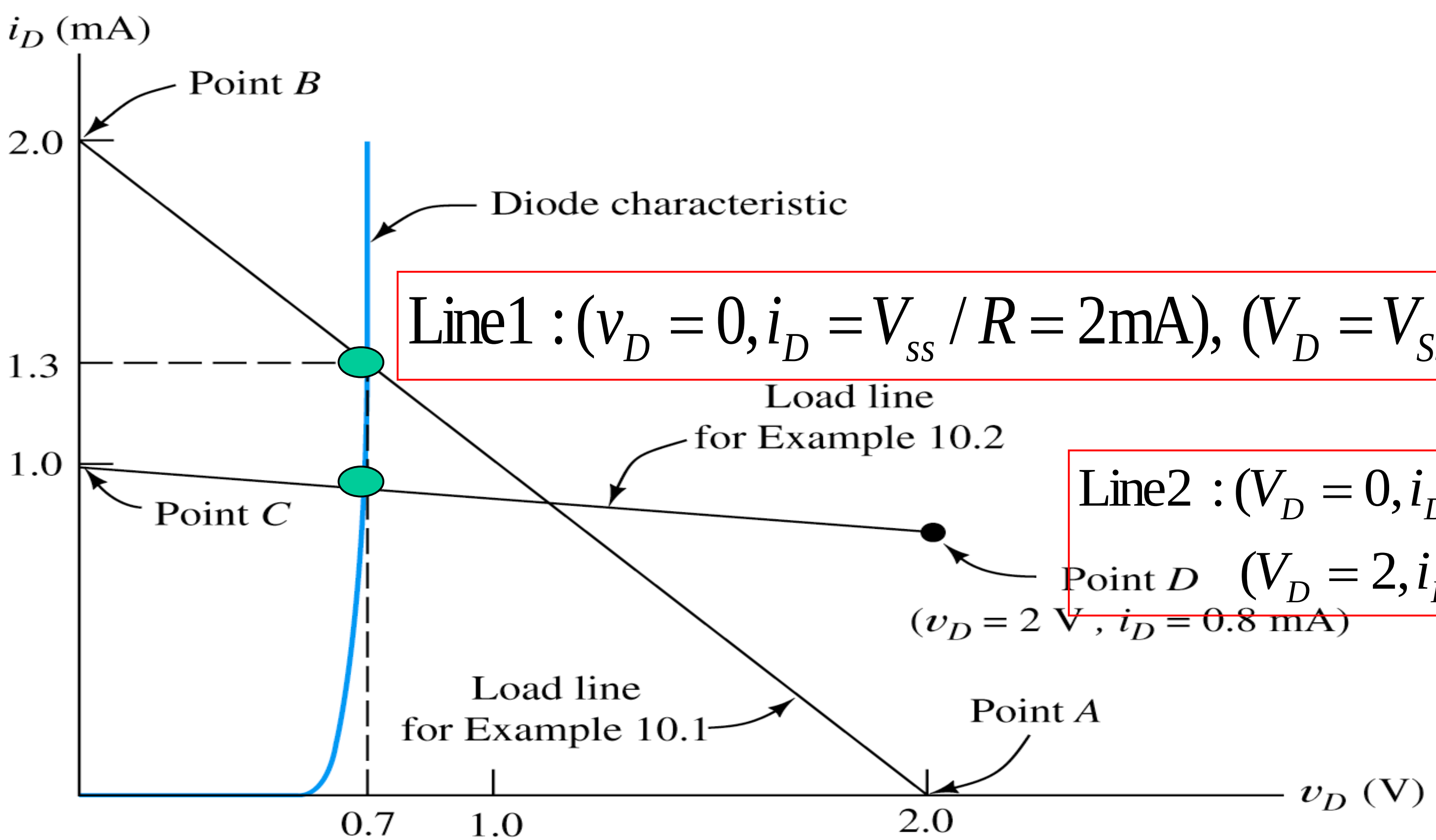
Example 10.1 & 10.2 Load line analysis



V_{ss}=2 V, R=1 kΩ. (load line 1)

V_{ss}=10 V, R=10 kΩ. (load line 2)

Find the diode voltage and current at the operating point.



$$\text{Line1}: (v_D = 0, i_D = V_{ss}/R = 2\text{mA}),\ (V_D = V_{SS} = 2\text{V}, i_D = 0)$$

$$\text{Line2}: (V_D = 0, i_D = V_{ss}/R = 1\text{mA}),\ (V_D = 2, i_D = 0.8\text{mA})$$

Figure 10.7 Load-line analysis for Examples 10.1 and 10.2.

Exercise 10.3

V_{ss}=2 V, R=100 Ω.

Find the diode voltage and current at the operating point.

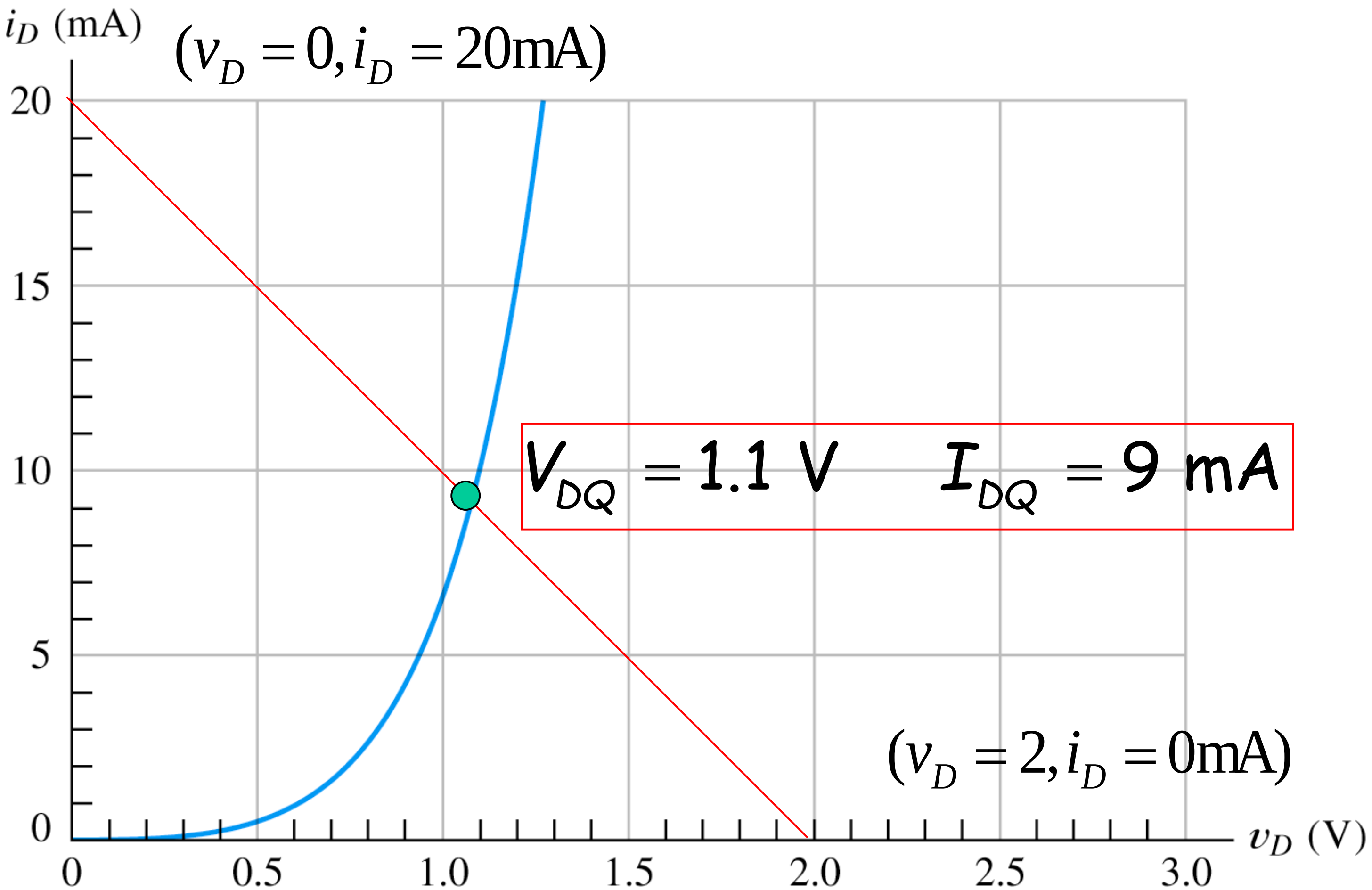
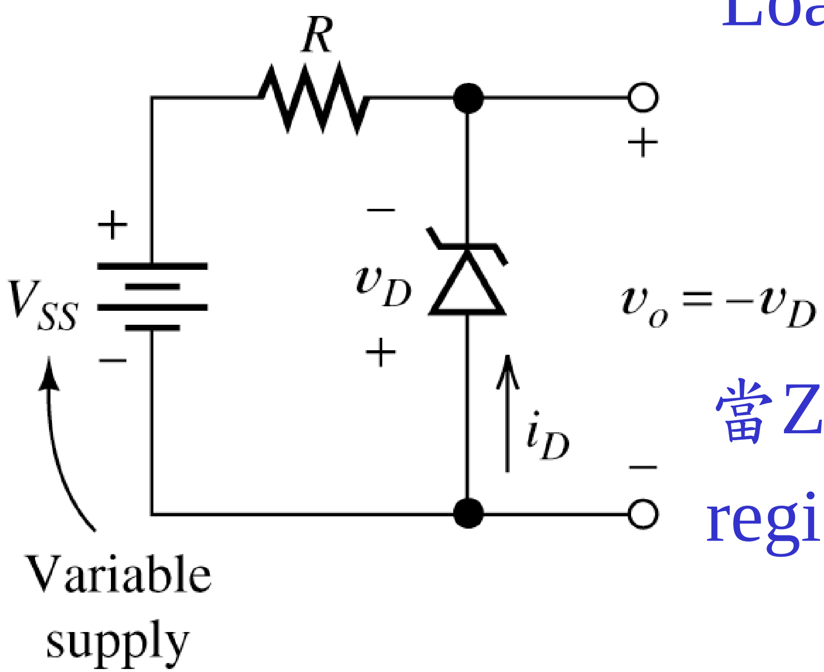


Figure 10.8 Diode characteristic for Exercise 10.3.

10-3 ZENER-DIODE VOLTAGE-REGULATOR CIRCUITS

A voltage regulator (穩壓) circuit provides a nearly constant voltage to a load from a variable source.



Load line

$$V_{SS} + Ri_D + v_D = 0$$

當Zener diode 操作在breakdown region 時, v_D 與 i_D都<0.

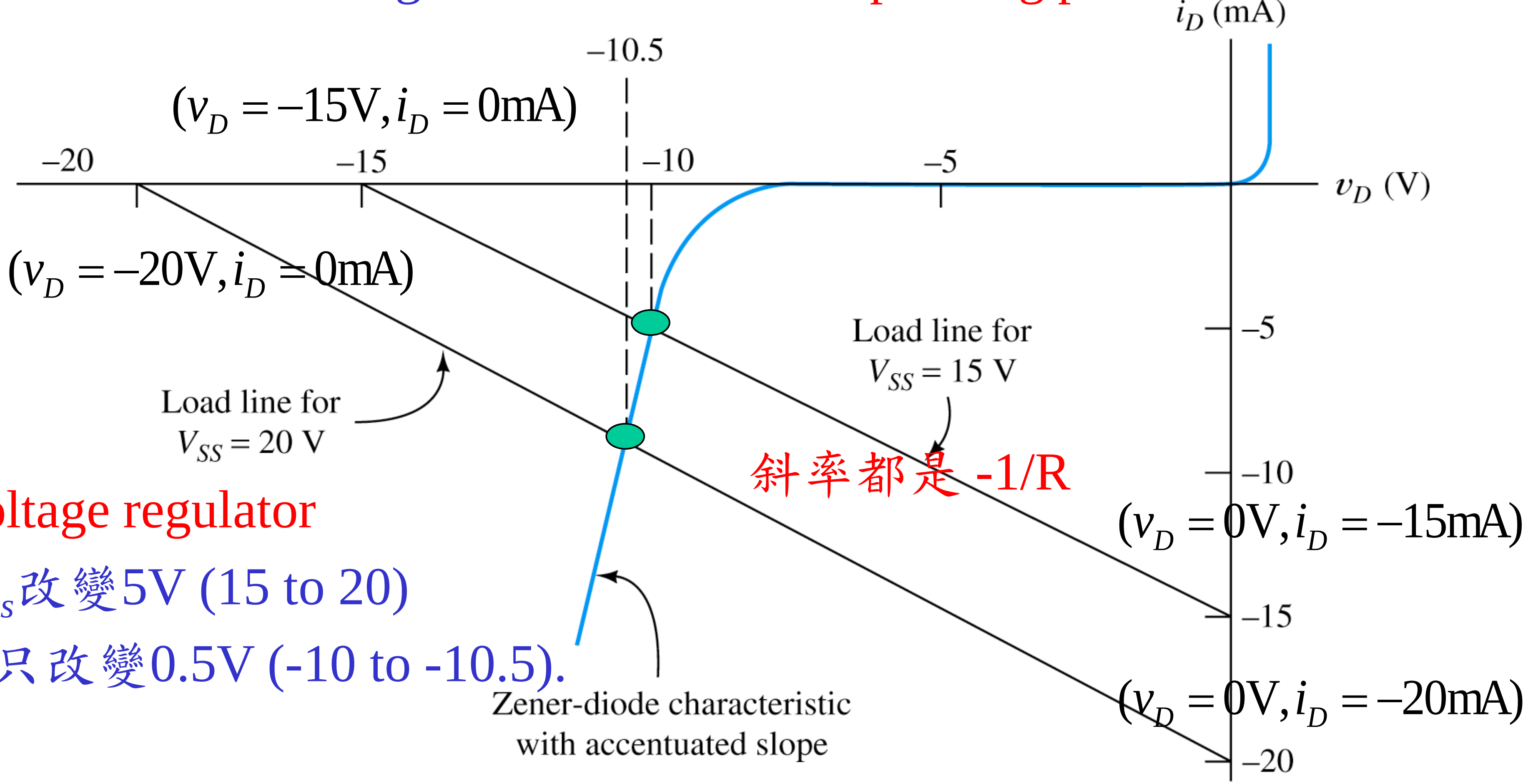
Example 10.3

R=1 kΩ, V_{ss}=15 V. (load line 1)

R=1 kΩ, V_{ss}=20 V. (load line 2)

Find the diode voltage and current at the operating point.

$$V_{SS} + Ri_D + v_D = 0$$



Voltage regulator

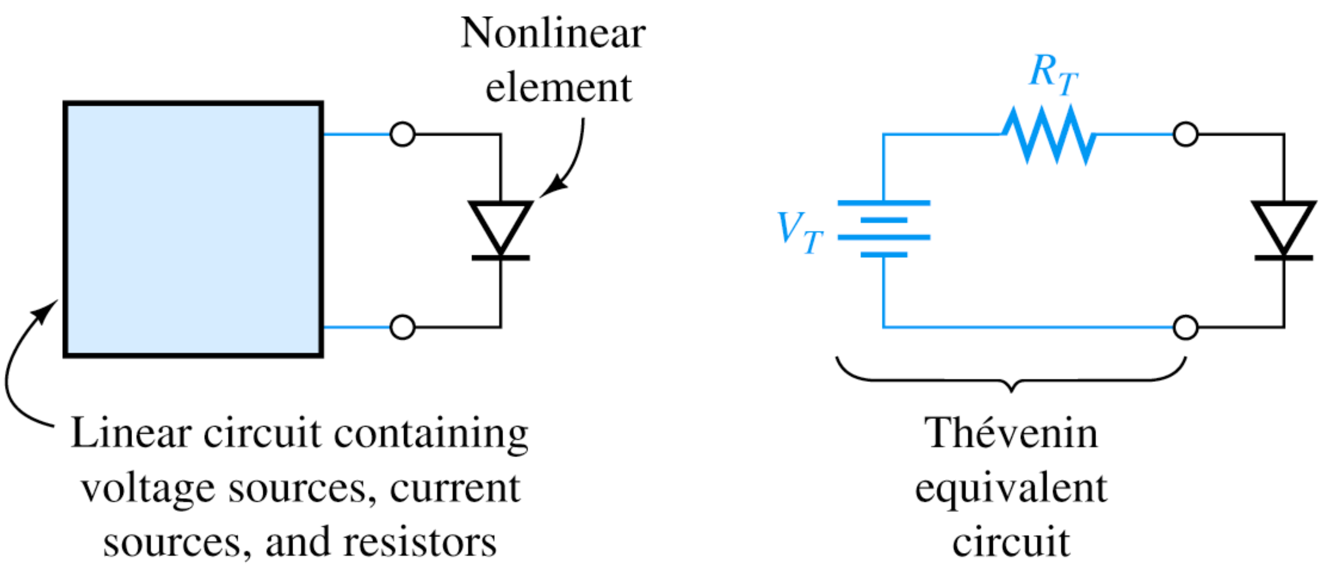
V_{ss}改變5V (15 to 20)

v_o只改變0.5V (-10 to -10.5).

Figure 10.10 See Example 10.3.

Load-Line Analysis of Complex Circuits

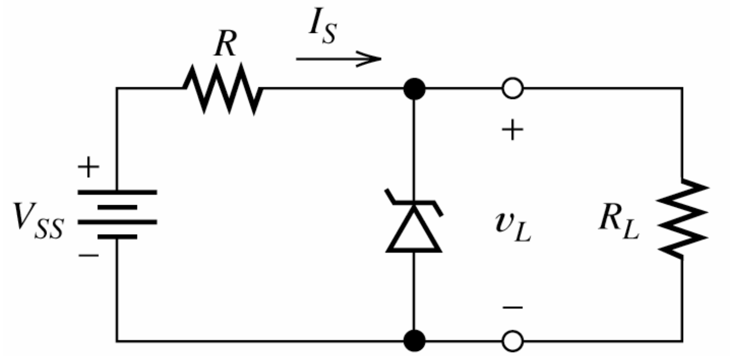
一個電路包含two-terminal 非線性元件(如diode)，首先將線性元件部分以戴維寧等效電路簡化後，再利用load-line analysis 求解。



(a) Original circuit (b) Simplified circuit

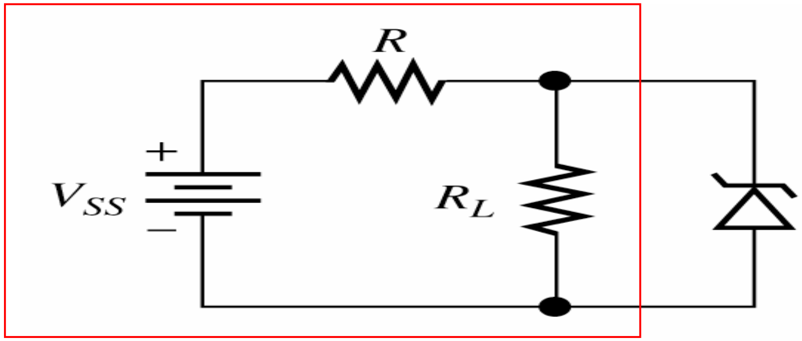
Example 10.4

V_{ss}=24 V, R=1.2 kΩ, R_L=6 kΩ.
Find v_L and I_s.



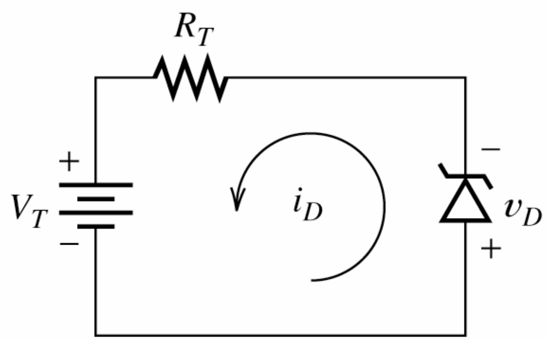
(a) Regulator circuit with load

1. 將線元件與非線性元件分離



(b) Circuit of (a) redrawn

2. Thévenin



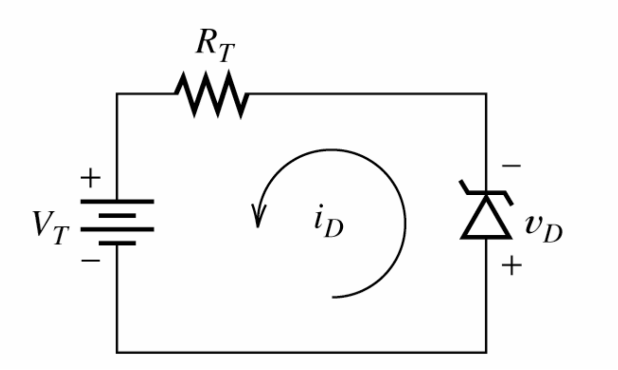
Open-loop voltage

$$V_T = V_{SS}\frac{R_L}{R+R_L} = 20V$$

Zeroing to find the Thévenin resistance

$$R_T = \frac{RR_L}{R+R_L} = 1k\Omega$$

3. Load-line analysis



$$V_T + R_T i_D + v_D = 0$$

Load-line will pass

$$(v_D = -v_T = -20\text{V}, i_D = 0\text{mA})$$

$$(v_D = 0\text{V}, i_D = -\frac{V_T}{R_T} = -20\text{mA})$$

$$V_L = -v_{DQ} = 10.0V$$

$$I_s = \frac{V_{ss} - v_L}{R} = 11.67\text{mA}$$

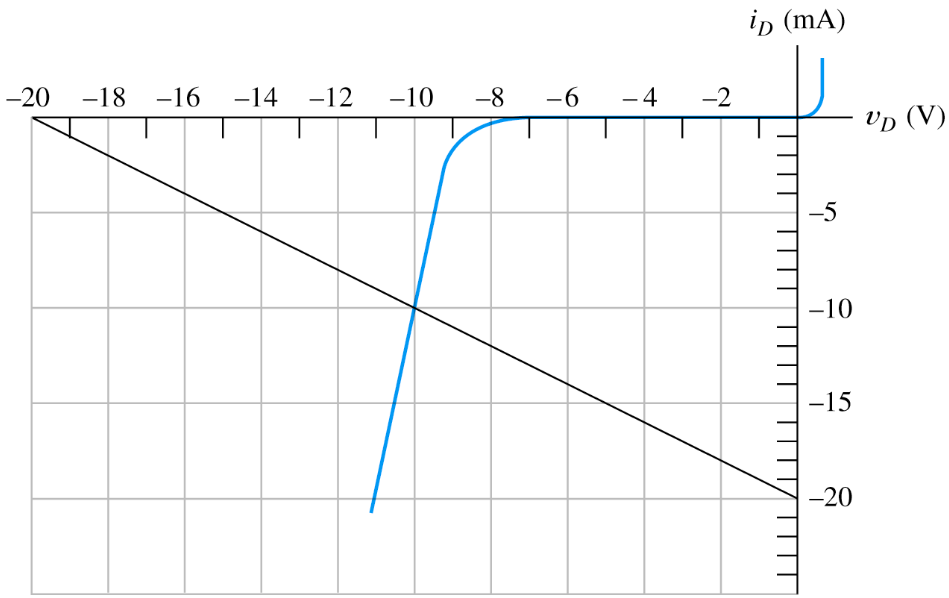
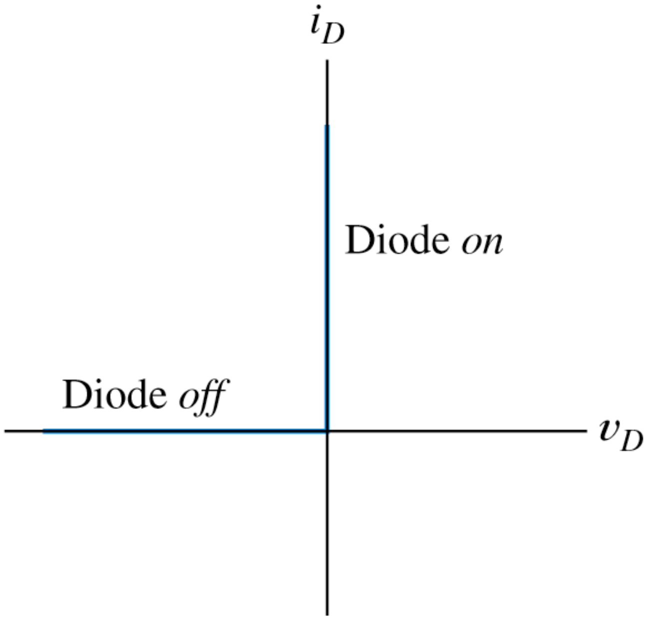


Figure 10.13 Zener-diode characteristic for Example 10.4 and Exercise 10.4.

10.4 IDEAL-DIODE MODEL

The ideal diode acts as a short circuit for forward currents and as an open circuit with reverse voltage applied.



Assumed States for Analysis of Ideal-Diode Circuits

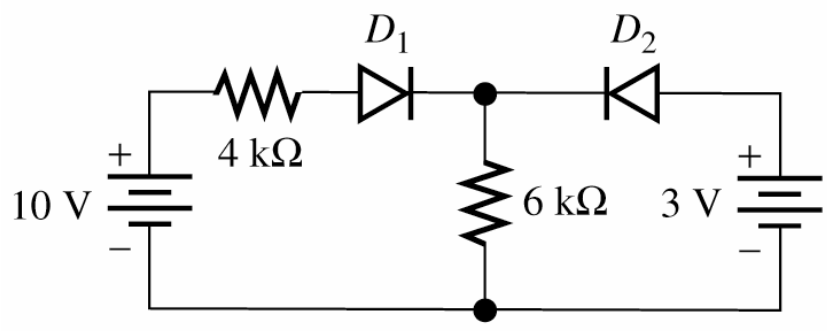
1. Assume a state for each diode, either on (i.e., a short circuit) or off (i.e., an open circuit). For ***n*** diodes there are 2^n possible combinations of diode states.

2. Analyze the circuit to determine the current through the diodes assumed to be on and the voltage across the diodes assumed to be off.

3. Check to see if the result is consistent with the assumed state for each diode. Current must flow in the forward direction for diodes assumed to be on. Furthermore, the voltage across the diodes assumed to be off must be positive at the cathode (i.e., reverse bias).

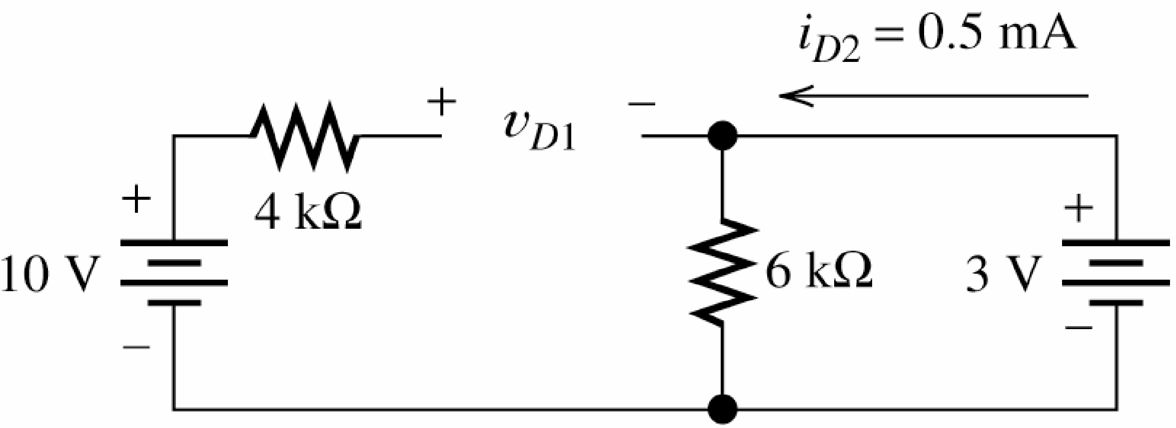
4. If the results are consistent with the assumed states, the analysis is finished. Otherwise, return to step 1 and choose a different combination of diode states.

Example 10.5 Using ideal-diode model to analyze the circuit. Assuming that D_1 is off and D_2 is on.



(a) Circuit diagram

1. Assume D1 is off and D2 is on



(b) Equivalent circuit assuming D_1 off and D_2 on (since $v_{D1} = +7$ V, this assumption is not correct)

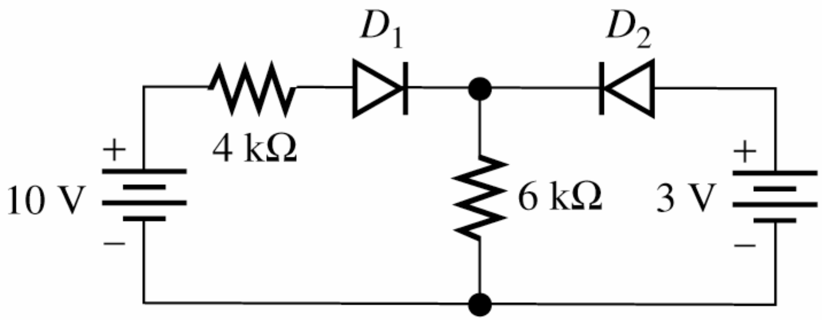
$$i_{D2} = \frac{3}{6k} = 0.5\text{mA}$$

D2 on is correct.

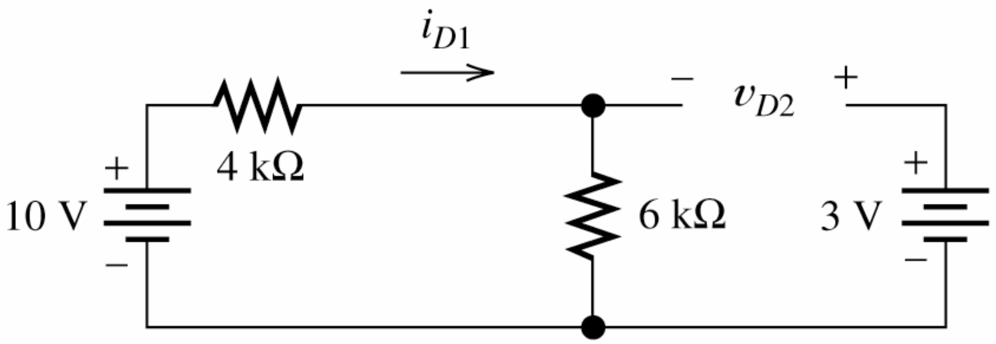
$$v_{D1} = 10 - 3 = 7\text{V}$$

D1 off is NOT correct.

2. Assume D1 is on and D2 is off



(a) Circuit diagram



(c) Equivalent circuit assuming D_1 on and D_2 off (this is the correct assumption since i_{D1} turns out to be a positive value and v_{D2} turns out negative)

$$i_{D1} = \frac{10}{(6+4)k} = 1\text{mA}$$

D1 on is correct.

$$6 = -v_{D2} + 3$$

$$v_{D2} = -3\text{V}$$

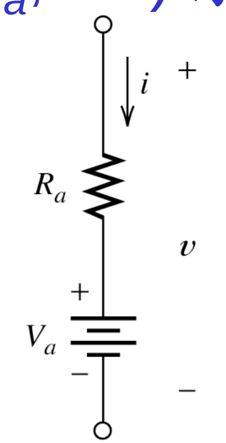
D2 off is correct.

10.5 PIECEWISE-LINEAR DIODE MODELS

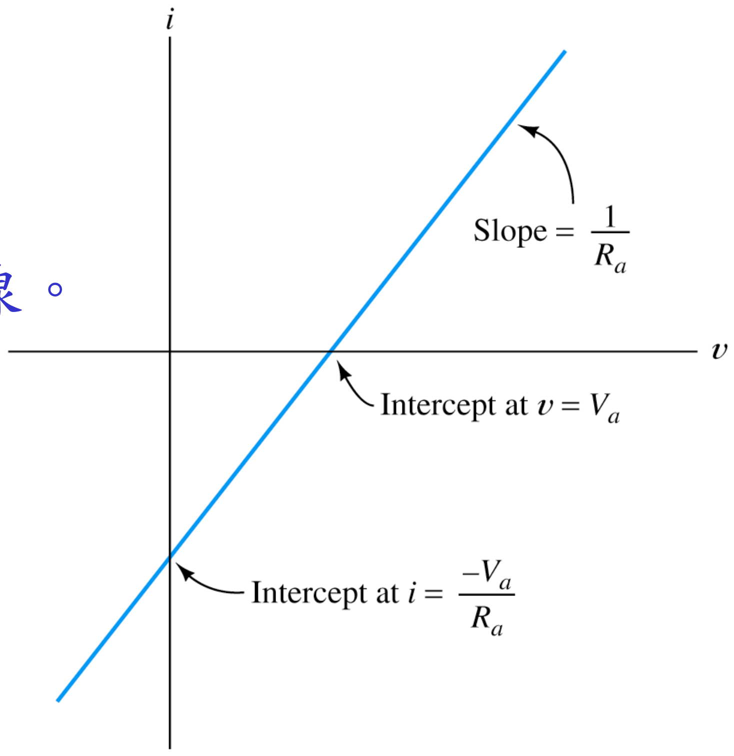
一個定電壓與電阻串接，其電壓電流關係式為

$$v = R_a i + V_a$$

I-V圖為斜率1/R_a且通過(v=v_a, i=0)的直線。



(a) Circuit diagram



(b) Volt–ampere characteristic

PIECEWISE-LINEAR DIODE MODELS

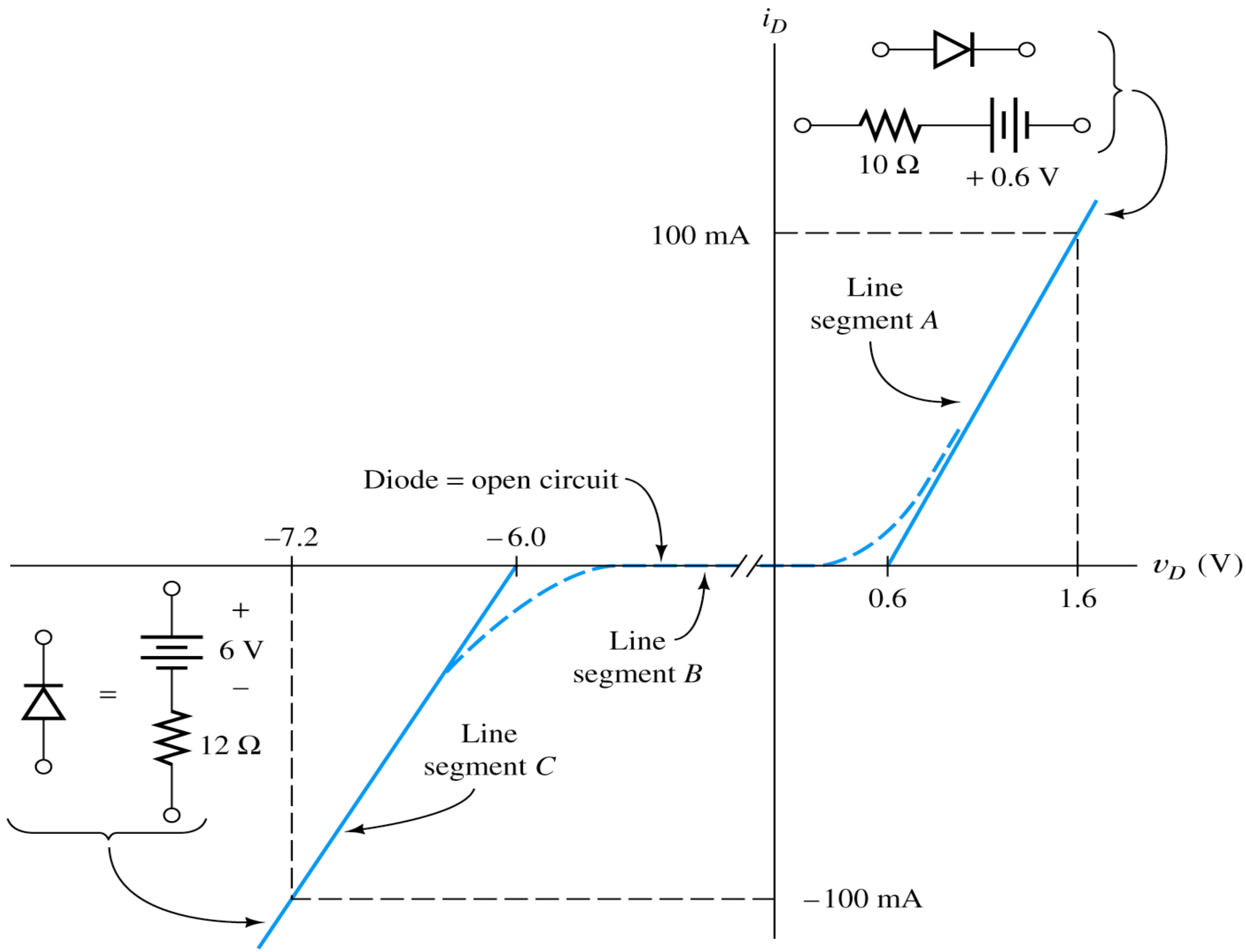
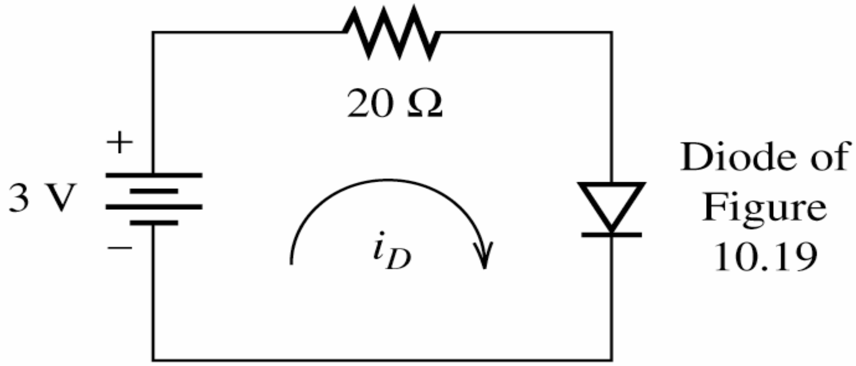


Figure 10.19 Piecewise-linear models for the diode of Example 10.6.

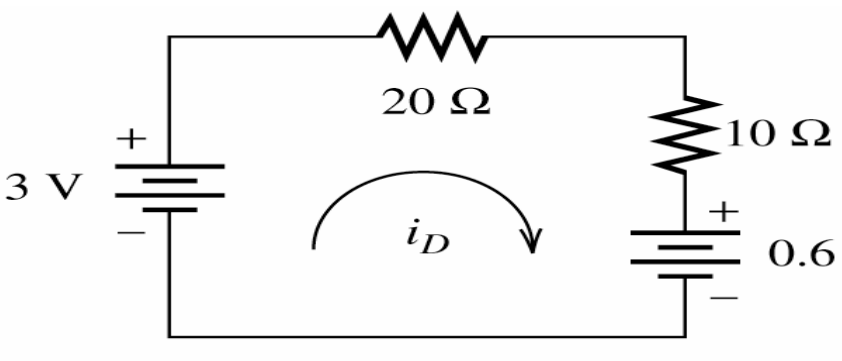
Example 10.7



(a) Circuit diagram

1. 3V> 0.6V(turn on voltage of the diode), assume the diode is forward bias.

2. The equivalent circuit



(b) Circuit with diode modeled by the equivalent circuit for the forward-bias region

$$i_D = \frac{3-0.6}{20+10} = 80\text{mA}$$

SIMPLE PIECEWISE-LINEAR DIODE MODELS

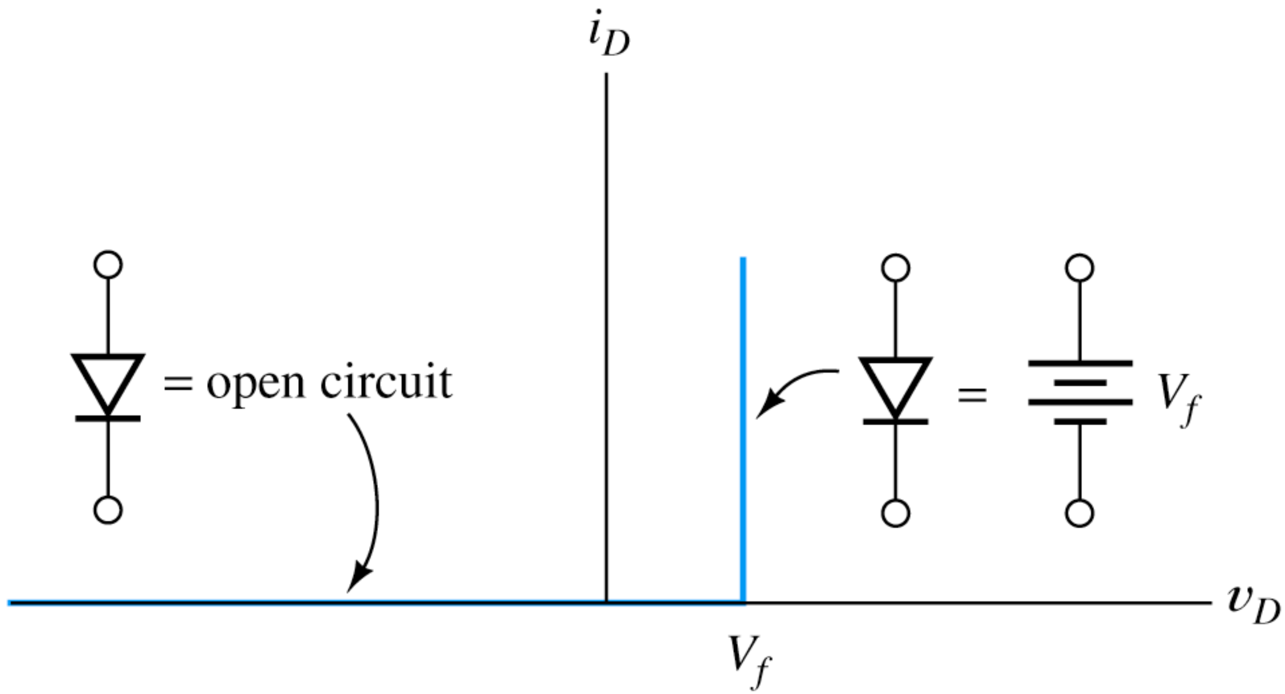


Figure 10.23 Simple piecewise-linear equivalent for the diode.

10.6 Rectifier Circuits (整流器)

Half-wave rectifier (半波整流器)

只有$v_s(t)>0$ 才有輸出(or $v_s(t)<0$時 $v_o(t)=0$)

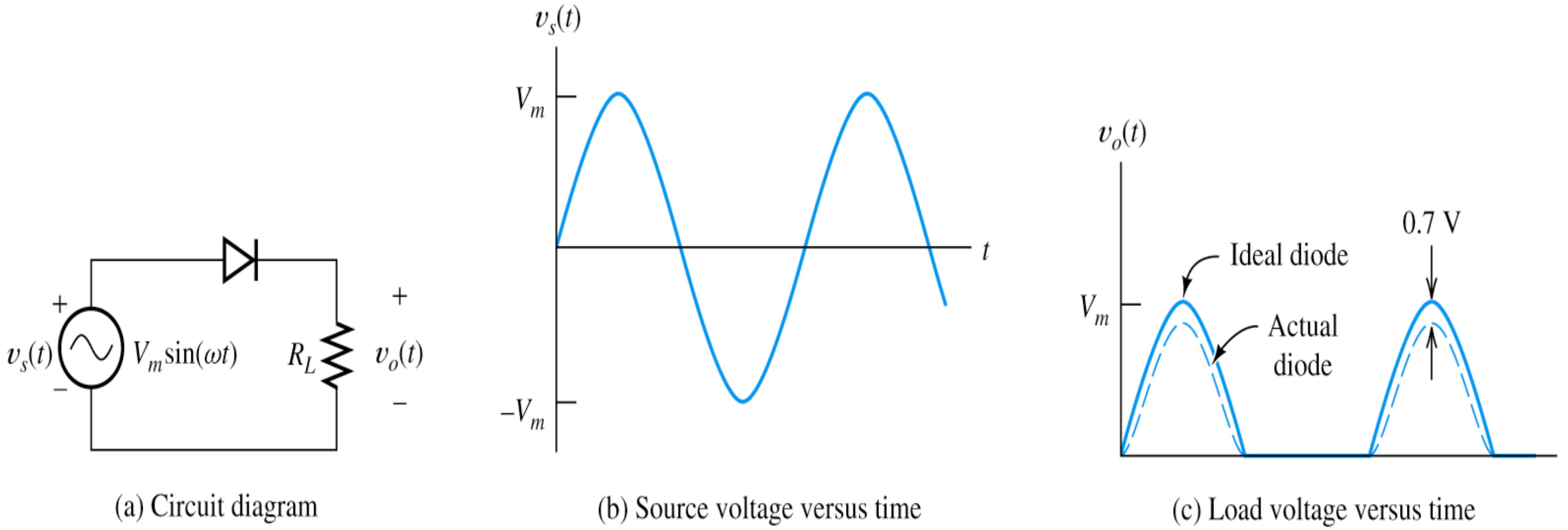


Figure 10.24 Half-wave rectifier with resistive load.

Battery-Charging Circuit

- 只有$v_s(t)>V_B$ (battery電壓)有電流輸出充電
- 當$v_s(t)<V_B$, diode off, 避免電池放電

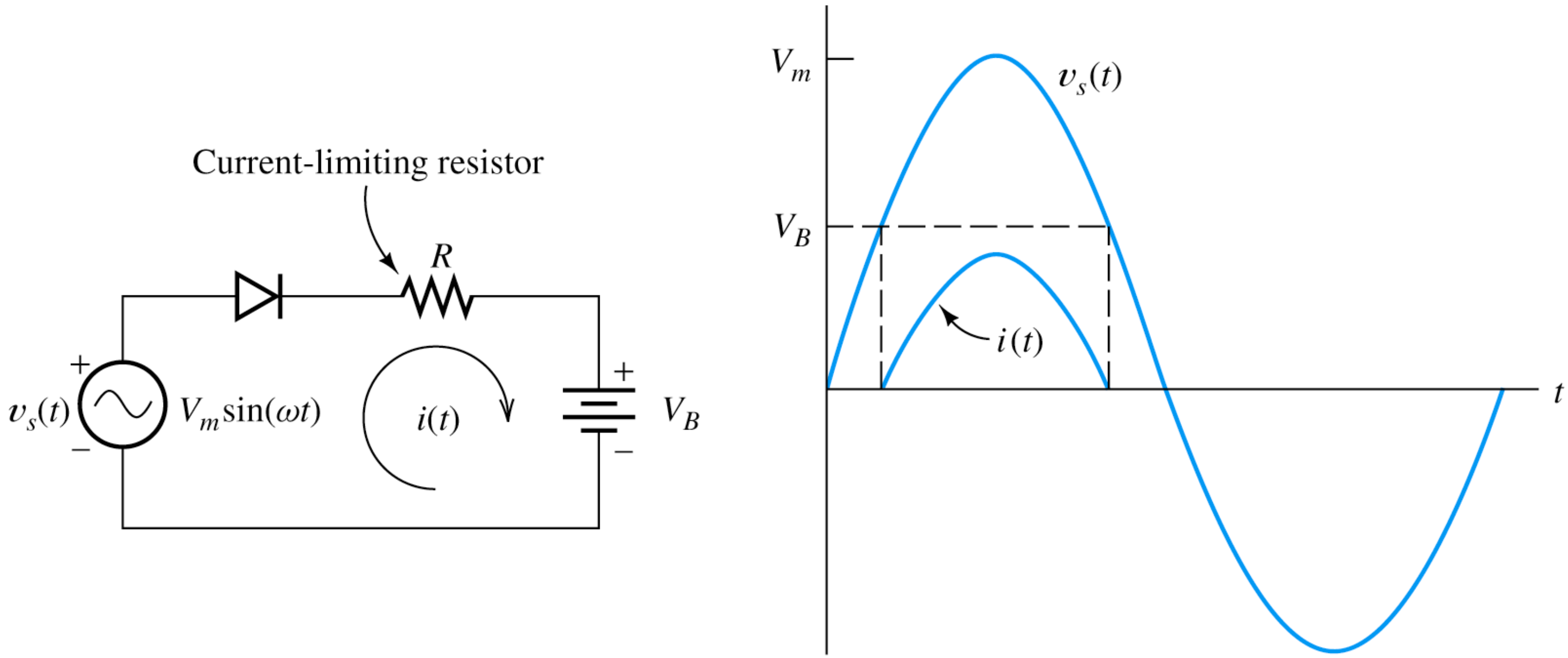


Figure 10.25 Half-wave rectifier used to charge a battery.

Half-Wave Rectifier (半波整流) with Smoothing Capacitor

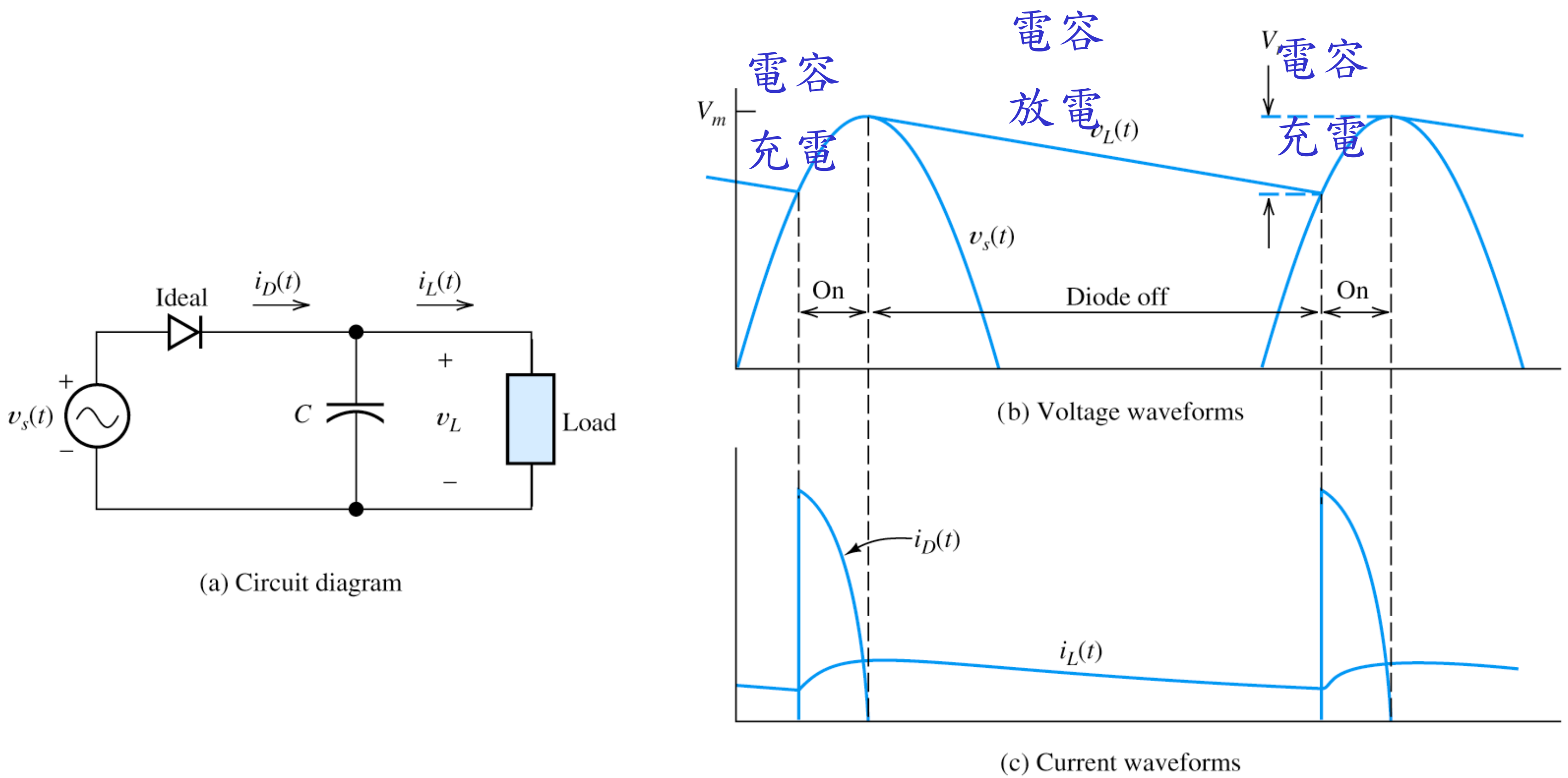
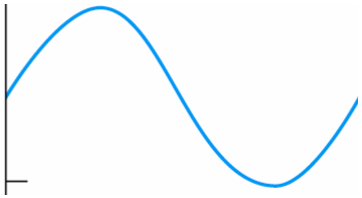


Figure 10.26 Half-wave rectifier with smoothing capacitor.

Full-Wave Rectifier (全波整流)

- 利用兩個電壓源兩個diode



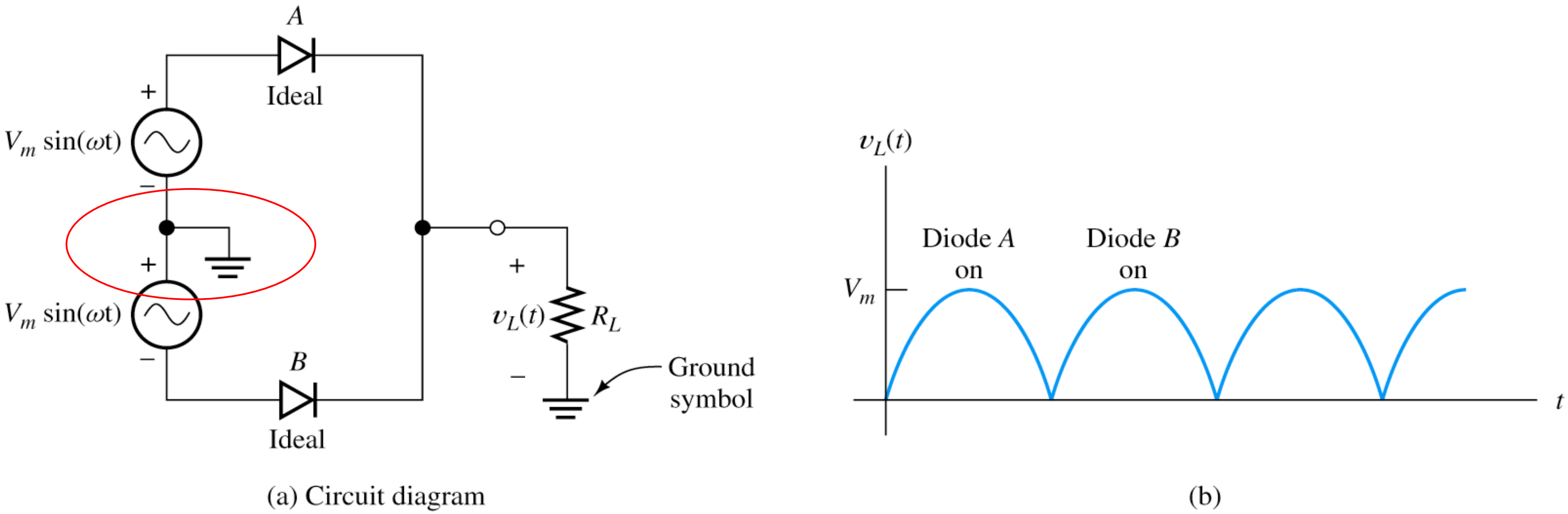
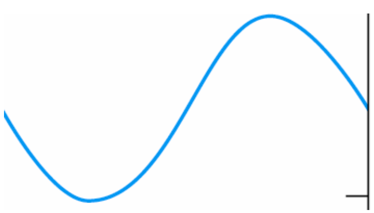


Figure 10.27 Full-wave rectifier.



- 利用一個電壓源

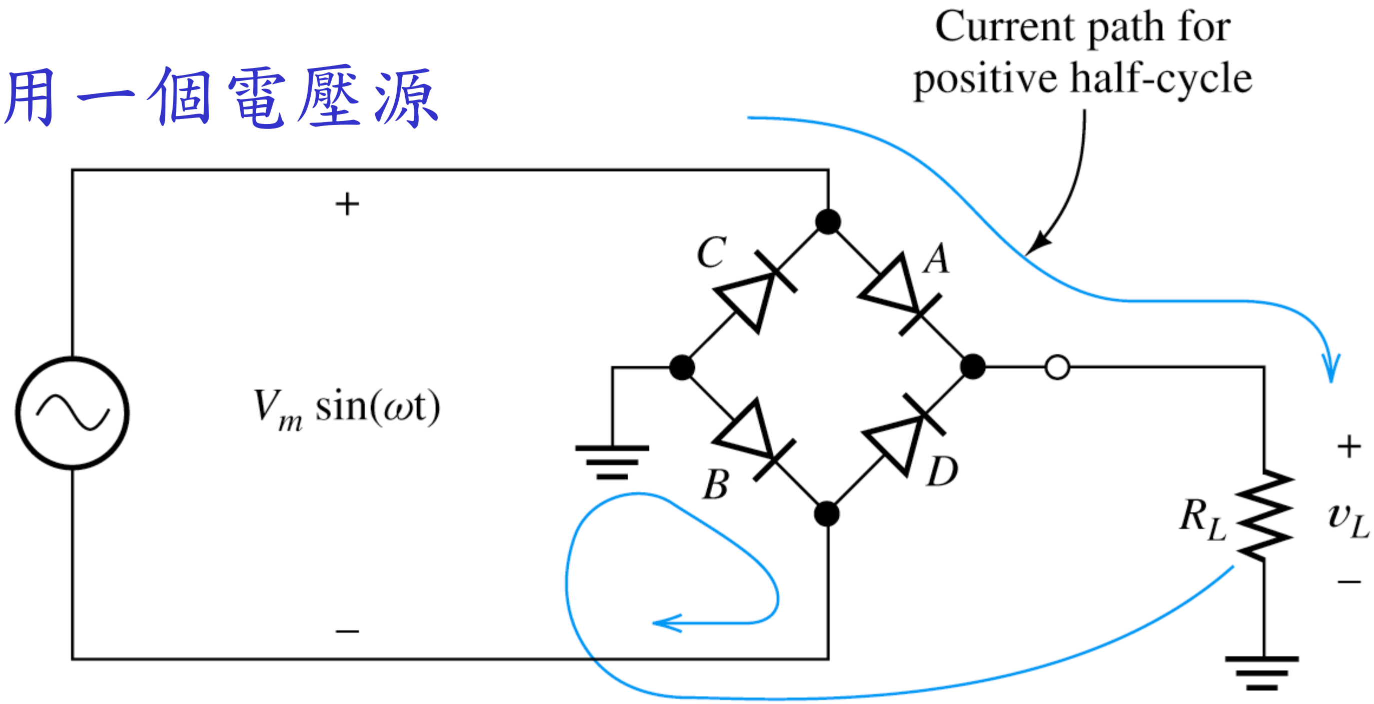
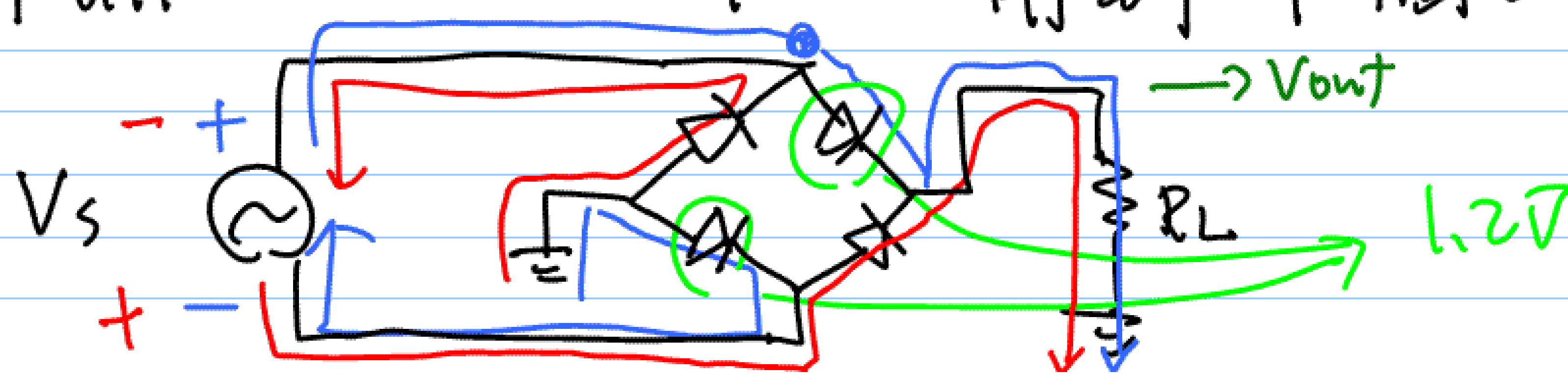


Figure 10.28 Diode-bridge full-wave rectifier.

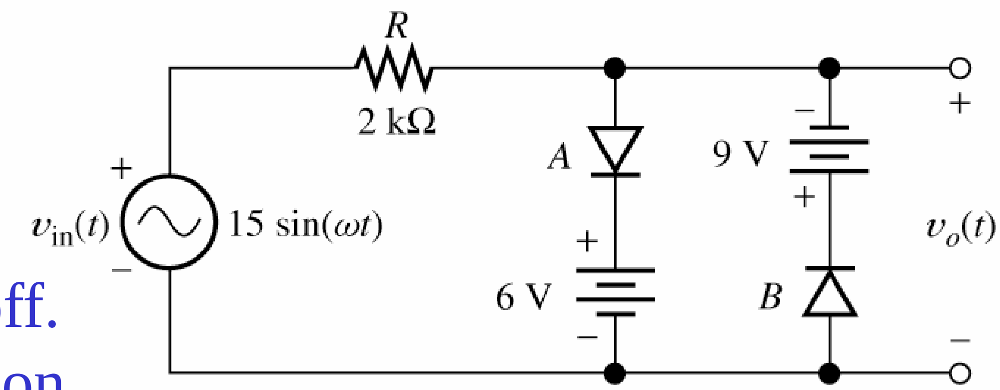
Full-Wave Rectifier: 用到 4 個 diodes



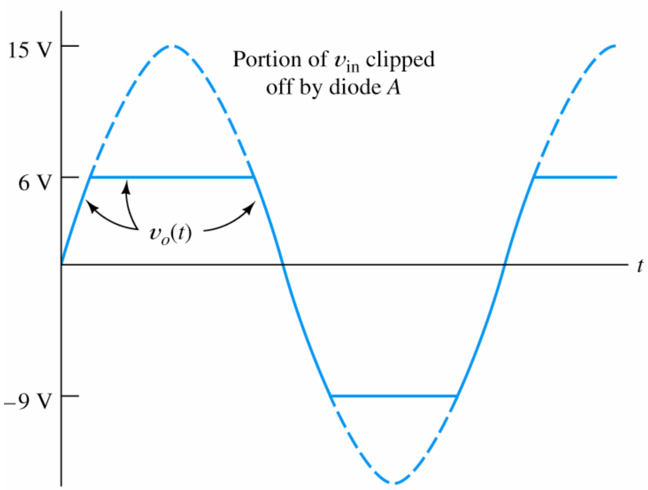
10.7 Wave-Shaping Circuits

Clipper Circuits
剪波器

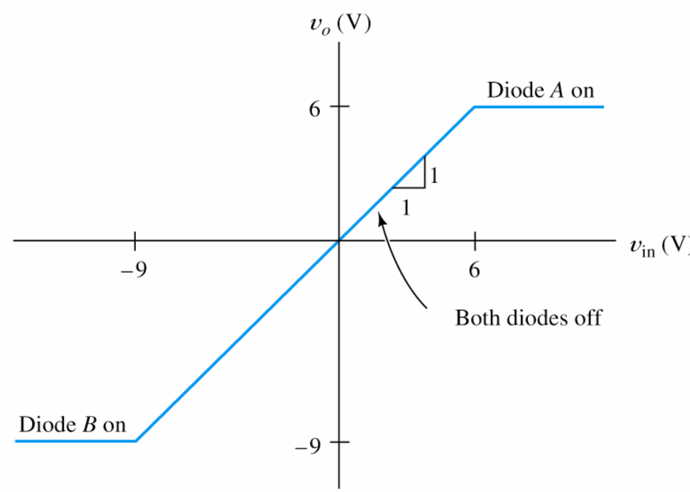
- 當v_{in}>6V，DA on, DB off.
- 當v_{in}<-9V，DA off, DB on.
- 當-9V< v_{in} <6V，DA&DB off.



(a) Circuit diagram



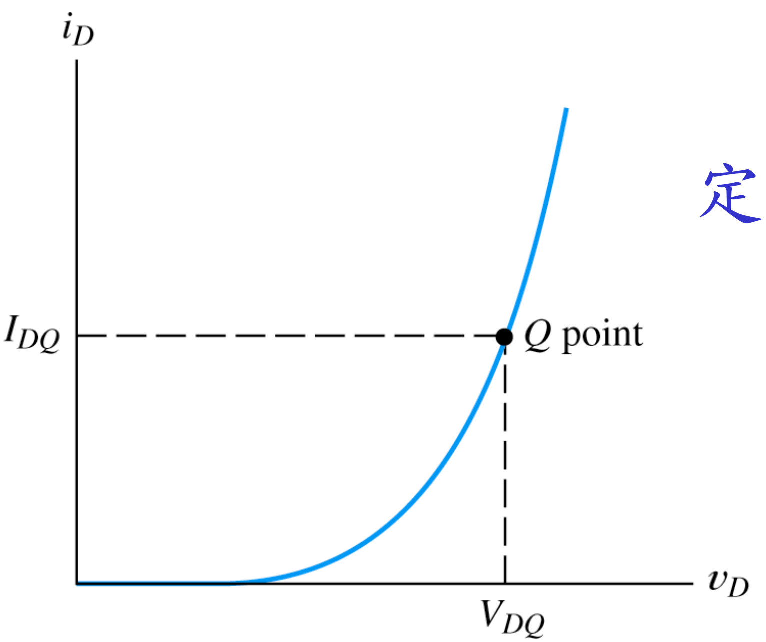
(b) Waveforms



(c) Transfer characteristic

10.8 LINEAR SMALL-SIGNAL EQUIVALENT CIRCUITS

- 分析在靜態操作點(quiescent point, Q point)上,電壓微幅改變(small signal)時，電流的變化。
- The small-signal equivalent circuit for a diode is a resistance.



$$\Delta i_D \cong \left(\frac{di_D}{dv_D}\right)_Q \Delta v_D$$

定義dynamic resistance of the diode

$$r_d \cong \left[\left(\frac{di_D}{dv_D}\right)_Q\right]^{-1}$$

$$i_d = \frac{v_d}{r_d}$$

$$r_d \cong \left[\left(\frac{di_D}{dv_D} \right)_Q \right]^{-1} = ?$$

$$i_D = I_S \left[\exp\left(\frac{v_D}{nV_T} \right) - 1 \right]$$ (Shockley Equation)

$$\frac{di_D}{dv_D} = I_S \frac{1}{nV_T} \exp\left(\frac{v_D}{nV_T} \right)$$

At Q-point $v_D = v_{DQ}$

$$\left(\frac{di_D}{dv_D} \right)_Q = I_S \frac{1}{nV_T} \exp\left(\frac{v_{DQ}}{nV_T} \right)$$

At $v_D = v_{DQ}$, determine i_{DQ}

$$I_{DQ} \cong I_S \exp\left(\frac{v_{DQ}}{nV_T} \right)$$ (將$v_D = v_{DQ}$ 代入Shockley Equation, 且忽略-1 項)

Q點越來越高

$$\left(\frac{di_D}{dv_D}\right)_Q = I_S \frac{1}{nV_T} \exp\left(\frac{v_{DQ}}{nV_T}\right) = \frac{I_{DQ}}{nV_T}$$

$$r_d = \frac{nV_T}{I_{DQ}}$$

- I_{DQ}越大，斜率 $(1/r_d)$越大，r_d越小

- *假設固定ac voltage* v_d，Q點越高(v_D越大), ac current i_d越大

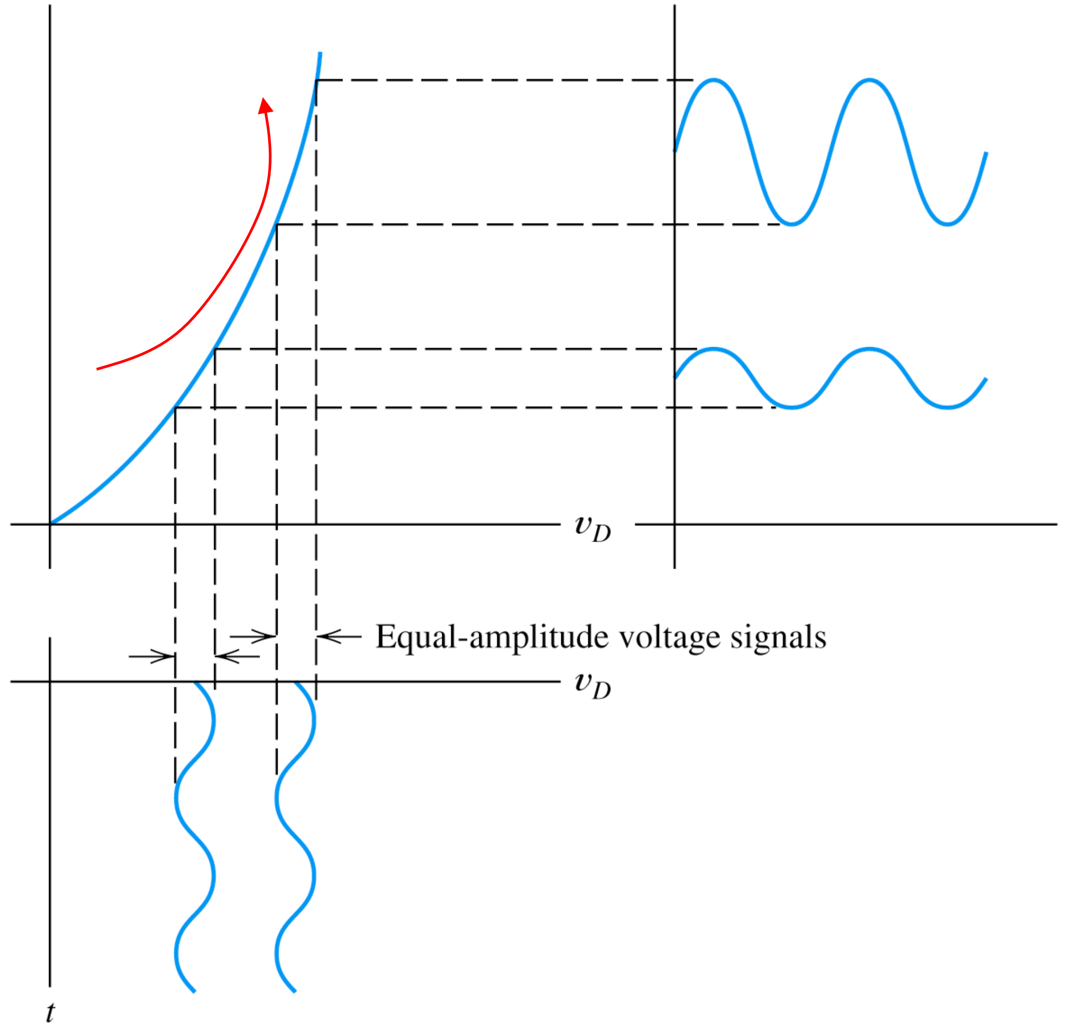
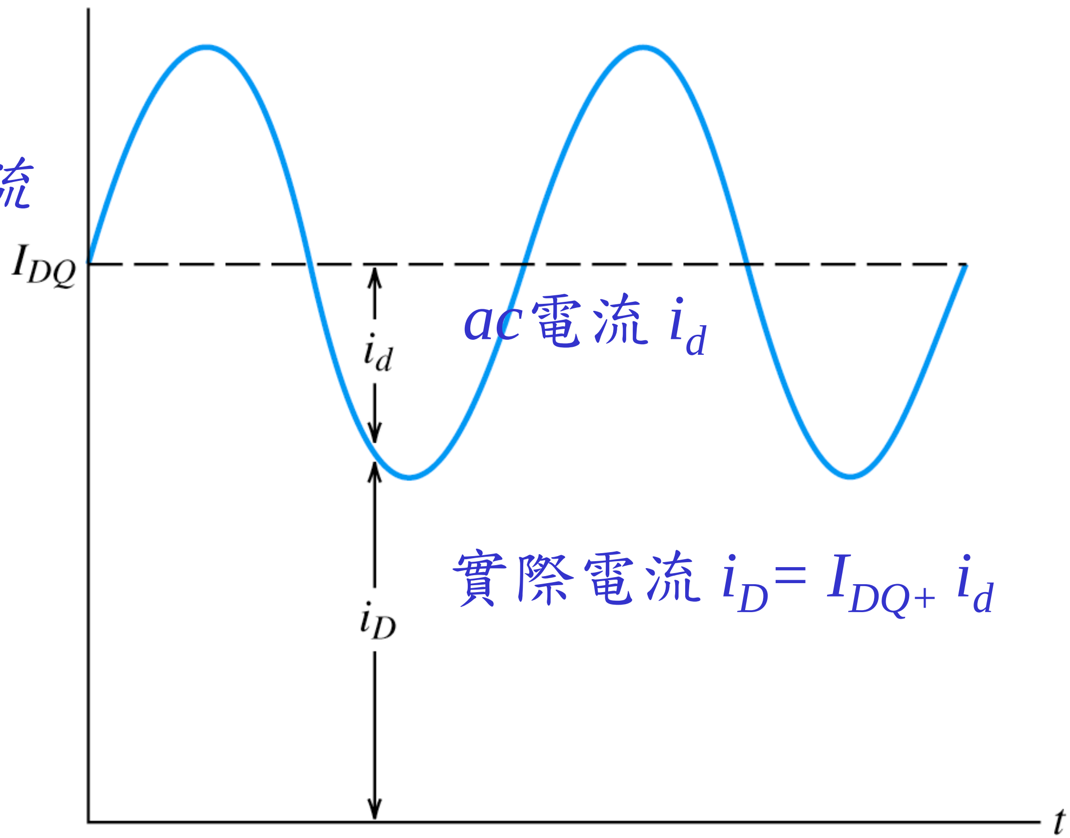


Figure 10.38 As the Q point moves higher, a fixed-amplitude ac voltage produces an ac current of larger amplitude.

Q點DC電流



ac電流 i_d

實際電流 $i_D = I_{DQ} + i_d$

Figure 10.39 Illustration of diode currents.

Notation for Currents and Voltages in Electronic Circuits

- v_D and i_D represent the total instantaneous diode voltage and current. At times, we may wish to emphasize the time-varying nature of these quantities, and then we use $v_D(t)$ and $i_D(t)$

- V_{DQ} and I_{DQ} represent the dc diode current and voltage at the quiescent point.

- $\boldsymbol{v}_d$ and $\boldsymbol{i}_d$ represent the (small) ac signals. If we wish to emphasize their time varying nature, we use $\boldsymbol{v}_d(\boldsymbol{t})$ and $\boldsymbol{i}_d(\boldsymbol{t})$.