Chapter 12
Field-Effect Transistors
場效電晶體

Field-Effect Transistors (FETs)

- FET (場效電晶體) 是利用電場來控制電流的大小，而且組成電流的載子僅限一種極性，即電洞或是自由電子。
- Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET,金氧半場效電晶體）可分為NMOS (以電子為電流載子)與PMOS(以電洞為電流載子)。
- MOSFET 包含source (源極)、gate (閘極)、drain(汲極)及body(基座)。

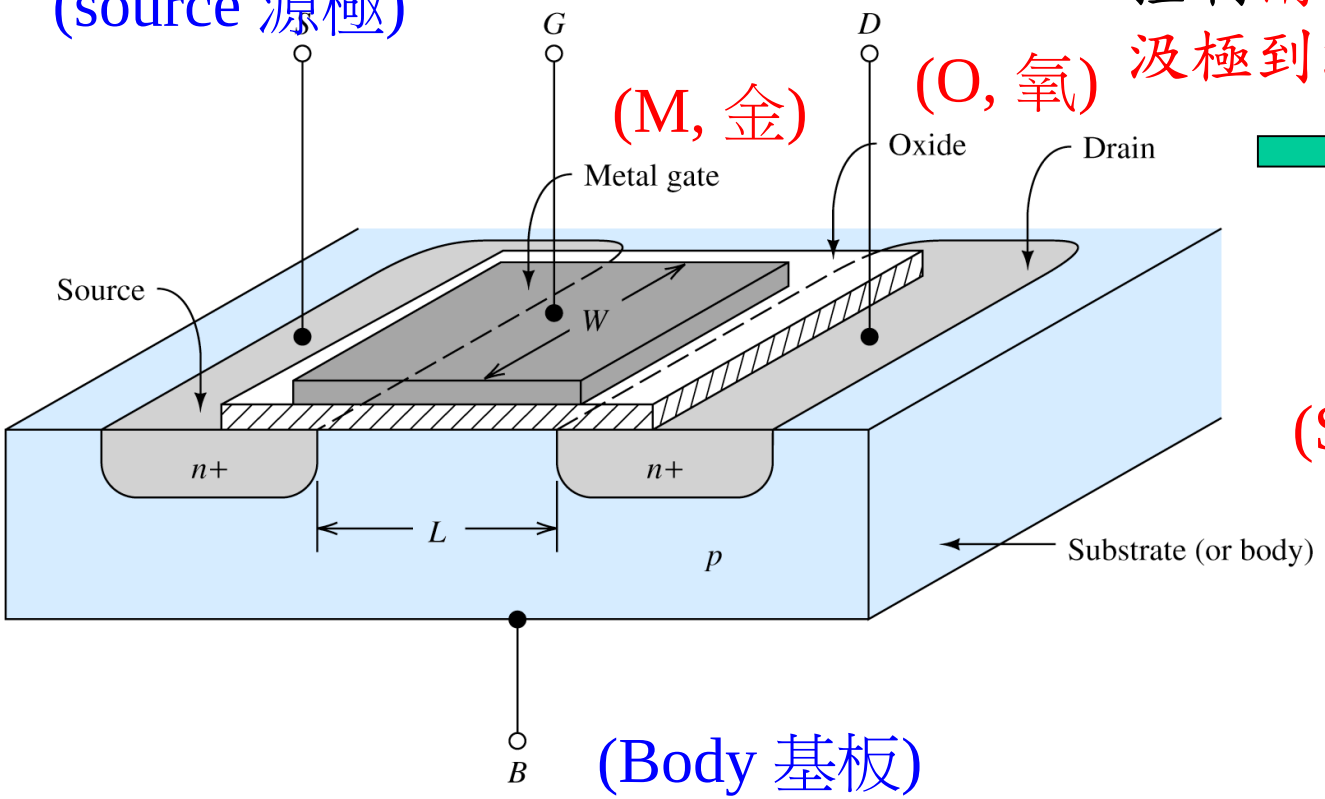
12.1 NMOS AND PMOS TRANSISTORS

NMOS Transistor (n-p-n)

氧化物為絕緣體，沒有電流能進入閘極端；
控制閘極電壓能夠調整汲極到源極的電流

➡ 場效

(source 源極) (gate 閘極) (drain 汲極)



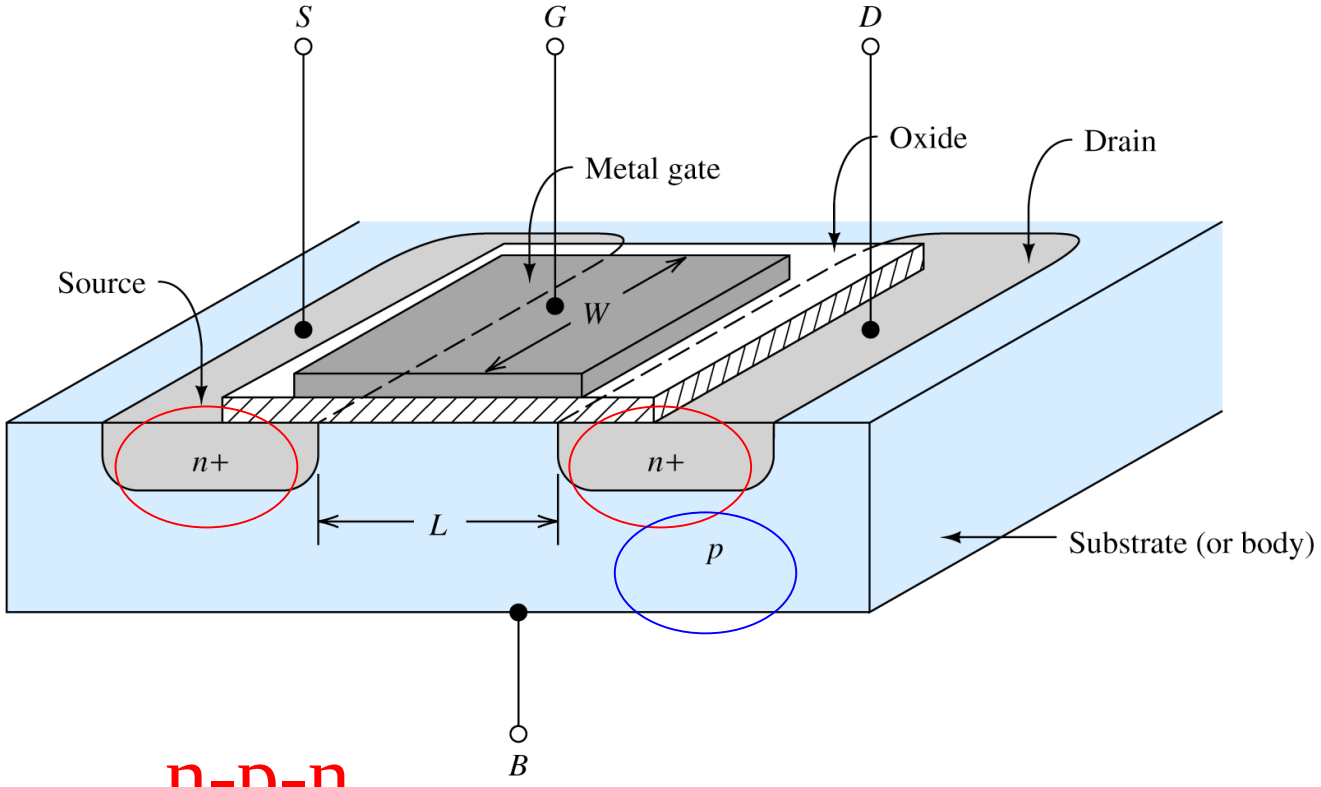
(M, 金) (O, 氧)

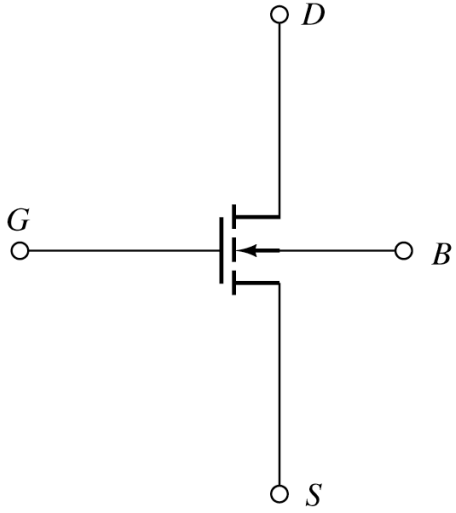
(S, 半)

(Body 基板)

NMOS (n-channel MOS)

- NMOS 之 source (源極)與drain(汲極)為n-type 半導體，body(基座) 為p-type 半導體，gate (閘極)為導體 。





n-p-n

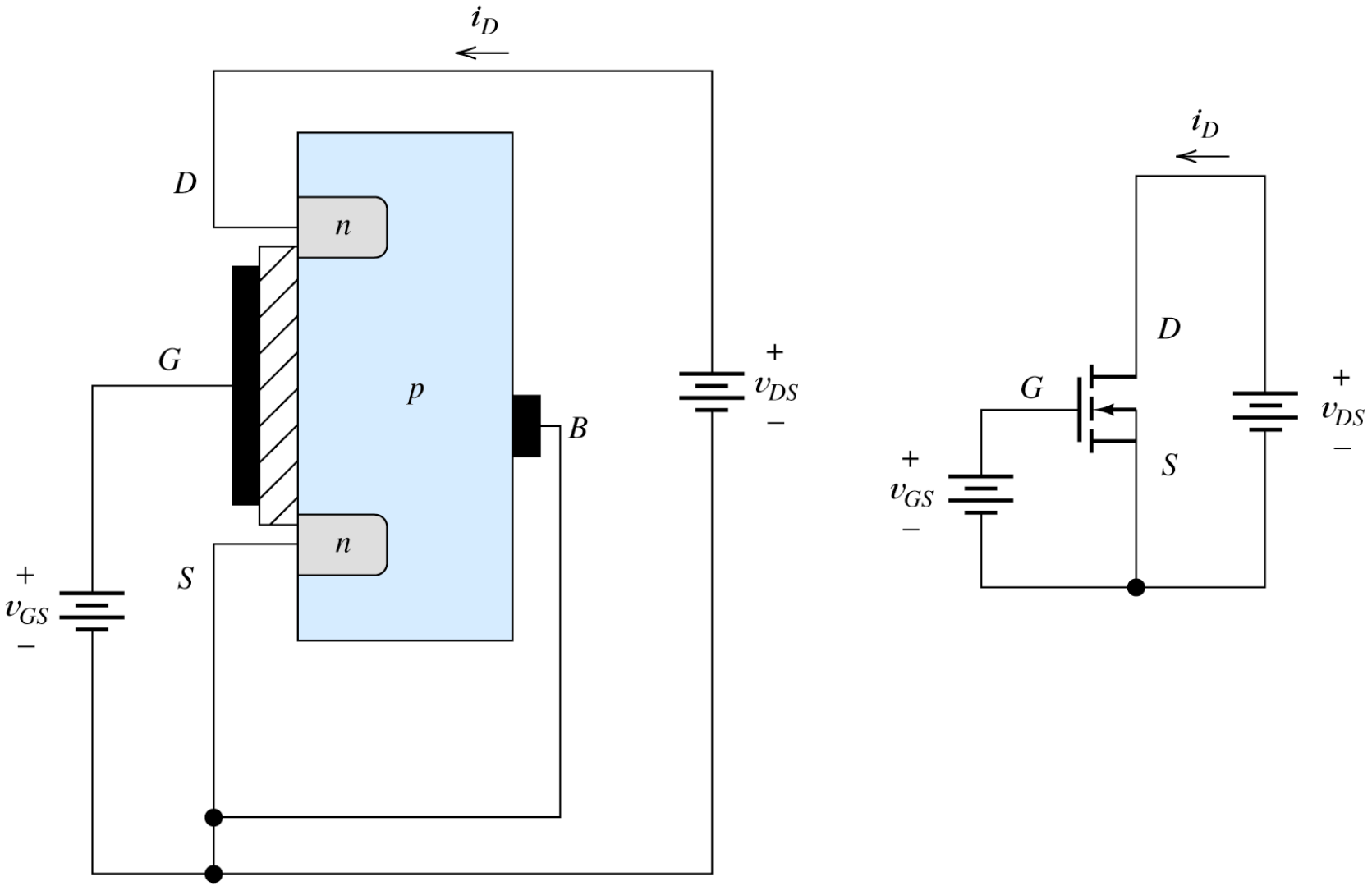


Figure 12.3 For $v_{GS} < V_{to}$, the pn junction between drain and body is reverse biased and $i_D = 0$.

NMOS 的運作 (Operation)

- NMOS 的運作可分為三區(region)
  - Cutoff Region (截止區)

$$v_{GS} \le V_{to}$$

  - Triode Region (三極區) or Linear Region (線性區)

$$v_{GS} > V_{to} \quad \text{and} \quad v_{DS} < v_{GS} - V_{to}$$

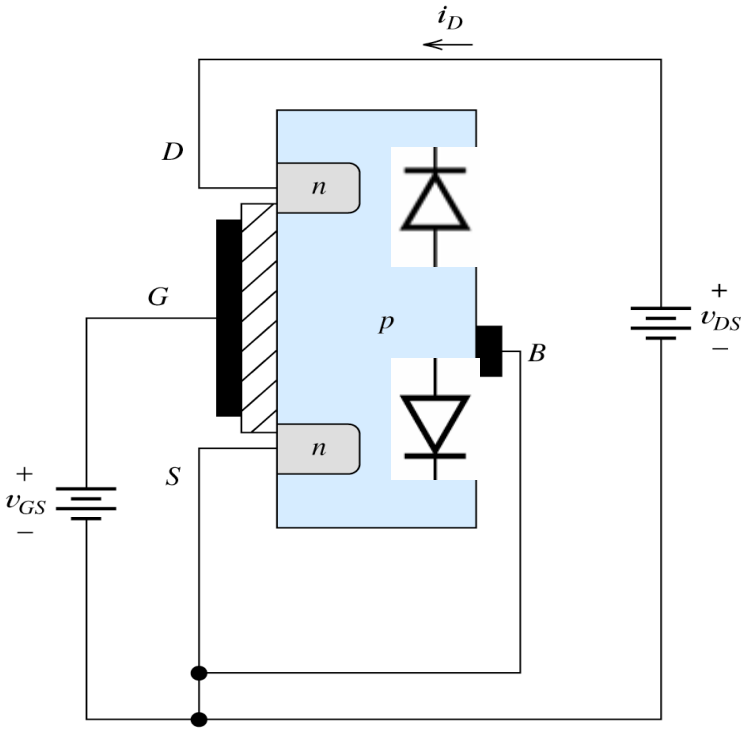
  - Saturation Region (飽合區)

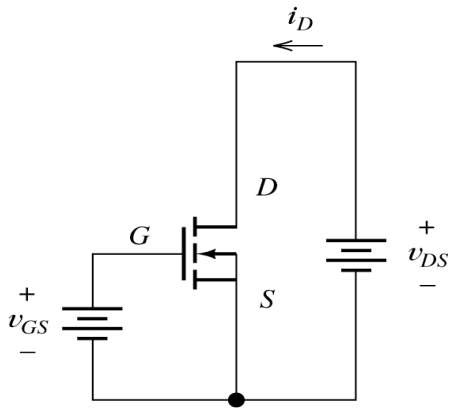
$$v_{GS} > V_{to} \quad \text{and} \quad v_{DS} \ge v_{GS} - V_{to}$$

Operation in the Cutoff Region

- 當閘極(gate)與源極(source)間電壓v_{GS}=0，兩個pn接面(body-source) 與(body-drain)可視為兩個方向相反的二極體，此時MOSFET為截止(cutoff)。

- 當閘極(gate)與源極(source)間電壓v_{GS}逐漸上升到>V_{to}(threshold voltage,臨限電壓)時，則NMOS才會開始導通。



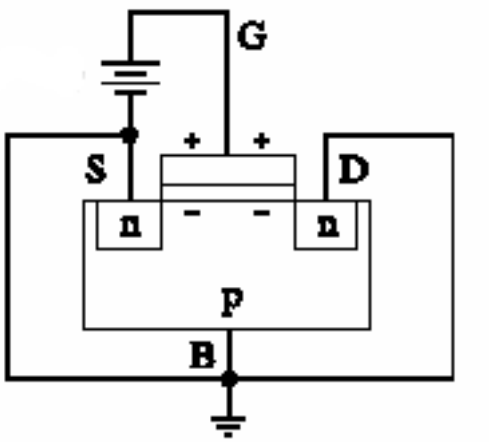


$$i_D = 0 \text{ for } v_{GS} \le V_{to}$$

Operation in the Triode Region

$$v_{GS} > V_{to} \quad \text{and} \quad v_{DS} < v_{GS} - V_{to}$$

- 當閘極(gate)帶正電時，可逐漸吸引自由電子聚集在絕緣層的下方，並將電洞推離絕緣層下方。



$$\begin{cases} v_{GD} > V_{to} \\ v_{DS} > 0 \end{cases} \equiv \begin{cases} v_{GS} - v_{DS} > V_{to} \\ v_{DS} > 0 \end{cases}$$

$$\equiv 0 < v_{DS} < v_{GS} - V_{to}$$

Operation in the Triode Region

$$v_{GS} > V_{to} \quad \text{and} \quad v_{DS} < v_{GS} - V_{to}$$

- 當閘極(gate)與源極(source)間電壓v_{GS}逐漸上升到>V_{to}(threshold voltage,臨限電壓)，且在drain和source之間加有電壓v_{DS}，則形成n-type通道(channel)，通道中的自由電子受到外加電場的驅動，形成汲極電流(drain current)i_D，其方向從drain流向source，和通道中的電子流方向相反。
- 當v_{DS}很小時，i_D與v_{DS}成正比，亦與v_{GS} - V_{to}成正比。
- 由於有氧化絕緣層，故閘極電流 $i_G = 0$。

$$v_{DS} < v_{GS} - V_{to} \equiv v_{GS} - v_{DS} > V_{to} \equiv v_{GD} > V_{to}$$

Operation in the Triode Region

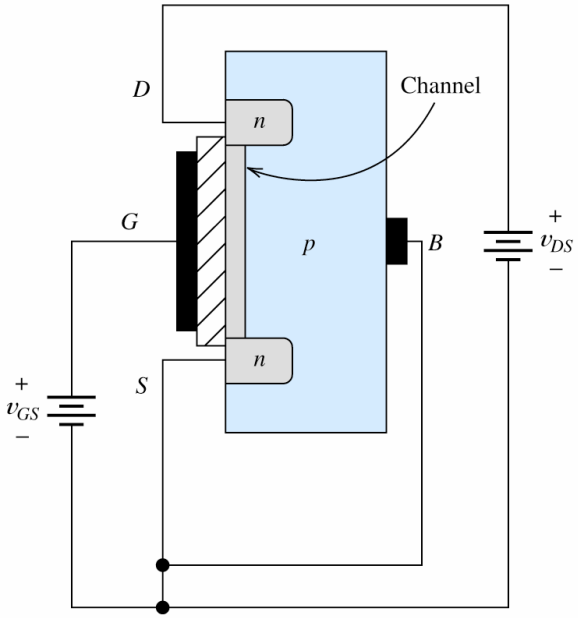
•In the triode region, the NMOS behaves as a resistor connected between drain and source, but the resistance decreases as v_{GS} increases.

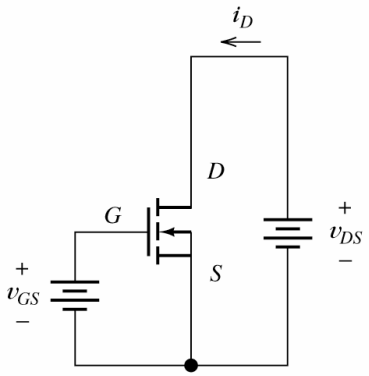
$$i_D = K\left[2\left(v_{GS} - V_{to}\right)v_{DS} - v_{DS}^2\right]$$

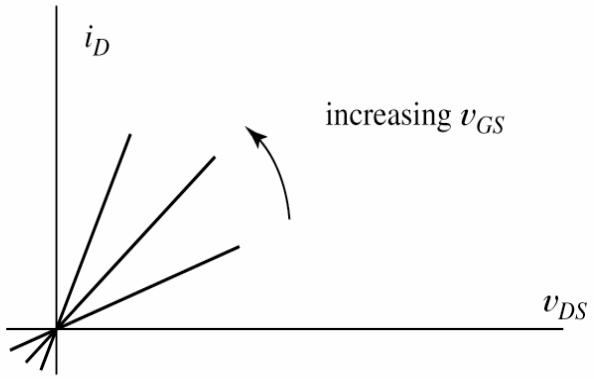
0, if v_{DS}~0

$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

Device parameter



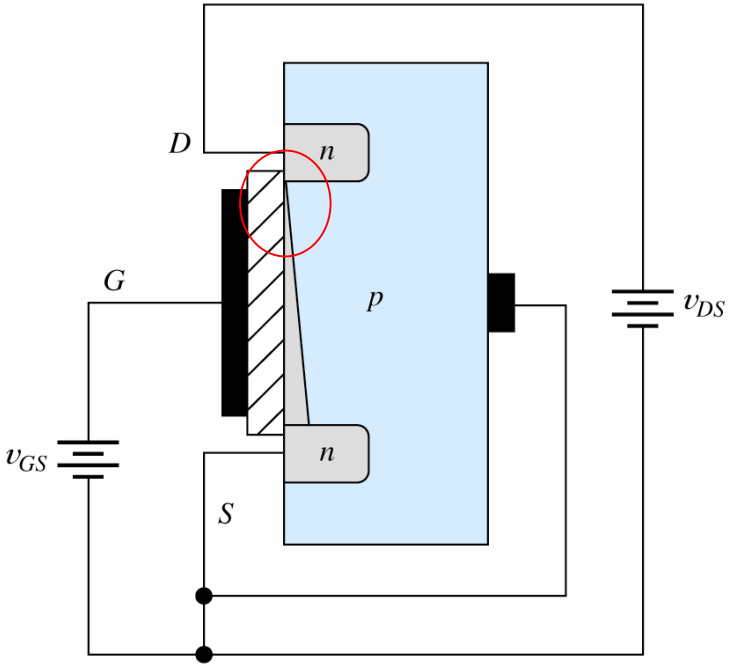


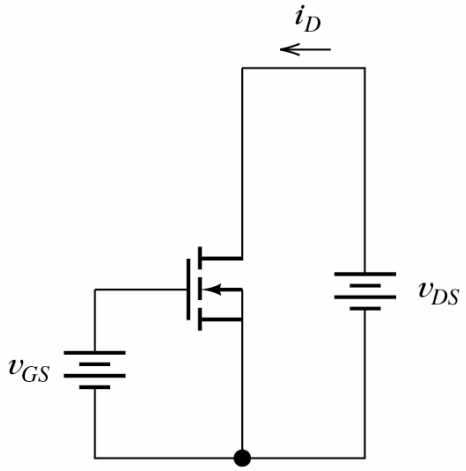


Operation in the Saturation Region

$$v_{GS} > V_{to} \quad \text{and} \quad v_{DS} \geq v_{GS} - V_{to}$$

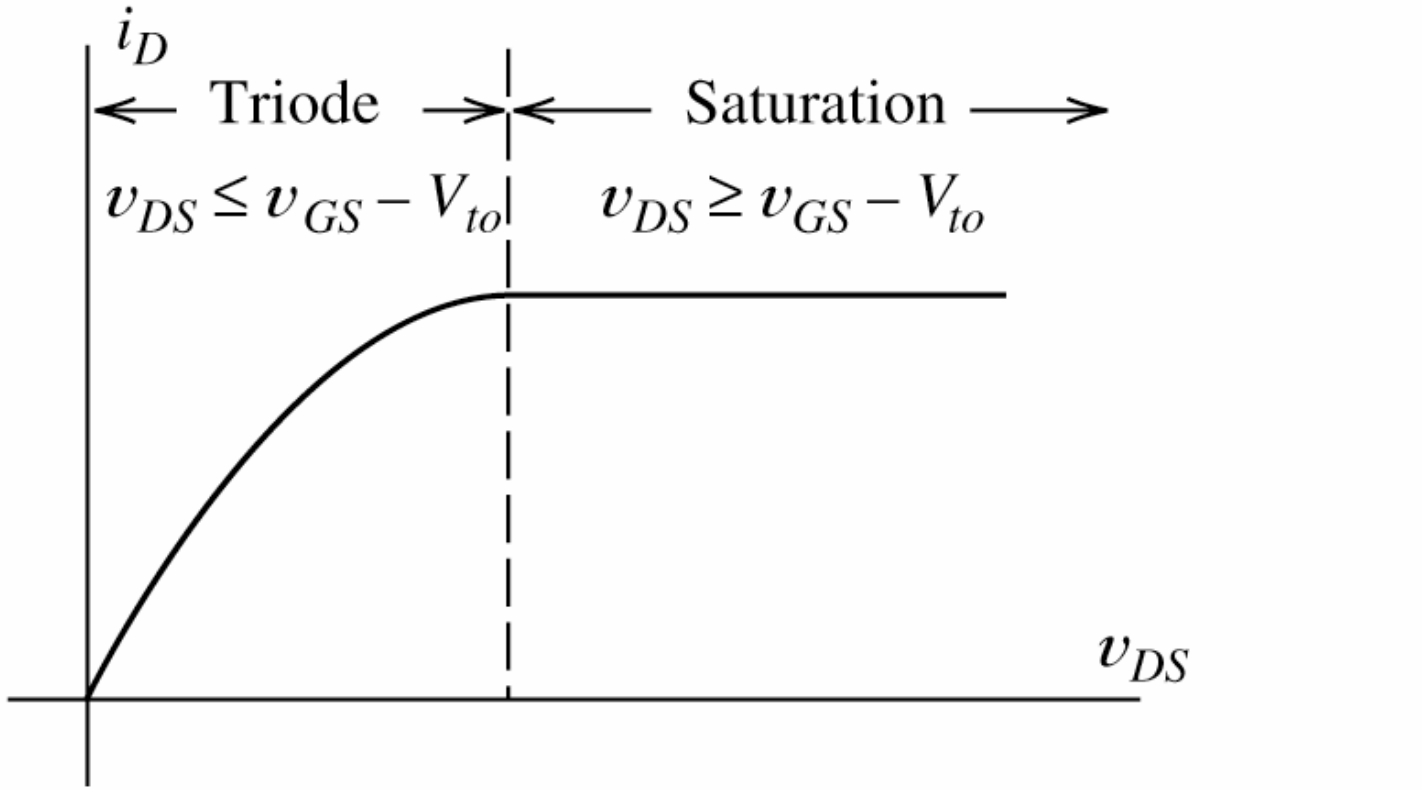
- 當drain和source之間電壓$v_{DS} \geq v_{GS} - V_{to}$(or $v_{GD} \leq V_{to}$) 則n-type通道在drain端寬度變為0，v_{DS}再變大，i_D不再上升，稱為飽合區。





Operation in the Saturation Region

$$i_D = K\left(v_{GS} - V_{to}\right)^2$$



Boundary between Triode and Saturation Regions

At boundary, 使得n-type通道在drain端寬度剛好為0

$$v_{GD} = V_{to}$$

$$\rightarrow \quad v_{GS} - v_{DS} = V_{to}$$

代入I-V equation in saturation region $i_D = K\left(v_{GS} - V_{to}\right)^2$

$$\rightarrow \quad i_D = K v_{DS}^2 \qquad (\because v_{GS} - V_{to} = v_{DS})$$

Boundary between Triode and Saturation Regions

將 $v_{GS} - V_{to} = v_{DS}$ 代入I-V equation in triode region

$$i_D = K\left[2\left(v_{GS} - V_{to}\right)v_{DS} - v_{DS}^2\right]$$

$$i_D = K\left[2v_{DS}^2 - v_{DS}^2\right] = Kv_{DS}^2$$

兩者結果一樣。

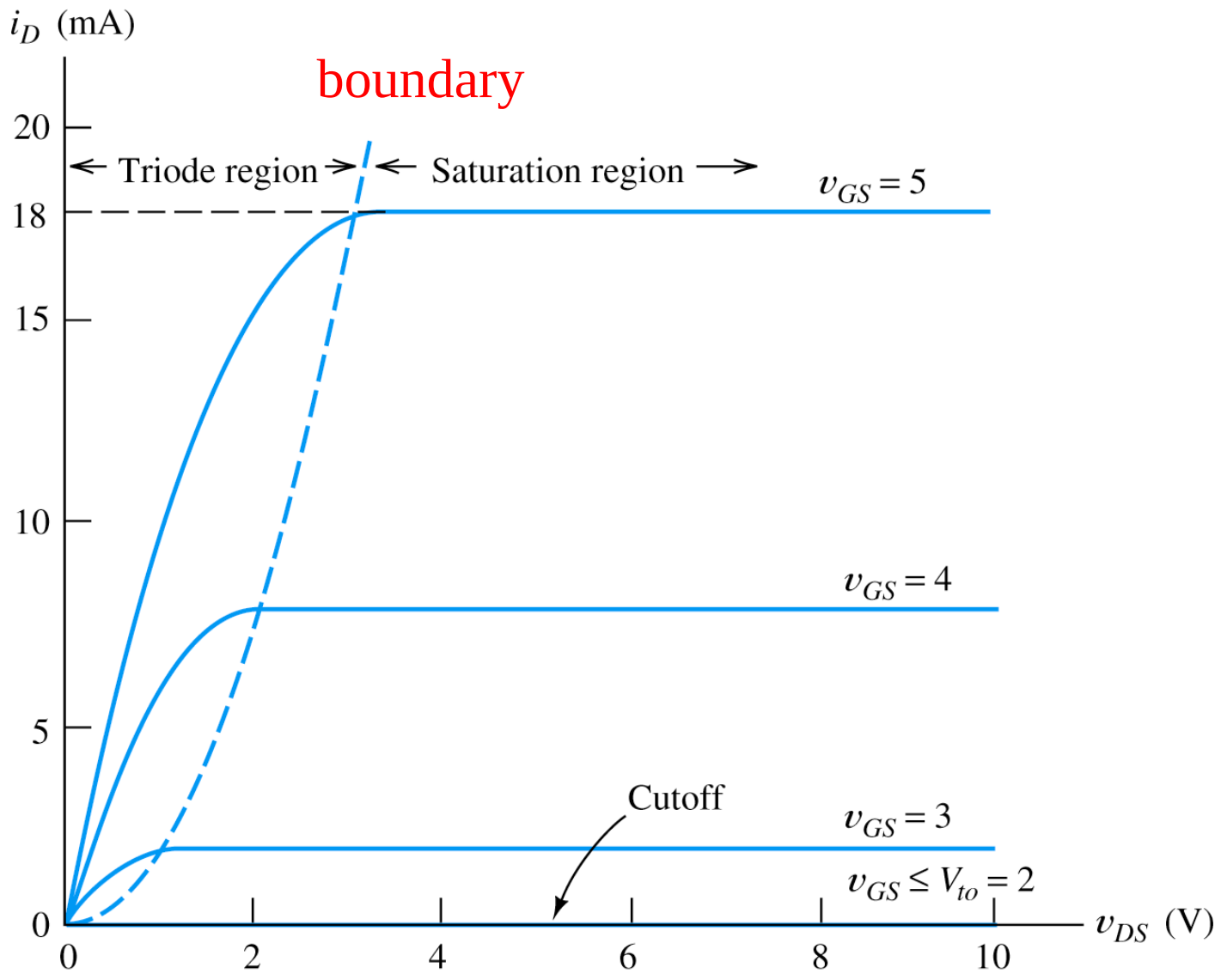


Figure 12.6 Characteristic curves for an NMOS transistor.

Example 12.1

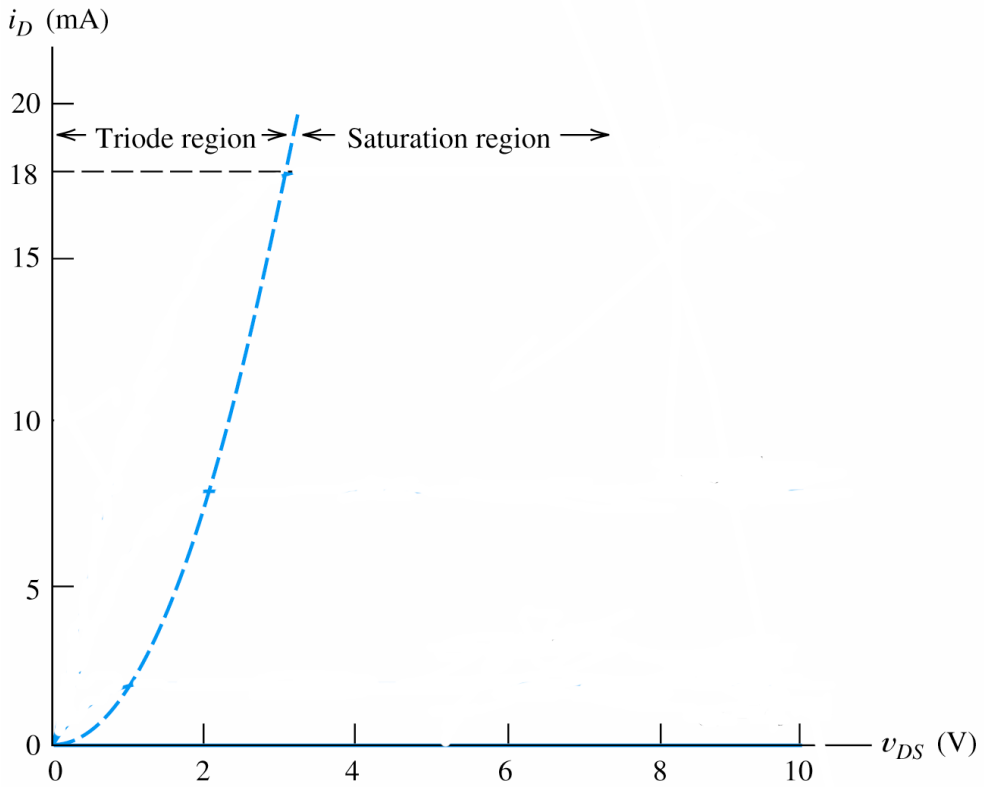
A NMOS transistor W=160*u*m, L=2*u*m, *KP*=50*u*A/V^2, and V_{to}=2 V. Plot the drain characteristic curves to scale for v_{GS}=0, 1,2, 3, 4, and 5 V.

1. 求 *K*

$$K = \left(\frac{W}{L}\right)\frac{KP}{2} = 2mA/V^2$$

2. 求 **boundary**

$$i_D = Kv^2{}_{DS} = 2\times10^{-3}\times v_{DS}^2$$



3. 求 **saturation currents**

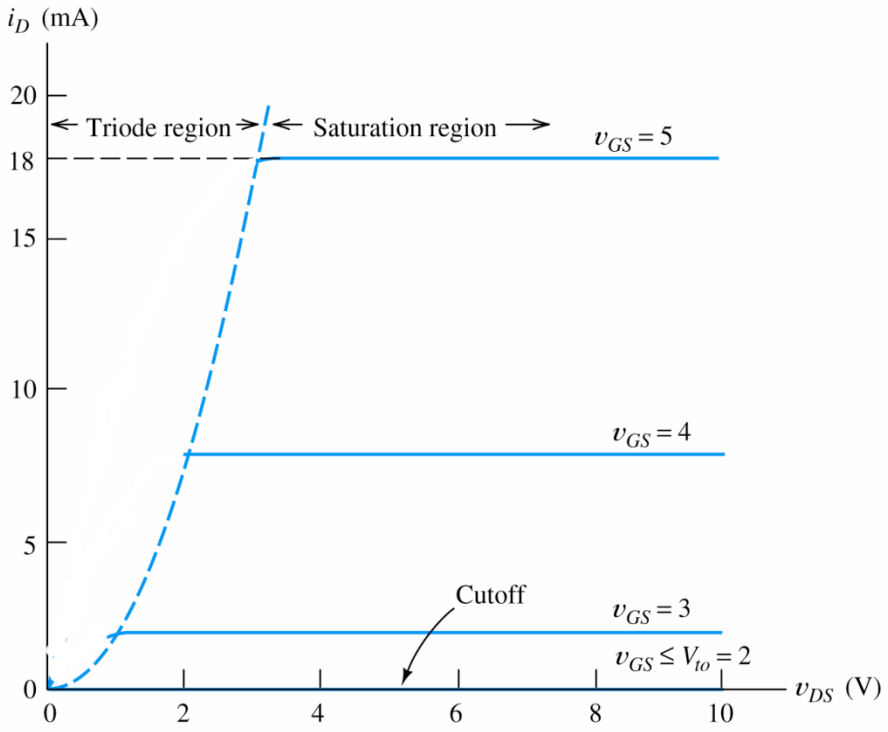
$$i_D = K(v_{GS} - V_{to})^2 = 2\times10^{-3}\times(v_{GS} - 2)^2$$

$$i_D = 18mA \quad \text{for } v_{GS} = 5V$$

$$i_D = 8mA \quad \text{for } v_{GS} = 4V$$

$$i_D = 2mA \quad \text{for } v_{GS} = 3V$$

$$i_D = 0mA \quad \text{for } v_{GS} = 2V$$



4. Plot characteristics in the triode region (parabola 拋物線).

$$i_D = K\left[2\left(v_{GS} - V_{to}\right)v_{DS} - v_{DS}^2\right],$$

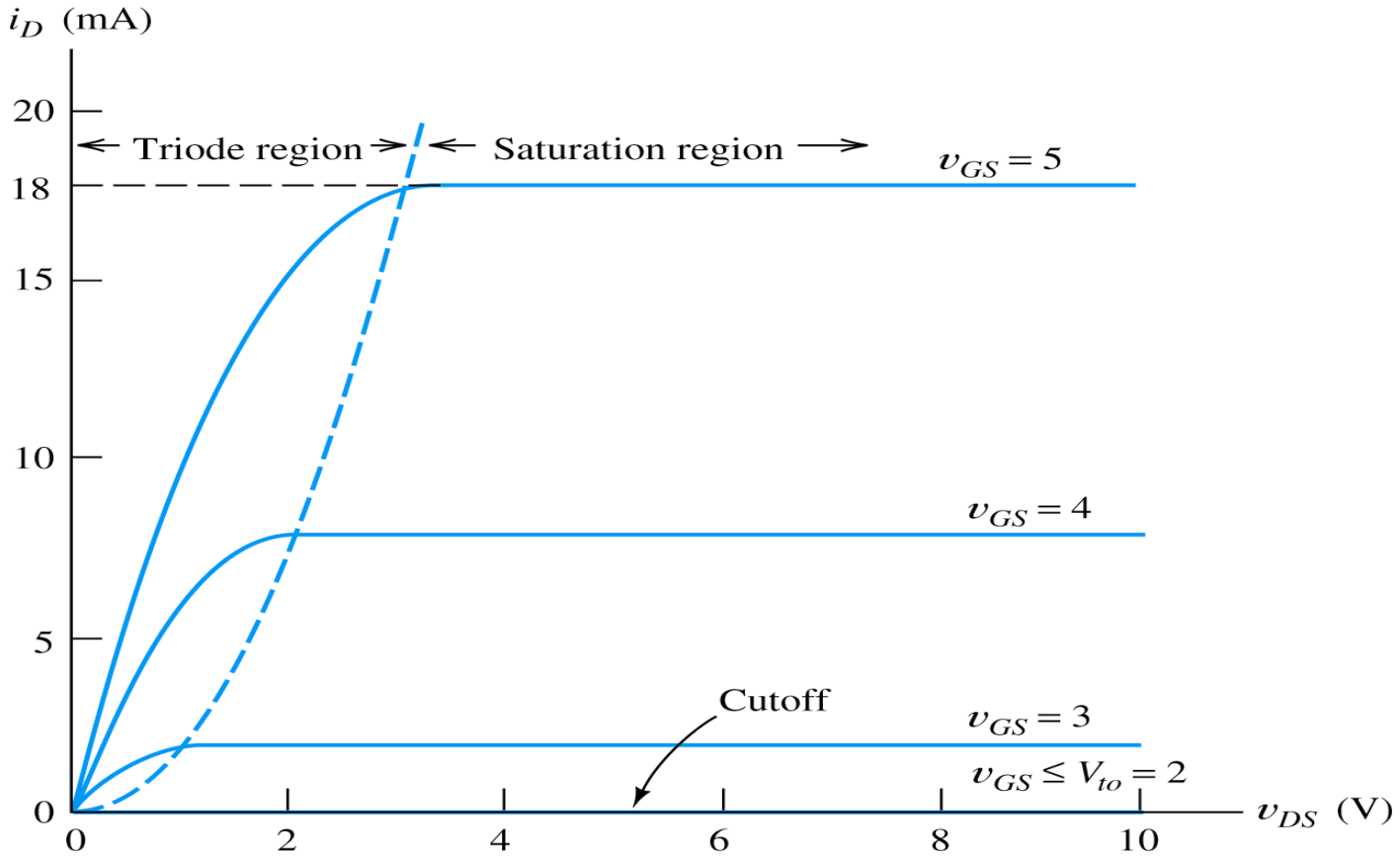
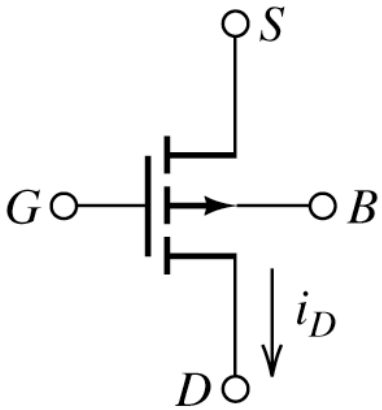


Figure 12.6 Characteristic curves for an NMOS transistor.

PMOS

- PMOS 之 source 與drain為p-type 半導體，body為n-type 半導體，gate (閘極)為導體 。
- 以電洞為電流載子。



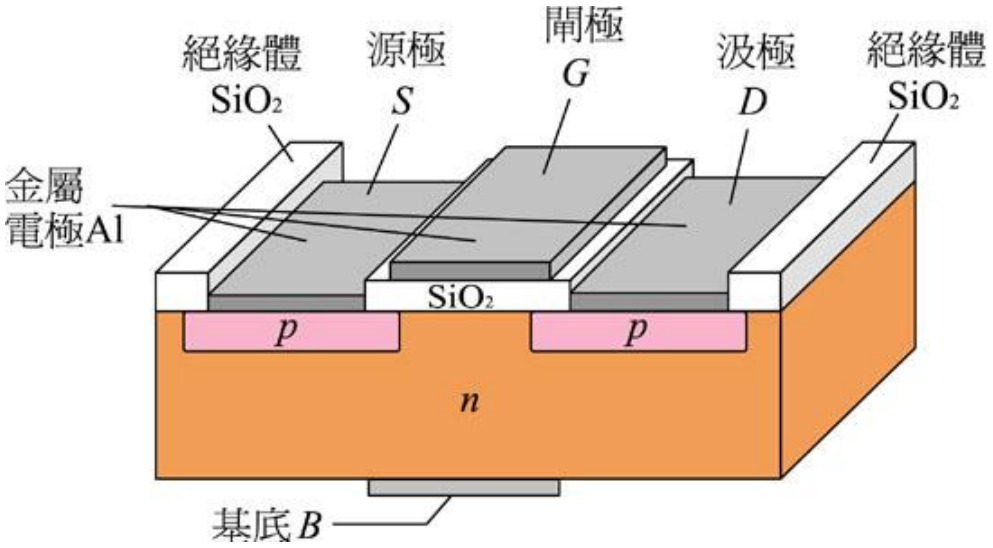
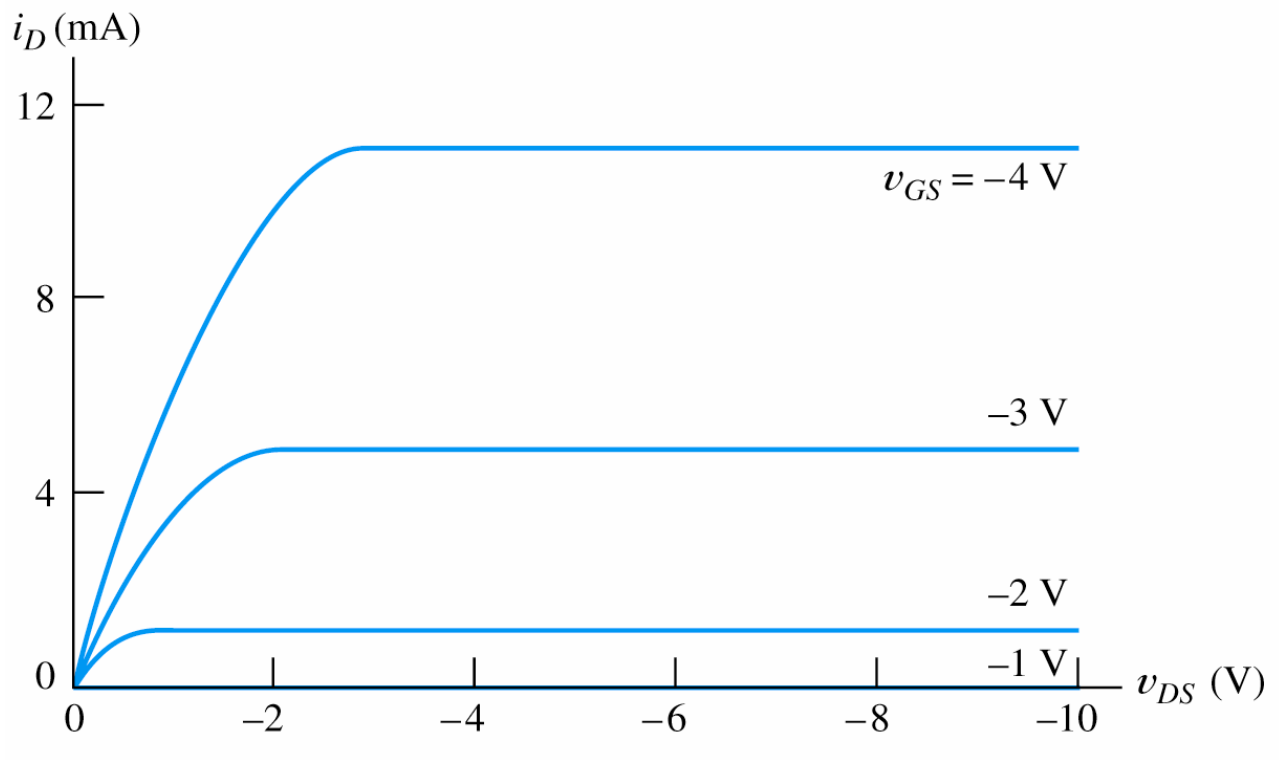
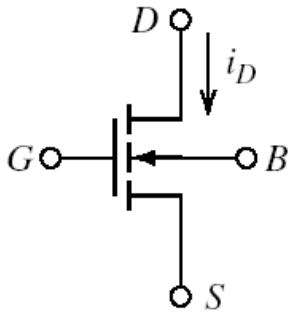
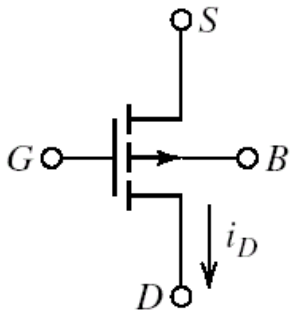


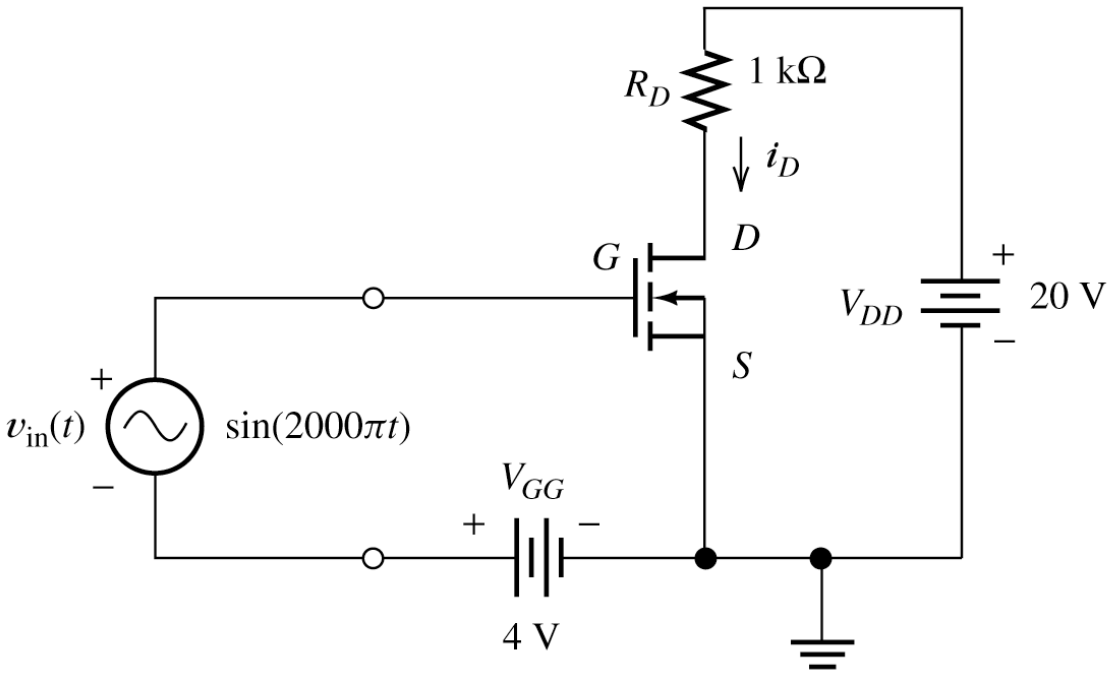
Figure 12.8 Circuit symbol for PMOS transistor.


i_D (mA)
12
8
4
0
$v_{GS} = -4$ V
–3 V
–2 V
–1 V
v_{DS} (V)
0
–2
–4
–6
–8
–10

MOSFET Summary

	NMOS	PMOS
Circuit symbol		
KP (typical value)	50 μA/V^2	25 μA/V^2
K	(1/2) *KP* (*W*/*L*)	(1/2) *KP* (*W*/*L*)
V_{to} (typical value)	+1 V	–1 V
Cutoff region	$v_{GS} \leq V_{to}$ $i_D = 0$	$v_{GS} \geq V_{to}$ $i_D = 0$
Triode region	$v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$	$v_{GS} \leq V_{to}$ and $0 \geq v_{DS} \geq v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$
Saturation region	$v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$	$v_{GS} \leq V_{to}$ and $v_{DS} \leq v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$
v_{DS} and v_{GS}	Normally assume positive values	Normally assume negative values

12.2 LOAD-LINE ANALYSIS OF A SIMPLE NMOS AMPLIFIER



12.2 LOAD-LINE ANALYSIS OF A SIMPLE NMOS AMPLIFIER

- V_{GG} (dc source) 對NMOS 產生偏壓(bias)，決定操作點， 當ac input 在操作點附近隨時間變化，導致v_{GS}, i_D亦隨時間改變。

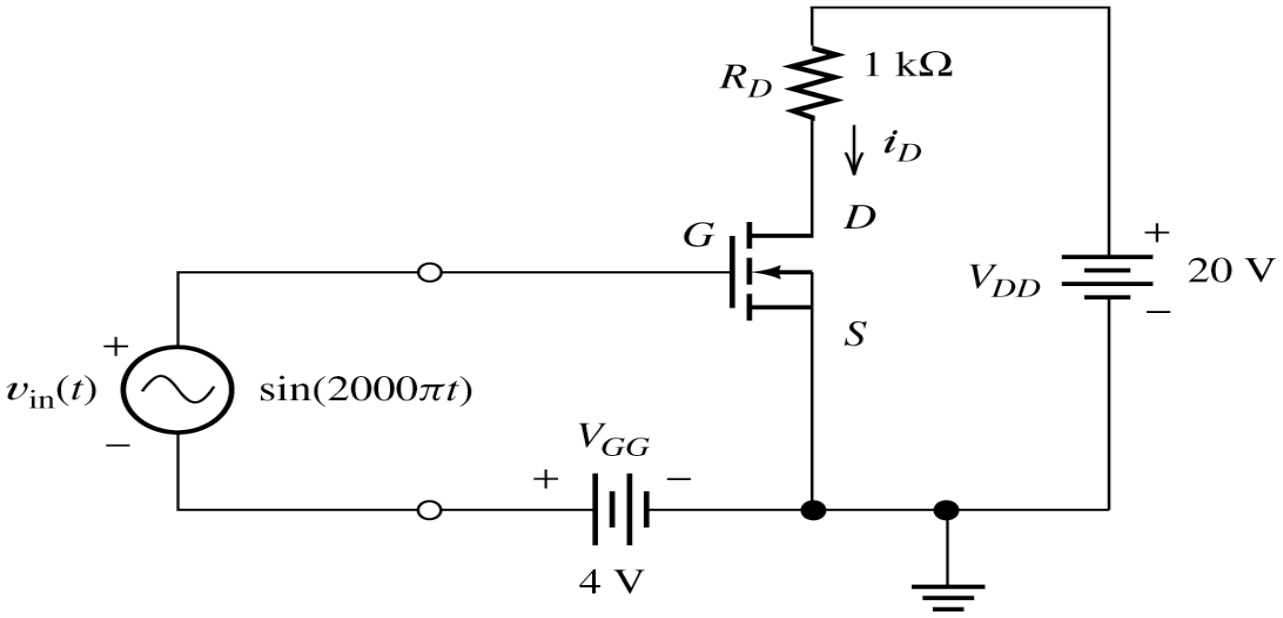


Figure 12.10 Simple NMOS amplifier circuit.

•i_D隨時間改變，導致R_D亦上的壓降隨時間改變，使得v_{DS}產生 ac output。

KVL $v_{GS}(t) = v_{in}(t) + V_{GG} = \sin(2000\pi t) + 4$

Load-line equation $v_{DD} = R_D i_D(t) + v_{DS}(t)$

$$20 = i_D(t)(mA) + v_{DS}(t)$$

Load-line 兩端點

$(v_{DS} = 0\text{V}, i_D = 20mA)$

$(v_{DS} = 20\text{V}, i_D = 0mA)$

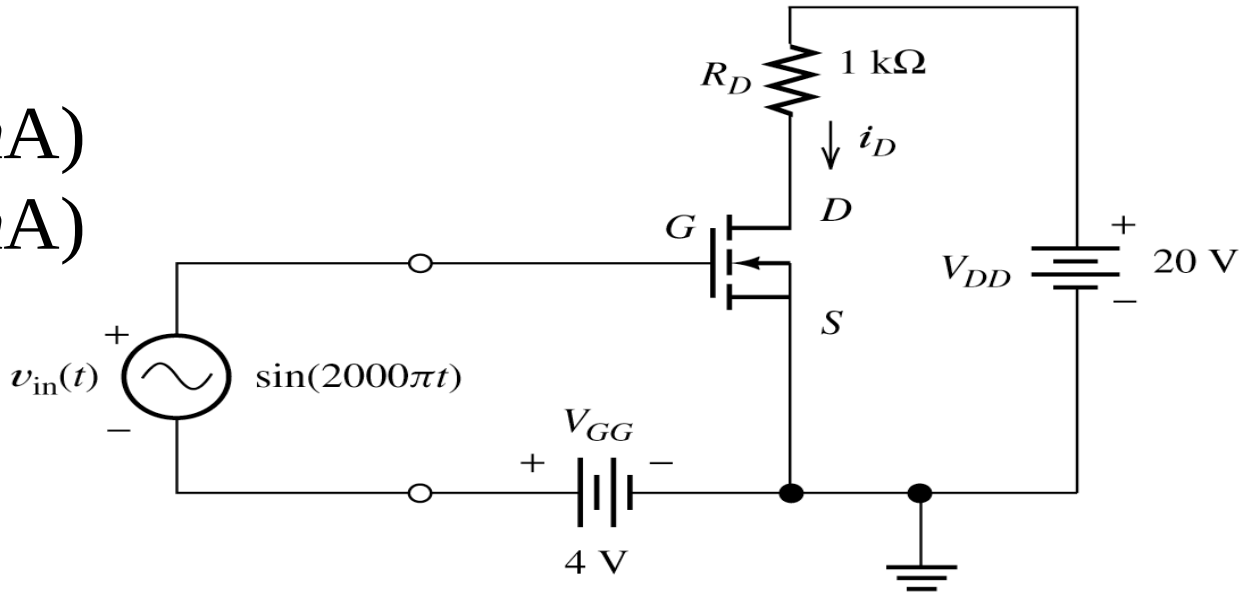
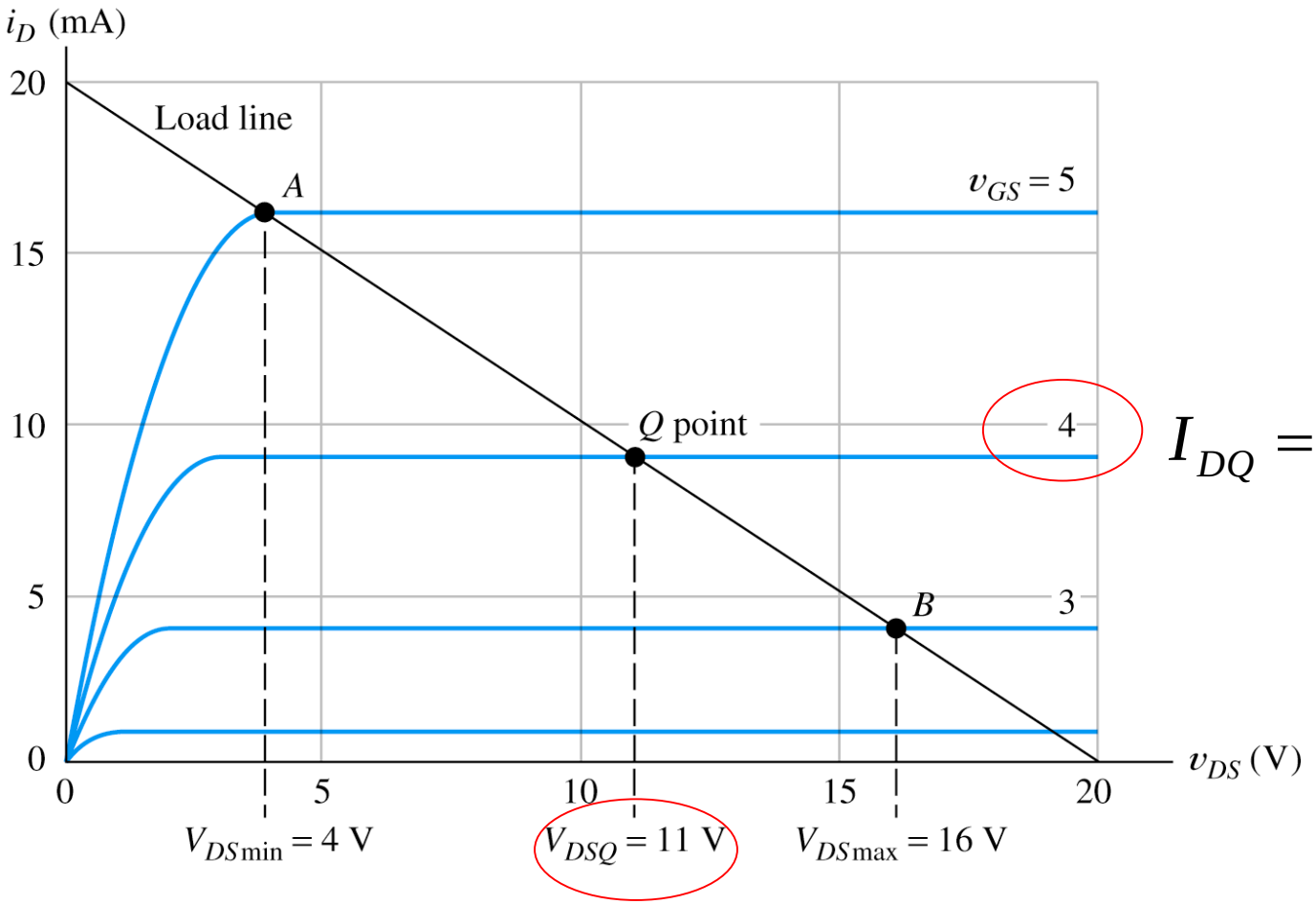


Figure 12.10 Simple NMOS amplifier circuit.

•Quiescent operation point (Q point) is at v_{in}=0.

$$v_{GS} = V_{GG} = 4\text{V}$$



$I_{DQ} = 9mA$

Figure 12.11 Drain characteristics and load line for the circuit of Figure 12.10.

$$\because v_{GS}(t) = v_{in}(t) + V_{GG} = \sin(2000\pi t) + 4$$

$$\Rightarrow \quad V_{GS\max} = 5\text{V(point A)}$$

$$V_{GS\min} = 3\text{V(point B)}$$

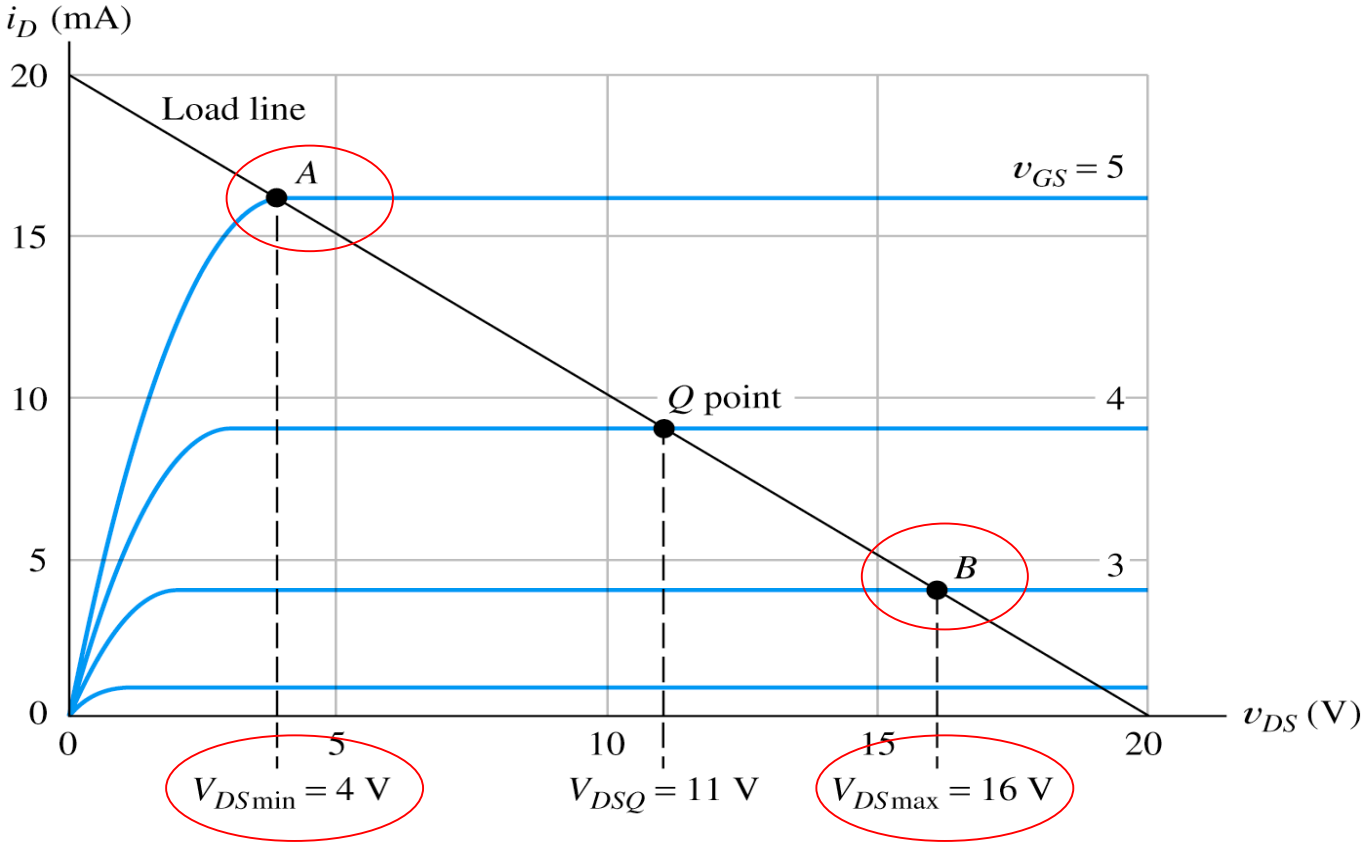


Figure 12.11 Drain characteristics and load line for the circuit of Figure 12.10.

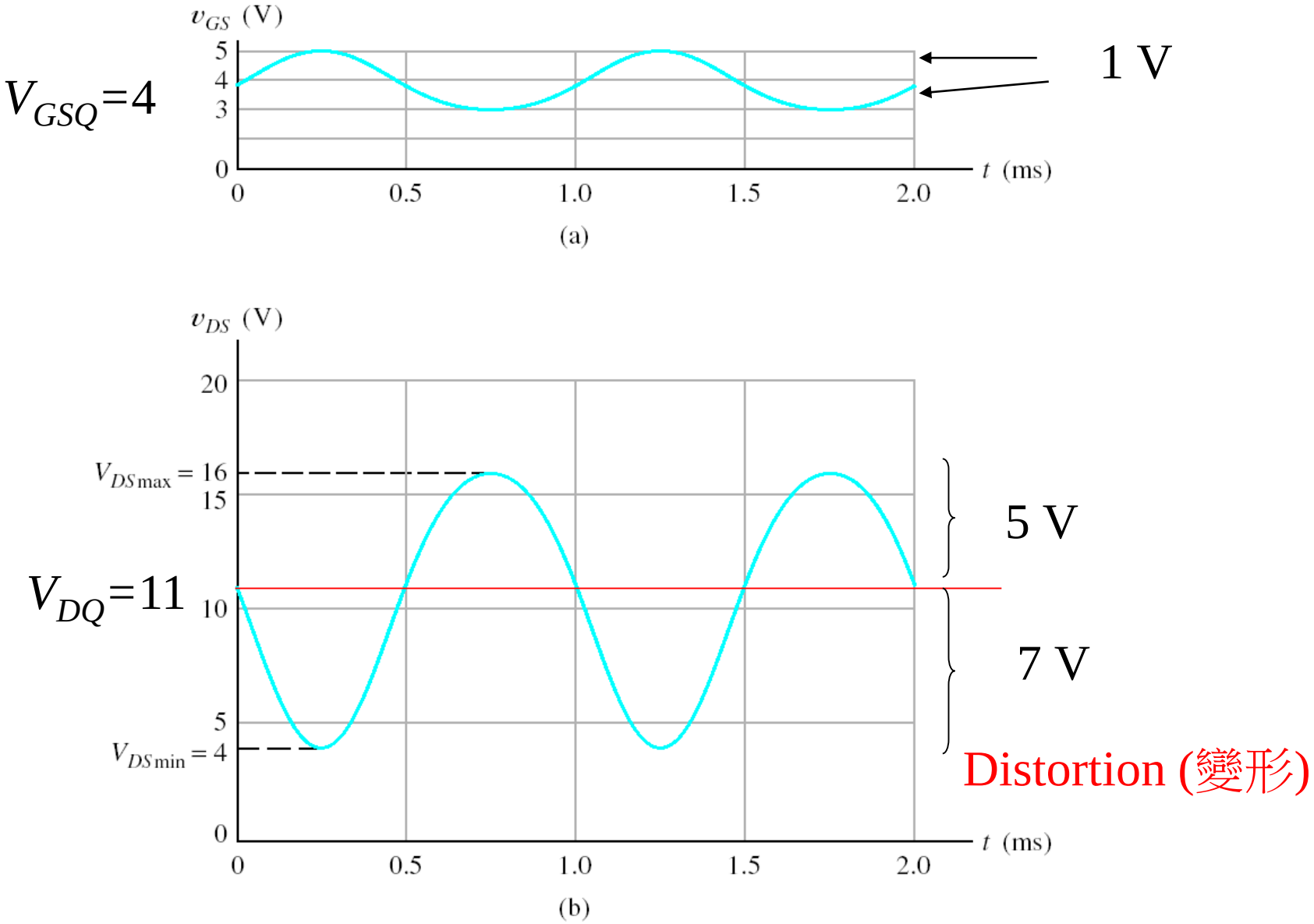


Figure 12.12 v_{GS} and v_{DS} versus time for the circuit of Figure 12.10.

Distortion

Distortion is due to that the characteristic curves for the FET are not uniformly spaced.

If a much smaller input amplitude was applied we would have amplification without appreciable distortion.

12.3 Bias Circuits

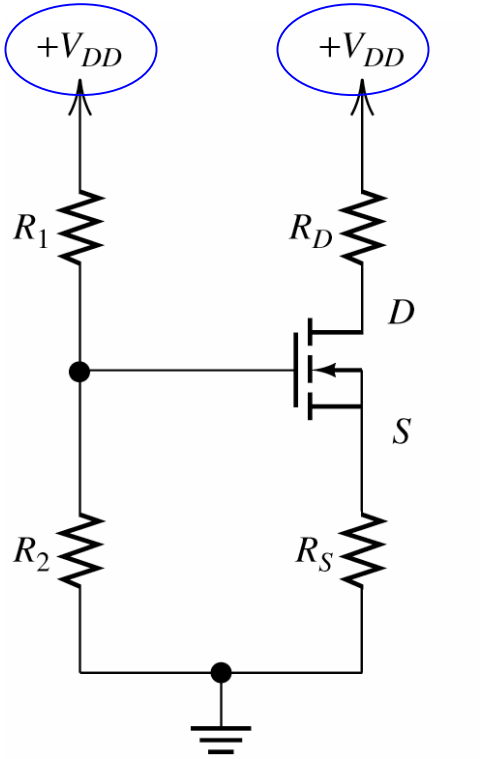
Amplifier Analysis

Amplifier analysis has two steps:

1. Determine the *Q* point.

2. Use a small-signal equivalent circuit to determine impedances and gains.

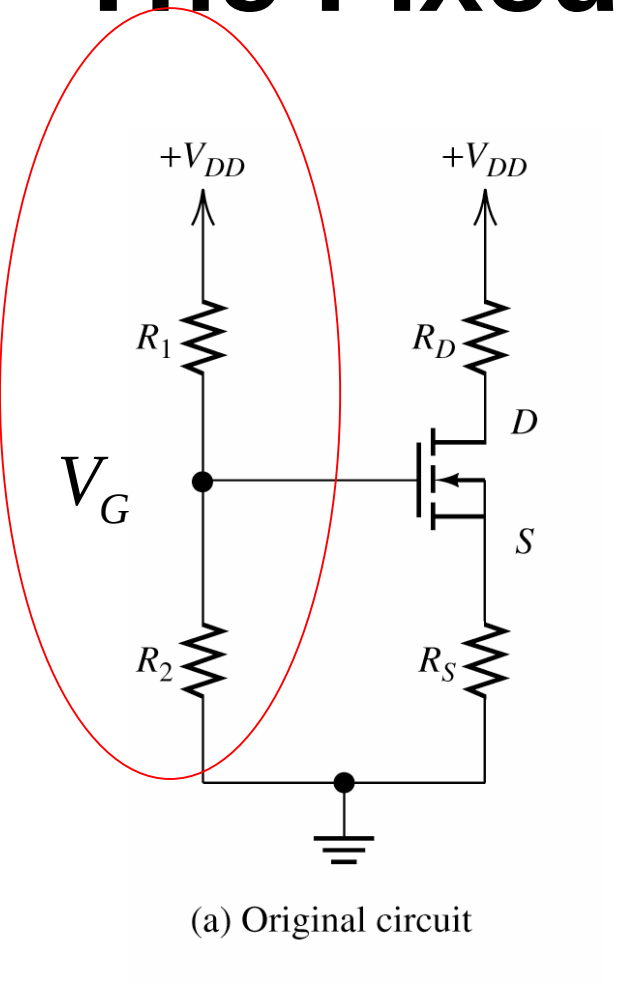
The Fixed- Plus Self-Bias Circuit



(a) Original circuit

v_{DS} ?

The Fixed- Plus Self-Bias Circuit

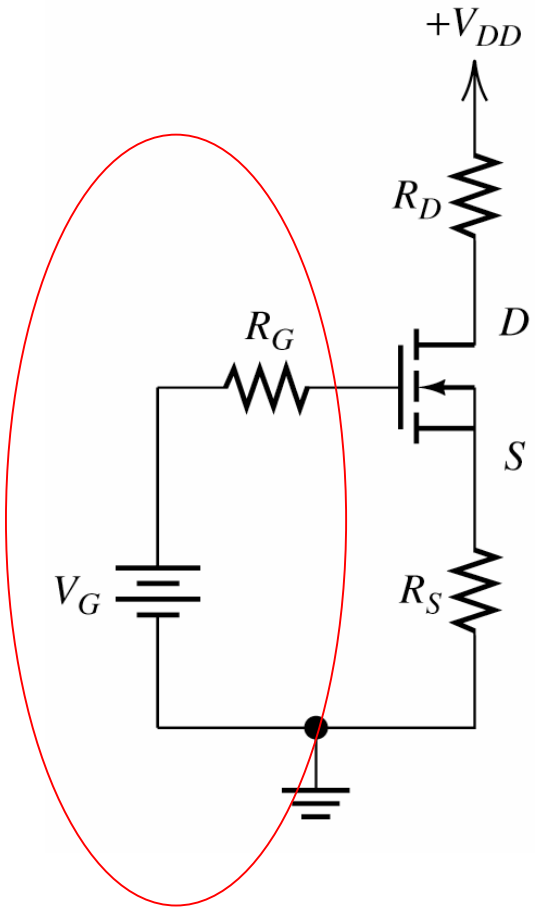


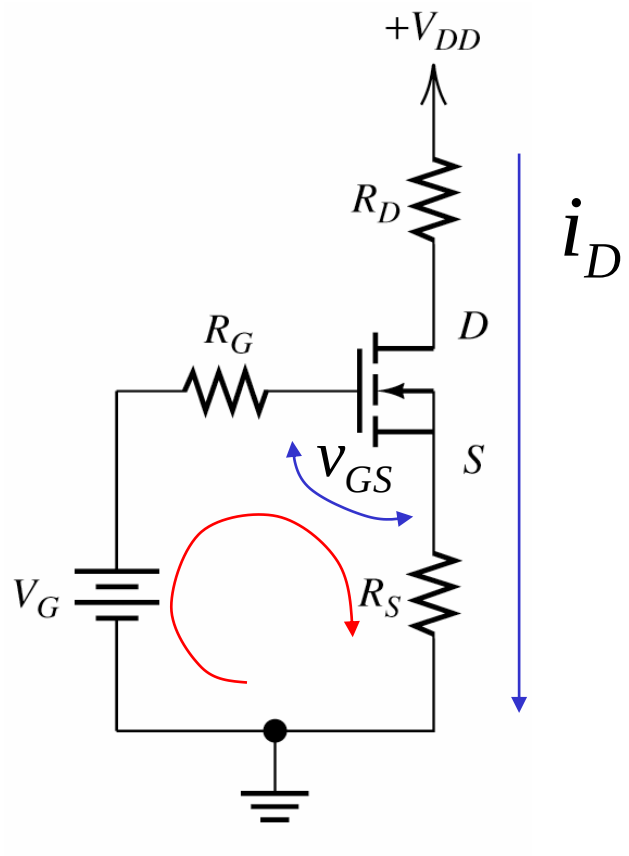
(a) Original circuit

1. Thévenin equivalent

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

$$R_G = \frac{R_1 R_2}{R_1 + R_2}$$





2. KVL

$$V_G = v_{GS} + R_s i_D \quad (\because i_G = 0)$$

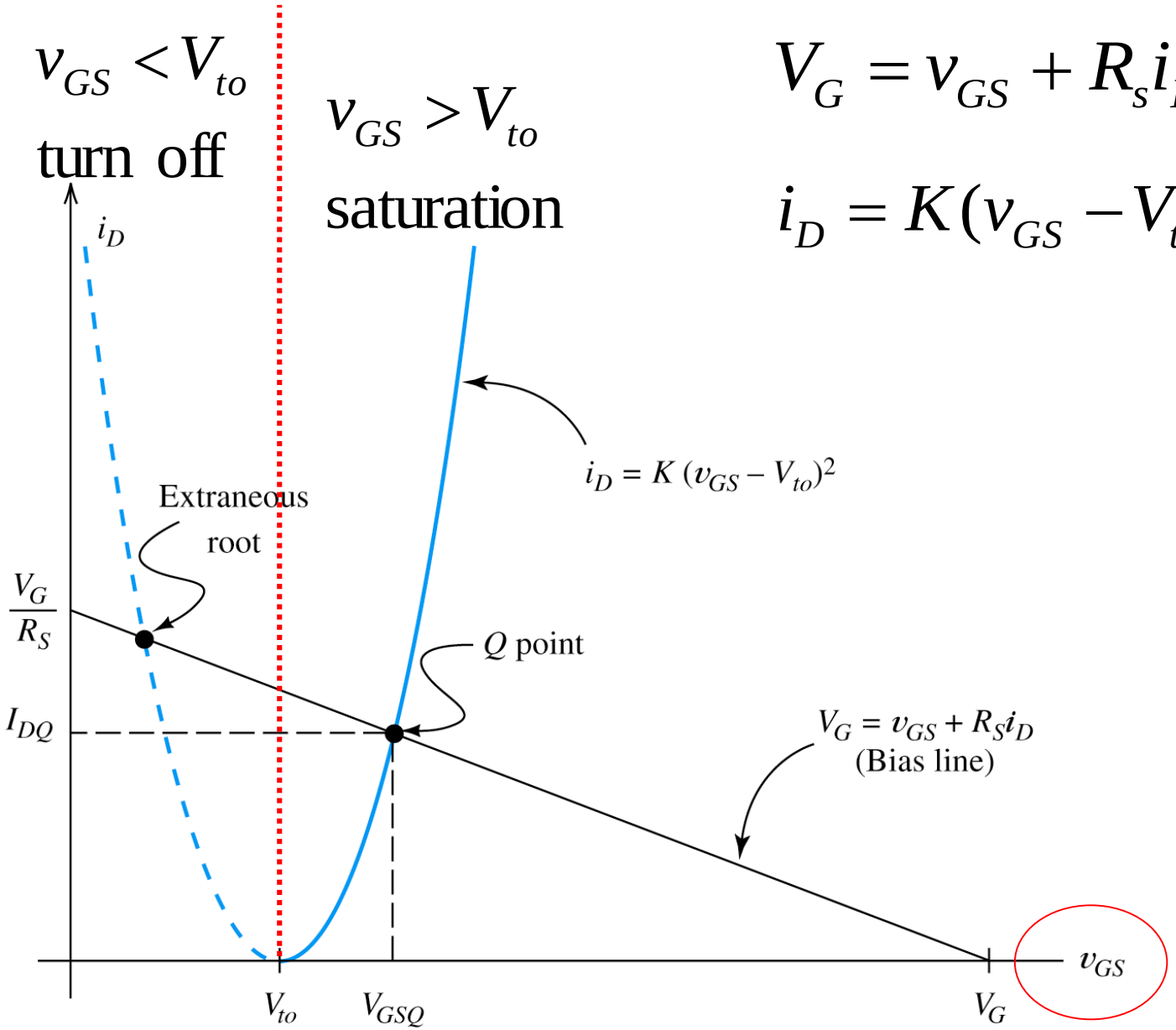
3. Usually, transistor operates in saturation region

$$i_D = K(v_{GS} - V_{to})^2$$

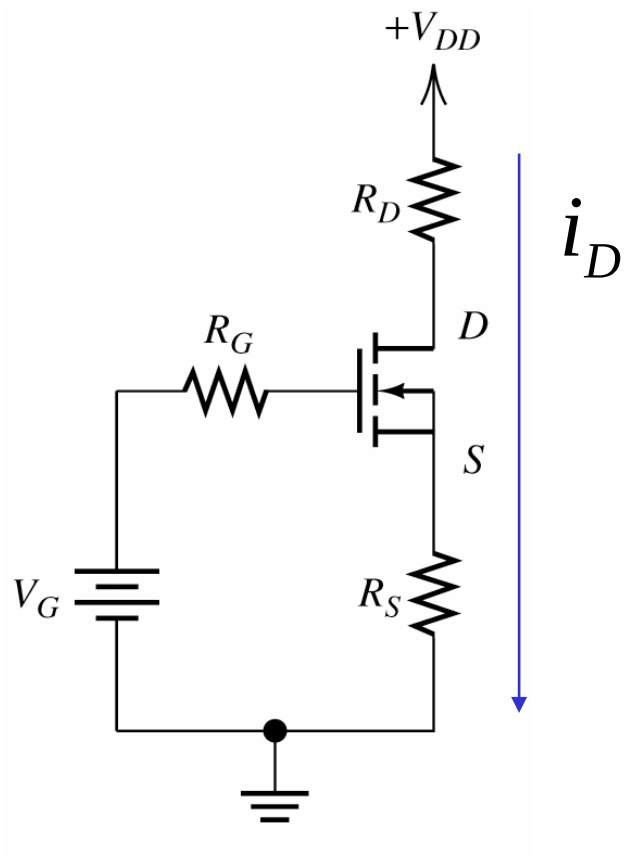
4. Load Line Analysis i_D vs. v_{GS}

$$V_G = v_{GS} + R_s i_D$$

$$i_D = K(v_{GS} - V_{to})^2$$



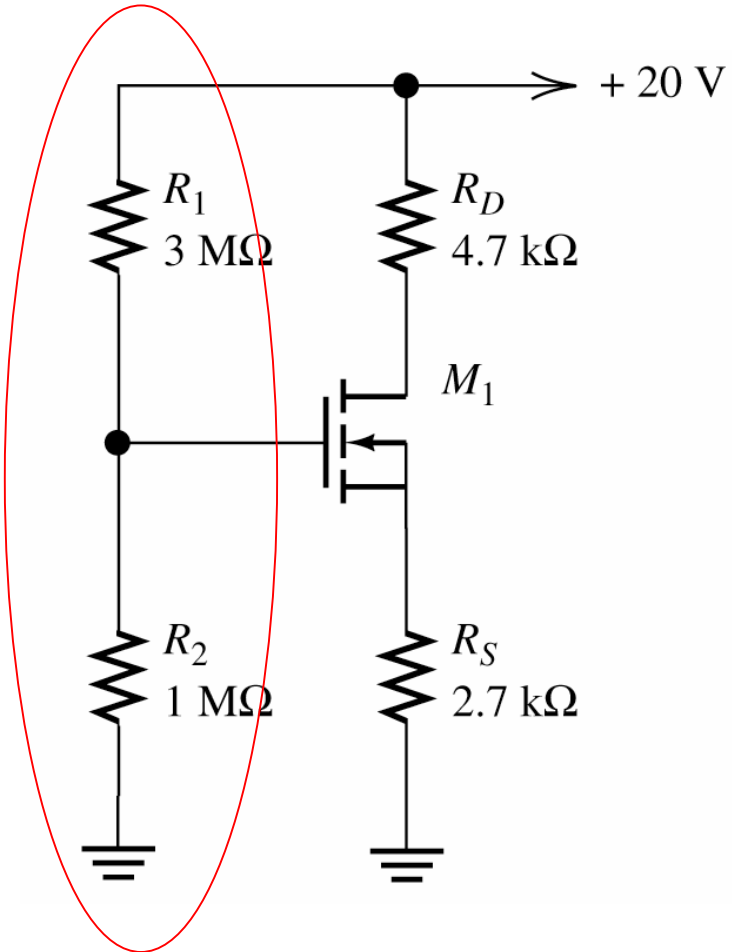
5. Determine v_{DS}



$$v_{DS} = v_{DD} - (R_D + R_s)i_D$$

Example 12.2

Analyze the following circuit. The transistor KP=50uA/V^2, V_{to}=2 V, L=10um, W=400um



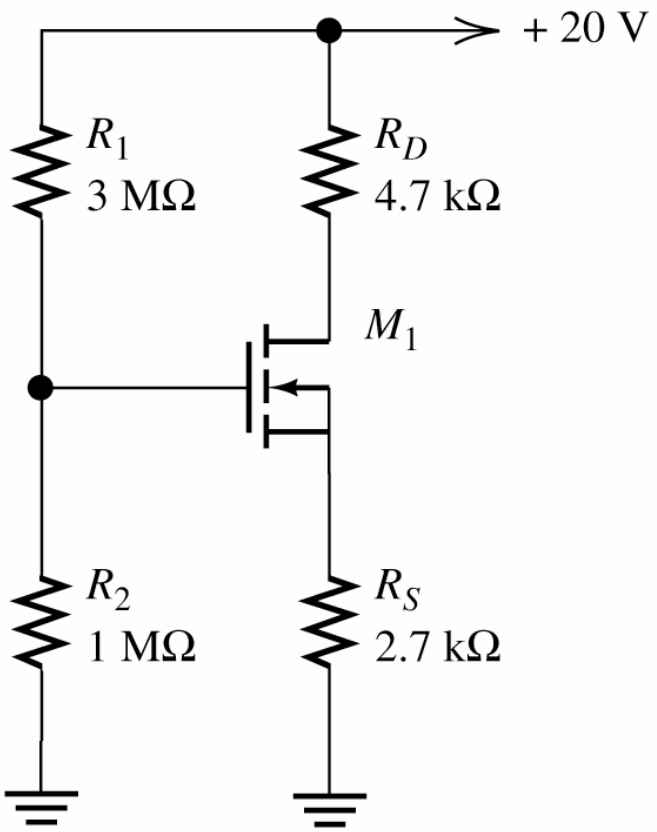
1. Determine K

$$K = (\frac{W}{L})\frac{KP}{2} = 1mA/V^2$$

2. Thévenin equivalent

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2} = 20\frac{1}{3+1} = 5V$$

3. Determine V_{GSQ}



$$\begin{cases} V_G = V_{GSQ} + R_s I_{DQ} \\ I_{DQ} = K(V_{GSQ} - V_{to})^2 \end{cases}$$

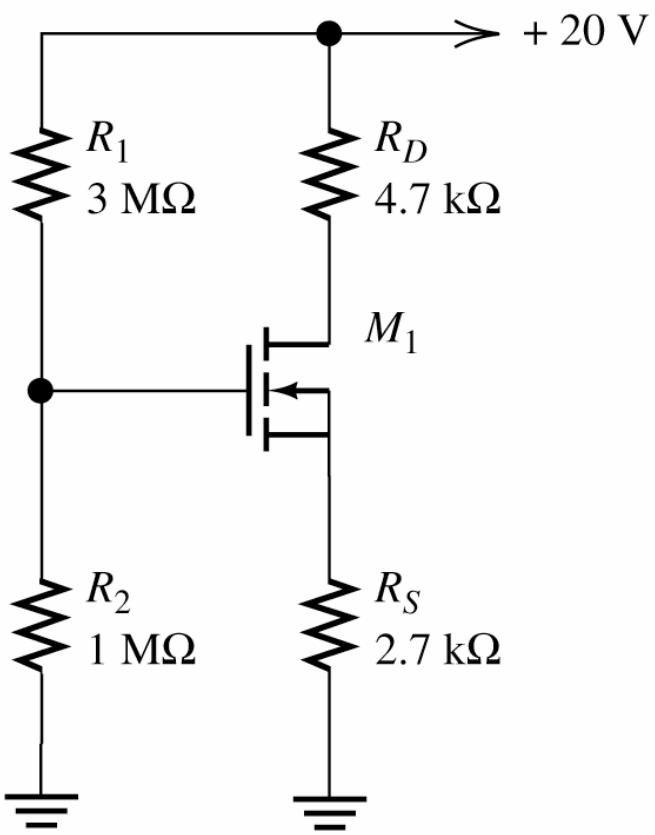
$$V_G = V_{GSQ} + R_s K(V_{GSQ} - V_{to})^2$$

$$V_{GSQ}^2 + \left(\frac{1}{R_s K} - 2V_{to}\right)V_{GSQ} + V_{to}^2 - \frac{V_G}{R_s K} = 0$$

$$V_{GSQ}^2 - 3.630 V_{GSQ} + 2.148 = 0$$

$$V_{GSQ} = 2.886 \text{ or } 0.744$$

○ ×



4. I_{DQ} & V_{DSQ}

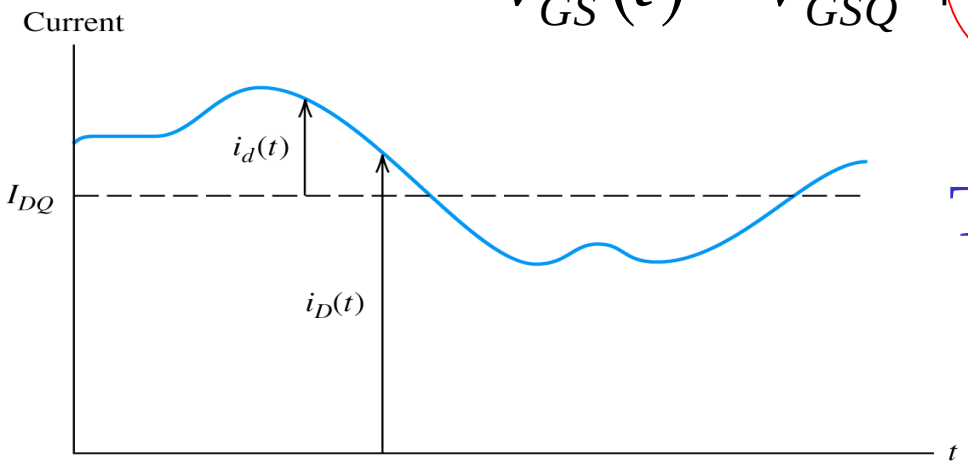
$$I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.784mA$$

$$V_{DSQ} = V_{DD} - (R_D + R_s)I_{DQ} = 14.2V$$

12.4 SMALL-SIGNAL EQUIVALENT CIRCUITS

$$i_D(t) = I_{DQ} + i_d(t)$$ Small signal (ac)

$$v_{GS}(t) = V_{GSQ} + v_{gs}(t)$$ Small signal (ac)



To determine $v_{gs}(t)$ vs. $i_d(t)$

$\because i_D = K(v_{GS} - V_{to})^2$ for satutation

$$I_{DQ} + i_d(t) = K[V_{GSQ} + v_{gs}(t) - V_{to}]^2$$

$$= K(V_{GSQ} - V_{to})^2 + 2K(V_{GSQ} - V_{to})v_{gs}(t) + Kv_{gs}^2(t)$$

SMALL-SIGNAL EQUIVALENT CIRCUITS

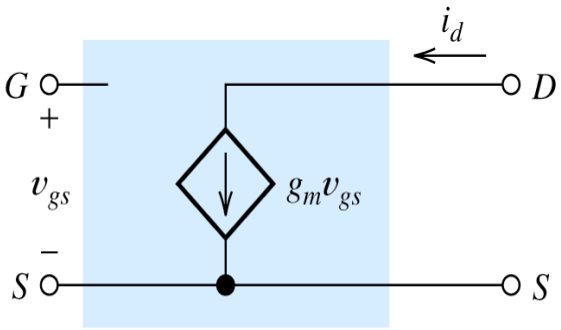


Figure 12.19 Small-signal equivalent circuit for FETs.

$$I_{DQ} + i_d(t) = K(V_{GSQ} - V_{to})^2 + 2K(V_{GSQ} - V_{to})v_{gs}(t) + Kv_{gs}^2(t)$$

At Q point

$$I_{DQ} = K(V_{GSQ} - V_{to})^2$$

$$(\because 2K(V_{GSQ} - V_{to})v_{gs}(t) >> Kv_{gs}^2(t))$$

$$I_{DQ} + i_d(t) = K(V_{GSQ} - V_{to})^2 + 2K(V_{GSQ} - V_{to})v_{gs}(t) + Kv_{gs}^2(t)$$

0

$$i_d(t) \cong 2K(V_{GSQ} - V_{to})v_{gs}(t) = g_m v_{gs}(t)$$

$$g_m = 2K(V_{GSQ} - V_{to})$$

$$= 2\sqrt{KI_{DQ}}$$

$$= \sqrt{2KP}\sqrt{W/L}\sqrt{I_{DQ}}$$

$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$