Computer Organization & Assembly Language

Final Exam – 2011/1/7

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1. Answer *True* or *False* to the following statements. (45%)

(A) In computer arithmetic, dividend and remainder must have the same signs when performing the signed division.

(B) In computer arithmetic, floating-point addition may not be associative; that is, x+(y+z) != (x+y)+z.

(C) Since computer arithmetic is with limited precision, computation results obtained from computers are usually erroneous and suspicious.

(D) The register is considered as a type of sequential elements.

(E) In the pipelined processor, all control signals can be immediately set after the current instruction is decoded in the 2nd stage.

(F) When designing the processor, the control signals RegRead and RegWrite are used for controlling the data access of register files.

(G) The CPI value of an ideal pipeline processor is the same as that of a single-cycle processor.

(H) The Zero output of ALU is only used for conditional branch instructions.

(I) Designing the control part of a processor is straightforward since it can be easily built on the basis of existing datapath.

(J) The critical path in the single-cycle design is referred to as the lw instruction.

(K) Reordering code is always possible to avoid pipeline stalls.

(L) Forwarding is primarily an attempt to fix data hazards in a pipeline.

(M) The CPI value of an ideal pipeline processor is the same as that of a single-cycle processor.

(N) Increasing the depth of pipeline (i.e., number of stages) can proportionally improve the overall performance

(O) Pipeline bubbles cause loss of performance since hardware utilization is relatively low.

2. When using the IEEE 754 format, what is the meaning of overflow and underflow, respectively? (4%)

3. Perform the following operations of computer arithmetic. (15%)

(A) Convert 0xCA50 to binary.

(B) Convert 0xFFF7 to decimal, interpreting it as a signed 16-bit integer.

(C) Subtract 0x001F from 0xFFF7, interpreting each as 2's complement 16-bit integer. Express the answer both in hex and decimal.

(D) Show the IEEE 754 representation of 2.25_{ten} in single precision.

(E) Show the IEEE 754 representation of $-5/6_{ten}$ in single precision.

4. Explain why there are only four pipeline registers in the 5-stage pipeline processor. (4%)

5. Suppose we want to execute the following code segment on the pipelined CPU:

```
add   $2, $5, $4
add   $4, $2, $5
lw    $5, 100($2)
add   $3, $2, $5
```

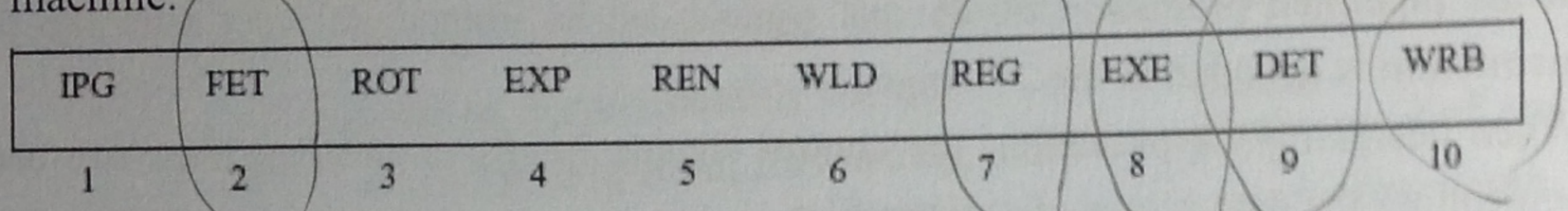
Suppose there is no hardware supports for the forwarding and stalling, but the register file can write a register at the first half of a cycle and read it at the second half of the cycle. (9%)

(A) How many NOPs and at what places that you can add to make the code segment execute correctly on our pipeline?

(B) Suppose the pipeline stalls, but no forwards, when there is data hazard. How many cycles will the above code segment execute?

(C) How many cycles will the above code segment execute if a single-cycle CPU is used?

6. One CPU manufacturer proposed the 10-stage pipeline below for a 500MHz (2ns clock cycle) machine.



Here are the correspondences between this and the MIPS pipeline:

- Instructions are fetched in the FET stage.
- Register reading is performed in the REG stage.
- ALU operations and memory access are both done in the EXE stage.
- Branches are resolved in the DET stage.
- WRB is the writeback stage.

(A) How much time is required to execute one million instructions on this processor, assuming there are no dependencies or branches in the code? (3%)

(B) Without forwarding, how many stall cycles are needed for the following code fragment? Assume that the register file could be written and read in the same clock cycle. (3 points) What is this hazard called? (3%)

```
lw   $t0, 0($a0)
add  $v1, $t0, $t0
```

(C) If a branch is mispredicted, how many instructions would have to be flushed from the pipeline? (3%)

(D) Assume that a program executes one million instructions. Of these, 15% are load instructions which stall, and 10% of the instructions are branches. The CPU predicts branches correctly 75% of the time. How much time will it take to execute this program? (4%)

7. Consider the following sequence of actual outcomes for a single static branch where T means the branch is taken and N means the branch is not taken. Also, assume that this is the only branch in the program.

T N T N T N T T T N N N T T T N T N

(A) Assume that we try to predict this sequence with the 1-bit predictor (which is initialized to the N state). What is the predicted sequence? How many branches are mis-predicted? (4%)

(B) How about using the 2-bit predictor (which is initialized to the T state)? (6%)