Final Exam. of Logic Design course (2007)

All of your solution must give the detail design procedures.

1. Implement a T type Flip-Flop from a JK type Flip-Flop. (10%)
2. Give the characteristic table, the excitation table, the state transition diagram, and the next state equation of a JK Flip-Flop. (10%)
3. Design a counter which can provide the following counting sequence by using D type Flip-Flops and assume each Flip-Flop with the Preset and Reset PINs. (20%)

ABC
0 0 0
1 0 0
1 1 0
1 1 1
0 1 1
0 0 1
0 0 0

4. Design a module 5 **asynchronous counter** by using JK type Flip-Flops. (20%)
5. Use T type Flip-Flops design a three bit up/down counter with the counting sequence **0 ←→ 2 ←→3 ←→1 ←→ 4 ←→6 ←→5 ←→7 ←→0**. (20%)
6. For the state diagram shown in Figure 1, give the corresponding table for presenting the relations of present-next states, input, and output, then design the logic circuits using T type Flip-Flops. (20%)

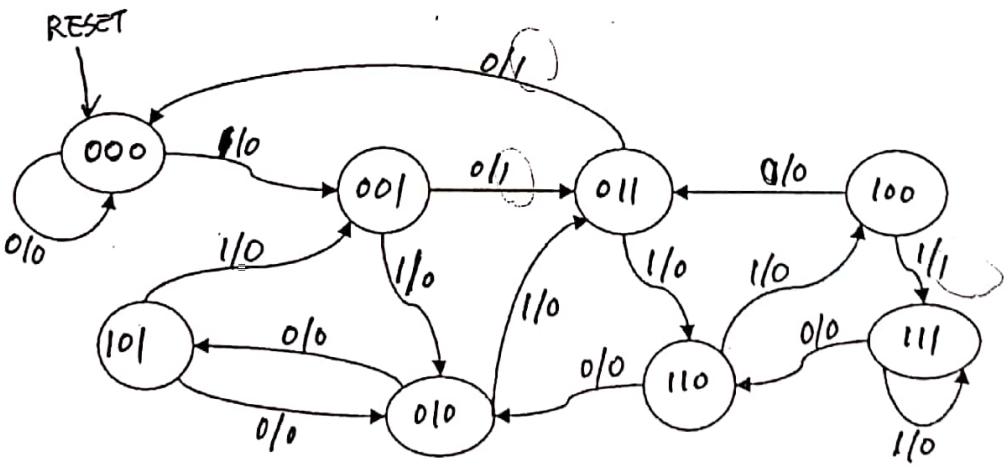

Figure 1

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