數位系統實驗

Thu 9:00 am – 12:00 am

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國立成功大學　資訊工程系

Schedule(乙)

- 9/10 Lab - 01 (Logic Gate on Chip)
- 9/17 Lab - 02 (Logic Gate on Chip)
- 9/24 Lab - 03 (Logic Gate on Chip)
- 10/01 Suspension(中秋)
- 10/7 Mid Exam (Lab - 01 ~ Lab - 02)
- 9 Lab + 1 Mid Exam (Hardware Description Language, HDL)
- 12/31 Final Project preparation)
- 01/07 Final Project Presentation

LAB - 01

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Outline

- Video preview for 數位系統簡介+邏輯閘
- Representations for a circuit
- 邏輯閘(logic gate), 晶片(chip)
- 麵包板(Breadboard) for function verification
- Lab

Three representations for a circuit

1. Boolean Algebra

$F_1 = x + y'z$

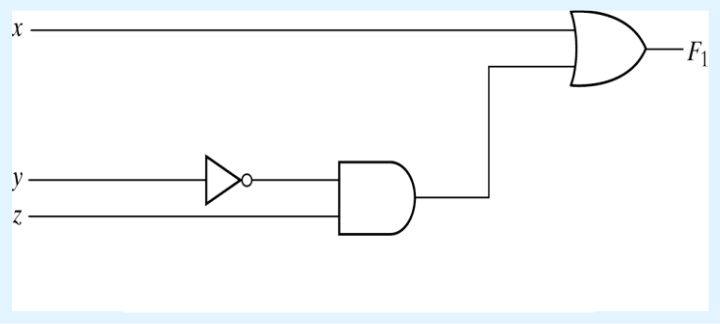
2. Truth Table

真值表

n input variables ➔ 2^n combinations

Inputs					
x	*y*	*z*	*y'*	*y'z*	F_1
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	0	1

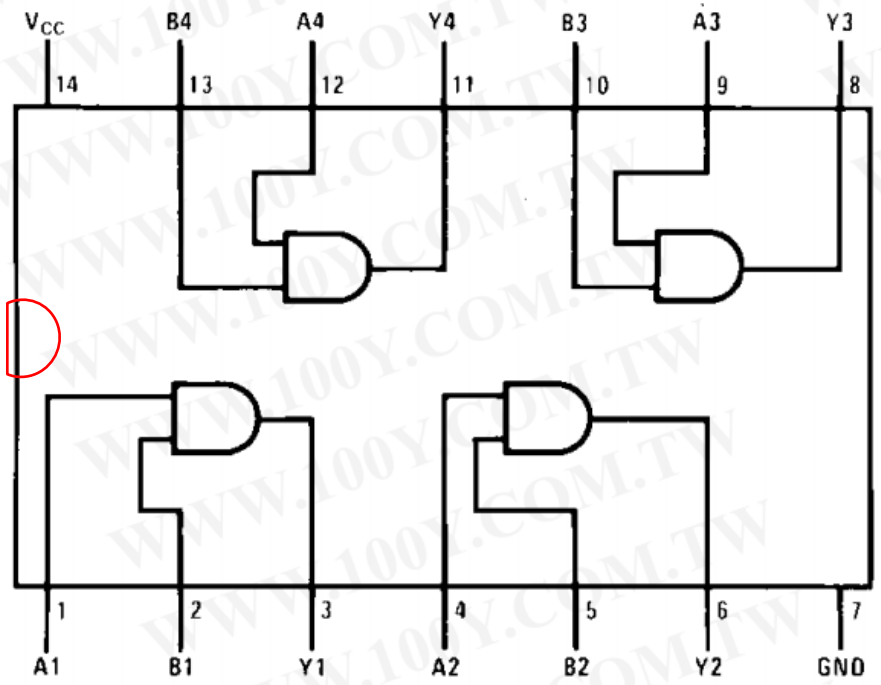
3. Circuit Diagram



74LS08

AND gate

Connection Diagram



Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

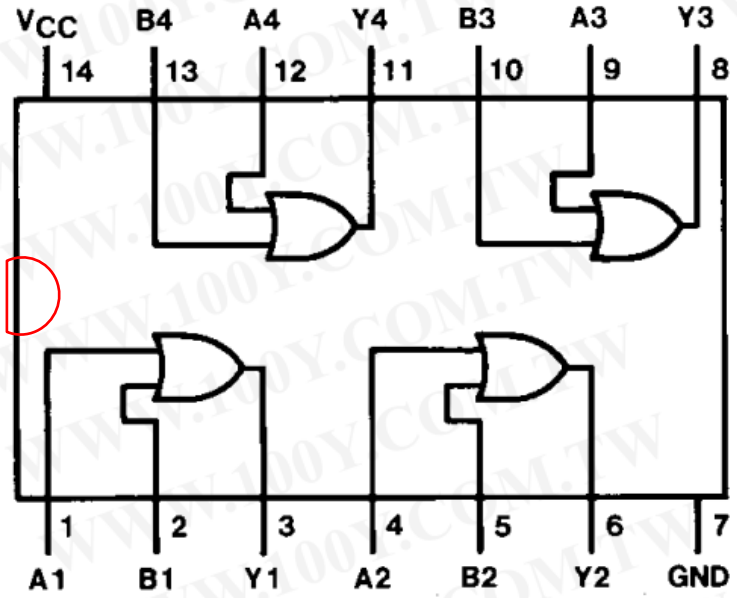
H = HIGH Logic Level
L = LOW Logic Level

Boolean Algebra *F=xy*

74LS32

OR gate

Connection Diagram



Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

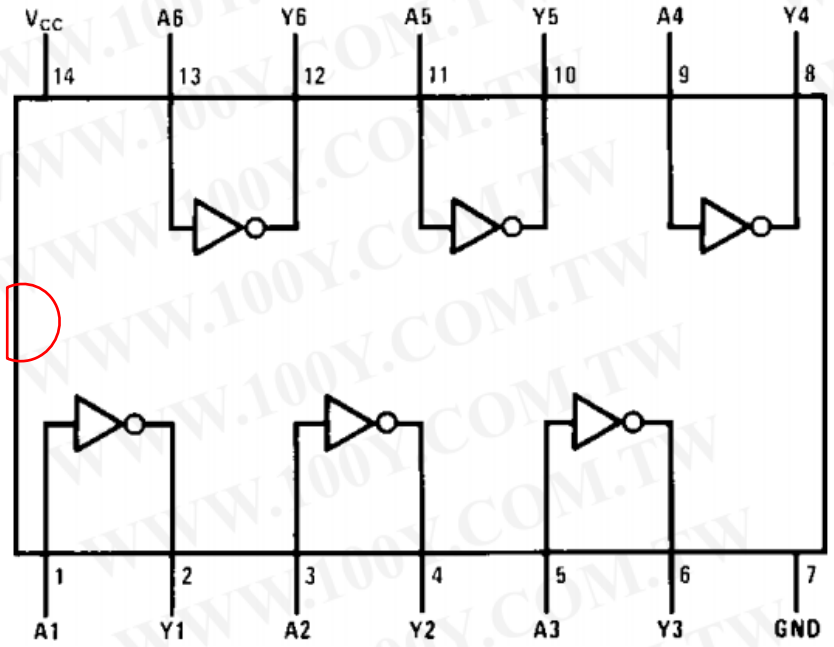
H = HIGH Logic Level
L = LOW Logic Level

Boolean Algebra *F=x+y*

74LS04

NOT gate

Connection Diagram



Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

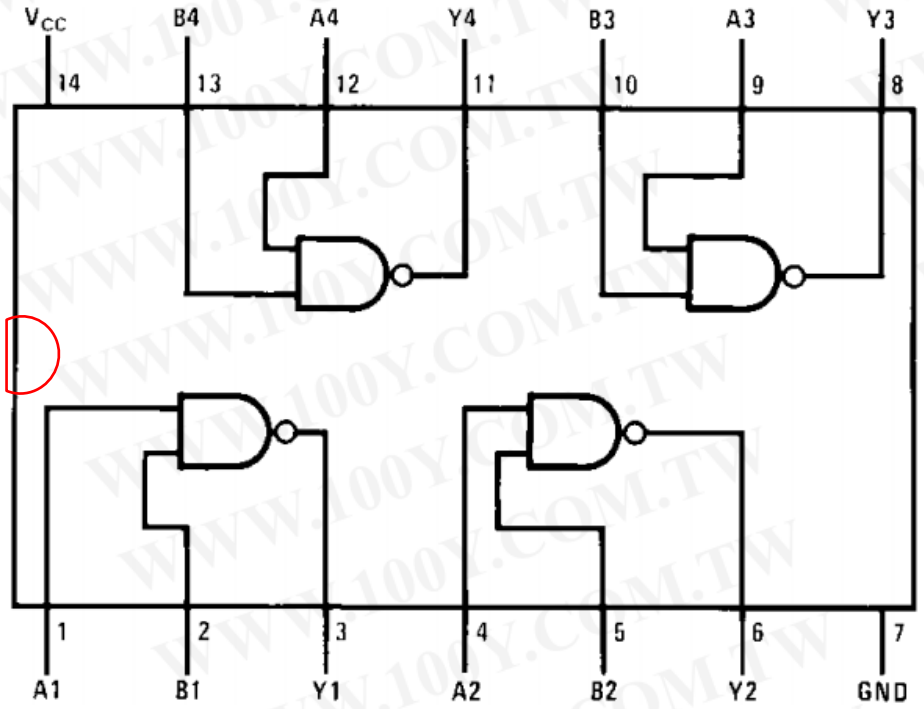
H = HIGH Logic Level
L = LOW Logic Level

Boolean Algebra *F=x'*

74LS00

NAND gate **Not - AND**

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

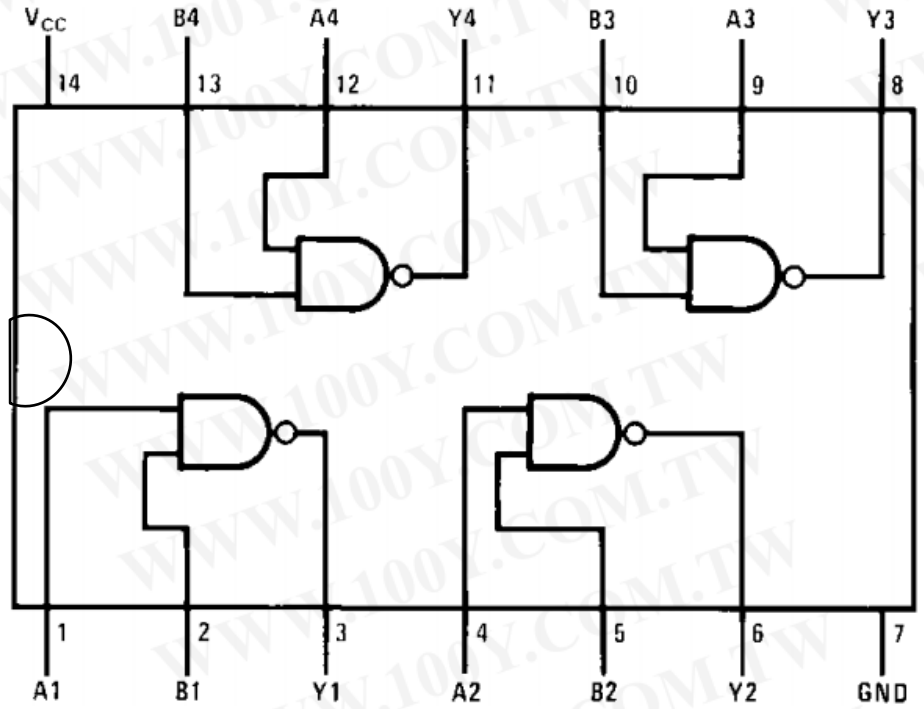
L = LOW Logic Level

Boolean Algebra ***F=(xy)'***

74LS00 (1/3)

NAND gate

Connection Diagram



Function Table

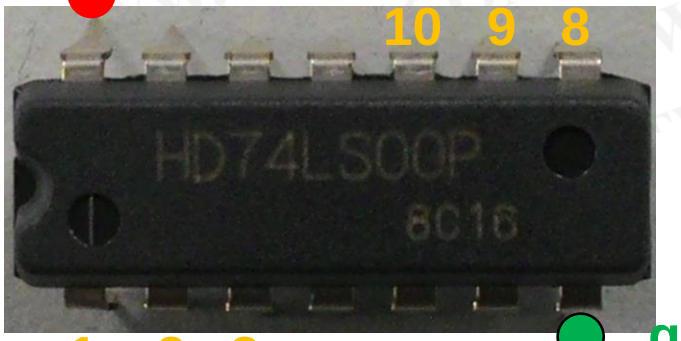
$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

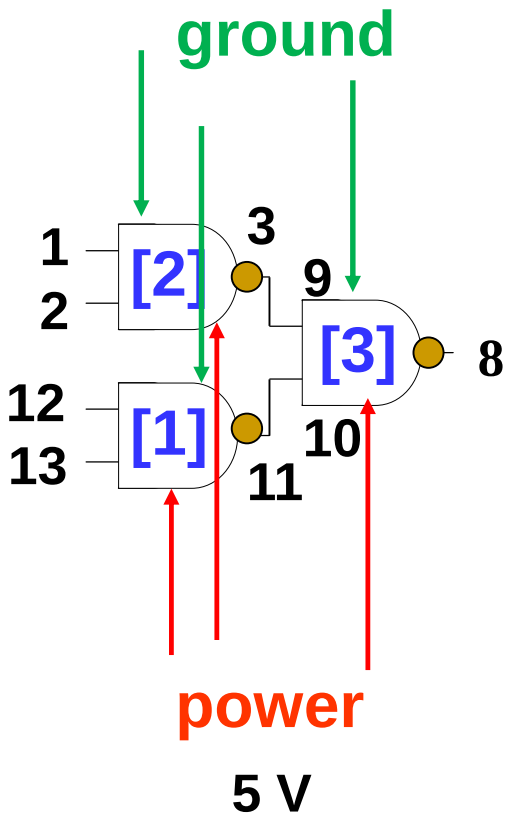
L = LOW Logic Level

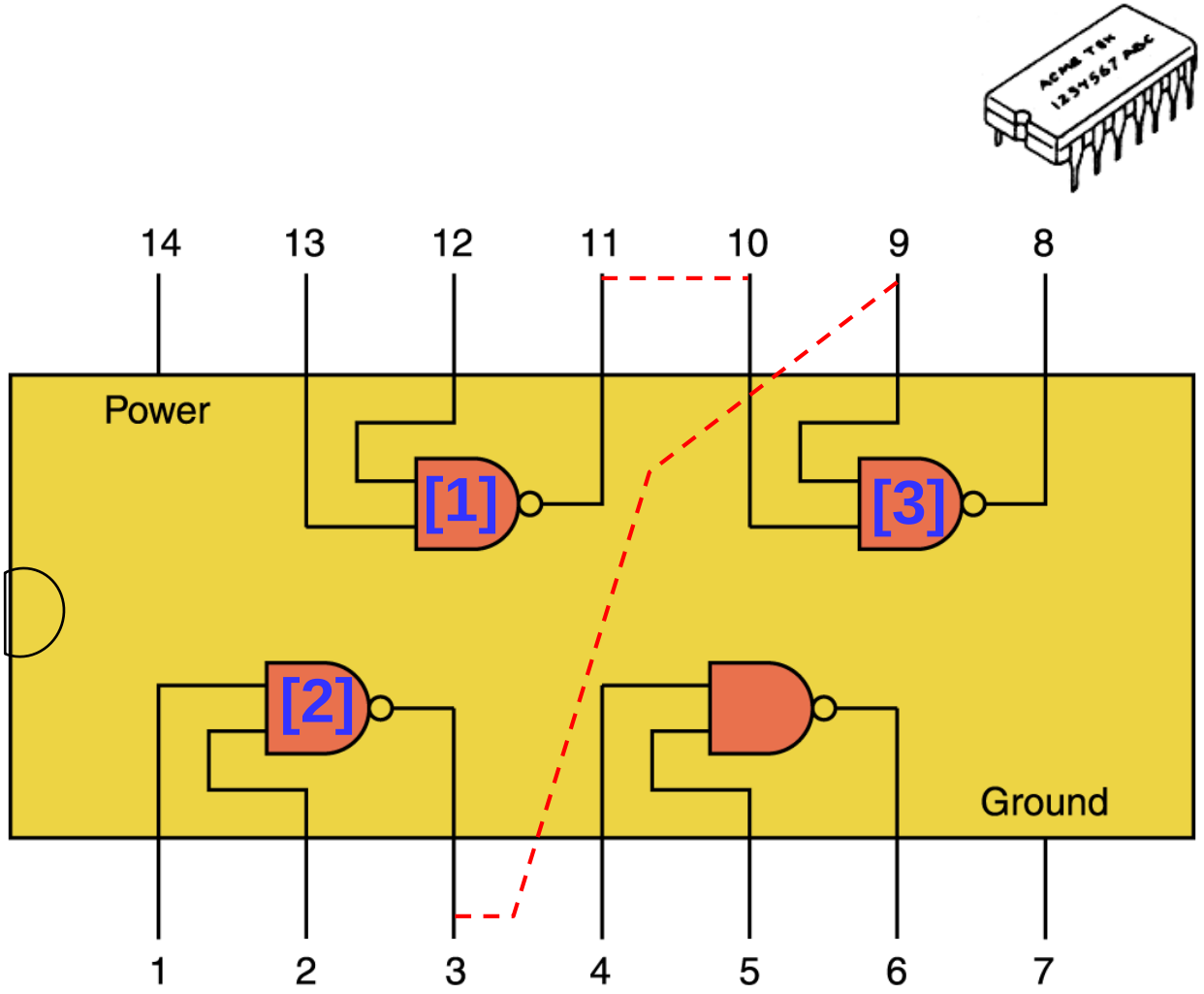
Vcc (5V)



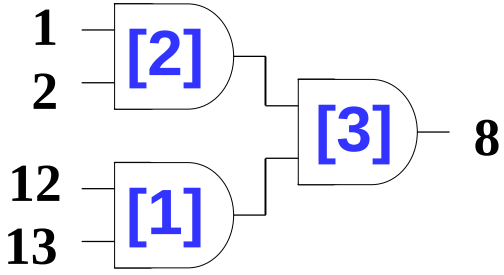
ground

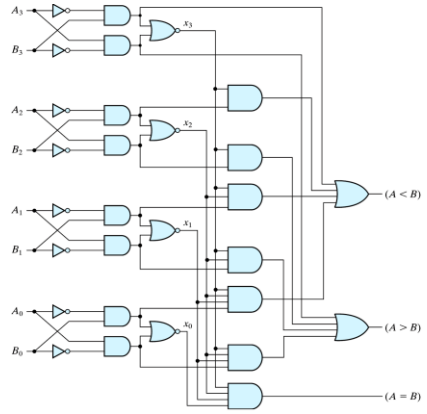
74LS00 (2/3)

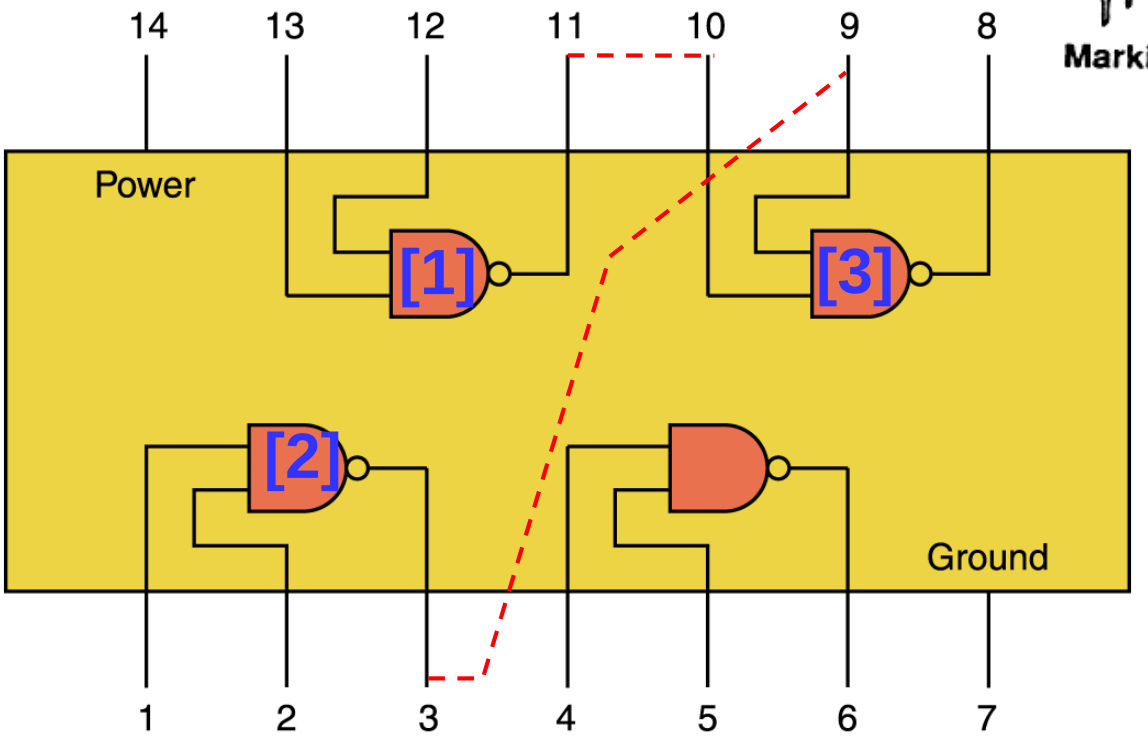

ground
1
2
[2]
3
9
[3]
8
12
13
[1]
11
10
power
5 V

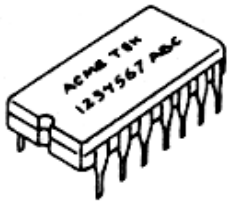

14
13
12
11
10
9
8
Power
[1]
[3]
[2]
Ground
1
2
3
4
5
6
7

74LS00 (3/3)









1. Multiple chips (gates) are used to realize a specific circuit
2. A dedicated chip (ASIC, application specific integrated circuit)

Introduction of Solderless Breadboard

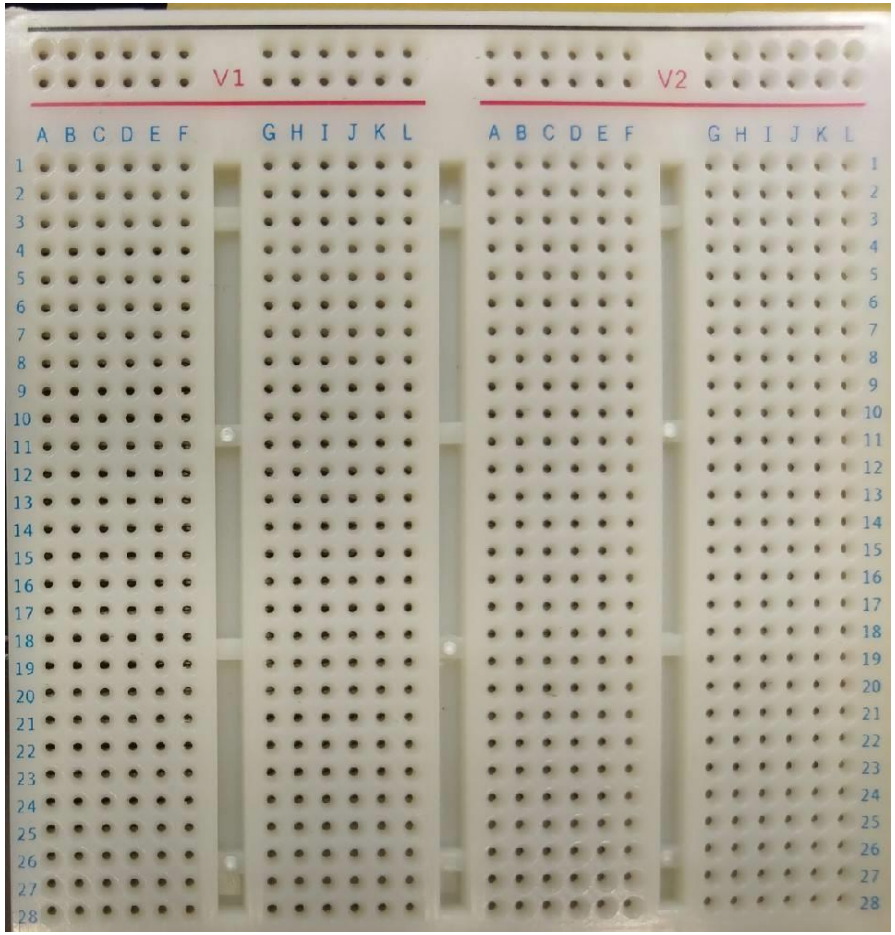
- Solderless Bredboard is a convenient kit for lay outing circuits without any soldering work. It is very useful for circuit test and modification during practical training.

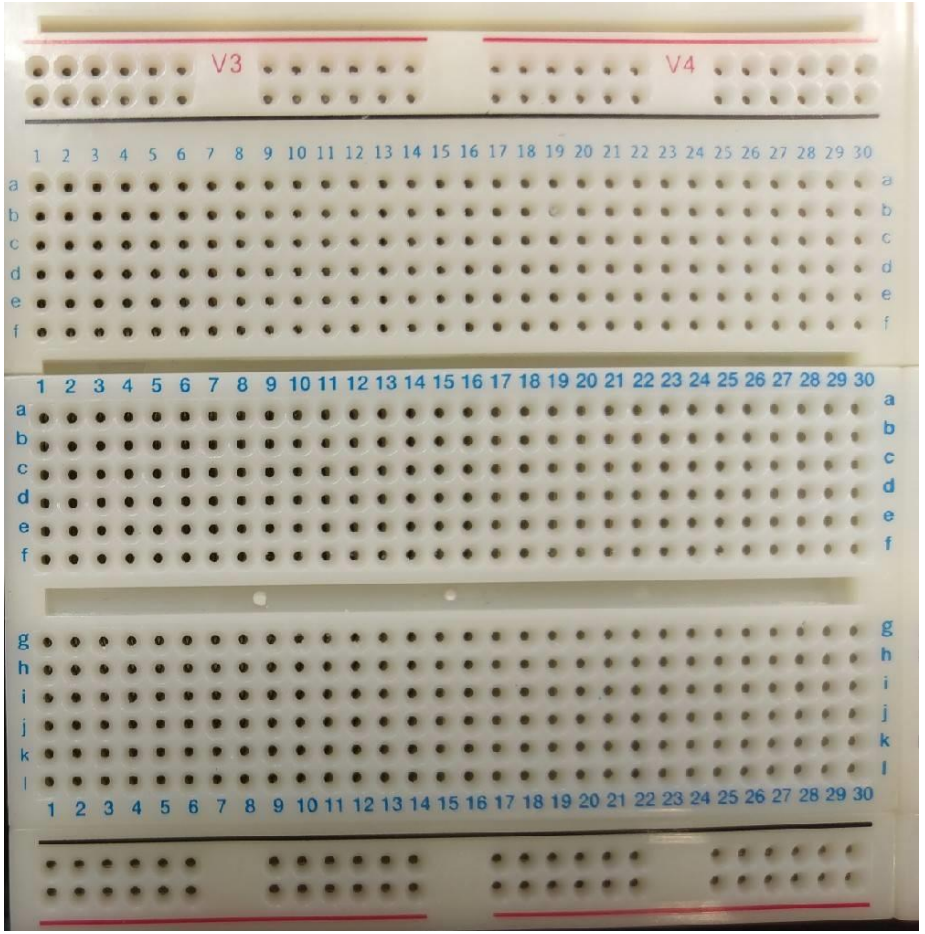
- Components in lab can be reused with breadboard.

- Normally, component’s pins are inserted into holes on breadboard. Every five holes are connected together by a brass stripe under plastic cover. One of holes is connected to component’s pin and the other holes are for circuit connection with jumpers.

Various Breadboards

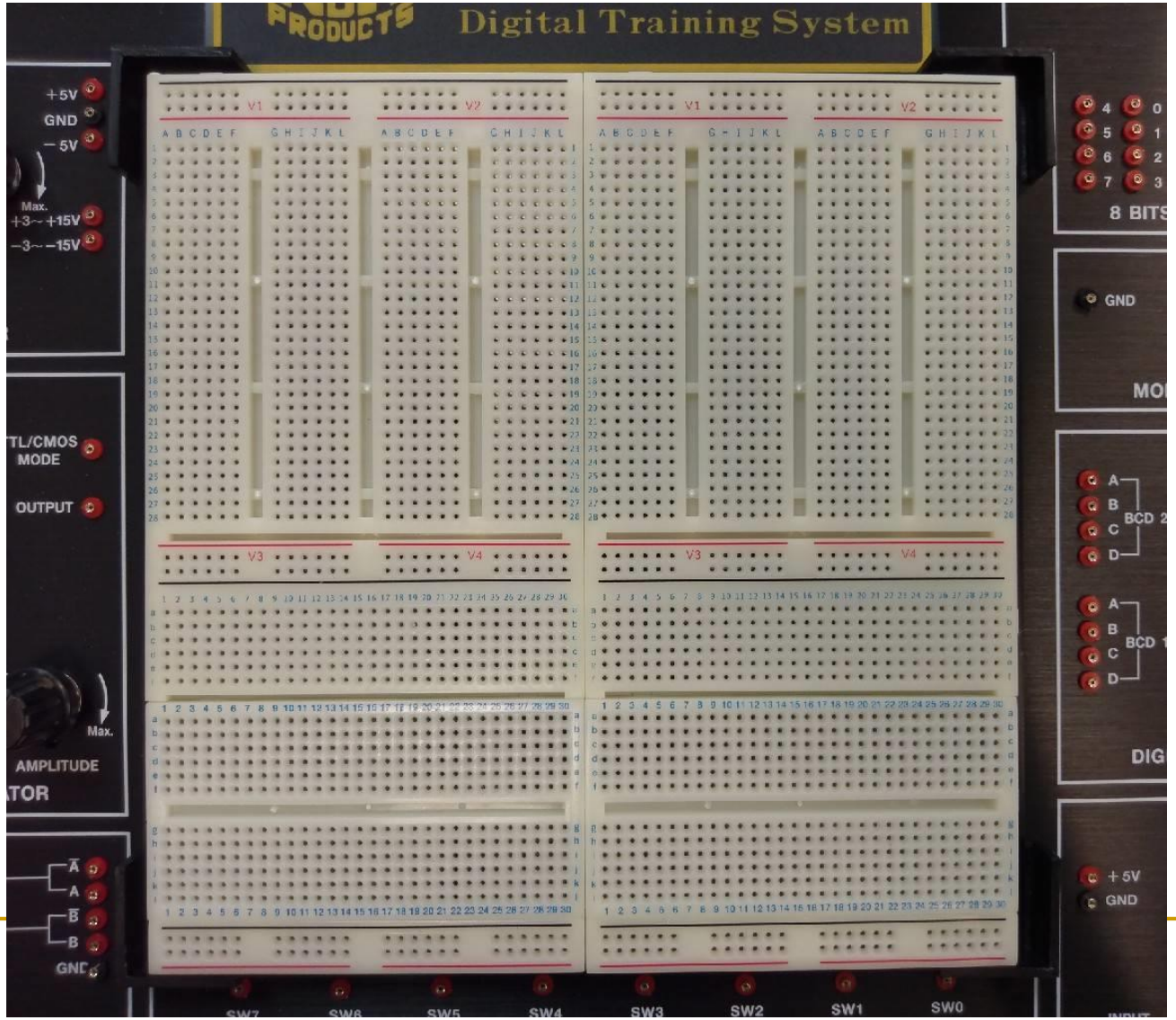
- Different types of Breadboards





The Solderless Breadboard in CSIE NCKU

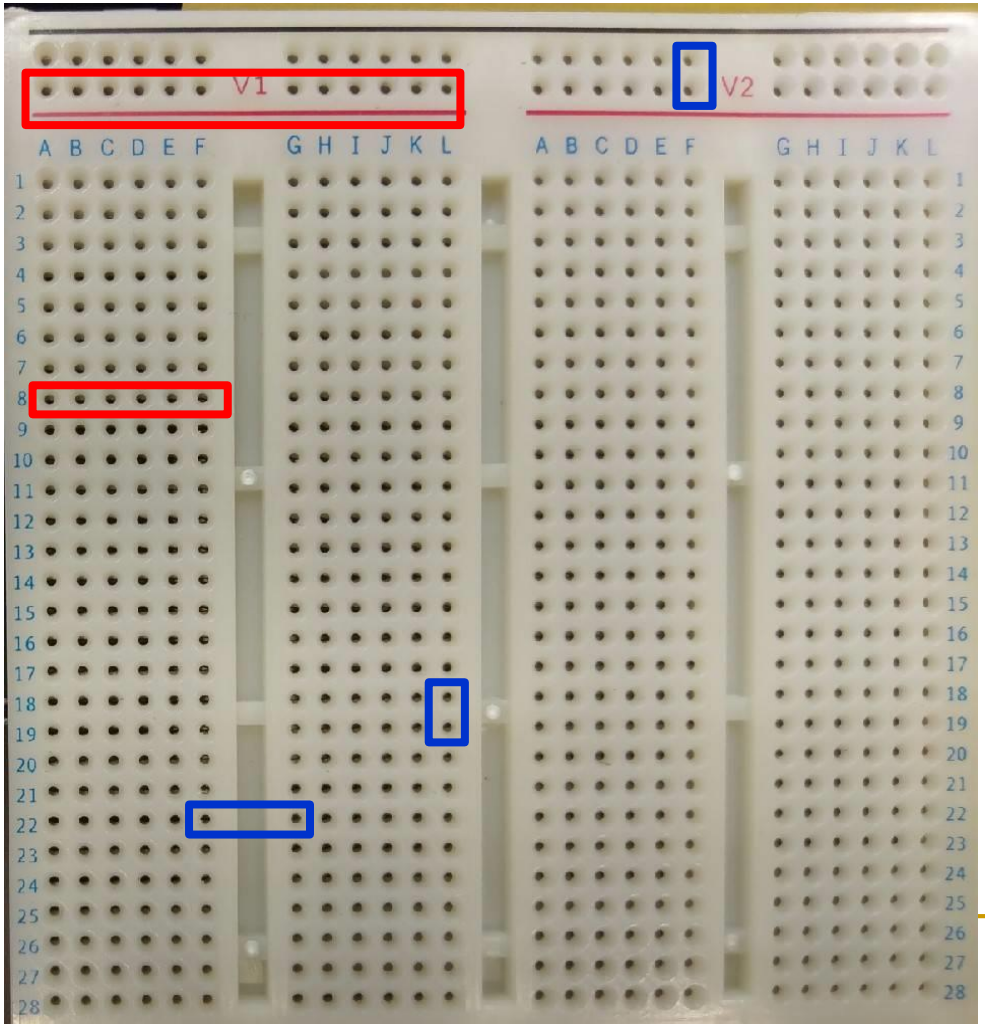
- **Top view of the breadboard**

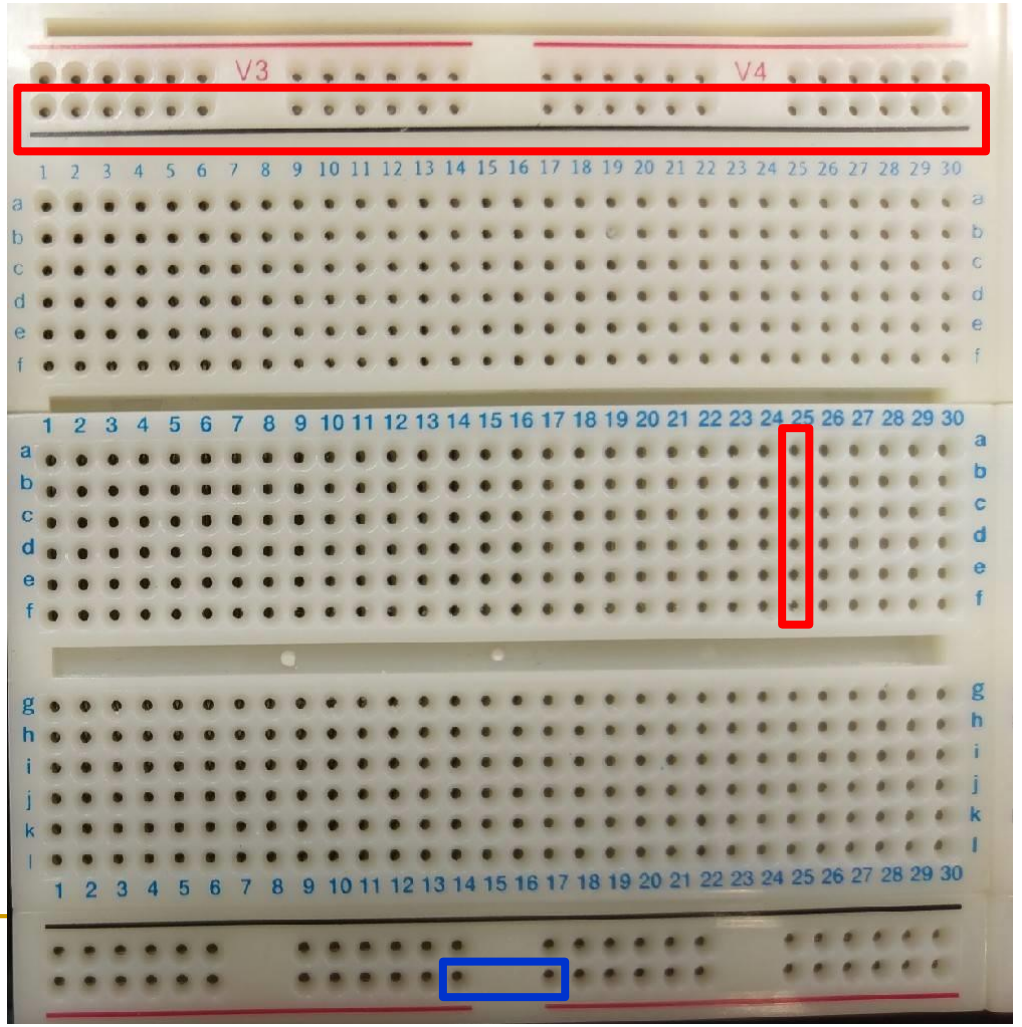


Top View of the Solderless Breadboard

: connected

: disconected



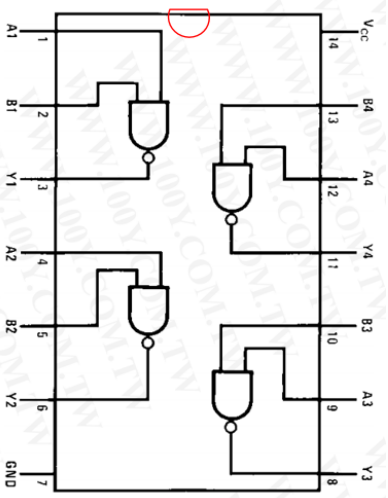


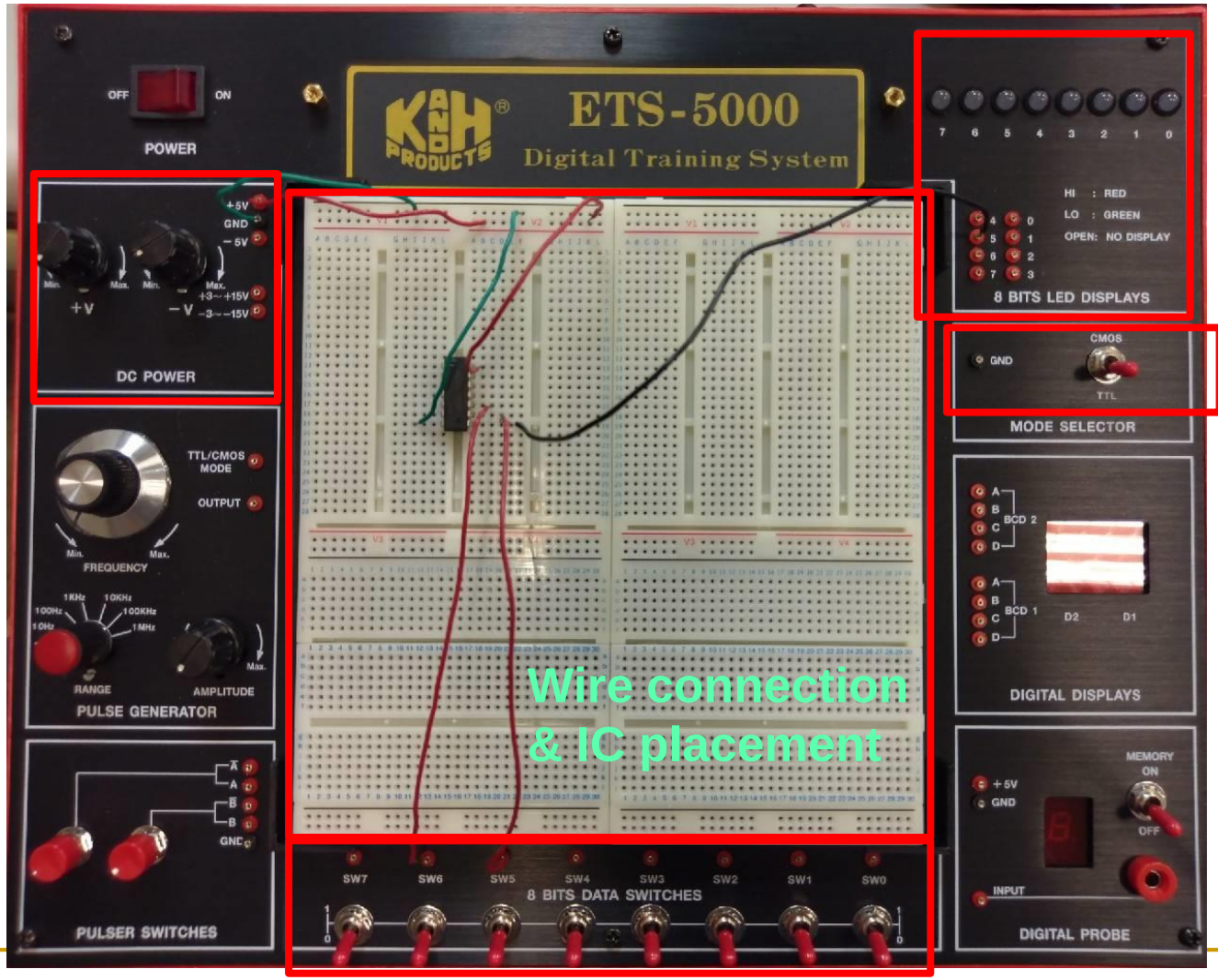
Example: Connection with 74LS00 Chip(1/7)

- **Board**

power supply

Chip(NAND)





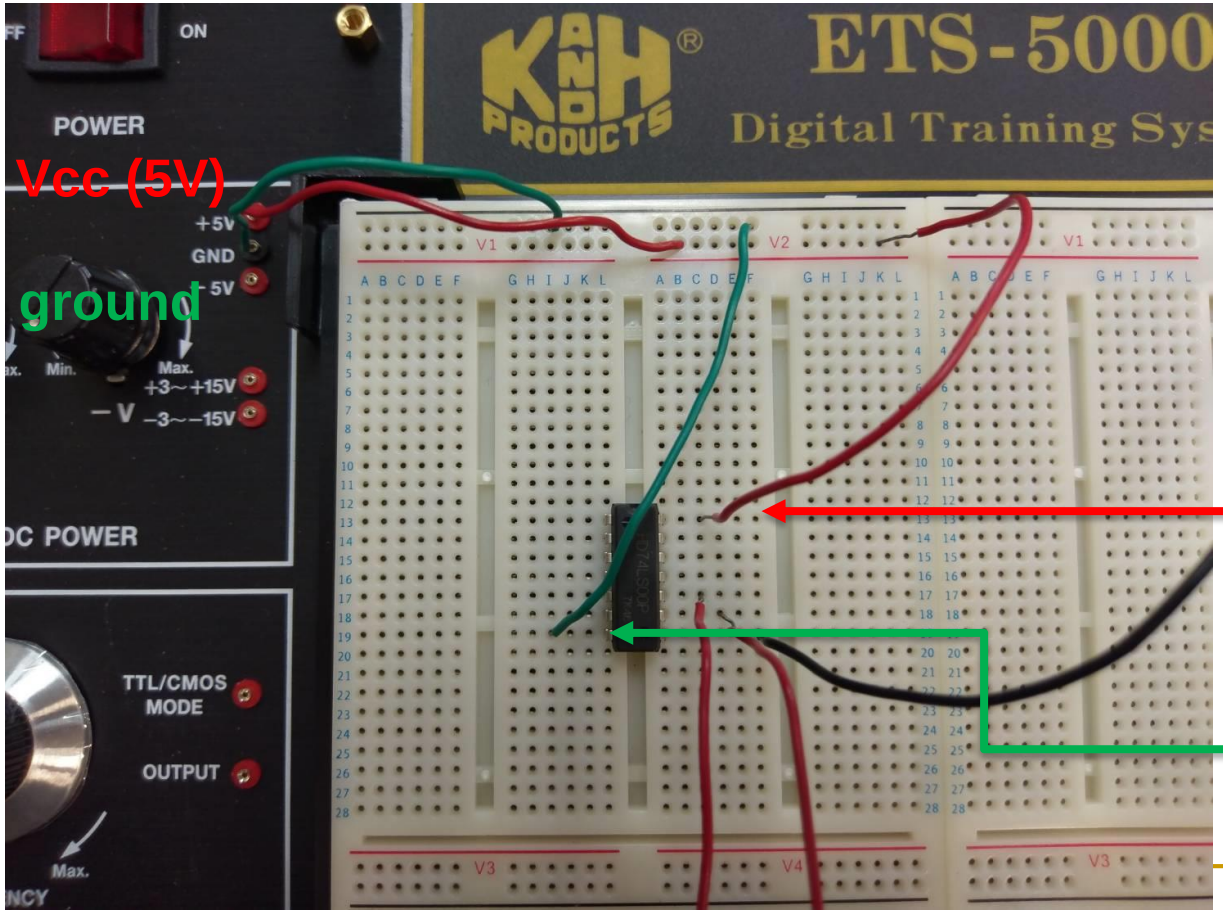
output

TTL mode

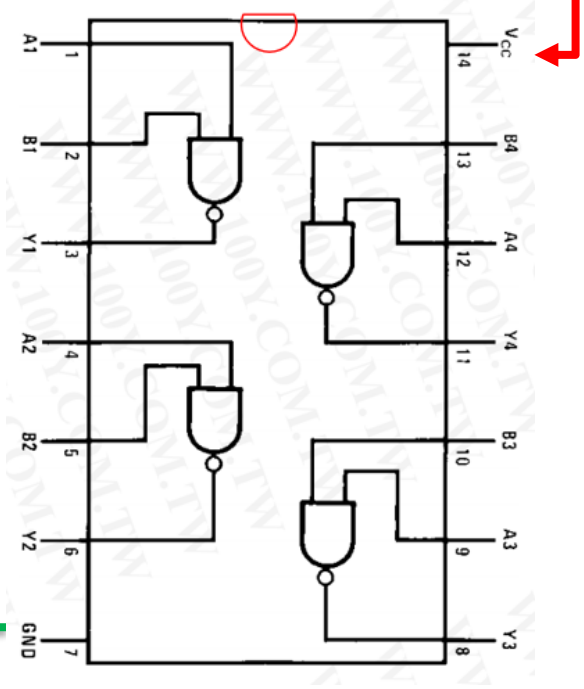
input

Example: Connection with 74LS00 Chip(2/7)

- **Board : wire connection**



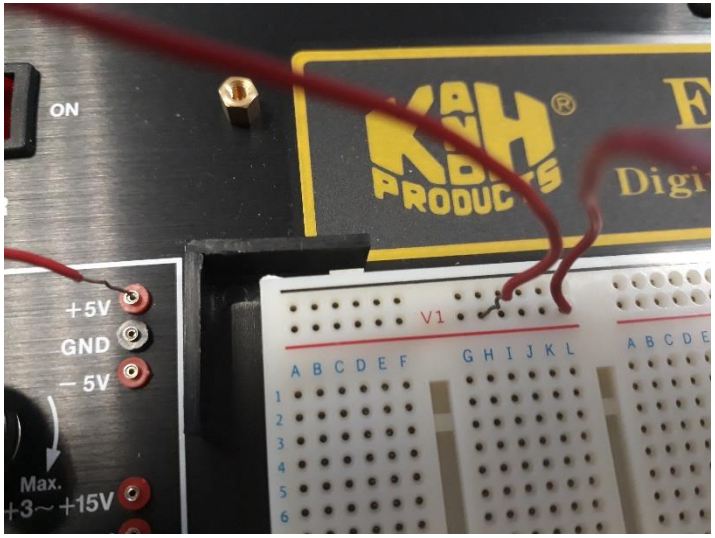
Chip(NAND)



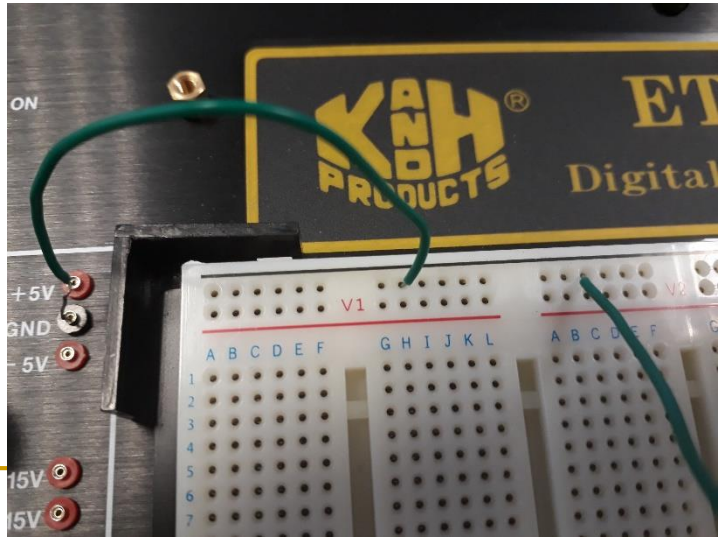
Example: Connection with 74LS00 Chip(3/7)

- **Power supply**

VCC

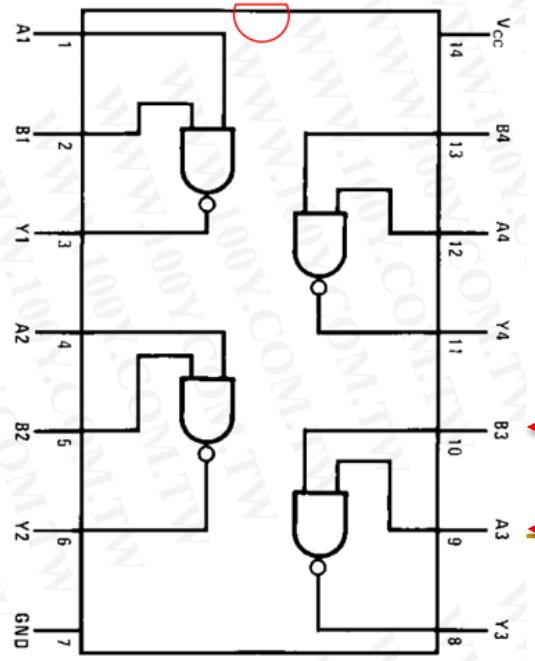


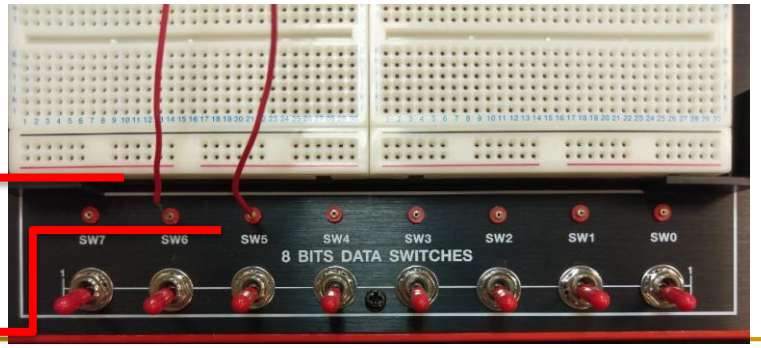
GND



Example: Connection with 74LS00 Chip(4/7)

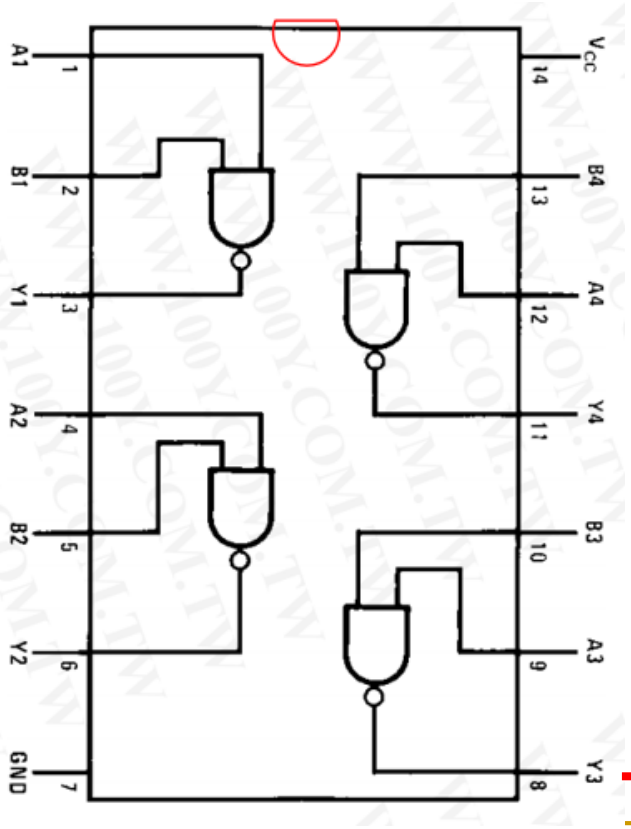
- Signal input





Example: Connection with 74LS00 Chip(5/7)

- **Signal output**

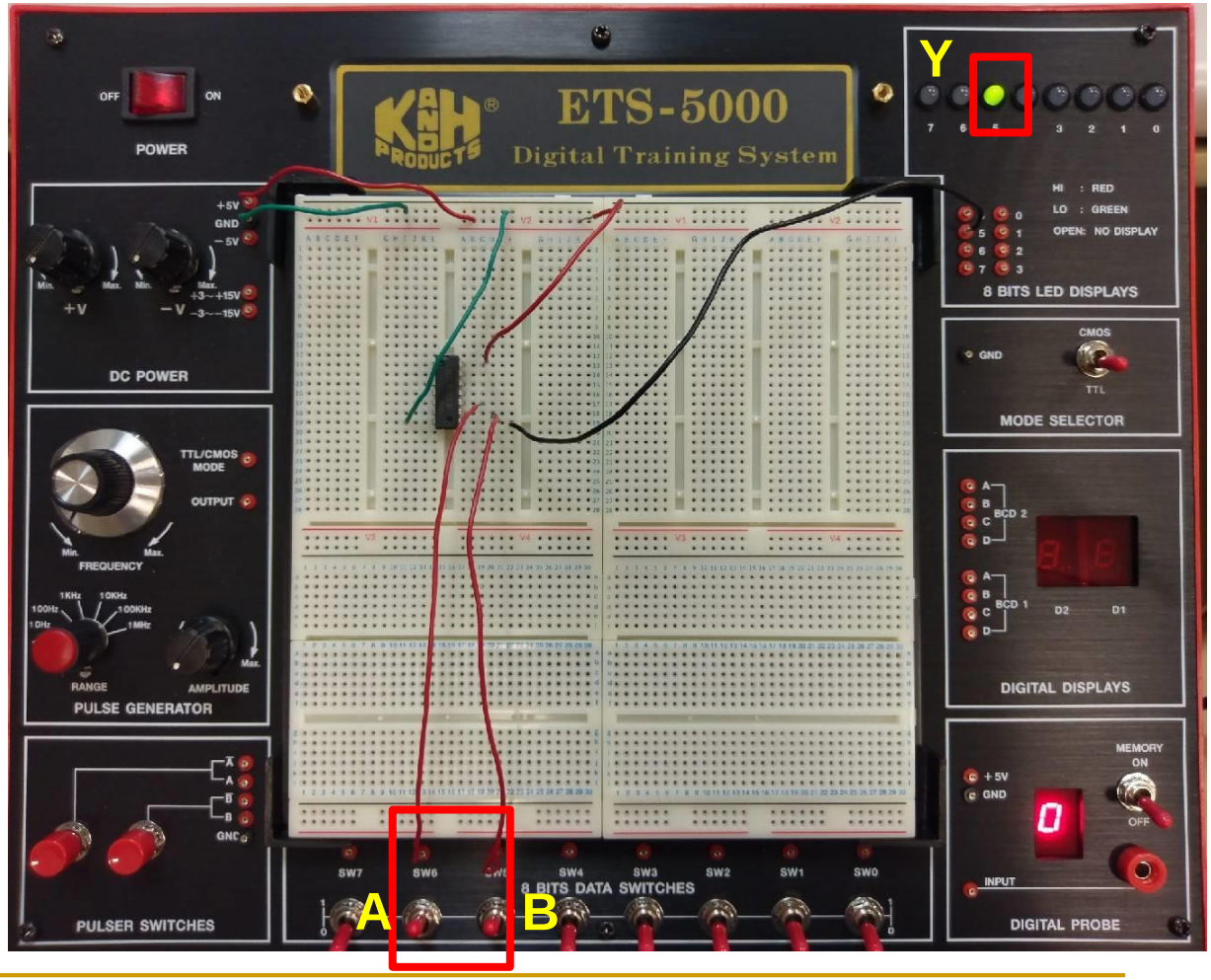


Example: Connection with 74LS00 Chip(6/7)

- **Input 11**
- **Output 0**

74LS00 truth table

Input		Output
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

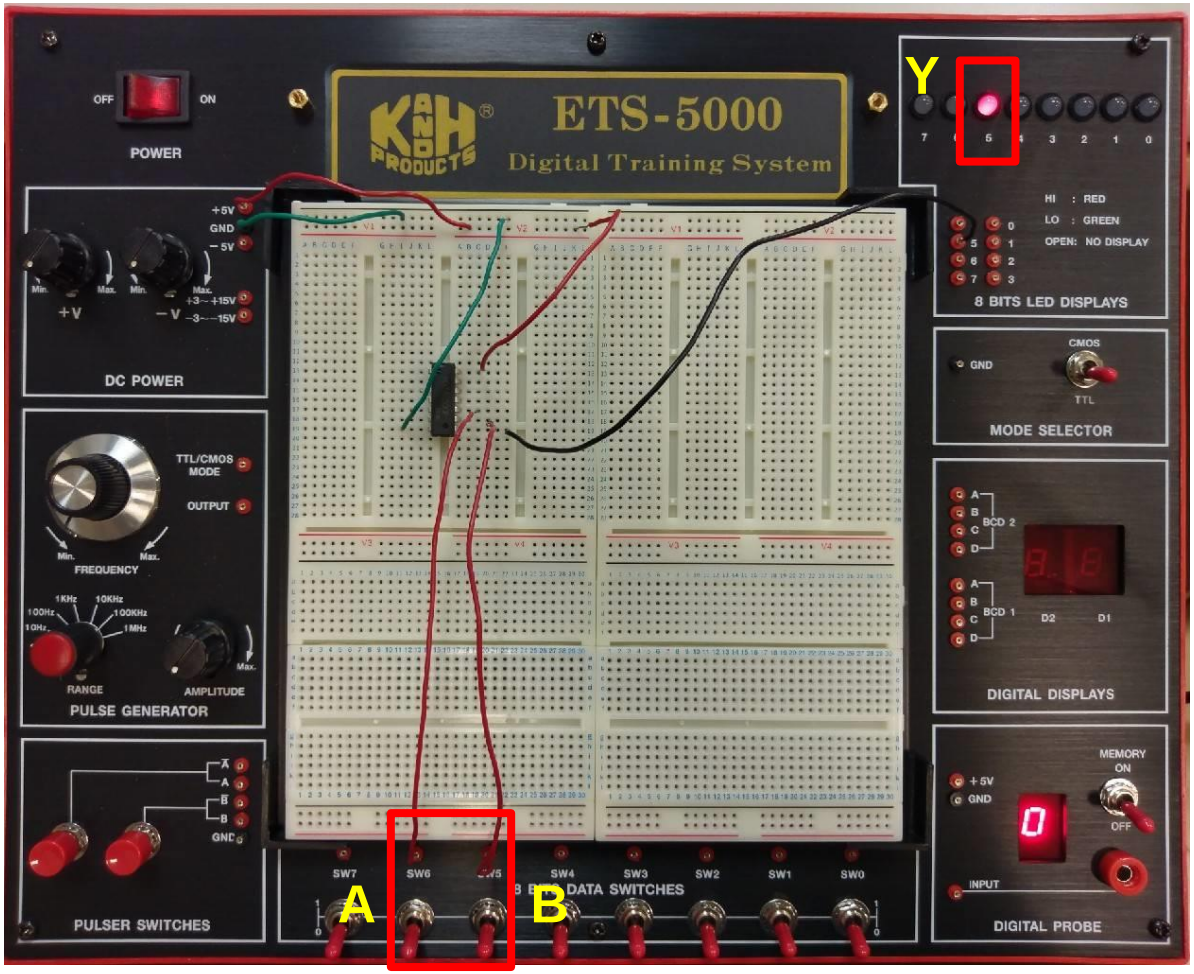


Example: Connection with 74LS00 Chip(7/7)

- **Input 00**
- **Output 1**

74LS00 truth table

Input		Output
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0



Equipment

Names	Amount
Solerless Breadboard	×1
74LS00	×1
74LS04	×1
74LS08	×1
74LS32	×1

Lab notice

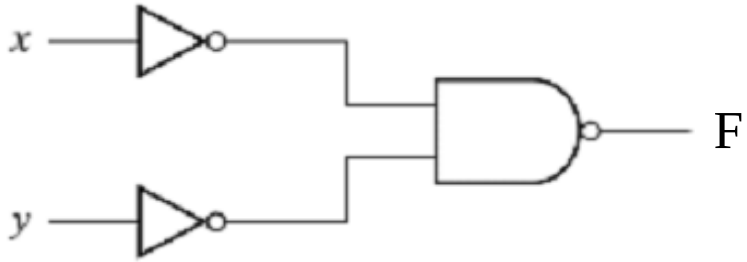
- **Input**

- **Output**

Lab I

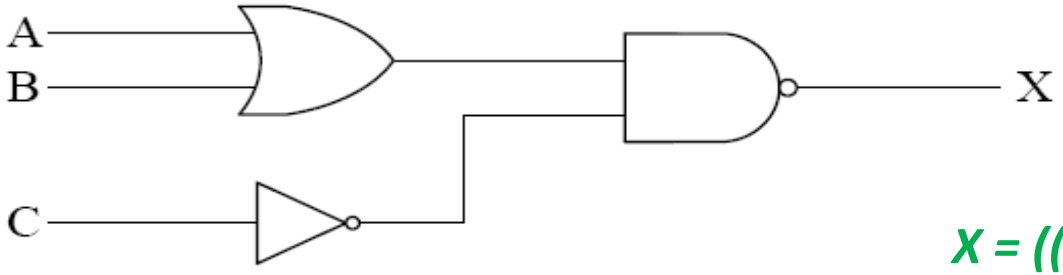
Please (a) draw the truth table of the following circuit and (b) implement the circuit on the breadboard.

(1)



F = (x'y')'

(2)



X = ((A + B)C')'

Lab II(additional)

- **Please draw their Truth Tables and implement the circuits with breadboard.**
  - **$F_1(A, B) = (A + B)'(A' + B')$**
  - **$F_2(A, B) = A' + AB$**