Time: 10:15~11:50 AM

All the design problems must be described as detail as possible for your answer.

Save the usage of the answer sheets!

1. (a) Design a four-bit binary adder/subtractor from basic logic gates. (10%)
   (b) Use the adder designed in (a) to construct a module 12 adder. (10%)

2. (a) Design a 2-to-1 multiplexer from basic logic gates. (10%)
   (b) Use the multiplexer designed in (a) to create an 8-to-1 multiplexer. (5%)
   (c) Implement a 3-input XOR function with the multiplexer designed in (b). (5%)

3. Design a decimal to Gray code converter from basic logic gates. (10%)

4. Design an adder that is controlled by two control inputs, M, and N. The inputs are used to specify what value is to be added to a 4-bit input number. If the control inputs are MN=00, do not change the input number. If the control inputs MN=01, then add the number 2, If the control inputs MN=10, then add the number 3. If the control inputs MN=11, then add the number 5. (15%)

5. Design a 3-to 8 priority encoder. (10%)

6. A 3-to-8 decoder is used to decode eight addresses. However several of the addresses are lost and never decoded. The circuit's output is shown as the table. Decide the cause of the lost addresses. (10%)

Decoder Inputs			Decoder Outputs							
C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	1	1	0	1	1	1	1	1
0	0	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	0
1	1	0	1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	0

7. Use the Gate-Level, Dataflow, and Behavioral of HDL Models to describe the function of a Four-Bit Comparator, respectively. (15%)