Computer Organization & Assembly Language

Final Exam – 2010/1/15

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1. Answer *True* or *False* to the following statements. (30%)

(A) When designing the processor, the control signals RegRead and RegWrite are used for controlling the data access of register files. 毫無關連

(B) The Zero output of ALU is only used for conditional branch instructions.

(C) In the single-cycle design, all control signals except the PCSrc can be set based on the contents of the instruction to be executed.

(D) Designing the control is more complicated than designing the datapath since it requires an understanding of how all the components in the processor operate. 了解處理器原件如何

(E) In an instruction set like the 80x86, where instructions are not of the same length, pipelining is considerably easier.

(F) In a pipelined system, forwarding will eliminate the need of any stalls.

(G) The CPI value of an ideal pipeline processor is the same as that of a single-cycle processor.

(H) Pipelining increases throughput and reduces individual instruction execution time.

(I) Pipeline bubbles cause loss of performance since that a number of pipeline stages are left empty.

(J) Data forwarding can help reducing the possible delay in control hazards.

2. For a single-cycle processor, assume the following latencies for logic blocks in the datapath:

I-Mem.	Reg. Read	ALU	D-Mem.	Reg. Write
500ps	220ps	180ps	1000ps	220ps

(A) What is the clock cycle time if the only type instructions we need to support are ALU instructions (i.e., add, and, ... etc)? (4%)

(B) What is the clock cycle time if we only had to support lw instructions? (4%)

(C) What is the clock cycle time if we must support add, beq, lw, and sw instructions? (4%)

For the remaining problems, assume that we use the above logic blocks in another pipelined processor. Also, assume that there are no pipeline stalls and that the breakdown of executed instructions is as follows:

add	addi	not	beq	lw	sw
25%	5%	5%	15%	35%	15%

(D) In what fraction of all cycles is the data memory used?

(E) If we can improve the latency of one of the given datapath components by 20%, which component should it be to optimize the overall performance? What is the speed-up from this improvement? (6%)

3. How many clock cycles does it take for the following codes to be executed on a single-cycle processor? and on a pipelined processor (with forwarding enabled)? (6%)

```
sub   $3, $4, $5
lw    $4, 10($6)
add   $7, $3, $4
sw    $7, 20($6)
add   $7, $2, $1
```

IF ID Ex MEM WB

5 10

4. Structural, data and control hazards typically required a processor pipeline to stall. For each of the following optimization techniques, state which pipeline hazard(s) it addresses. Note that some optimization techniques may address more than one hazard. (12%)

(A) branch prediction control

(B) instruction scheduling data

(C) forwarding data

(D) increasing availability of functional units (i.e., ALUs, adders, ... etc)

5. Consider the following sequence of actual outcomes for a single static branch where T means the branch is taken and N means the branch is not taken. Also, assume that this is the only branch in the program.

N T T T NT N T T T N T N T T T N T N
T T T NTNTTTNTNTTTNTN

(A) Assume that we try to predict this sequence with the 1-bit predictor (which is initialized to the N state). What is the predicted sequence? How many branches are mis-predicted? (6%)

(B) How about using the 2-bit predictor (which is initialized to the T state)? (6%)

6. Consider a MIPS machine with a 5-stage pipeline with a cycle time of 10ns. Assume that you are executing a program where a fraction f of all instructions immediately follow a load upon which they are dependent (i.e., load-use hazard).

(A) With forwarding enabled, what is the total execution time for N instructions (in terms of f)? (6%)

(B) Consider a scenario where the MEM stage, along with its pipeline registers, needs 12ns. There are now two options:

(1) add another MEM stage so that there are MEM1 and MEM2 stages (but an extra stall is introduced for load-use hazards)

(2) increase the cycle time to 12ns so that the MEM stage fit within the new cycle time and the number of pipeline stages remain unaffected.

For a program mix with the above characteristics, when is the first option better than the second? (Your answer should be based on the value of f.) (12%)