12.5 Common Source Amplifiers

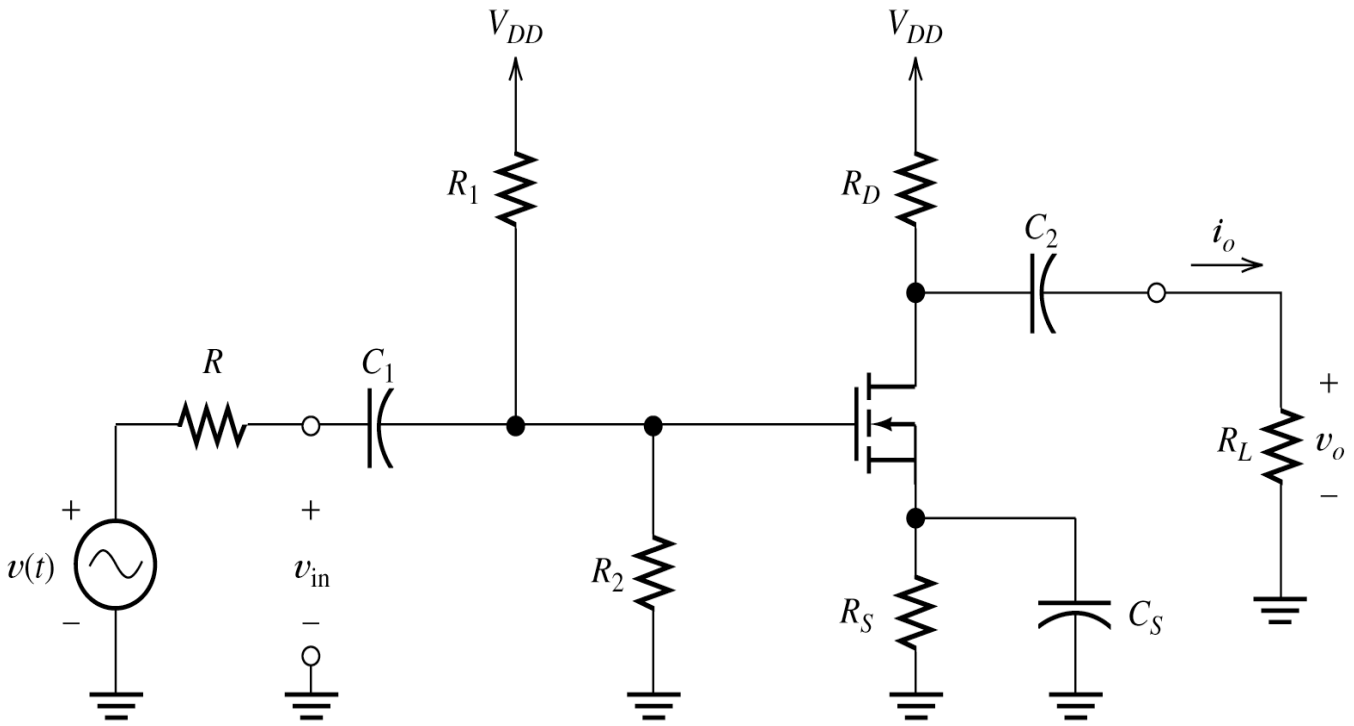


Figure 12.22 Common-source amplifier.

v_{in}?

v_o?

Voltage gain

$A_v = v_o / v_{in}$?

Common-Source Amplifiers

- C_1 and C_2 are coupling capacitors and C_s is the bypass capacitor. The capacitors are intended to have large impedances for the dc signal and very small impedances for the ac signal.

$$Zc = \frac{1}{j2\pi fC}$$

$$\begin{cases} Zc \to \infty, \ f = 0 \\ Zc \to 0, \ f >> 0, \text{or } C \text{ is large} \end{cases}$$

Common-Source Amplifiers

- For DC analysis, the capacitors are replaced by open circuits to determine the quiescent operation point (Q point). The **transconductance** g_m for the small-signal equivalent circuit is also determined.

- For AC analysis, the capacitor are replaced by short circuits to determine the ac voltage gain $A_v = v_o / v_{in}$.

DC Analysis

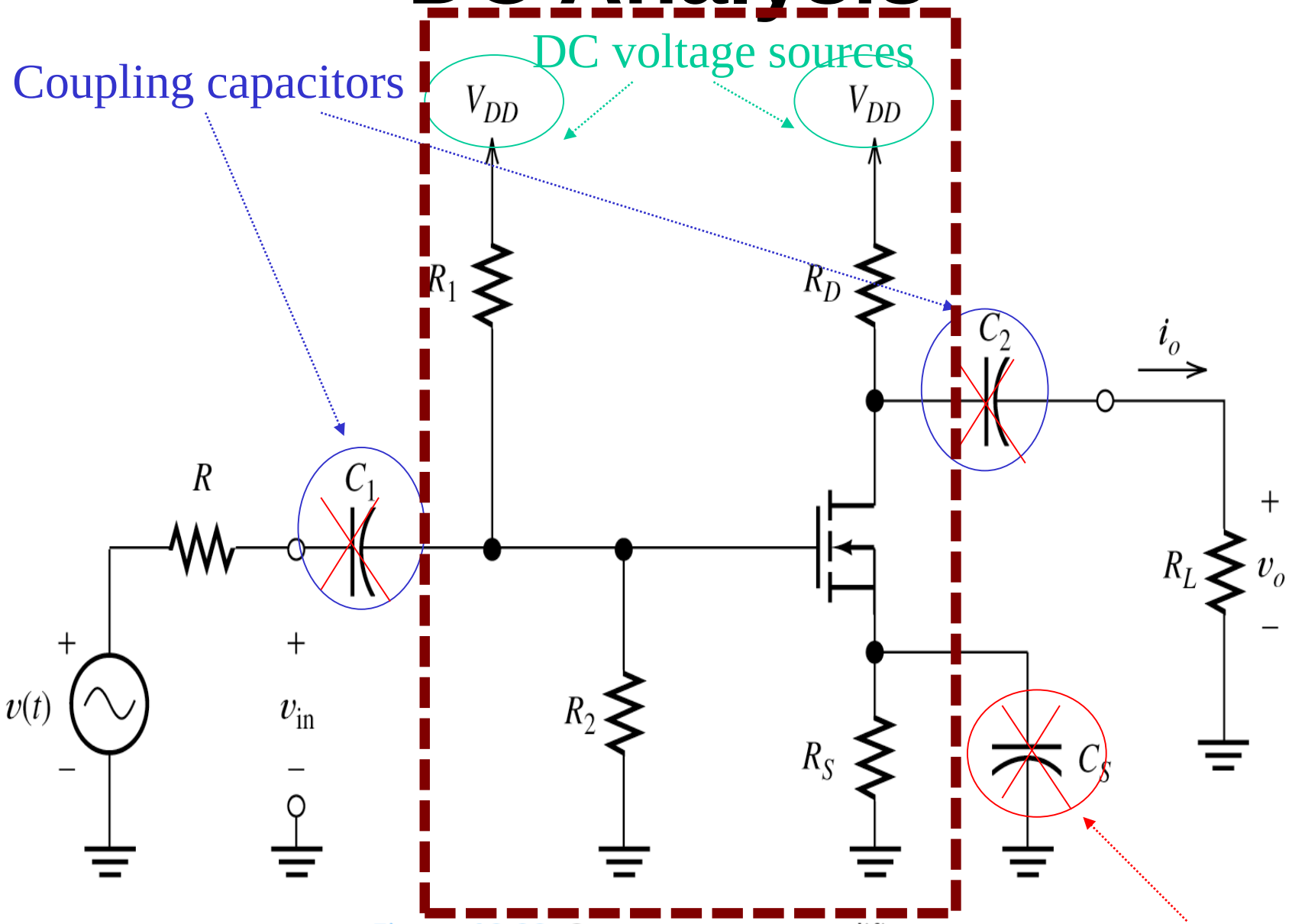


Figure 12.22 Common-source amplifier.

The Small-Signal Equivalent Circuit

- In small-signal midband analysis of FET amplifiers, the coupling capacitors, bypass capacitors, and dc voltage sources are replaced by short circuits.
- The FET is replaced with its small-signal equivalent circuit. Then, we write circuit equations and derive useful expressions for gains, input impedance, and output impedance.

AC Analysis

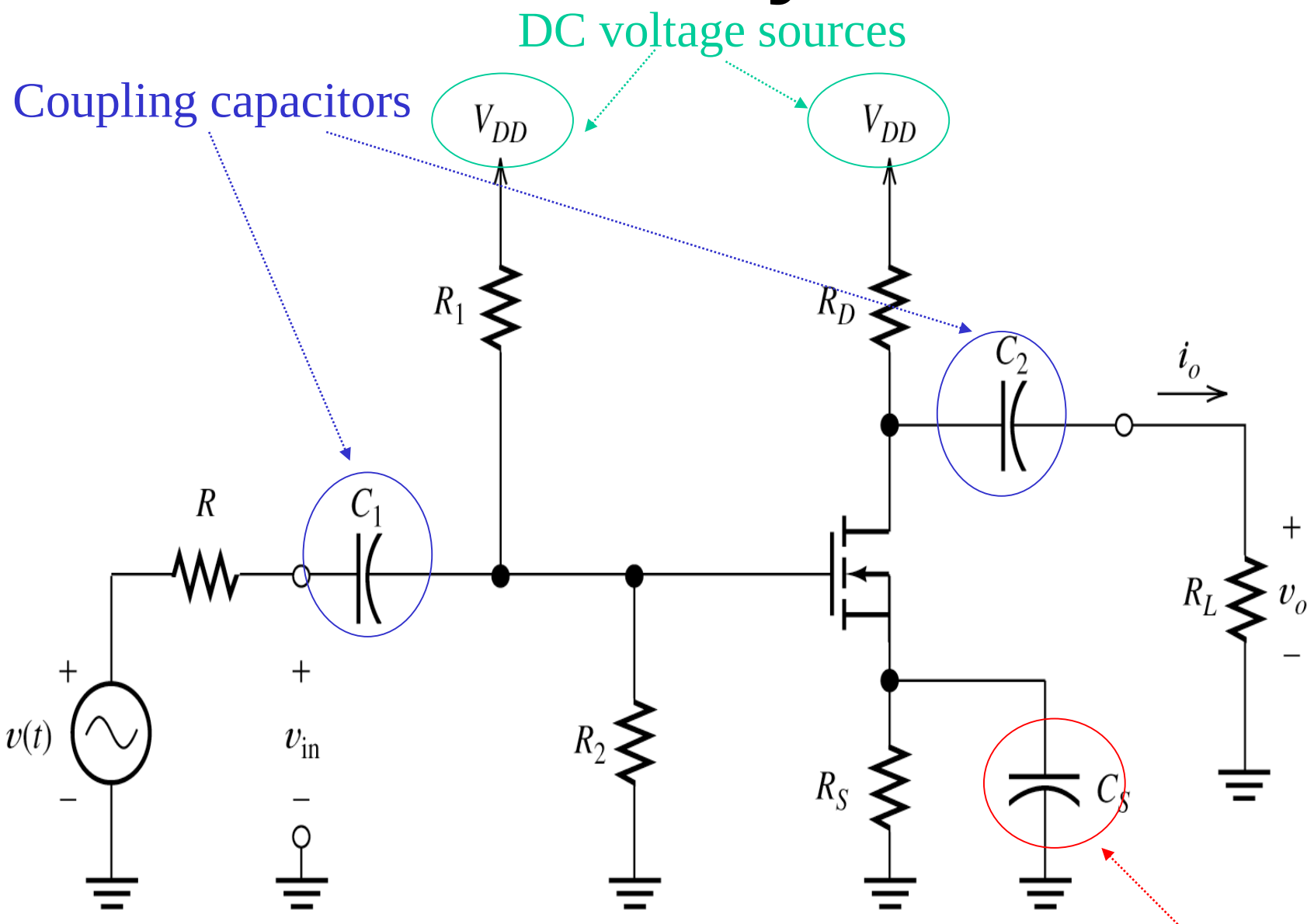


Figure 12.22 Common-source amplifier.

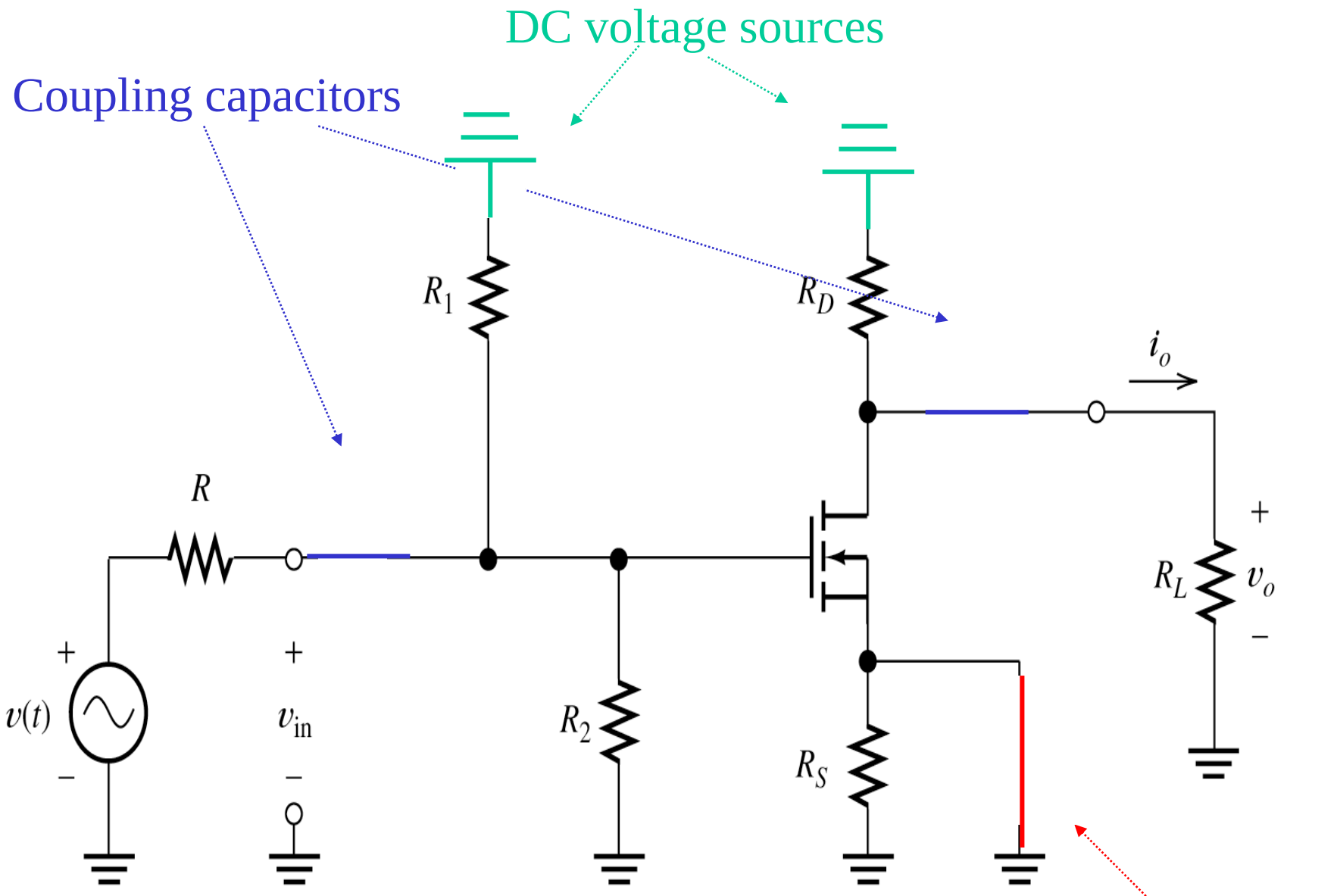
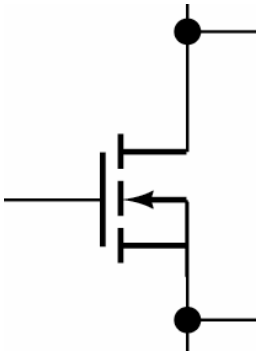


Figure 12.22 Common-source amplifier.

SMALL-SIGNAL EQUIVALENT CIRCUITS (12.4)



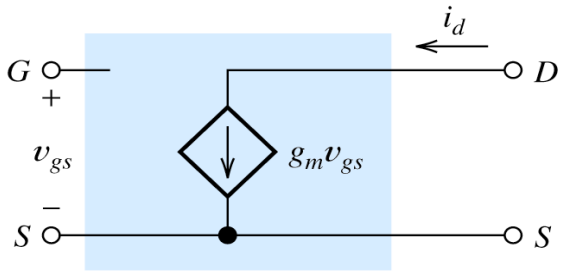


Figure 12.19 Small-signal equivalent circuit for FETs.

$$i_d(t) = g_m v_{gs}(t)$$

A more complex equivalent circuit consider drain resistance r_d

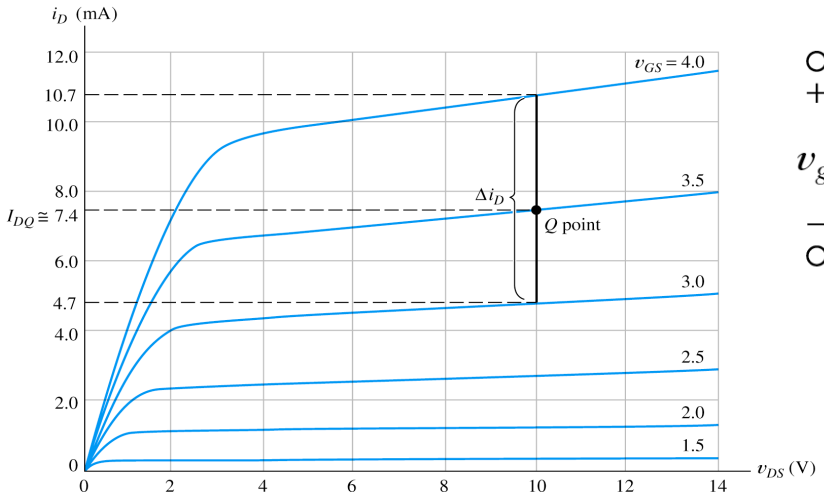
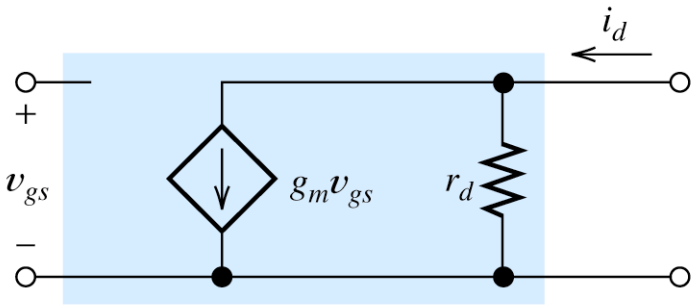


Figure 12.21 Determination of g_m and r_d. See Example 12.3.



$$1/r_d = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q-\text{point}}$$

$$i_d(t) = g_m v_{gs}(t) + v_{ds} / r_d$$

Common Source Amplifiers: FET source 端接ground

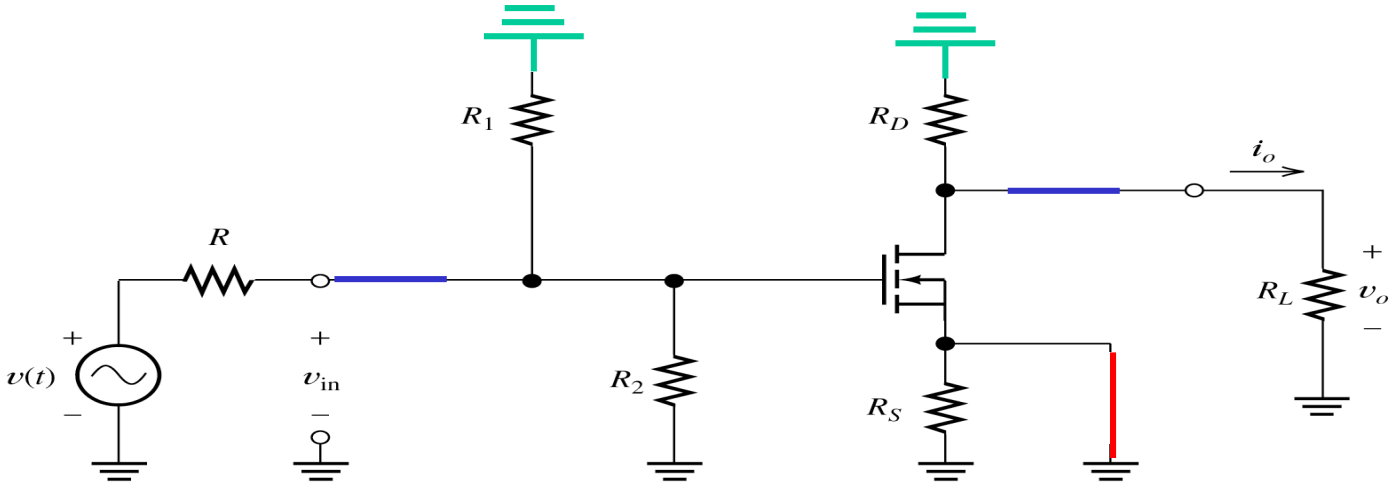


Figure 12.22 Common-source amplifier.

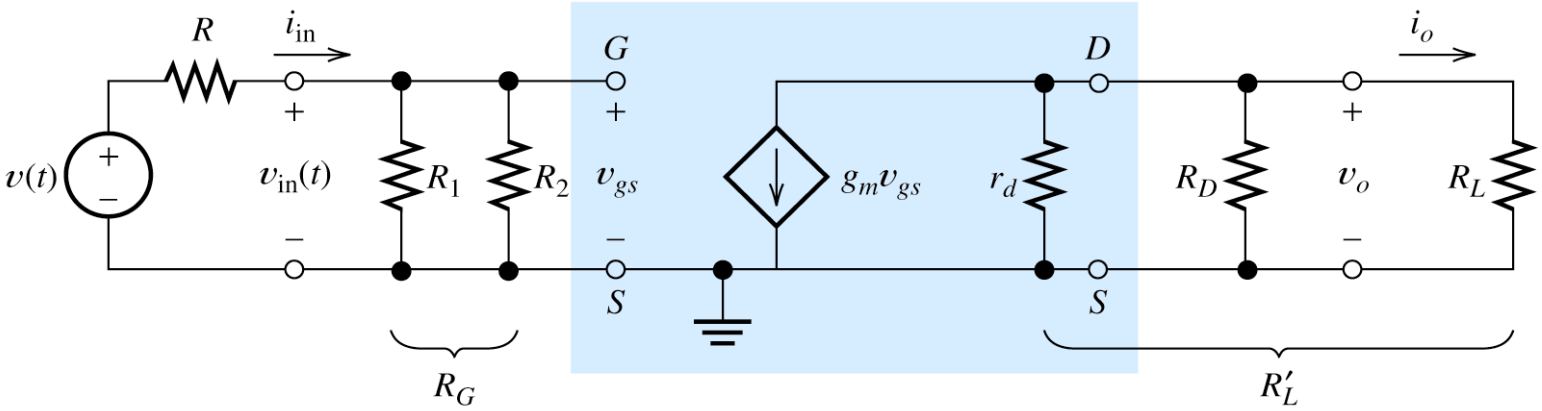


Figure 12.23 Small-signal equivalent circuit for the common-source amplifier.

Common Source Amplifiers:

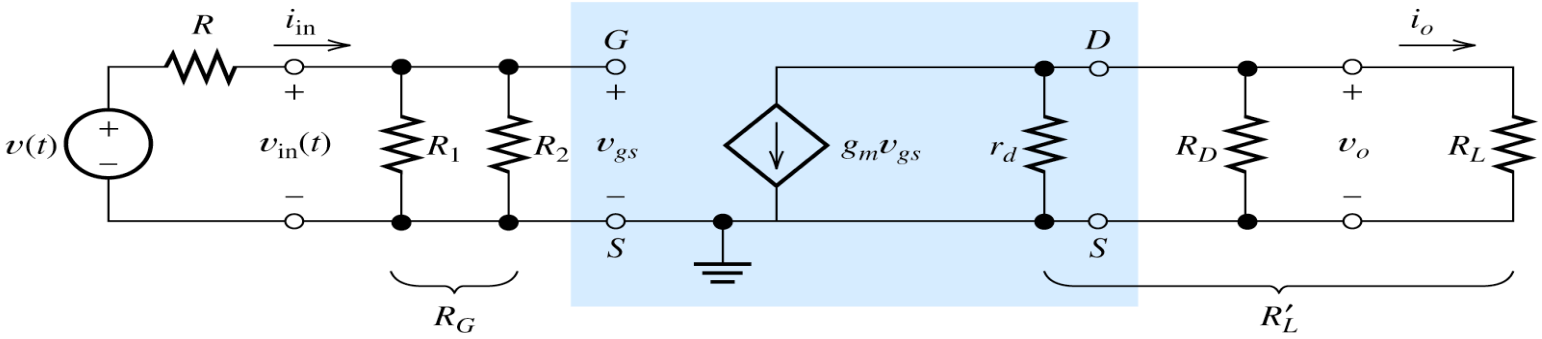


Figure 12.23 Small-signal equivalent circuit for the common-source amplifier.

Equivalent load resistance

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L}$$

Input voltage & output voltage

$$\begin{cases} v_o = -g_m v_{gs} R'_L \\ v_{in} = v_{gs} \end{cases}$$

Voltage Gain

$$A_v = \frac{v_o}{v_{\text{in}}} = -g_m R'_L$$

Common Source Amplifiers:

Input Resistance

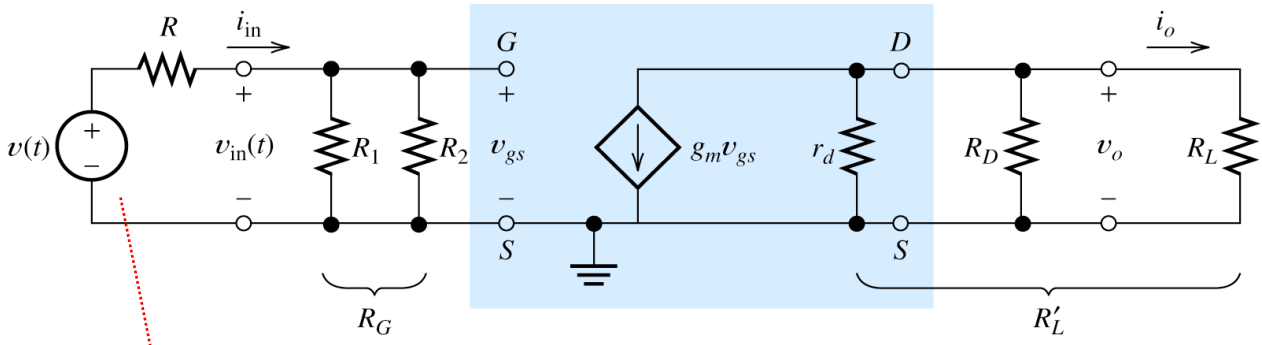


Figure 12.23 Small-signal equivalent circuit for the common-source amplifier.

$$R_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} = R_G = R_1 \| R_2$$

Output resistance

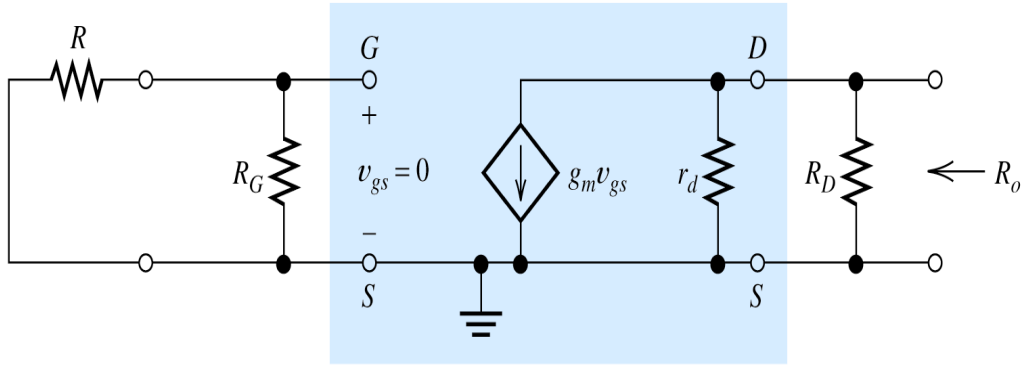


Figure 12.24 Circuit used to find R_o.

- disconnect the load,
- replace the signal source by the internal resistance,
- find the resistance by looking into the output terminals.

$$R_o = \frac{1}{1/R_D + 1/r_d}$$

Example 12.4

Analyze the following circuit. KP=50uA/V^2, V_{to}=2 V, L=10um, W=400um (identical to example 12.2).

Assume

$$\begin{cases} v(t) = 100\sin(2000\pi t)\text{mV} \\ r_d = \infty \end{cases}$$

Find

- midband voltage gain
- input resistance
- output resistance
- output voltage

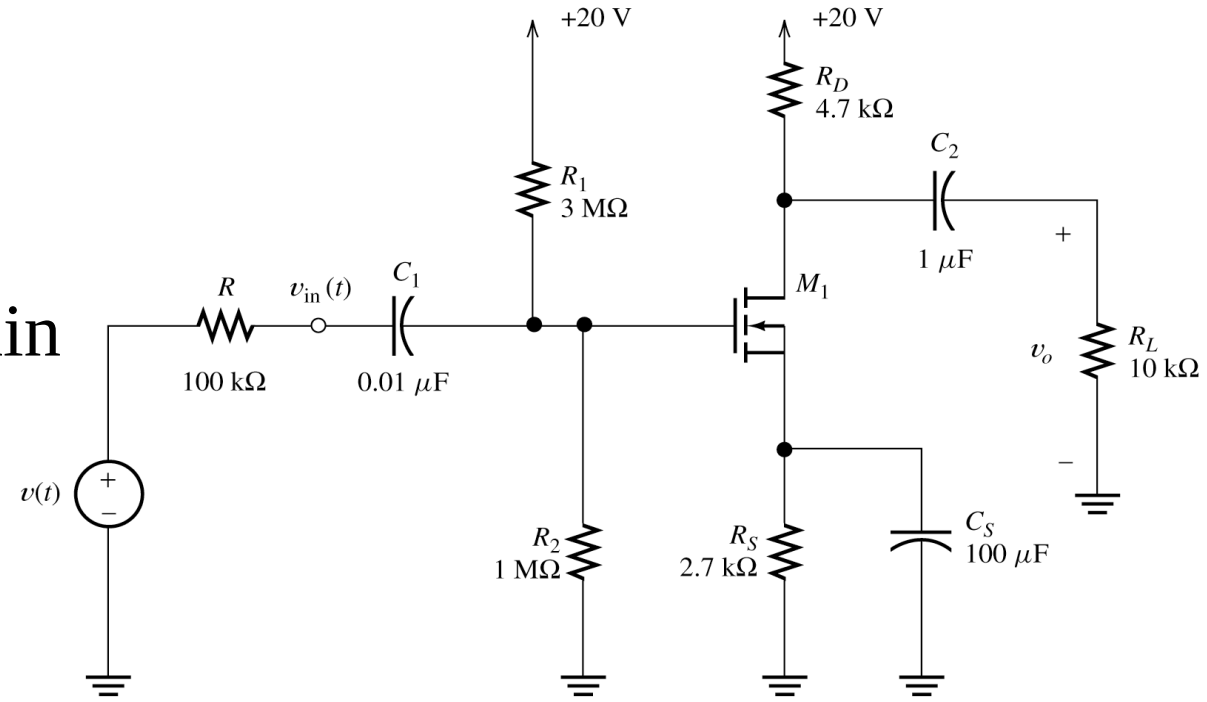


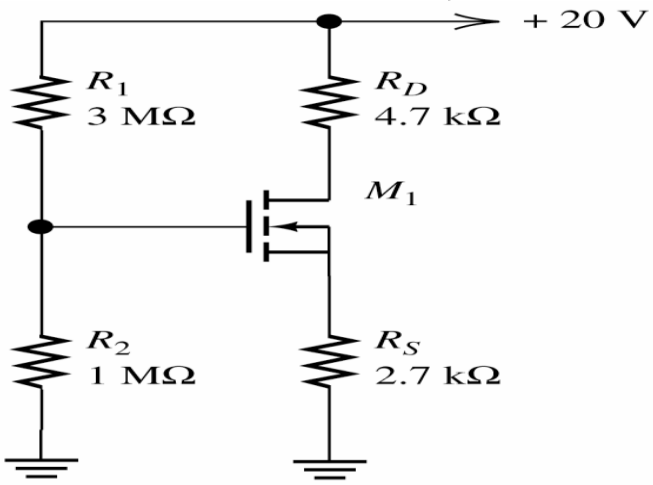
Figure 12.25 Common-source amplifier.

Example 12.4

Analyze the following circuit. KP=50uA/V^2, V_{to}=2 V, L=10um, W=400um (identical to example 12.2).

DC Analysis

Fine Q point (see example 12.2)



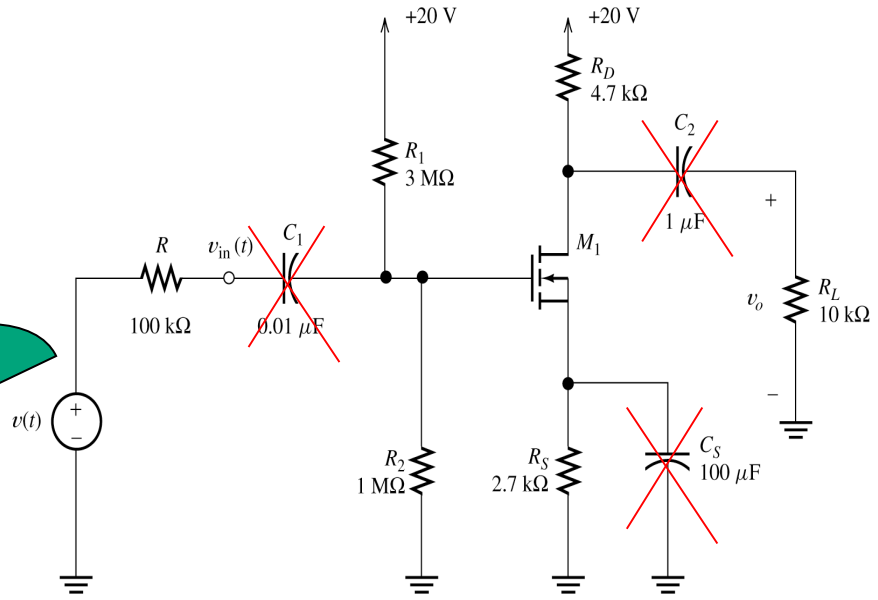


Figure 12.25 Common-source amplifier.

$$I_{DQ} = K(V_{GSQ} - V_{to})^2 = 0.784mA$$

Example 12.4

Analyze the following circuit. KP=50uA/V^2, V_{to}=2 V, L=10um, W=400um (identical to example 12.2).

AC Analysis

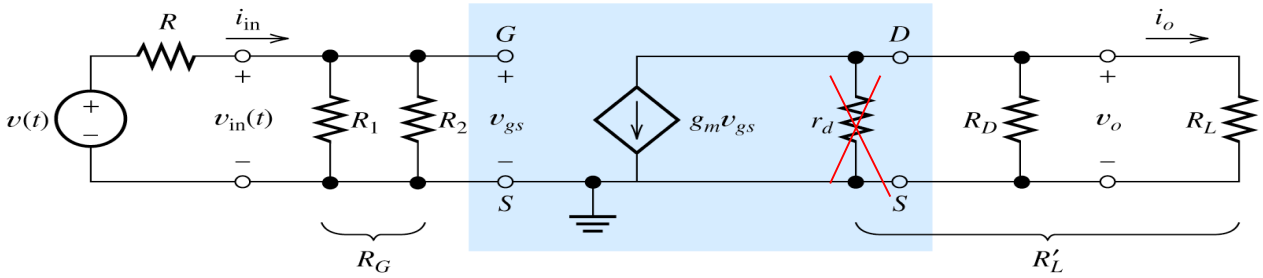


Figure 12.23 Small-signal equivalent circuit for the common-source amplifier.

Fine g_m(see Ch 12.4)

$$g_m = 2K(V_{GSQ} - V_{to}) = \sqrt{2KP}\sqrt{W/L}\sqrt{I_{DQ}} = 1.77mS$$

Equivalent load resistance

$$R'_L = \frac{1}{1/r_d + 1/R_D + 1/R_L} = 3197\Omega \qquad (r_d = \infty)$$

Voltage Gain

$$A_v = \frac{v_o}{v_{in}} = -g_m R'_L = -5.66$$

Example 12.4

Analyze the following circuit. KP=50uA/V^2, V_{to}=2 V, L=10um, W=400um (identical to example 12.2).

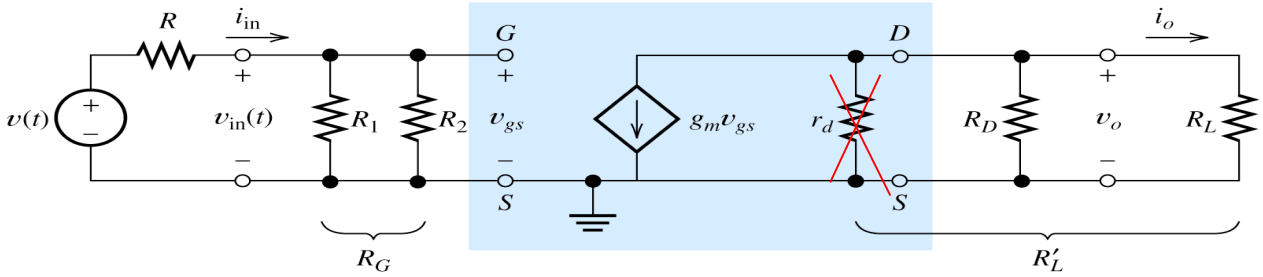


Figure 12.23 Small-signal equivalent circuit for the common-source amplifier.

Input Resistance

$$R_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} = R_G = R_1 \| R_2 = 750k\Omega$$

Output Resistance

$$R_o = \frac{1}{1/R_D + 1/r_d} = R_D = 4.7k\Omega$$

Input voltage

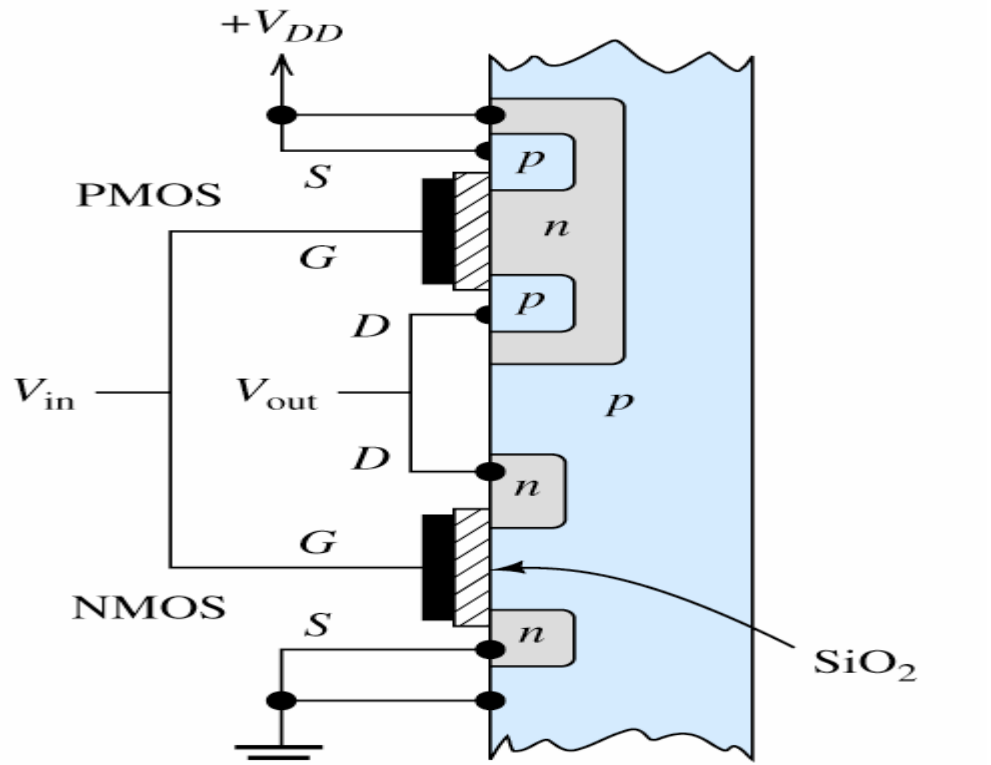
$$v_{in}(t) = v_{gs}(t) = v(t)\frac{R_{in}}{R_{in}+R} = 88.23\sin(2000\pi t)\text{mV}$$

Output voltage

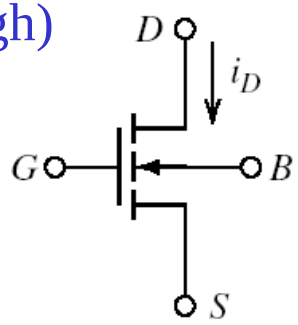
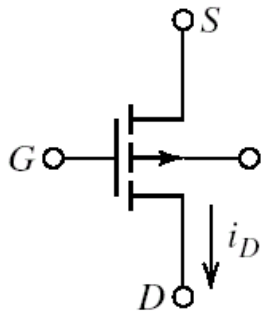
$$v_o(t) = A_v v_{in}(t) = -500\sin(2000\pi t)\text{mV}$$

12.7 CMOS Logic Gate

CMOS: Complementary Metal-Oxide- Semiconductor (互補式金氧半導體是一種積體電路製程，可在矽晶圓上製作出PMOS（P-channel MOSFET）和NMOS（N-channel MOSFET）元件，由於PMOS與NMOS在特性上為互補性，因此稱為CMOS。



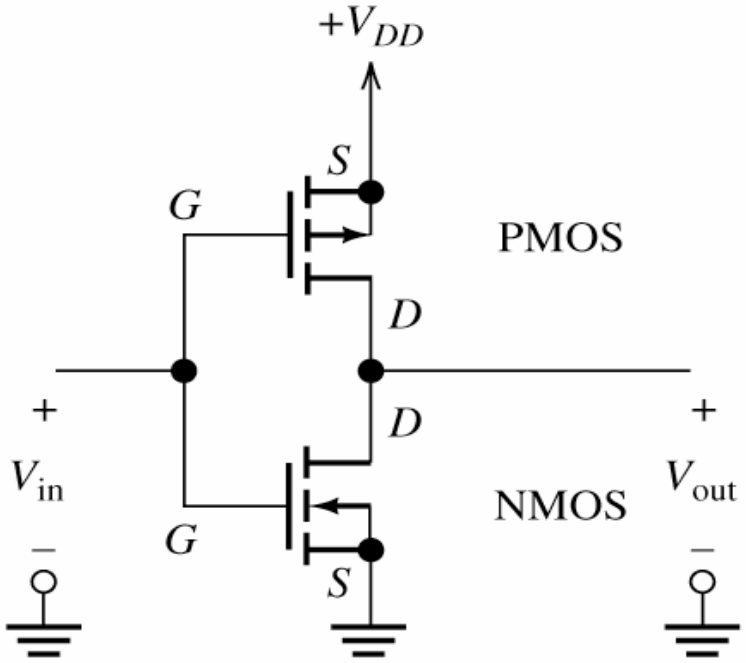
MOSFET Summary

	NMOS	PMOS
Circuit symbol	$V_{GS}=V_{DD}$ (high) NMOS ON $V_{GS}=0$ (low) NMOS OFF 	 $V_{GS}=-V_{DD}$ PMOS ON $V_{GS}=0$ PMOS OFF
KP (typical value)	50 μA/V^2	25 μA/V^2
K	(1/2) *KP* (*W*/*L*)	(1/2) *KP* (*W*/*L*)
V_{to} (typical value)	+1 V	–1 V
Cutoff region	$v_{GS} \le V_{to}$ $i_D = 0$	$v_{GS} \ge V_{to}$ $i_D = 0$
Triode region	$v_{GS} \ge V_{to}$ and $0 \le v_{DS} \le v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$	$v_{GS} \le V_{to}$ and $0 \ge v_{DS} \ge v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$
Saturation region	$v_{GS} \ge V_{to}$ and $v_{DS} \ge v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$	$v_{GS} \le V_{to}$ and $v_{DS} \le v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$
v_{DS} and v_{GS}	Normally assume positive values	Normally assume negative values

CMOS Inverter

NMOS $V_{GS}=V_{in}$

PMOS $V_{GS}= V_{in} -V_{DD}$



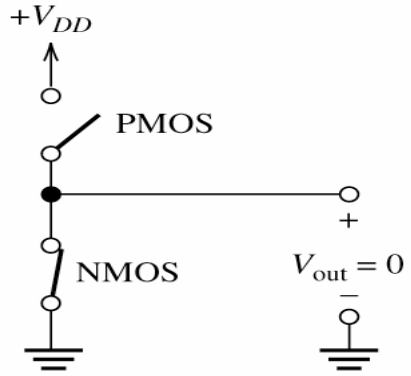
(b) Circuit diagram

$V_{in}=V_{DD}$ (high)

NMOS $V_{GS}= V_{DD}$ ON,

PMOS $V_{GS}= 0$ OFF,

$V_{out}=0$ (low)



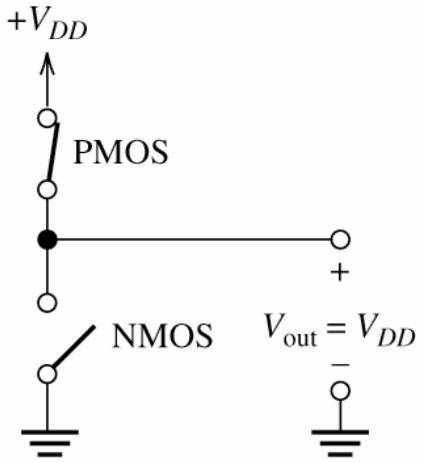
(c) Equivalent circuit with V_{in} high

$V_{in}=0$ (low)

NMOS $V_{GS}= 0$ OFF

PMOS $V_{GS}= -V_{DD}$ ON,

$V_{out}= V_{DD}$ (high)



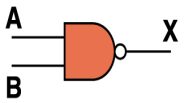
(d) Equivalent circuit with V_{in} low

CMOS NAND Gate

Boolean Expression

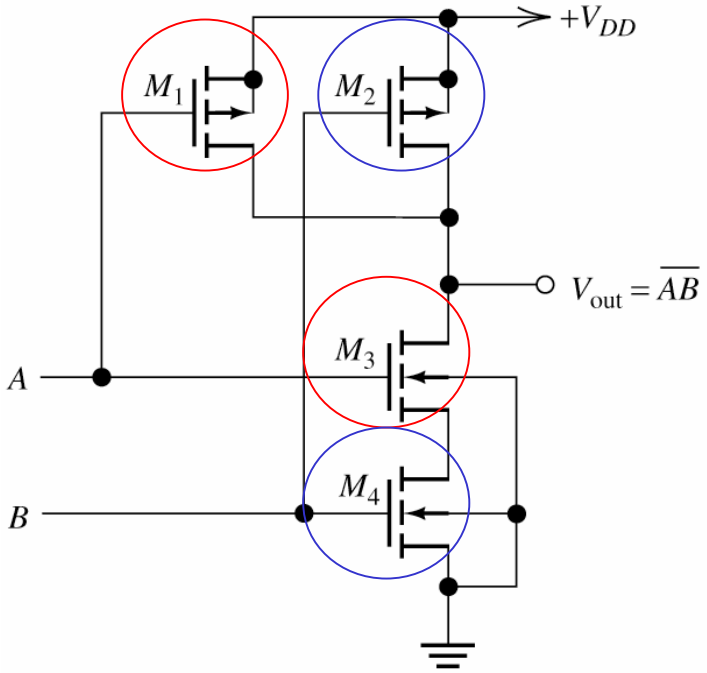
$X = (A \cdot B)'$

Logic Diagram Symbol



Truth Table

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0



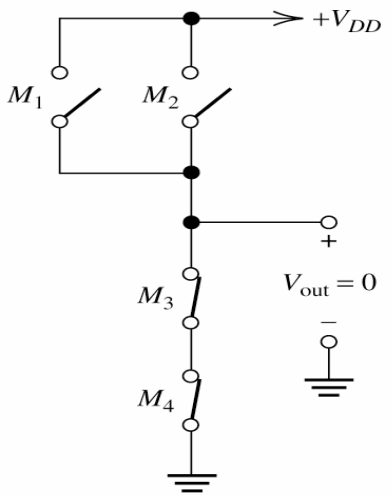
(a) Circuit diagram

1. A= high & B= high

M1 and M2 OFF

M3 and M4 ON

V_{out} low



(c) Both *A* and *B* are high

2. A= low & B= low

M1 and M2 ON

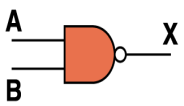
M3 and M4 OFF

V_{out} high

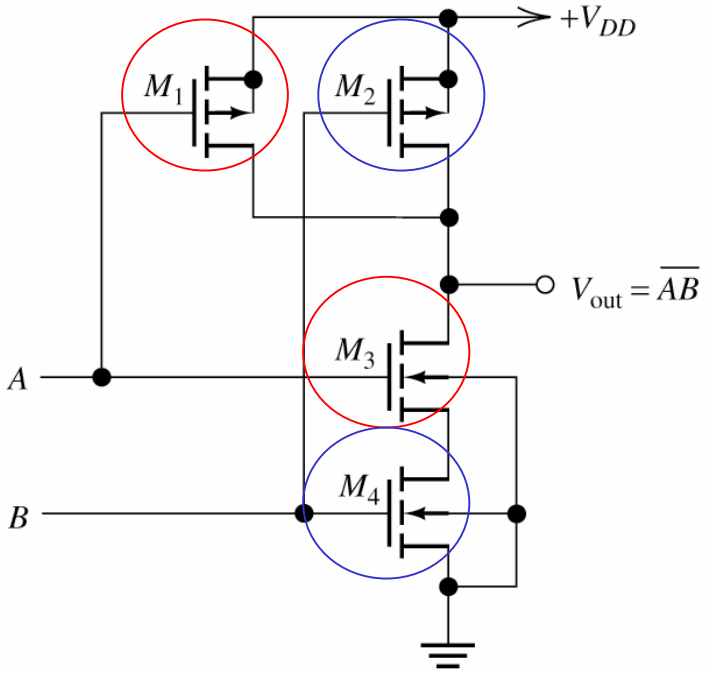
CMOS NAND Gate

Boolean Expression	Logic Diagram Symbol	Truth Table

$X = (A \cdot B)'$



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0



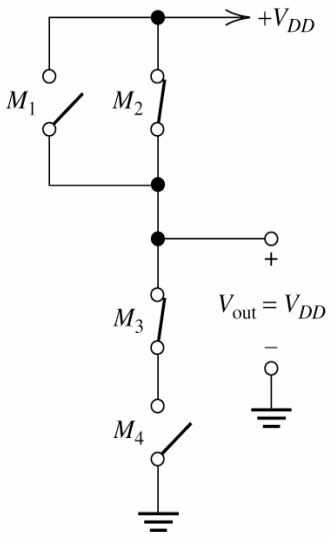
(a) Circuit diagram

3. A= high & B= low

M1 OFF and M2 ON

M3 ON and M4 OFF

V_{out} high



(b) *A* high and *B* low

4. A= low & B= high

M1 ON and M2 OFF

M3 OFF and M4 ON

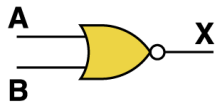
V_{out} high

CMOS NOR Gate

Boolean Expression

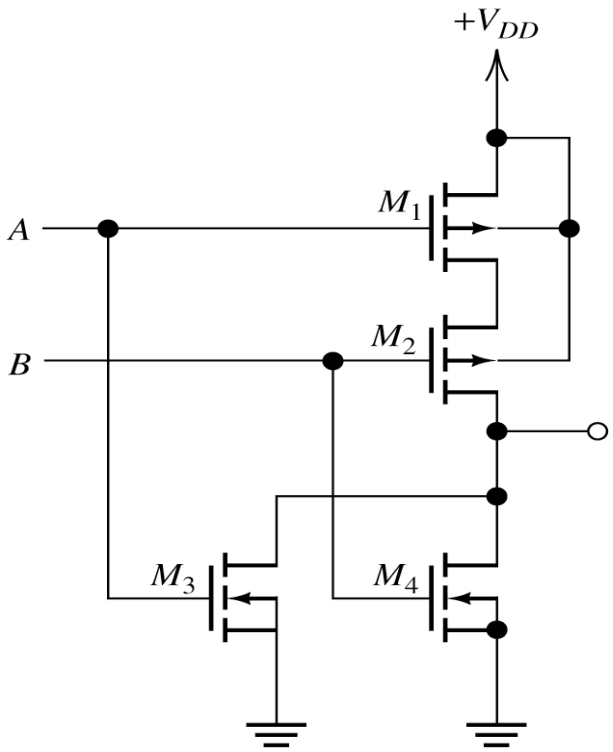
$X = (A + B)'$

Logic Diagram Symbol



Truth Table

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



1. A= low & B= low

M1 and M2 ON

M3 and M4 OFF

V_{out} high

2. A= high & B= low

M1 and M4 OFF

M2 and M3 ON

V_{out} low

3. A= high & B= high

M1 and M2 OFF

M3 and M4 ON

V_{out} low

Figure 12.33 Two-input CMOS NOR gate.