Switching Circuit and Logic Design

Final Exam (2008/6/20)

100 分鐘 Name:

Student ID:

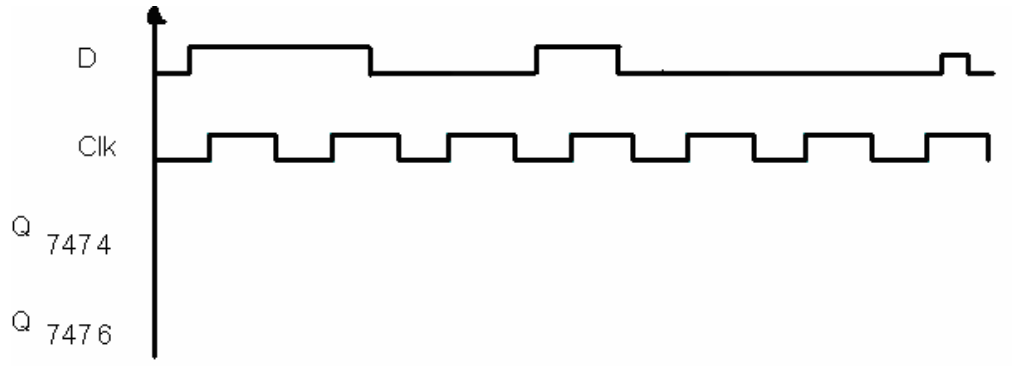
1. 20% Design a 3-bit counter with counting sequence of 1, 3, 7, 2.
   Direct ALL illegal states to state 3.
   Note: Use the symbol in order of CBA (違者扣分)
   (1) Draw the resulting circuit using T-type flip flops.
   (2) Draw the complete state diagram corresponding to your circuit.

2. 30% Design a 3-bit counter with counting sequence of 1, 3, 7, 2.
   Note: Use the symbol in order of CBA (違者扣分).
   (1) Draw the resulting circuit using JK-type flip flops.
   (2) Draw the complete state diagram corresponding to your circuit.

3. 15% Implement the logic function $F=\sum m(0,4,5,6,7,10,13)+d(8,15)$
   Using a 2: 1 Mux

4. 15% Determine the minimized realization of the following Boolean functions.
   $F(A,B,C,D)=\sum m(0,2,8,9,13)+\sum d(1,3)$

5. 10% Complete the waveforms of Q_{7474} and Q_{7476}



6. 10% 舉兩個實例藉以說明 FSM (有限狀態機器)