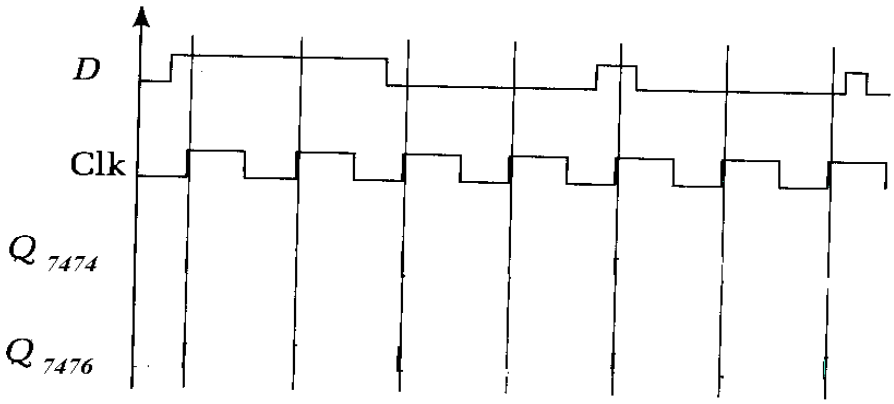
06/2000 *Contemporary Logic Design* Final Exam. 請寫學號

一. (30 pts).Given the input and clock transitions in the following figure,

indicate the output of a D device assuming:

(a) It is a positive edge-triggered flip-flop (7474).
(b) It is a (positive) level-sensitive latch (7476)
Note: You may assume 0 setup, hold, and propagation delays.



二 (30pts) Implement the logic function F(A,B,C,D)=∑ m(5,7,9,13)+ d(1,3,4,14,15), using

(a) a 4: 1 Mux
(b) a Decoder

三. (40 pts).Design a self-starting counter that has a normal counting sequence : 3, 7,5,0,2, and repeat. Direct all illegal states to the state 5. 註: 爲統一閱卷, 請以 **CBA之順序代表狀態 違者此題零分!**

(a) Use T flip-flops
(b) Use D flip-flops