Microprocessor and interfacing, Final Exam. Chapter 11.2~Chapter 15,
June 16, 2008. Please complete the close book part (50%) first. Then go to the
teaching assistant for the open book part (50%). 請在題目上直接作答.
Class: Name: Student ID:
Part I. CLOSE BOOK: Answer directly on the exam sheet.
A. True or false. If your answer is false, please explain your reasons. (20%)
1. () 8051 cannot change the fixed priority level of interrupts.
2. () 8051 only supports level-triggered interrupts.
3. () 8051 does not support software interrupt.
4. () The serial port of 8051 does not support interrupt. That is, a programmer will have to use polling to send and receive data.
5. () 8051 does not allow interrupt inside an interrupt.
6. () 8051 has 8-bit address bus and 16-bit data bus.
7. () A given memory block uses address 1000H – 3FFFH. The memory block ha 8K bytes.
8. () 8255 is an interrupt controller chip.
9. ().8051 can only access 64K bytes of memory. However, we can use "memory bank" to make 8051 able to access more than 64K bytes.
10. (). 8051 generally uses memory-mapped I/O to connect to 8255. A programme uses MOVC instruction to access 8255 ports.
B. Answer the following questions briefly. (30%)
1. (10%)What are the full names of the following terms:
(1) EEPROM
(2) RAS (in DRAM) (3) SRAM(4)ALE (8051 pin)
(5) NV-RAM(4)ALE (8051 pin)
(3) IN V-KAIVI

3. (4%) A 1M memory chip has 8 pins for data. Find (a) the organization, and (b) the number of address pins for this memory chip? 4. (4%) Why DRAM chips would have RAS and CAS signals? 5. (4%) Why do we need a 74LS373 (latch) when 8051 needs to access external memory? Why 8051 has an ALE pin? (Or what is ALE for?) 6. (4%) What is "address alias"? Can you show an example? 7. 請就你所知,設計一組合理的 handshake 訊號.請說明硬體時序圖及軟體的配合動作.你可以參考 8255 和 printer 之間的 handshake,也可以自行構想. (此題可用背面作答) (Uint 注意與是屬於 hange 分數在 0.9% 115.9% 之間 對在 及 終發的問意物則	2.	(4%) If you are a designer of an 8051-based application and you need extend memory for data space. You are free to choose either SRAM or DRAM chips. Which kind of chips you would choose? Why? Why would you not choose the other?
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面作合)(Hint: 這越是屬於 bonus, 万數在 0%~15%之间.對在及格邊緣的问字加 分較多,對成績在 85 分以上的同學可能全對也只加 1~2 分.建議就你所知嘗試一 下.)	動面分	作.你可以參考 8255 和 printer 之間的 handshake,也可以自行構想. (此題可用背作答) (Hint:這題是屬於 bonus,分數在 0%~15%之間.對在及格邊緣的同學加較多,對成績在 85 分以上的同學可能全對也只加 1~2 分.建議就你所知嘗試一

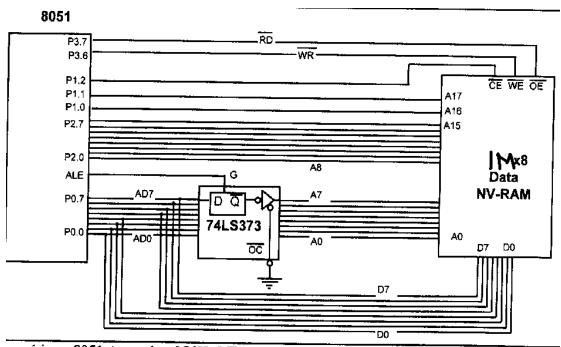
Class:	Name:	Student ID:

Part II. OPEN BOOK: Answer directly on the exam sheet.

1. (10%) Is it possible to program the 8051 priority level to make Serial communication has the highest priority, Timer interrupt 1 has the second highest priority, external interrupt 1 has the third highest priority, timer 0 interrupt the forth, and external interrupt 0 has the fifth? If your answer is NO, please explain. If your answer is YES, please show how you will do it. (Note: no need to write assembly code.)

2. (1)(10%)Refer to Example 15-4 (p. 456) Please design an address decoder for 8255 port A using 74LS138. Make port A of address FF00H. Note that: You must specify which bit is LSB, and you can use more than one 74LS138.)
(2)(5%)Find the control byte for PC = out, PB = in, and PA= in.
(3)(5%) Find the control byte to set the LSB of port C to be 1 using BSR mode.

- 3. Refer to Fig. 14-18 (p.435) If the NV-RAM is required to be $1M \times 8$.
- (1) (10%)Add the required hardware lines directly on the figure below to make all the 1Mx8 memory available to 8051.
- (2) (10%)Refer to example 14-14. Show how various blocks of this single chip are accessed.



8051 Accessing 256Kx8 External NV-RAM