Computer Organization & Assembly Language

Final Exam – 2015/1/9

Dept. of Engineering Science, National Cheng Kung University

1. Answer *True* or *False* to the following statements. (36%)

(A) Overflow cannot occur when subtracting operands with same signs.

(B) When implementing the hardware for 32-bit integer division, the remainder and the quotient can share the 64-bit space for better utilization.

(C) There is always a trade-off between precision and range when representing a floating-point number because a fixed size is used.

(D) In computer arithmetic, floating-point addition may not be associative; that is, x+(y+z) != (x+y)+z.

(E) The register is considered as a type of combinational elements.

(F) When designing the processor, the control signals RegRead and RegWrite are used for controlling the data access of register files.

(G) Designing the control is more complicated than designing the datapath since it requires an understanding of how all the components in the processor operate.

(H) In the pipelined processor, all control signals can be immediately set after the current instruction is decoded in the 2nd stage.

(I) Increasing the depth of pipeline (i.e., number of stages) without balancing the cost of each stage may reduce the overall performance.

(J) The CPI value of an ideal pipeline processor is 1.0.

(K) Pipelining increases throughput and reduces individual instruction execution time.

(L) Pipeline bubbles cause loss of performance since that a number of pipeline stages are left empty.

2. Perform the following operations of computer arithmetic.

(A) Add $3.63_{ten} \times 10^4$ to $6.87_{ten} \times 10^3$, assuming that you have only three significant digits, first with guard and round digits and then without them. (4%)

(B) Assuming single precision IEEE 754 format, what decimal number is represent by this word: 10111110100100000000000000000000 ? (4%)

(C) Show the IEEE 754 binary representation for the floating-point number 20.25_{ten} and $-4/7_{ten}$ in single precision, respectively. (10%)

3. Suppose that the function unit times are given as follows: (1 ns = 10^{-9} seconds)

2 ns for memory access,

1 ns for ALU operation, and

0.5 ns for register file read or write.

(A) According to our design, what is the desirable clock rate for the single-cycle machine and the pipelined machine, respectively? (6%)

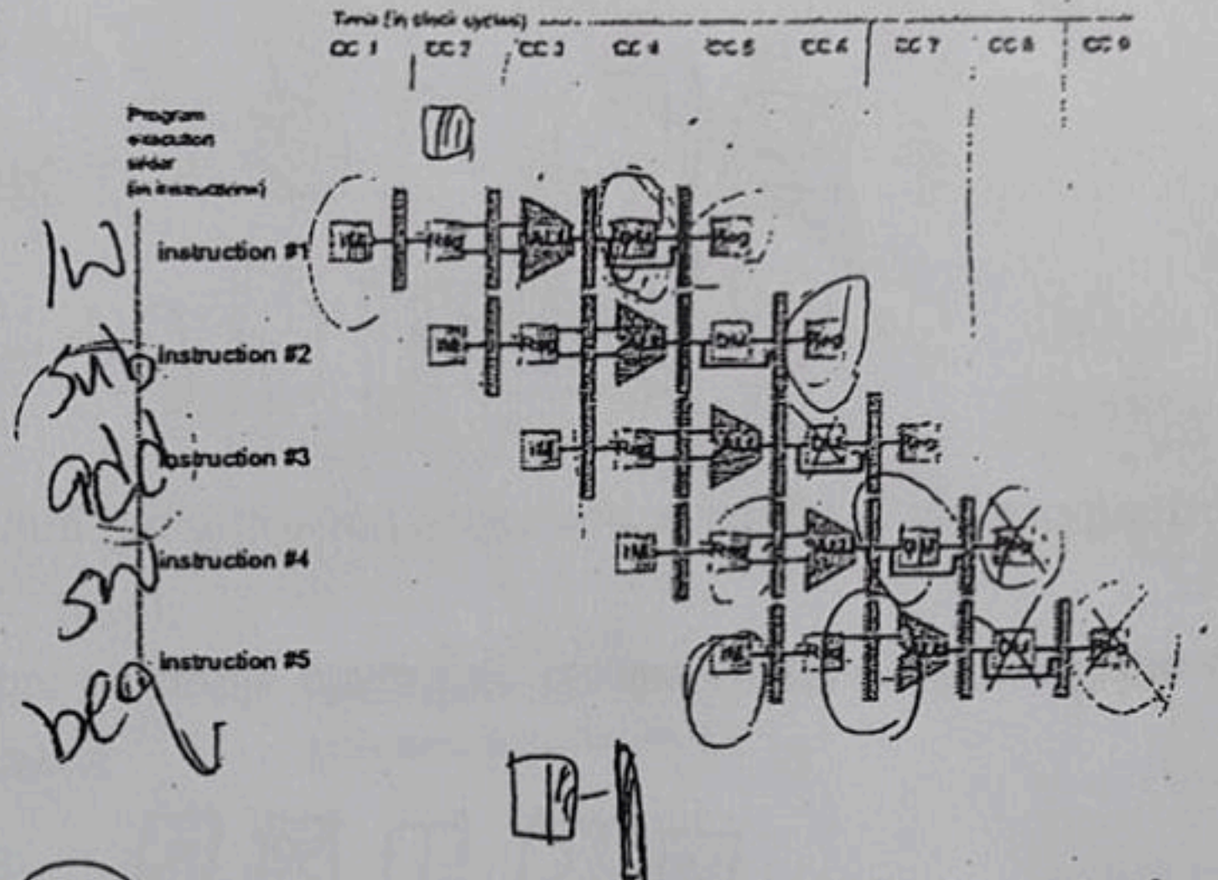
(B) What is the execution time for running the following codes on the single-cycle and the pipelined machine, respectively? (6%)

```
sub   $3,  $4,  $5
lw    $4,  10($6)
add   $7,  $3,  $4
sw    $7,  20($6)
add   $1,  $2,  $1
```

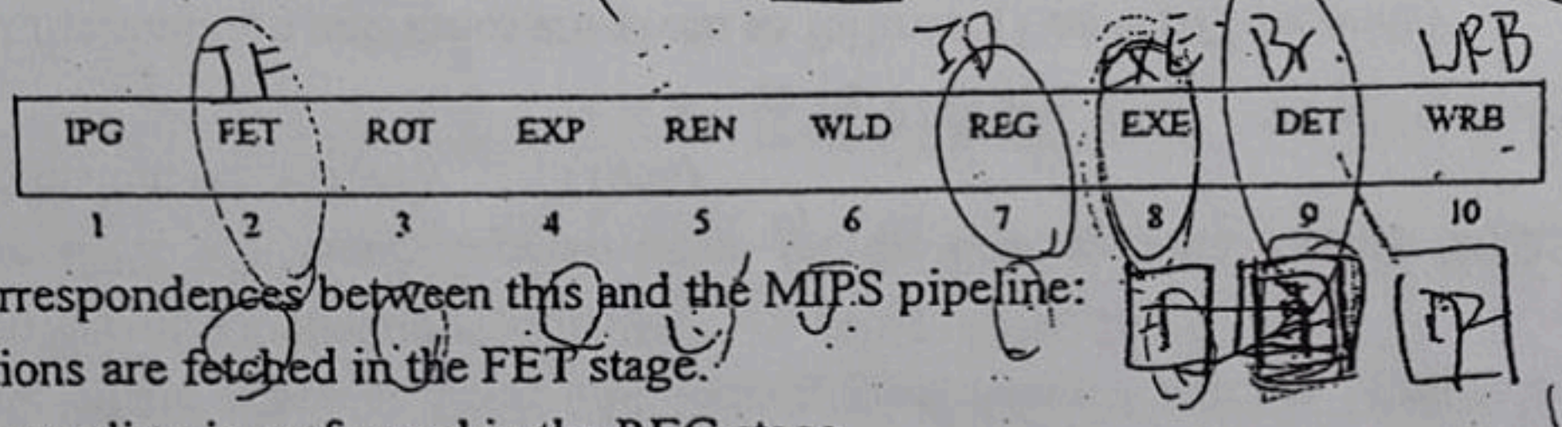
4. Given the following instructions #1~#5, identify and correct the errors (or inconsistencies) in the multiple-cycle pipeline diagram. (10%)

(Hint: indicate the instruction number(s) with errors, and then redraw the corresponding diagram.)

```
lw    $10, 20($1)
sub   $11, $2, $3
add   $12, $3, $4
sw    $13, 24($1)
beq   $14, $5, 6
```



5. One CPU manufacturer proposed the 10-stage pipeline below for a 500MHz (2ns clock cycle) machine.



Here are the correspondences between this and the MIPS pipeline:

- Instructions are fetched in the FET stage.
- Register reading is performed in the REG stage.
- ALU operations and memory access are both done in the EXE stage.
- Branches are resolved in the DET stage.
- WRB is the writeback stage.

(A) How much time is required to execute one million instructions on this processor, assuming there are no dependencies or branches in the code? (3%)

(B) Without forwarding, how many stall cycles are needed for the following code fragment? Assume that the register file could be written and read in the same clock cycle. (3%) What is this hazard called? (3%)

```
lw   $t0, 0($a0)
add  $v1, $t0, $t0
```

(C) If a branch is mispredicted, how many instructions would have to be flushed from the pipeline? (3%)

(D) Assume that a program executes one million instructions. Of these, 15% are load instructions which stall, and 10% of the instructions are branches. The CPU predicts branches correctly 75% of the time. How much time will it take to execute this program? (4%)

6. Consider the following sequence of actual outcomes for a single static branch where T means the branch is taken and N means the branch is not taken. Also, assume that this is the only branch in the program.

T T T T T T T T T T N N N T T T T N T N T N T T T N N N T T T N T N

(A) Assume that we try to predict this sequence with the 1-bit predictor (which is initialized to the N state). What is the predicted sequence? How many branches are mis-predicted? (4%)

(B) How about using the 2-bit predictor (which is initialized to the T state)? (4%)