Final Exam **_Digital Logic Design_** 2006/1/20

考試時間: **100 Mins** **作弊一律零分計算**

Name:_____ID:_____

一、**10pts** 解釋何謂組合電路？何謂序向電路？並各舉兩個例子。

Combinational means "memory-less", a digital circuit is combinational if its output values only depend on its input values.

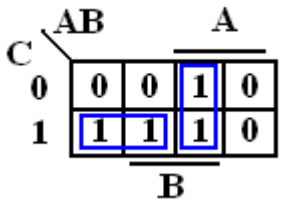
Ex: AND gate, OR gate.

Sequential systems exhibit behaviors (output values) that depend not only on the current input values, but also on previous input values.

Ex: R-S latch, J-K flip flop.

二、**10pts** **Prove** (by any means you like) the equation: AB+BC+A'C=AB+A'C

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |




F=AB+A'C

三、**15pts** Given $F_0 = B'C'$ $F_1 = AB+A'C$ $F_2 = B'C'+AB$ $F_3 = A'C+B$,

Use the PLA of *Fig.1* to implement the above four functions, i.e. by taking out those fuses that you don't need and draw the final configuration.

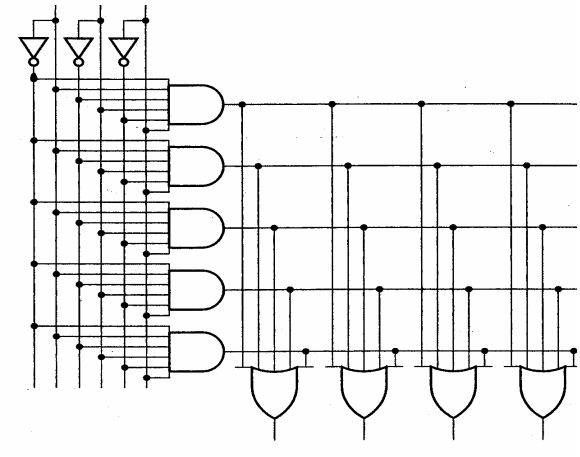
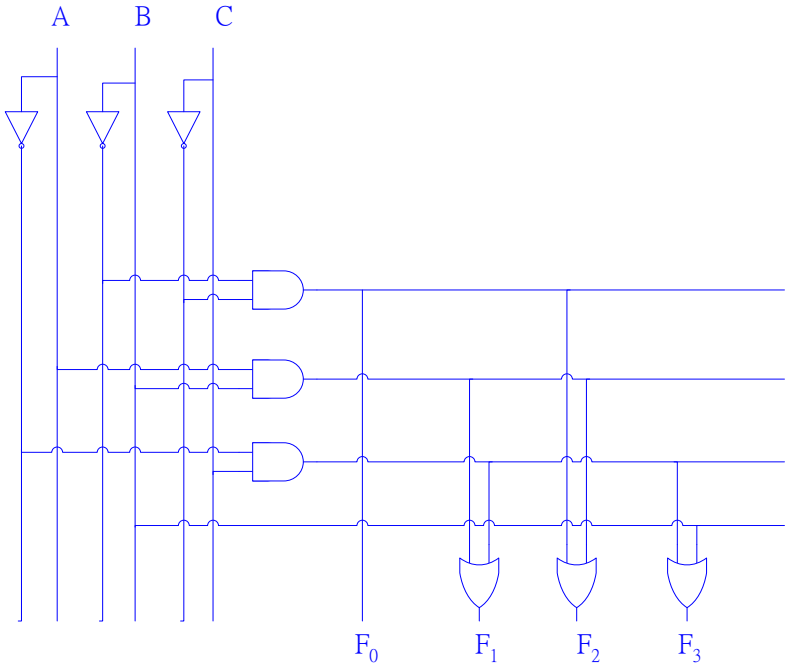


*Fig.1*

$F_0$ $F_1$ $F_2$ $F_3$




**四、15pts** (a) Draw the state diagram (including the race condition) for the R-S latch.

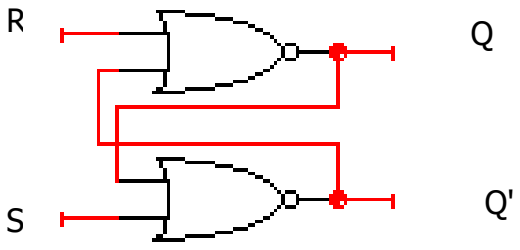
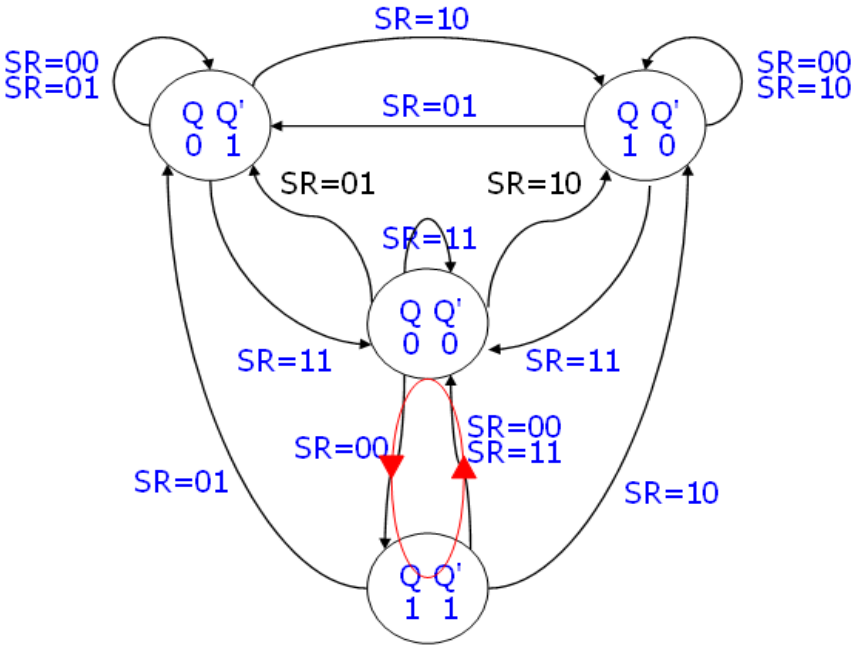


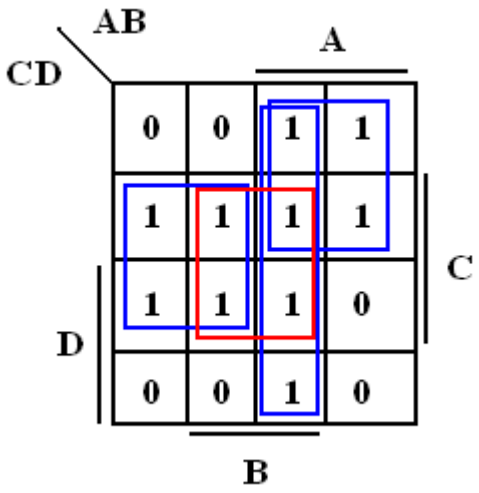

*Fig.2*




possible oscillation between states 00 and 11

(b) **Explain** the condition under which the R-S latch starts the race-condition (i.e. oscillation).
（請由推論電路圖之流程來解釋，故在此省略說明。）

五、**15pts** F(A,B,C,D)=Σm(1,3,5,7,8,9,12,13,14,15), implement a hazard-free design for F.




F=AB+AD'+A'C

According to avoid hazard,

F=AB+AD'+A'C+BC

六、**15pts** Complete the waveform for $Q_0$ and $Q_1$.

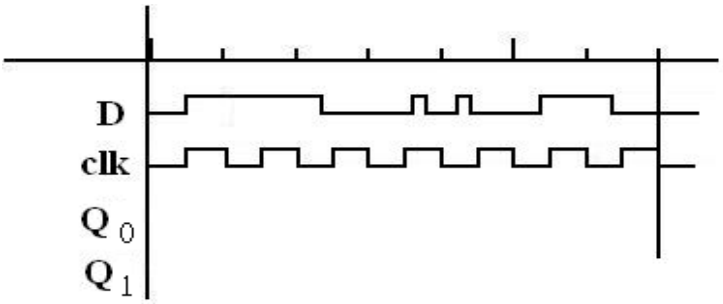



*Fig.3*

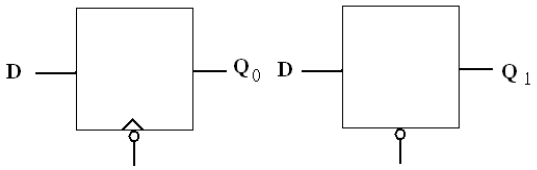
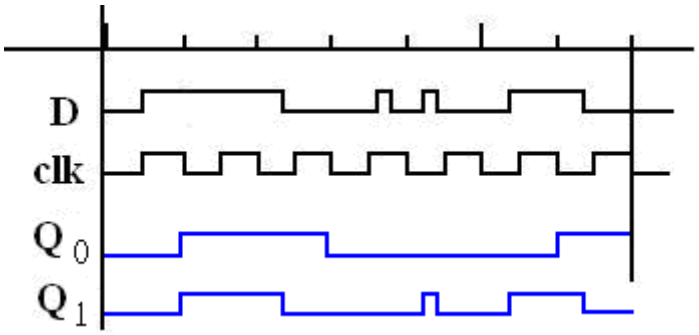



*Fig.4*




七、**20pts** **Given a 2-bit right**-shift register in *Fig.5*

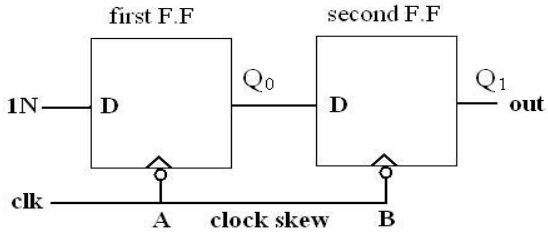



*Fig.5*

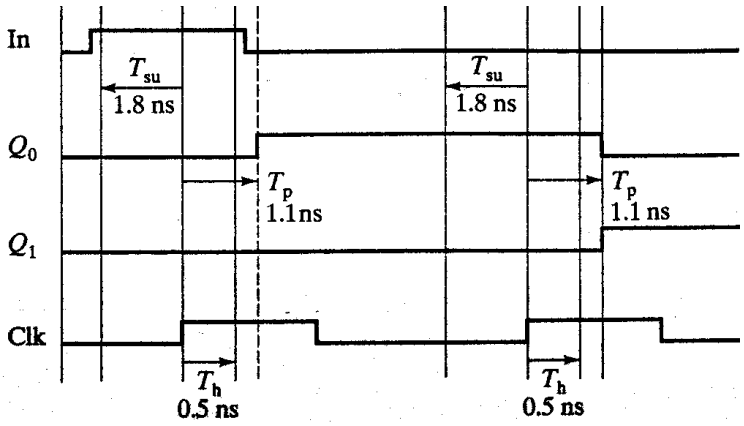



*Fig.6*

(a) **<u>Explain</u>** why $T_p > T_n$ is a must-be-true condition for the 2-bit shift register to work property.
因為若 $T_p < T_h$，$Q_0$ 輸出給 second F.F 的 D 之值可能已經改變，無法達到"shift register" 之效果。

(b) Assume the wire length between A and B is so long that it adds a clock delay $T_{skew}$ to the second FF (Flip Flop). In that case, how the condition in (a) should be changed so that the shift register can work properly?
$T_p > T_h + T_{skew}$

(c) According to (b) and the parameters in *Fig.6*, calculate max($T_{skew}$ )=?
$T_{skew} < T_p - T_h = 1.1 - 0.5 = 0.6$ns