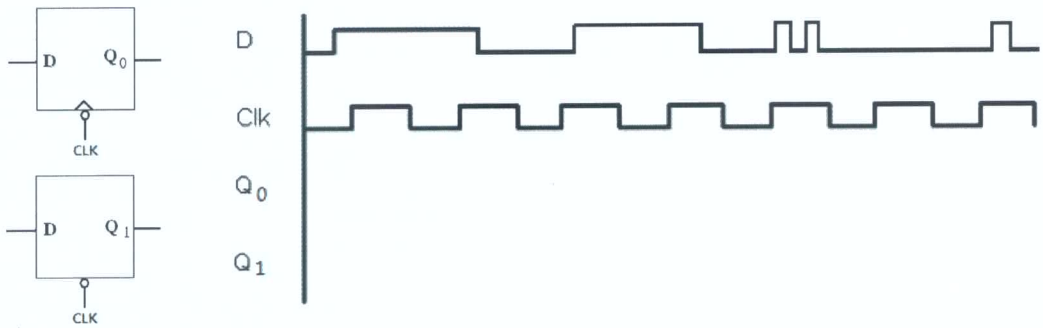
Digital Logic Design Final-term Exam June/21/2013

考試時間: 100 mins 姓名:

注意:總分 120 分 ，作弊一律以零分計 學號:

一. (10pts) Complete the waveforms of Q_0 and Q_1



二. (10pts) **Explain briefly** at least four reasons that digital circuits are more advantageous over analog circuits.

三. (30pts) (a) Use Quine-McCluskey method to minimize $F(A,B,C,D) = \Sigma m(4,5,6,8,10,13) + d(0,2,7,9,15)$. (b) Draw the *all* NAND gates circuit corresponding to the minimized SOP form in (a). (c) if input=0111 to the circuit in (b), what will be the output?

四. (30pts) Design an optimal 3-bit sequence recognizer by use the **implication chart method** for detecting 010 or 101.

五. (25pts) Design 3-bit counters with cycling sequence of 1, 7, 5, 2 by using JK flip flops. **Note: Use the symbols in order of CBA.**

六. (15pts) (a) What logic function does the circuit perform in Fig.1? Explain **by drawing the truth table**

(b) Given a Flip-Flop (one bit memory cell, FF) as in Fig.2, it is known that the equivalent circuit of FF is shown in Fig. 3, identify the two NOT gates I_1 and I_2 **by using transistors M_1,M_2,M_3,M_4**, that is, in Fig.3 which transistors constitute I_1 and I_2 respectively?

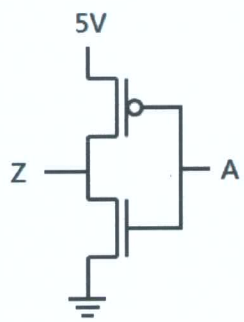


Fig.1

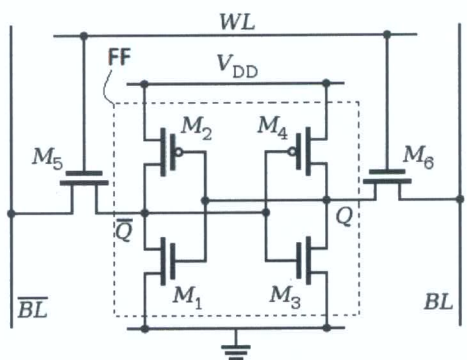


Fig.2

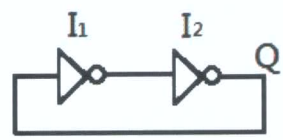
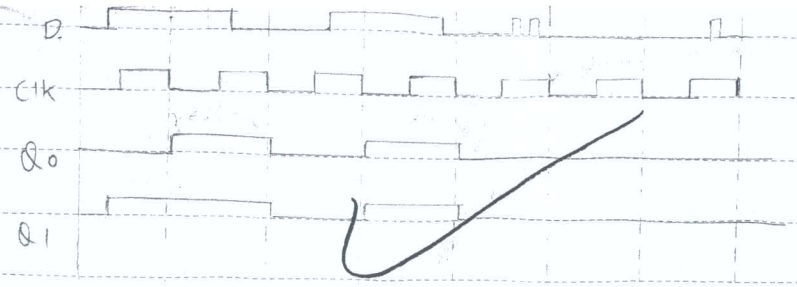


Fig.3

1.



2. 模組化

可用軟體編輯，自動化

可去除雜訊，不失真

防密資訊理論

3.

A B C D	F
0 0 0 0	X
0 0 0 1	0
0 0 1 0	X
0 0 1 1	0
0 1 0 0	1
0 1 0 1	1
0 1 1 0	1
0 1 1 1	X
1 0 0 0	1
1 0 0 1	X
1 0 1 0	1
1 0 1 1	0
1 1 0 0	0
1 1 0 1	1
1 1 1 0	0
1 1 1 1	X

I	II	III
0000 0	00-0 0,2	0--0 0,2,9,6 *
0010 2	0-00 0,4	-0-0 0,2,8,10 *
0100 4	-000 0,8 *	
1000 8	0-10 2,6	01-- 4,5,6,7 *
0101 5	-01a 2,10	
0110 6	010- 4,5	-1-1 5,7,13,15 *
1001 9	01-0 4,6	
1010 10	100- 8,9 *	
0111 7	10-0 8,10	
1101 13	01-1 5,7	
1111 15	-101 5,13	
	011- 6,7	
	1-01 9,13 *	
	-111 7,15	
	11-1 13,15	

4 ✓ 6 ✓ 8 ✓ 10 ✓ 13

0--0 ✓ ×

-0-0 ← ⊗ ⊗

01-- × × ×

-1-1 × ← ⊗

100-

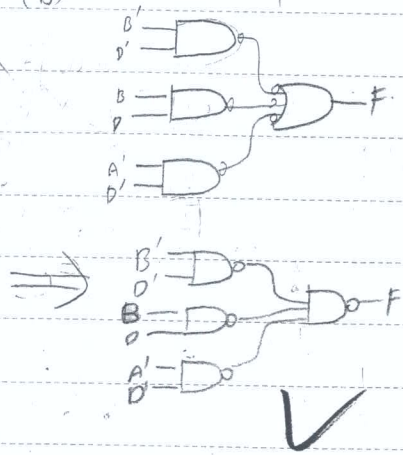
1-01

解 F = B'D' + BD + A'D'

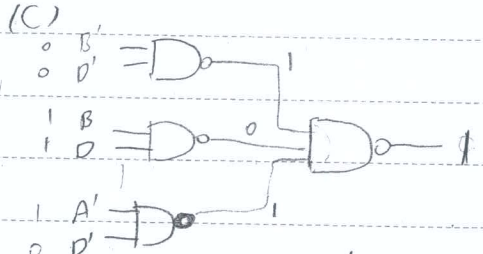
或

F = B'D' + BD + A'B

(b) 取第一種解



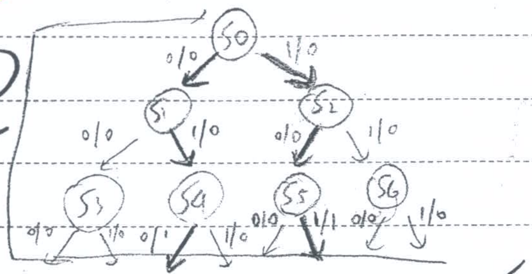
(C)



output = 1

(4) 10

010 101



input sequence	present state	next state X=0	next state X=1	output X=0	output X=1
reset	S0	S1	S2	0	0
0	S1	S3	S4	0	0
1	S2	S5	S6	0	0
00	S3	S0	S0	0	0
01	S4	S0	S0	1	0
10	S5	S0	S0	0	1
11	S6	S0	S0	0	0

	S0	S1	S2	S3	S4	S5
S1	S1=S3 S2=S4 (X)					
S2	S1=S5 S2=S6 (X)	S3=S5 S4=S6 (X)				
S3	S1=S0 S2=S0 (X)	S3=S0 S4=S0 (X)	S5=S0 S6=S0 (X)			
S4	X	X	X	X		
S5	X	X	X	X	X	
S6	S1=S0 S2=S0 (X)	S3=S0 S4=S0 (X)	S5=S0 S6=S0 (X)	S0=S0 S0=S0	X	X

S0 = S0.
S3 = S6

(6) 5

(a)

A	Z
0	5
1	0

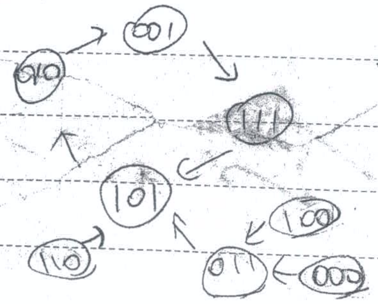
(b)

M1 M2 取代 I1,
M3 M4 取代 I2

Not gates

(5) 25

1→7→5→2



S R

CBA	$C^+B^+A^+$	J_CK_C	J_BK_B	J_AK_A
000	XXX	XX	XX	XX
001	111	1X	1X	X0
010	001	0X	X1	1X
011	XXX	XX	XX	XX
100	XXX	XX	XX	XX
101	010	X1	1X	X1
110	XXX	XX	XX	XX
111	101	X0	X1	X0

0→1	1X
0→0	0X
1→0	X1
1→1	X0

J_C

A \ CB	00	01	11	10
0	X	0	X	X
1	1	X	X	X

$J_C = A$

K_C

A \ CB	00	01	11	10
0	X	X	X	X
1	X	X	0	1

$K_C = B'$

J_B

A \ CB	00	01	11	10
0	X	X	X	X
1	1	X	X	1

$J_B = 1$

K_B

A \ CB	00	01	11	10
0	X	1	X	X
1	X	X	1	X

$K_B = 1$

J_A

A \ CB	00	01	11	10
0	X	1	X	X
1	X	X	X	X

$J_A = 1$

K_A

A \ CB	00	01	11	10
0	X	X	X	X
1	0	X	0	1

$K_A = CB'$