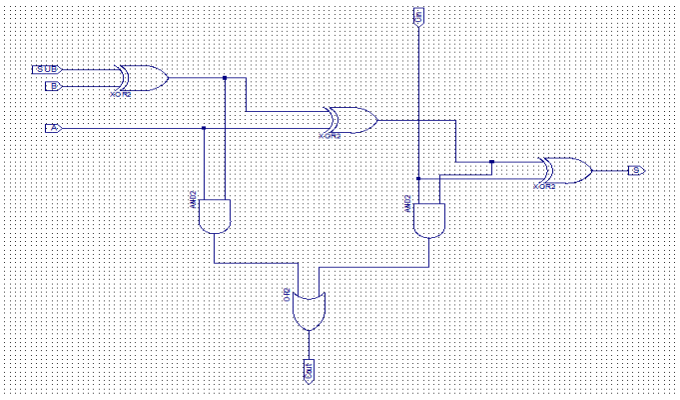
EE 142 Project report

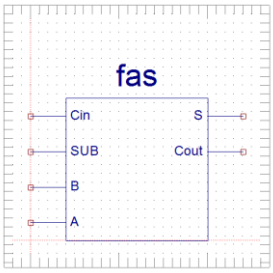
The project is about designing 2-digit binary coded decimal (BCD) adder/subtractor consisting of 2 4-bit adder/subtractor units and two add-six units . Individual components of the design are given below step by step and the design schematics and strategies are explaned too.

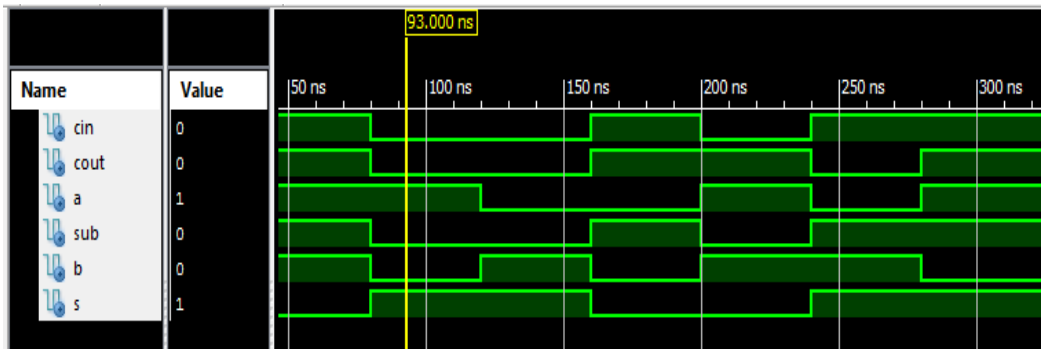
1-**1-bit full adder-subtractor**

1-bit full adder-subtractor has 3 inputs a, b and Cin=sub, 2 outputs s,Cout. A and b are added,when sub=0. But when sub=1, a and b are subtracted. Cin is the carry in. We use it when we should make ripple addition. S is sum.Moreover the Sub and Cin are tied together, but not shown on the picture left.

The simulation is shown here and it is true theoritically.You should create a symbol for this 1-bit full adder-subtractor,because it will be very useful in the following steps.





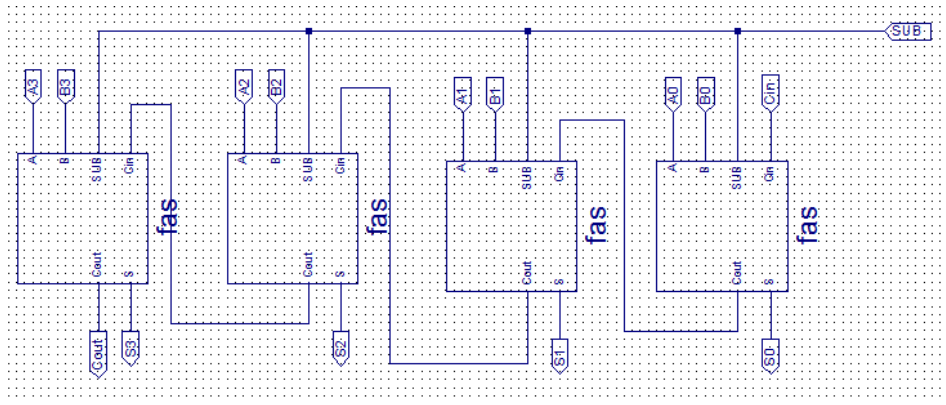


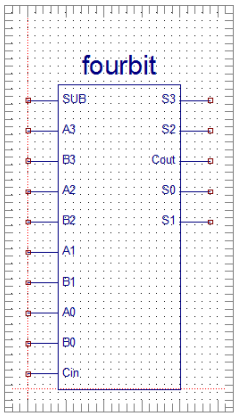
Karnaugh map for S					A	A
		Cin(Sub)/AB	00	01	11	10
		0	0	1	0	1
	Cin	1	0	1	0	1
				B	B	

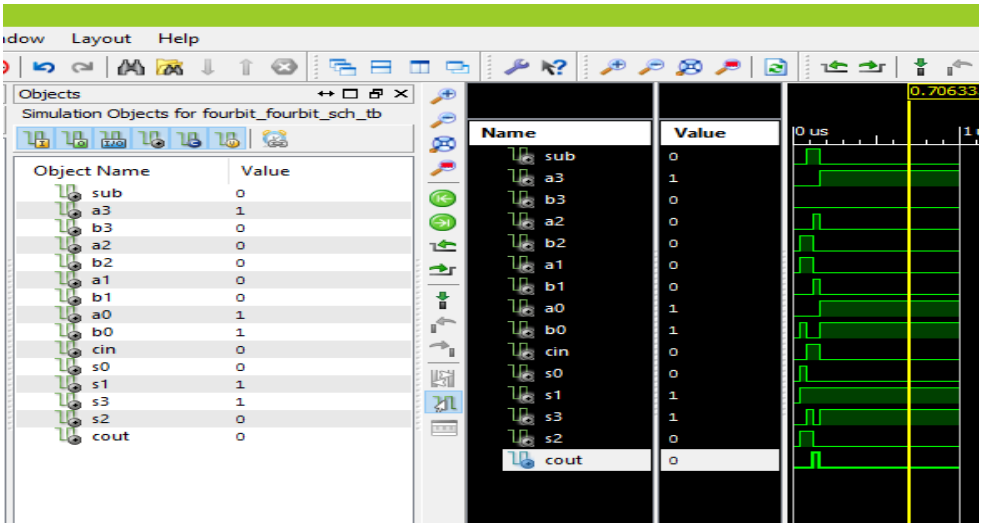
Karnaugh map for Cout					A	A
		Cin(Sub)/AB	00	01	11	10
		0	0	0	1	0
	Cin	1	1	0	1	1
				B	B	

2- 4-Bit full adder subtractor

Since a bcd number can not be shown as 1-bit, we need 4-bit. 0000 through 1001 are valid, the others not. The Cin is tied to sub because flexibility is needed in the design of this circuit.[1]







The Cout of each full adder subtractor is tied to Cin of the next full adder subtractor. This 4-bit full adder subtractor needs a carry in, because we should create 2 digit bcd full adder subtractor. One 4-bit full-adder subtractor represents one digit. In simulation Cin is tied to SUB(Cin=SUB, because we should produce 2's complements when Sub=1. First simulation is: (SUB=Cin=0) 0101+0010 = 0111(5+2=7), which is true. Second simulation is: (SUB=Cin=1) 0100-0010=0010.Third simulation is: (SUB=Cin=0) 1001+0001=1010. All of them are true. So the 4-bit full adder subtractor works. But in third simulation the result is 1010 in binary, which is not a valid BCD number. So a correction should be done. This correction is called 'add-six-technique design', which is arranged in next step. In the end I arranged a symbol for 4-bit full adder subtractor.

3- Add-six technique design

When the 4-bit FAS is adding (SUB=0), a carryout (c_{in}) of "1" signifies an "overflow" which means

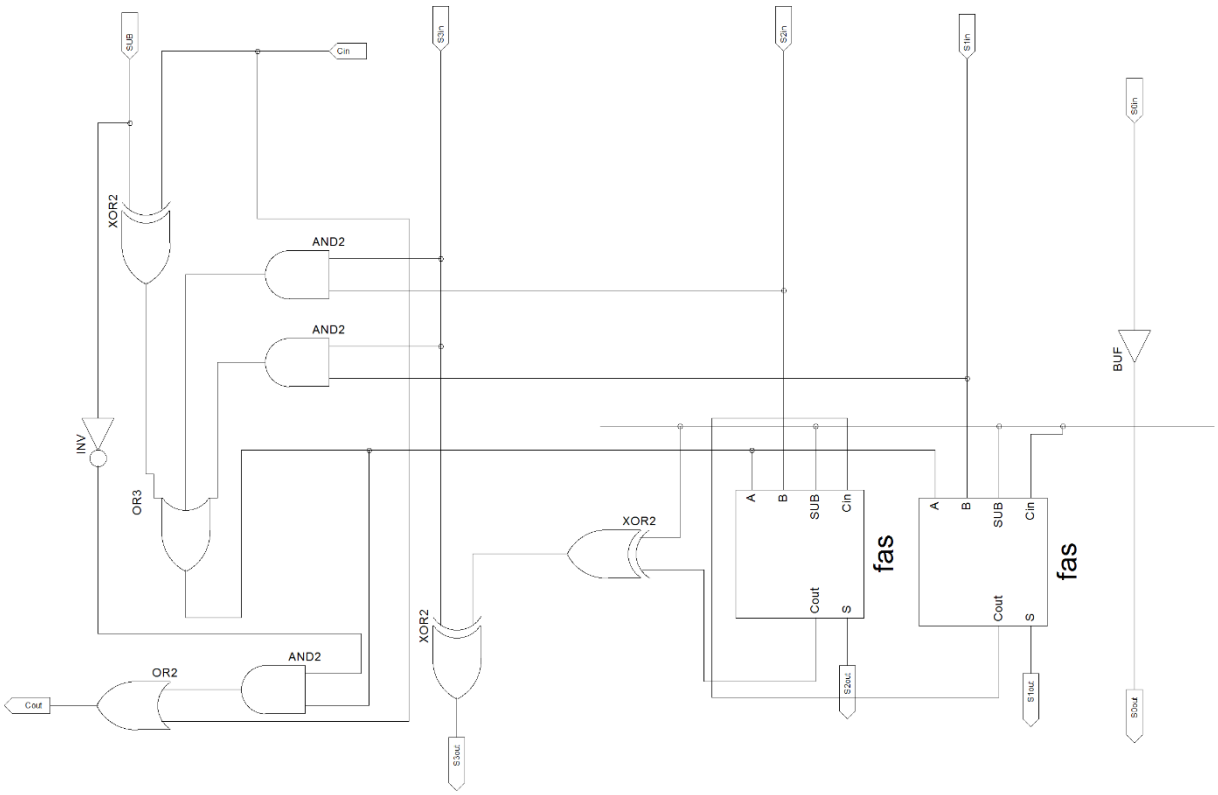
1) the carry (out of the add six) must be "1"

2) the add six correction must be performed (Wcondition must be asserted).[2]

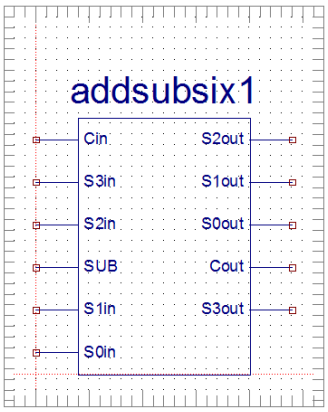
When the 4-bit FAS is subtracting (SUB=1), a carryout (c_{in}) of "0" signifies that a "negative" number resulted which means

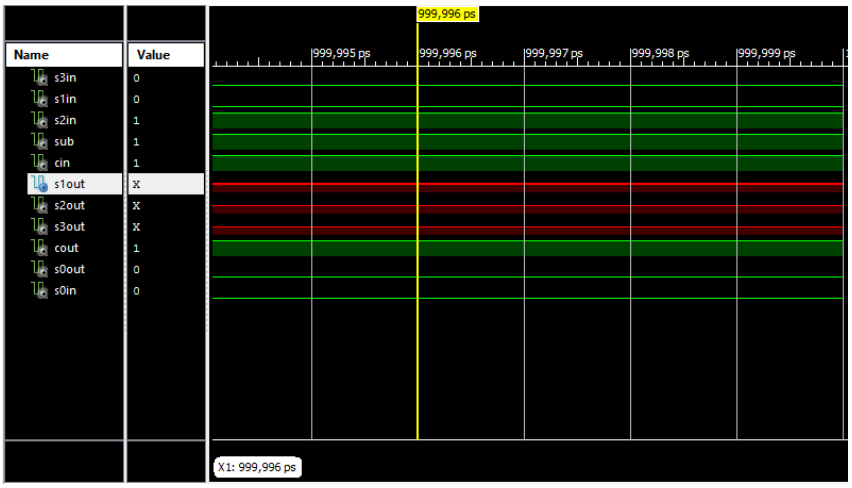
1) carry (out of the add six) should be 0, and

2) the *subtract* six correction must be performed. [3]

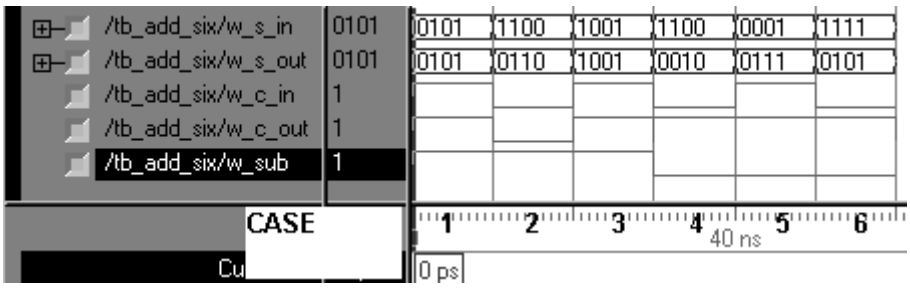


[4] Structure of add/sub six





But there is a problem with my simulation.



Therefore here is timing diagram for the structure given above.[5]

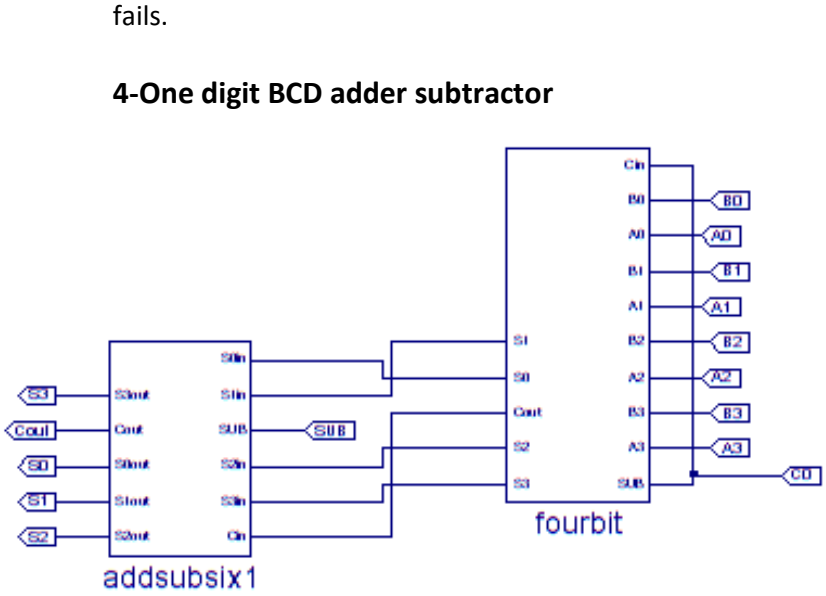
In case 1: SUB=1, so it is a subtraction. Sum input is 0101. The output does not change,because it is a valid Bcd number.When Cin=sub=0, the subtraction is true, don’ need to be corrected.

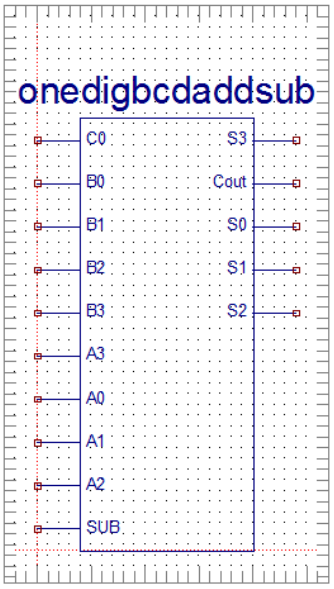
In case 2: Sum input is not a valid BCD number. Cin != SUB, so we the add six methode is useful.

Subtracting six is like adding the 2's compliment of the binary code for six, 0110, to the input sum. 2's complement of 0110 is 1010. 1010 + 1100 = 1 0110. So carry out is 1. Sum out is 0110.

In the end I create a symbol for this step which will be useful in the next step, although my simulation fails.

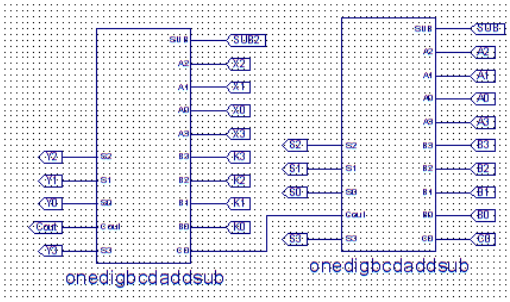
4-One digit BCD adder subtractor





The one digit BCD adder/subtractor consists of a 4-bit full adder subtractor and the previous addsix component. The inputs are 2 BCD numbers called A and B. This component adds or subtracts A and B computing a new BCD number called S. Moreover it has a Cout too. The simulation file fails, because I have a problem in the previous step, add six technique.

5-2 digit BCD adder subtractor



The two digit BCD adder/subtractor consists of 2 one digit BCD adder/subtractor to then compute two digit BCD additions and subtractions. Cout from the adder/subtractor dealing with the ones digit is connected to the Cin of the adder/subtractor dealing with the tens digit. The outputs are two 4-bit BCD numbers (YS: shown in figure), and a carry out from the ten's place BCD adder/subtractor

References

[1],[2],[3],[4],[5] BCD Adder,Subtractor, Second Revision, EE 365, Chris Ouellette,Joshua Smith, 10-19-2004