ELECTRONICS I SYLLABUS

This is a partial syllabus for the 1st semester portion of a 2 semester sequence in undergraduate Electronics. It's based on a 14 week semester with two 50 minute lectures and one 160 minute laboratory each week. To stay within the Fulbright syllabus length limitation, only that portion describing the lecture and lab content is shown. I continue to use this syllabus content every Fall semester at McNeese State University.

NOTE: ***This syllabus represents the aggressive content approach that's required to cover all the material needed to help students master both the academic & practical sides of 1st semester electronics. It's feasible to use at my home university because I've had the opportunity to interact with most of my students for two years prior to this course. At a foreign host university I would distribute the same material normally covered in two 50 minute lectures over three 50 minute lectures instead. In addition I would hold one 75 minute problem-solving session each week. The lab content would remain the same.***

WEEK 1

Lecture 1: **diagnostic test on circuit theory analysis (to determine need for off-line remedial sessions and/or homework); introduction to semiconductor material & physics; ideal diode model; ideal diode circuits; homework → analysis of multiple ideal diodes logic circuit;**

Lecture 2: **previous homework review; non-ideal diode models; half-wave rectifier; zener diodes; homework → full-wave rectifier analysis;**

Lab: **lab safety review; organize student lab teams; bench equipment functions, operation, precautions, & demo; student hands-on exercises using bench equipment; review lab report criteria;**

WEEK 2

Lecture 1: **previous homework review; diode clipper circuit example; photodiode concept & applications; homework → clipper circuit problem;**

Lecture 2: **previous homework review; diode clamper circuit example; LED application examples; homework → clamper circuit analysis; design of reverse voltage protection circuit;**

Lab: **answer any equipment operation questions; bridge rectifier circuit characterization; outline lab report;**

WEEK 3

Lecture 1: previous homework review; basic bi-polar junction (BJT) transistor (Tx) conceptual model & operation; relationships between base, emitter, & collector currents; BJT Tx parameter characterization; homework → define "Q point", load line, and Tx power dissipation;

Lecture 2: review previous homework; maximum Tx power & collector-base voltage bias limitations; Tx functionality tests using multi-meter; homework → define Iceo and Icbo; use spec sheets to determine max power for Tx type 2N2222 operating @ 20^oC, 25^oC, 30^oC, & 35^oC;

Lab: week 2 lab report due; BJT Ic vs. Vce characterization; outline lab report; homework → applied engineering exercise A;

WEEK 4

Lecture 1: review previous homework; dc analysis of common emitter amplifier biased with R_B to collector supply (Vcc); cutoff; saturation; operating point variations; homework → in-class amplifier example Q point determination with (a) beta = 100 and (b) with beta = 300;

Lecture 2: review previous homework; strategy to stabilize Q point when Tx parameters vary; analysis of 4 resistor (4R) dc bias circuit; in-class exercise → 4R bias Q point variation with (a) beta = 100 and (b) beta = 300; homework → prepare for 30 minute quiz next class;

Lab: week 3 lab report due; design 4R bias for common emitter amplifier using 2N2222 Tx; determine Q point values using Electronic Work Bench (EWB); build and measure Q point values in lab; explain any differences; outline lab report;

WEEK 5

Lecture 1: 30 minute quiz on diodes and Tx dc analysis; BJT small signal equivalent circuit; ac equivalent circuit for common emitter amplifier; homework → write the necessary node equations for the equivalent circuit shown in class;

Lecture 2: review previous homework; solve node equations for ac voltage gain; simplifying assumptions; homework → determine expressions for output and input impedances (Z); design 2N2222 Tx amplifier for gain of 2 with v_{in} = 10 millivolts;

Lab: week 4 lab report due; exercise A due; use EWB to analyze given multi-stage amplifier; build and test; analyze analytically; compare

results of all three methods; explain differences; outline lab report; homework → applied engineering exercise B;

WEEK 6

Lecture 1: **review previous homework; in-class exercise → determine ac model for common collector amplifier using small signal equivalent Tx circuit; homework → write node equations for ac model developed in class; prepare for mid-term exam during week 7 during lecture 1;**

Lecture 2: **review previous homework; in-class exercise → solve node equations for ac voltage gain and Z_{IN}; common base amplifier circuit diagram; homework → determine expression for Z_{OUT} for common collector amplifier; determine voltage gain, Z_{IN}, & Z_{OUT} for common base amplifier; continue preparing for mid-term exam next lecture;**

Lab: **week 5 lab report due; carry out the 4 phase analysis used in Lab 4 on the common collector amplifier configuration given in class; outline lab report;**

WEEK 7

Lecture 1: **mid-term exam; homework → re-work mid-term exam;**

Lecture 2: **mid-term exam problem discussion & problem solution details; homework → study JFET chapter in text and text examples;**

Lab: **week 6 lab report due; exercise B due; lab make-up session; homework → applied engineering exercise C;**

WEEK 8

Lecture 1: **JFET device; physics of operation; I_D vs V_{DS} curve generation; pinch-off voltage (V_P), I_D vs.V_{GS} non-linear transfer curve; homework → numerical calculation of drain supply voltage (V_{DD}) for constant I_D;**

Lecture 2: **review previous homework; JFET bias concepts; (a) self bias; example; R_S graphical solution; analysis using 2N5457 parameter spread; homework → numerical calculation using transfer curve;**

Lab: **week 7 lab report due; determine JFET device characteristics; outline lab report;**

WEEK 9

Lecture 1: **review previous homework: (b) JFET voltage divider bias stability; voltage divider bias examples; I_D saturation region equation; JFET amplifier intro; homework → bias design per specs;**

Lecture 2: **review previous homework; in-class problem solving session: common source JFET ac voltage gain example; homework → common drain JFET amplifier exercises; prepare for 30 minute quiz next lecture;**

Lab: **week 8 lab report due; exercise C due; 4 phase common source JFET amplifier analysis; outline lab report; homework → applied engineering exercise D;**

WEEK 10

Lecture 1: **30 minute quiz quiz; common gate JFET amplifier; (c) current source bias; homework → JFET current source bias exercises;**

Lecture 2: **quiz problem solution; JFET amplifier applications; homework → JFET amplifier design exercises;**

Lab: **week 9 lab report due; 4 phase analysis of JFET current source bias; explain any differences of data results of phases; outline lab report;**

WEEK 11

Lecture 1: **review previous homework; ideal op amp characteristics; open loop vs. closed loop operation; inverting, non-inverting, & summing op amp analyses; homework → analysis of difference mode op amp;**

Lecture 2: **review previous homework; op amps driven by a current source; the concept of feedback; negative vs. positive feedback; calculating Z_{IN} and Z_{OUT} in an op amp circuit; homework → analysis of various op amp configurations;**

Lab: **week 10 lab report due; exercise D due; 4 phase analysis of frequency response of non-inverting 741 op amp; explain any inconsistencies; outline lab report;**

WEEK 12

Lecture 1: **review previous homework; difference op amp with high input impedance; op amp linearity; cascaded op amps; multiple op amp configuration analysis; homework → op amp linearity exercise;**

Lecture 2: **review previous homework; important non-ideal op amp characteristics; output current limitations; common mode rejection ratio (CMRR); homework → CMRR exercise;**

Lab: **week 11 lab report due; analysis of difference mode 741 op amp by 4 phase method; explain if any data inconsistencies; outline lab report;**

WEEK 13

Lecture 1: **review previous homework; general op amp block diagram; BJT based op amps; JFET based op amps; other op amp technologies; homework → study for lab final exam;**

Lecture 2: **general closed loop feedback block diagram; open loop gain, closed loop gain, & loop gain relationships; closed loop non-inverting op amp block diagram; homework → determine inverting op amp closed loop block diagram; study for lecture final exam;**

Lab: **week 12 lab report due; lab make-up session; applied engineering exercise E in-class exercise;**

WEEK 14

Lecture 1: **review previous homework; lab final exam review;**

Lecture 2: **lecture final exam review;**

Lab: **lab final exam;**

LECTURE FINAL EXAM

ELECTRONICS II SYLLABUS

This is a partial syllabus for the 2nd semester portion of a 2 semester sequence in undergraduate Electronics. It's based on a 14 week semester with two 50 minute lectures and one 160 minute laboratory each week. To stay within the Fulbright length limitation, only that portion describing the lecture and lab content is shown. I continue to use this syllabus content every Spring semester at McNeese State University.

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WEEK 1

Lecture 1: **review of diodes, BJTs, JFETs, & ideal op amps; homework → analysis of ideal op amp circuits;**

Lecture 2: **previous homework review; review of actual 741 op amp specs; major non-ideal characteristics; op amp theoretical vs. actual performance; homework → define op amp open loop gain (OLG), closed loop gain (CLG), loop gain (LG), & gain-bandwidth (GB) product; give examples of each; sketch OLG, CLG, & LG on the same set of axes;**

Lab: **design, build, & test a variable voltage gain (x1 - x100) non-inverting (NI) amplifier using a 741 op amp; using test data determine 3 db freq. with x1, x10, & x 100 gains; compare results to Electronic Work Bench (EWB) results; explain differences; outline lab report;**

WEEK 2

Lecture 1: **previous homework review; 741 specs of OL freq. dependence of gain & phase; practical op amp OL model to handle freq. dependence; typical 741 specs; observations & approximations; homework → use analog model of actual op amp to analyze CL NI op amp;**

Lecture 2: **previous homework review; analyze actual inverting (I) & NI CL op amp circuits; practical observations & shortcuts; actual op amp gain**

as a function of frequency; homework → at what point does the ideal op amp model break down? Study for 15 min. quiz next lecture;

Lab: **week 1 lab report due; use a 741 to design a CL op amp with a variable gain (x1– x1000); use EWB to gather data & plot the phase of V_{out}/V_{in} (radians) ratio vs. normalized frequency (radians / GB); discuss results; outline lab report;**

WEEK 3

Lecture 1: **previous homework review; 15 min. quiz; develop the gain exp. for I op amp; frequency dependence expression of $\{V^+ - V^-\}$ difference in actual op amp; example showing problem in assuming $\{V^+ - V^-\} = 0$; homework → compare / contrast NI & I freq. dep. gain exp.;**

Lecture 2: **review previous homework; summary of actual NI op amp observations; example of feedback effects on CL gain with large op amp OL gain variations; summing amplifier analysis;; homework → add a 3rd input source to summing op amp shown in lecture and calculate the new 3 db point;**

Lab: **week 2 lab report due; use 741 to design a NI CL amp. having voltage gain of 20 at low frequency; input = 50×10^{-3} v; sketch output & determine rise time; verify by simulation & hardware; outline report; homework → applied engineering exercise F;**

WEEK 4

Lecture 1: **previous homework review; op amp output impedance frequency dependence; expression derivation; example; effects on amplifier performance; homework → calculate 2nd order 3 db frequency;**

Lecture 2: **review previous homework; amplification using 2 cascaded 741 op amps vs. 1 741 op amp; V_{out} / V_{in} expressions; bandwidth (BW) comparisons; effect of gain on BW; nested feedback configurations; homework → determine gain expression for 2 741 op amps with nested feedback loops;**

Lab: **week 3 lab report due; simulate/build/test nested feedback system from lecture 2 homework; determine BW; explain data; compare to BW of cascaded & single op amp systems; team written & oral presentation to class during next lab; outline report;**

WEEK 5

Lecture 1: **general discussion of previous homework; op amp dynamic range (DR); examples; homework → voltage & current DR exercises; review common mode rejection ratio (CMRR) concepts;**

Lecture 2: **review previous homework; slew rate (SR) effects; SR vs. BW limitations on output response; examples; homework → SR exercises; review CMRR calculations; study offset voltage & current concepts;**

Lab: **exercise F due; lab 4 written reports and oral presentations by each team; homework → applied engineering exercise G;**

WEEK 6

Lecture 1: **review previous homework; CMRR review; typical finite CMRR specs; actual CMRR causes & effects; 741 example; homework → non-ideal CMRR caused by circuit mismatch; offset current & voltage example; prepare for mid-term exam;**

Lecture 2: **review previous homework; model for non-ideal CMRR; example; design example using 741 CMRR specs; homework → analysis of multiple finite CMRR op amps; prepare for mid-term exam;**

Lab: **analyze/simulate/build/test difference amplifier with finite CMRR; explain results; outline lab report;**

WEEK 7

Lecture 1: **review previous homework & labs; review for mid-term exam;**

Lecture 2: **mid-term exam; homework → re-work exam; study MOSFET chap.**

Lab: **week 6 lab report due; exercise G due; exam problem discussion; lab makeup session; homework → applied engineering exercise H;**

WEEK 8

Lecture 1: **overview of pn junction physics; MOSFET geometry; physics of operation; threshold voltage; excess gate voltage; ohmic region; channel geometry; pinch off voltage; homework → determine I_D for V_{GS} = 9v & V_{DS} = 2v for BS170 MOSFET; for V_{GS} = 9v and 2v < V_{DS} < 3v what is BS170 equivalent resistance?**

Lecture 2: **review previous homework; I_D saturation region; NMOS vs. PMOS; $I_D = K_S(V_{GS} - V_T)$; BS170 spec sheet; I_D vs. V_{DS} curves; enhancement mode vs. depletion mode I_D equations; symbols; homework → calculation of ID for enhancement & depletion mode MOSFETs**

Lab: **NMOS device characterization using BS170; outline lab report;**

WEEK 9

Lecture 1: **review previous homework; Q point variations; stabilizing bias using drain-to-gate feedback resistor; stabilizing Q point by constant gate voltage; graphical & numerical examples; homework → Q point calculations;**

Lecture 2: **review previous homework; MOSFET load configuration; MOSFET as load resistor; application example; MOSFET power calculations; examples; homework → MOSFET power calc. exercises;**

Lab: **week 8 lab report due; exercise H due; design constant gate voltage bias circuit for BS170; simulate/build/test: explain results; outline lab report; homework → applied engineering exercise I;**

WEEK 10

Lecture 1: **review previous homework; in-class MOSFET dc circuit analysis practice examples; homework → MOSFET dc analysis exercises;**

Lecture 2: **review previous homework; in-class MOSFET dc design examples; homework → MOSFET dc design exercises; study MOSFET ac amplifier examples;**

Lab: **week 9 lab report due; dc circuit design per given specs using BS170; simulate/build/test; explain strategy & results; outline lab report;**

WEEK 11

Lecture 1: **review previous homework; MOSFET ac amplifiers; small signal equivalent circuit; common source amplifier; ac voltage gain of NMOS common source circuit; homework → NMOS common source amplifier input impedance determination;**

Lecture 2: **review previous homework; common drain amplifier; input & output impedances; in class exercises; homework → ac voltage gain of PMOS common drain amplifier;**

Lab: **week 10 lab report due; exercise I due; NMOS common source ac amplifier simulation; compare ac gain results to lecture 1 analytical model results; outline lab report;**

WEEK 12

Lecture 1: **review previous homework; common gate amplifier; ac voltage gain of PMOS amplifier; in class exercises; summary of 3 basic configurations; homework → PMOS common gate output impedance;**

Lecture 2: **review previous homework; integrated circuit MOSFET amplifiers; NMOS with depletion load; NMOS amplifier with active load; CMOS amplifiers; homework → design exercises per given specs;**

Lab: **week 11 lab report due; simulate CMOS common source amplifier; determine ac voltage gain; outline lab report;**

WEEK 13

Lecture 1: **review previous homework; CMOS source follower amplifier; ac voltage gain & output impedance; design example; homework → study for lab final;**

Lecture 2: **CMOS common gate amplifier; design example; ac voltage gain & output resistance; homework → study for lecture final exam;**

Lab: **week 12 lab report due; lab make-up session; applied engineering exercise J in-class exercise;**

WEEK 14

Lecture 1: **lab final exam review;**

Lecture 2: **lecture final exam review;**

Lab: **lab final exam;**

ELECTRONICS II LECTURE FINAL EXAM