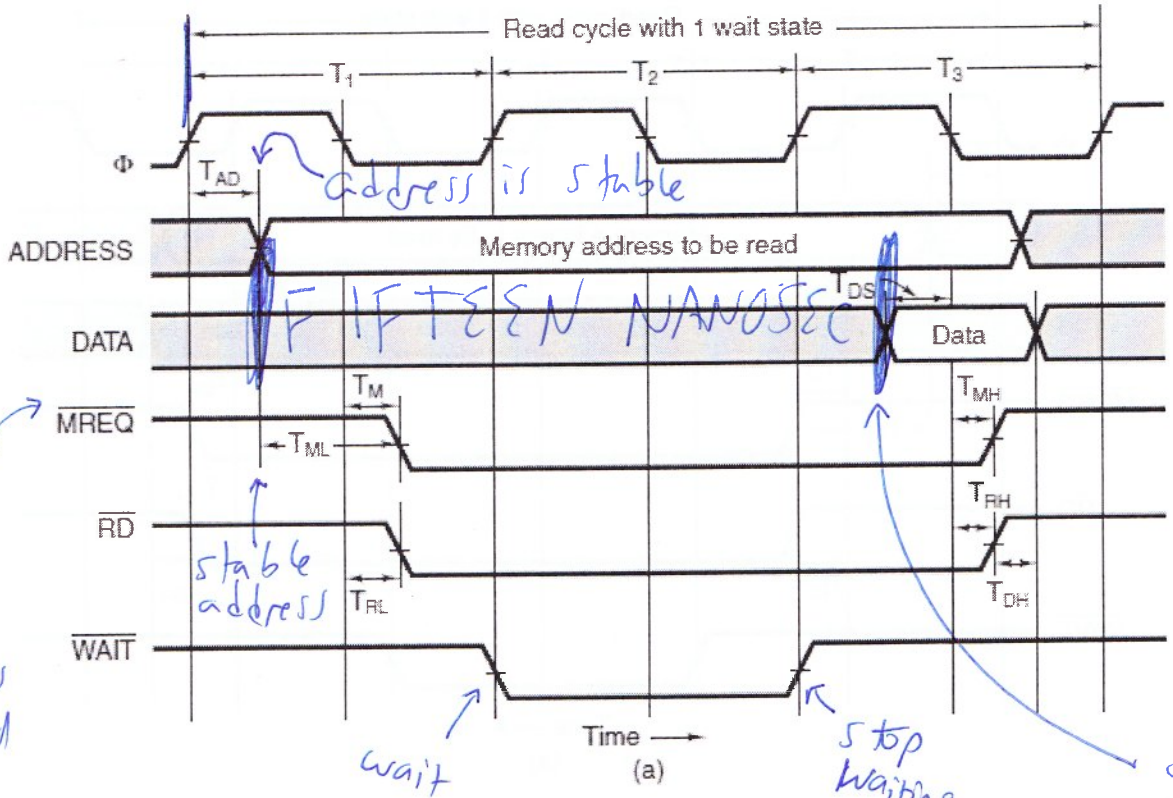
10ns 10ns 5ns



bar means this signal is asserted when LOW

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	RD delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

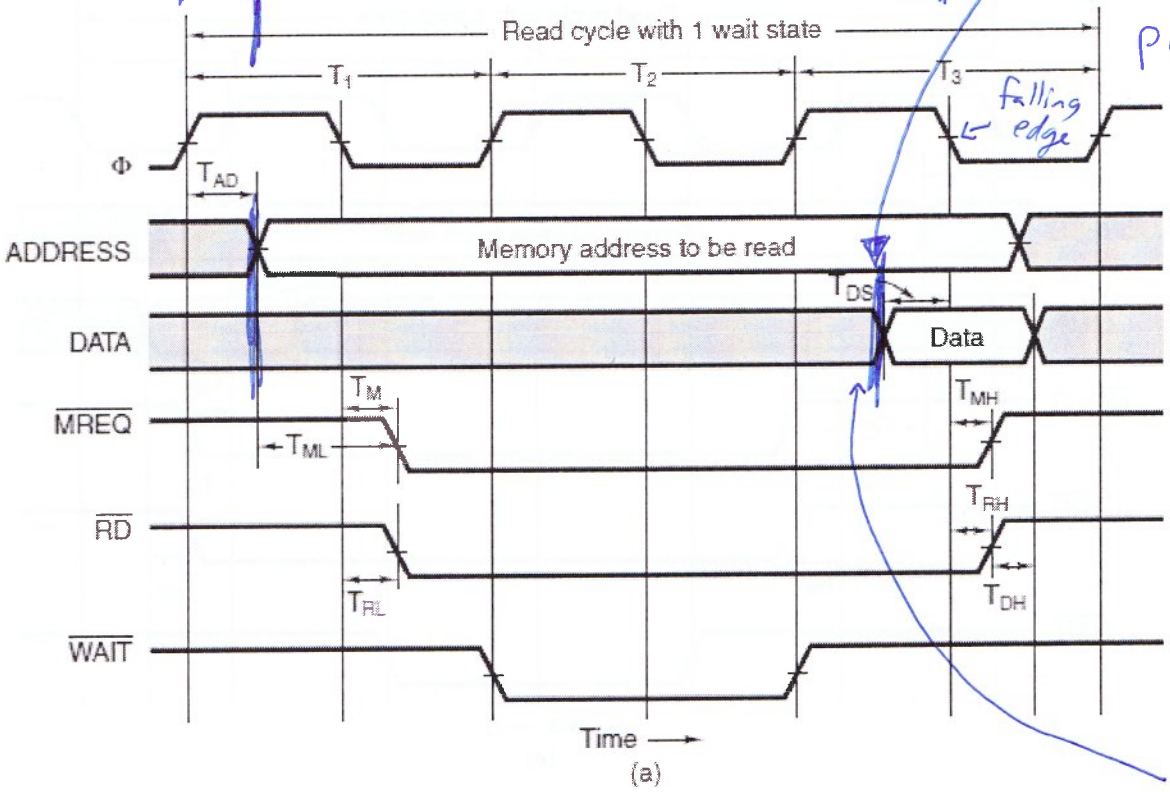
Also from text: (1) 100 MHz => 10 ns/cycle

(2) Memory takes 15ns to produce data from when the address is stable

Earliest starting point for memory is

$2\frac{1}{2}$ cycles × 10 nsec/cycle = 25 nsec

data deadline is always here @ Tos nsec prior to some falling edge



data should be ready for cpu about here

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	$\overline{RD}$ delay from falling edge of Φ in T_1		3	nsec
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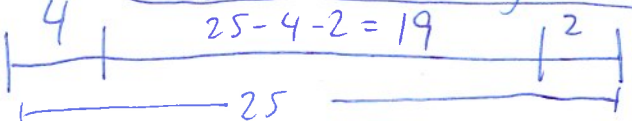
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

Q] Will 15 nsec memory be fast enough to match this picture.

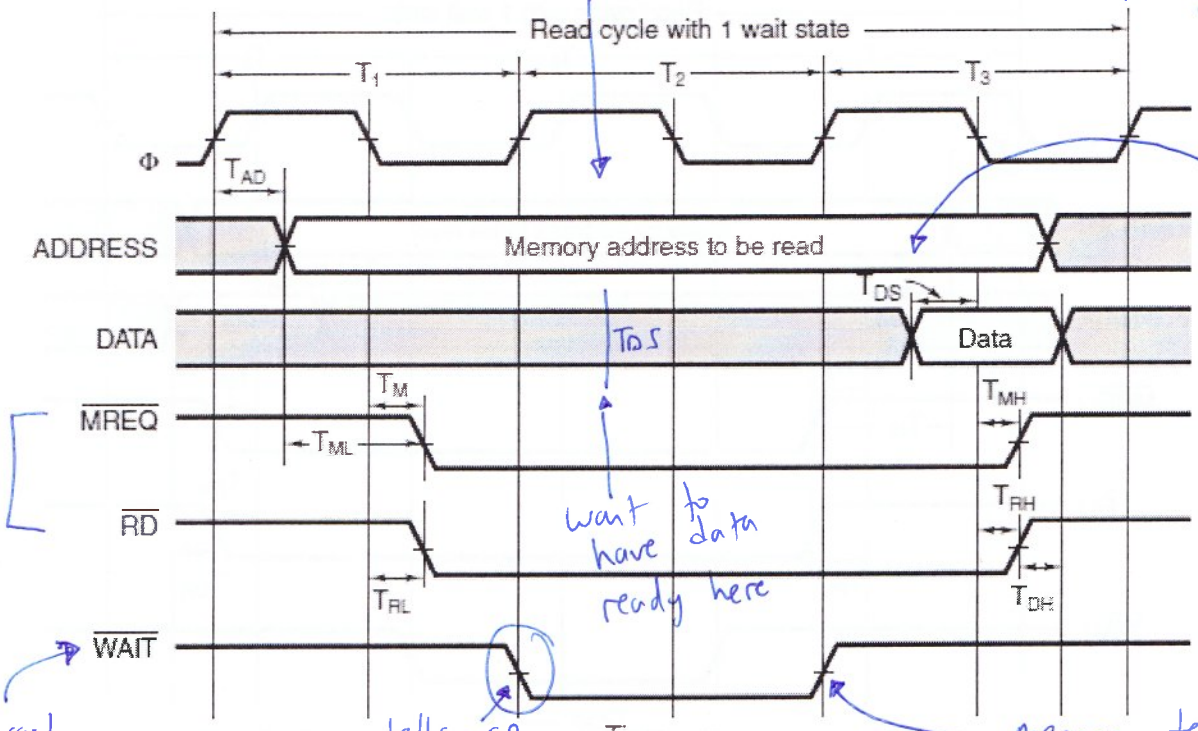
A] Yes: 25 nsec − 4 nsec TAD − 2 nsec TDS
= 19 nsec window

and our memory can do it in 15 nsec ✓



needs 9nsec memory

but Since 15 > 9, memory tells cpu its data cannot be ready in T_2



this needs 19nsec memory, we can do it in 15 therefore

only wait for whole # of cycles

memory tells cpu its data will NOT be ready TDS nsec before T2's falling edge.

memory tells cpu its data will be ready in T_3

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	RD delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

We could have bought 19 nsec memory instead of 15 nsec memory + it'd be just as fast.

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14 nsec memory is a waste of memory

A good investment would be 9 nsec memory

19nsec - 10nsec (one cycle) would let us finish TDS nsec before T2's falling edge.

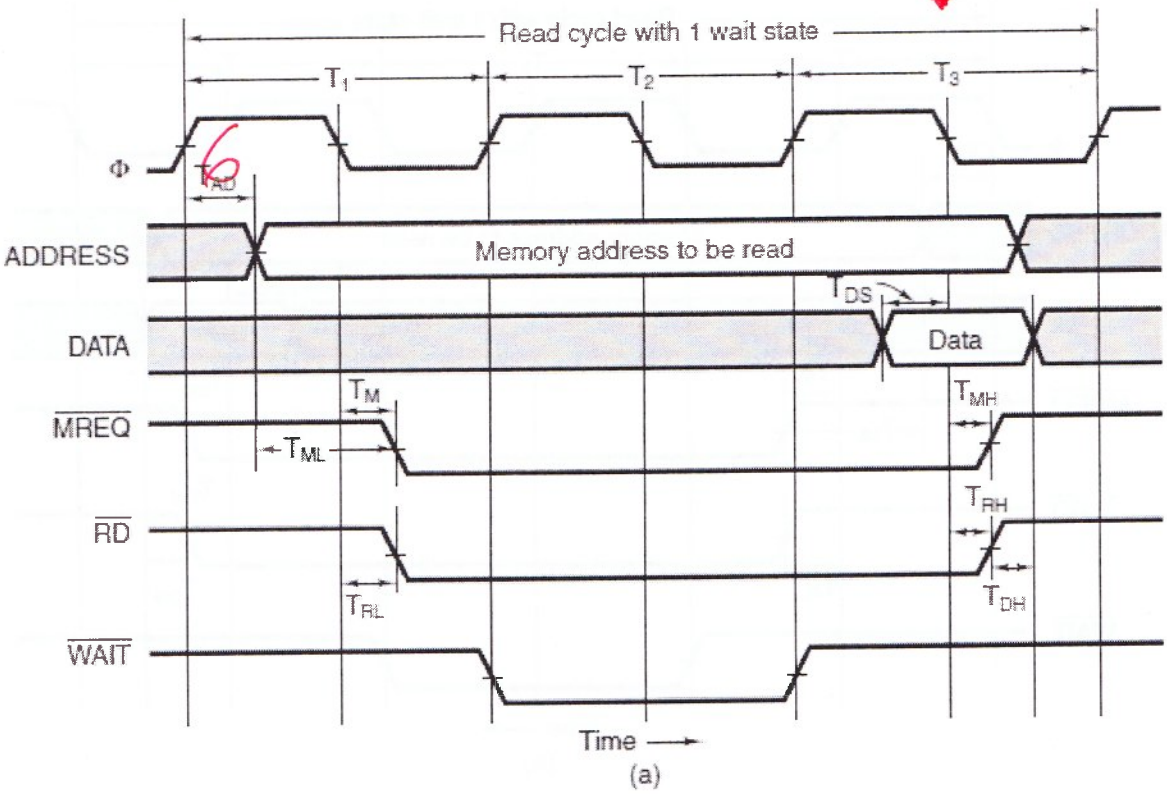
Q) How long does memory have to produce a word from an address, from when the address is stable:

bus frequency is 50 MHz.
T_{AD} = 6 nsec
T_{DS} = 3 nsec.

(a) with one wait state

(b) with no wait state.

rising — $n\frac{1}{2}$ cycles — falling



Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
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T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
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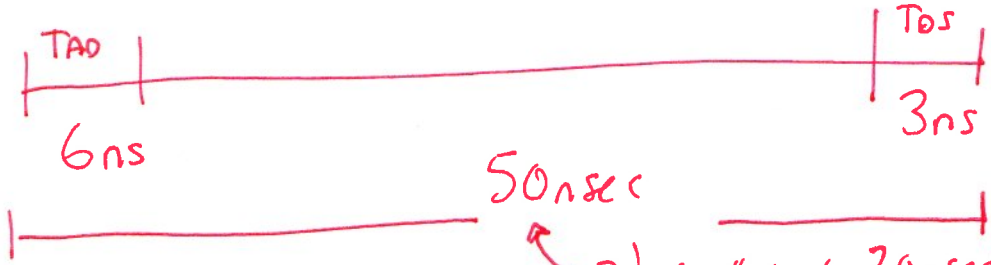
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

50MHz => 20 nsec/cycle

50
-6
-3
41nsec

(a)



(b) 41-20=
21nsec
(one fewer cycle)

Q) How much time does MM have to produce a word from the when the address is stable (with no wait states):

200 MHz bus

T_{AD} = 2 nsec

T_{DS} = 1 nsec

A) $1\frac{1}{2}$ cycles $\times \frac{5 \text{ nsec}}{\text{cycle}} = 7\frac{1}{2}$ nsec

-2 T_{AD}

-1 T_{DS}

$4\frac{1}{2}$ nsec

With one wait state: $9\frac{1}{2}$ nsec