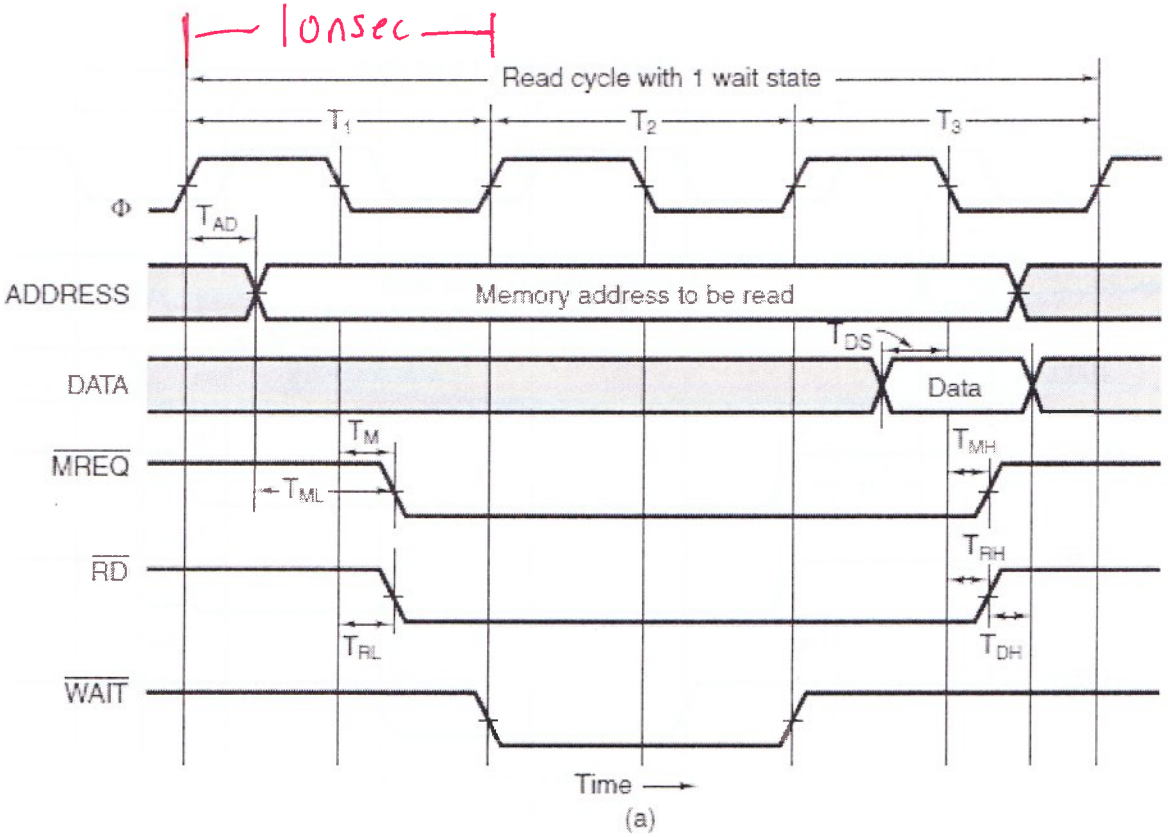


(a)

1

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	$\overline{RD}$ delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

2

3 100 MHz frequency bus → 10 nsec/cycle

4 Memory takes 15 nsec to put the data on the bus from the memory address when is stable.

frequency Hz, cycles/second	clock cycle time seconds/cycle
100 MHz	10 nsec/cycle
→ 1 GHz	1 nsec/cycle ←
40 mHz	25 sec/cycle
250 μHz	4 ksec/cycle 4000 sec/cycle
5 Hz	200 msec/cycle
2 GHz	500 picosec/cycle
8 Hz	125 msec/cycle

$100^{*} \times 10^{6}$

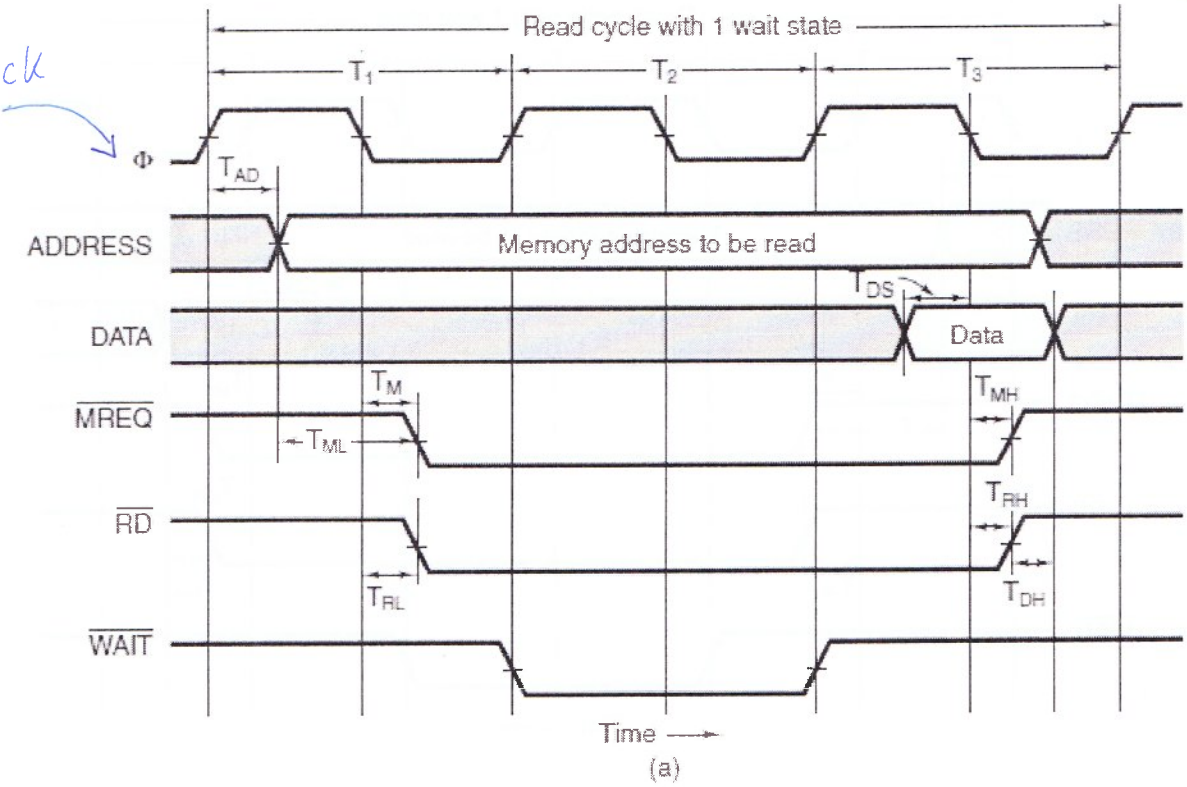
100 million cycles/second

$\equiv \frac{1}{100\,000\,000}$ sec/cycle

$\frac{1}{2}$ $\frac{1}{4}$ $\frac{1}{8}$ $\frac{1}{16}$ $\frac{1}{32}$ $\frac{1}{64}$

Synchronous bus timing diagram

clock



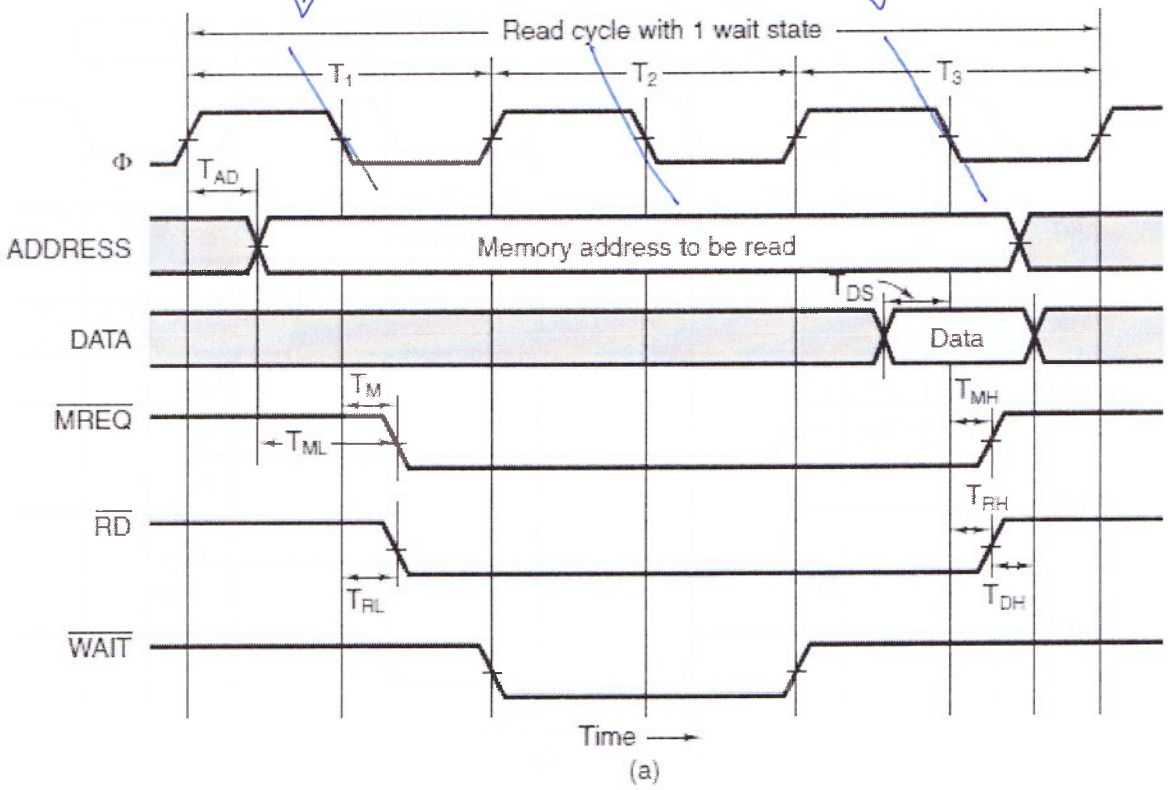
Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	RD delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

Picture of orders and deadlines. Requests and responses.

CPU puts an address on the bus and then issues a READ requests. Memory receives the address and the request from the bus. Memory cannot keep up with the speed so it tells the CPU it'll be a while. Then it tells the CPU the data is ready, the CPU reads the data and uses it.

falling edges

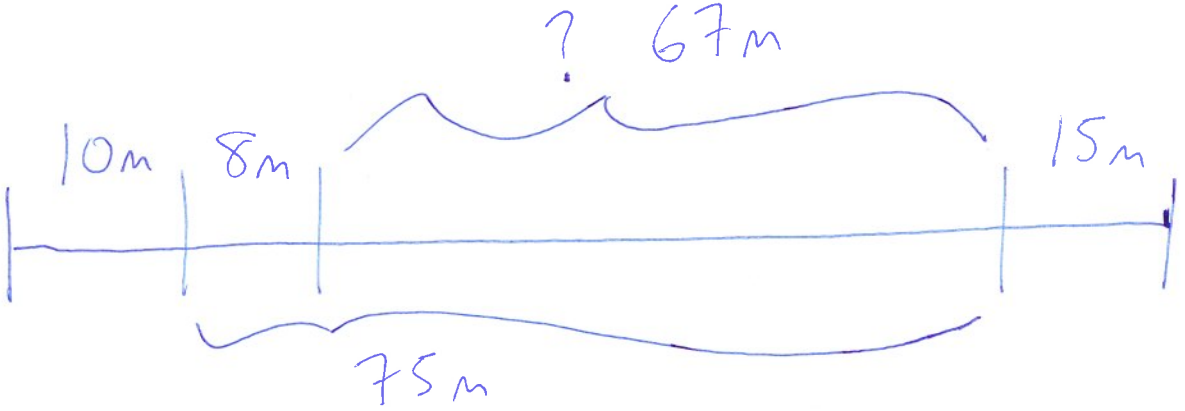


(a)

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	$\overline{RD}$ delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

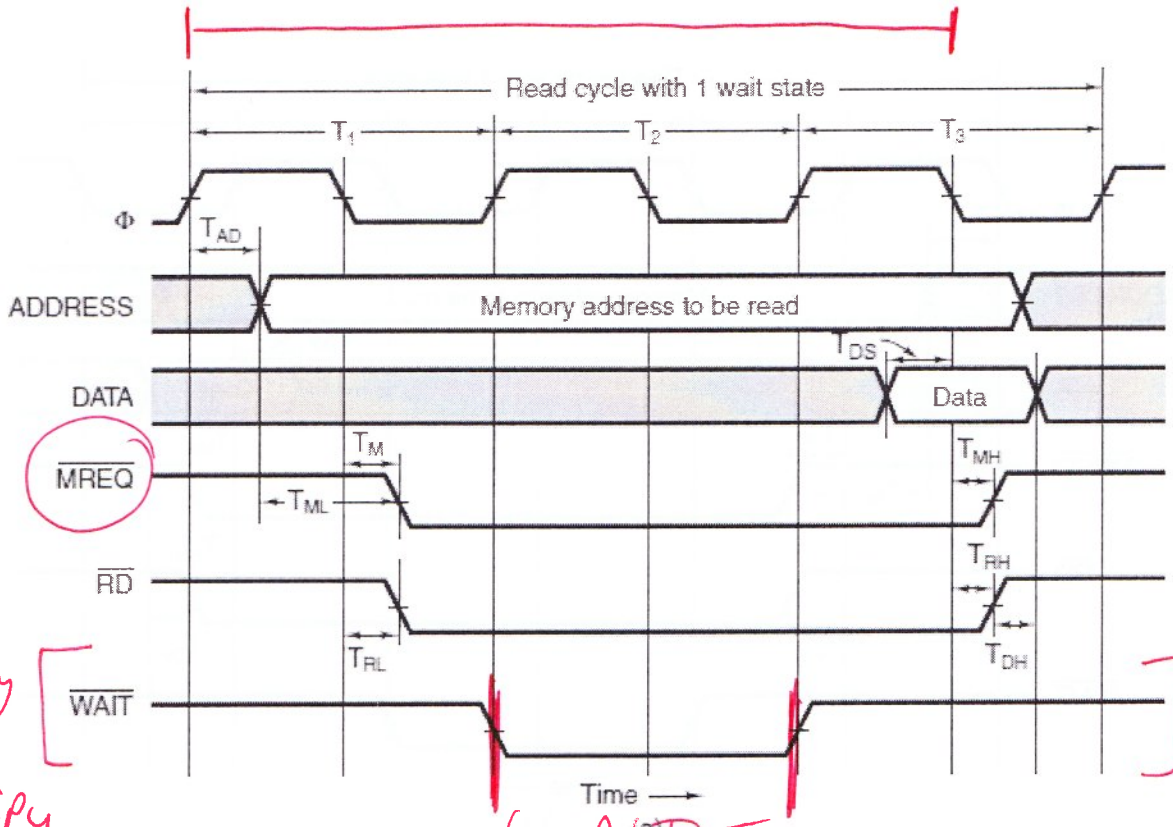
(b)

CPU is requesting data from memory and the CPU's deadline to receive it is measured from the falling edge of the clock.



100 metre long field

$2\frac{1}{2}$ cycles



WAIT

memory tells the CPU the data @ the CPU requested will not be ready ∴ do not check

one wait state must be a whole # of cycles

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	$\overline{RD}$ delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

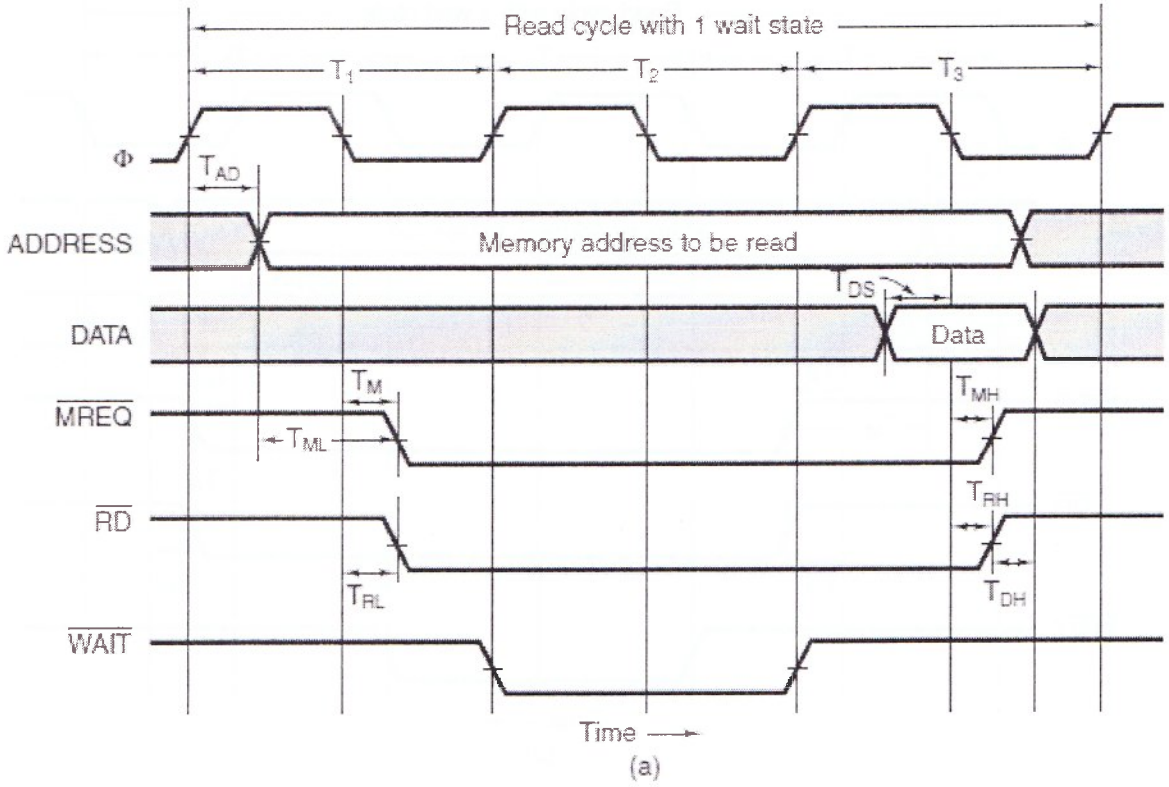
order a pizza:

phone order ← $\overline{MREQ}$

address ← T_{AD}

start $\frac{1}{2}$ hour countdown

6:50 arrival to eat 7:00 ← T_{DS}



(a)

Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	$\overline{RD}$ delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

Midterm 330-530 Feb. 22
Ne 1-331 Wednesday

Thursday - review
- timing diagram
} Set reps