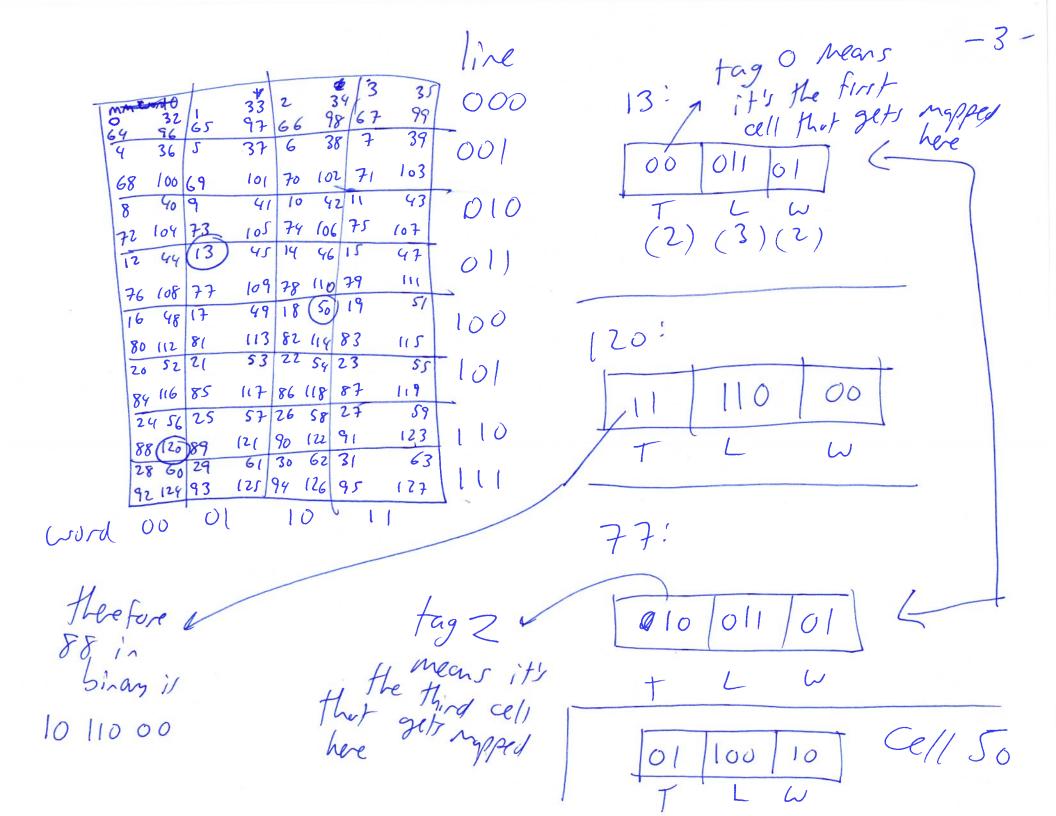
2+21 Logical us vistal address. Direct - mapped cache Virbul address is attemain-memory address of the MM cell being requested by the Cps. Consists of three fields: tag, line, and word.

The number of bits
in the main-memory address

MM: 128 Words Cache: 8 lives 1 B/word /cell 4 words/line 1092128= 7-6,7 mm address. ic Mm = 2 = 4 times MM= 27 w + 25 w cache bigger than cache Consider mm cells! all 120 word _ 100 7 5/1 W 000 1011



1024 lines / 210 / 2006 + 2 W = 2 18
256 words/line / 2006 + 2 W = 2 words
Cache 1024 lines/ 32 bit address 1 Bytelward l Byte/all Now Many bits V.A. Malegup! 32-10 10 8 make the tag, line, and word Tag Lire Work of the virtual is it really 14? address? That means there must be 2' empetiters competing block for every line. ... Mr must be 2'4 times bigger than cache. Chech: 2 mi 2 18 words = 2 14 cache memory

Save question! 2942 m = 220 -5-512. lines 2048 words/line ore gigabyte 2 Bytes/word 1 Byte/cell What is the size of the tog! the line The word in the virtual address