

2721

52!

Wed Apr 19  
NES1 - 331  
3pm - 5pm

No calculator

-1-

Exam: ① Synch bus timing diagrams  
Asynch

② n-bus datapath microcode (memory / bus)

③ cache - addressing mm block  
mapping: passes tag  
line  
set  
word

hex  $\leftrightarrow$  binary  $\leftrightarrow$  decimal

- off by 1
- modify questions
- time

MHz  $\Leftrightarrow$  Seconds/cycle

1GHz  $\Leftrightarrow$  1 nsec/cycle

KHz

25kHz  $\Leftrightarrow$  40,000 Sec/cycle

EXAM

50 Hz

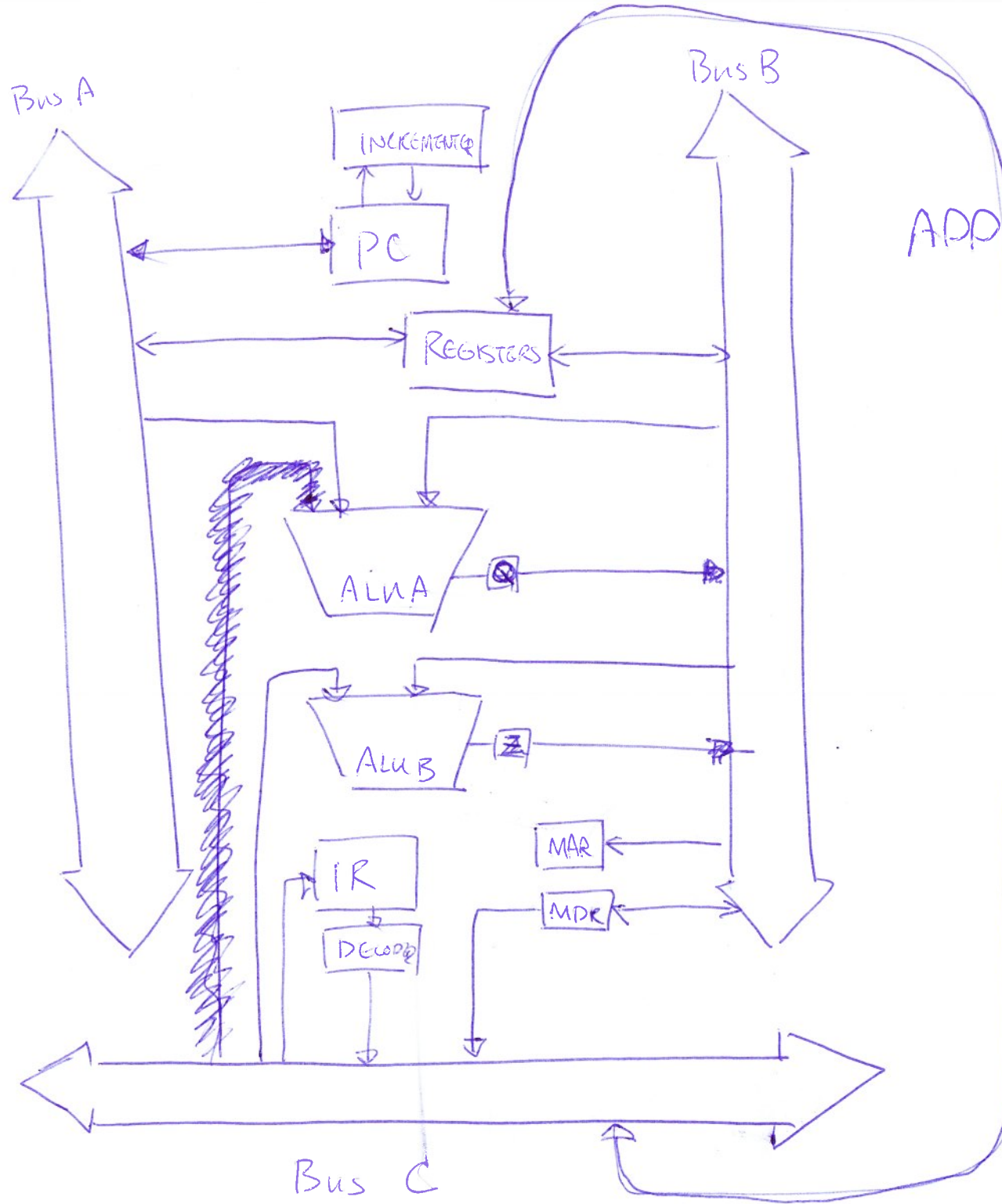
Draw a synch bus. timing diagram.

~~30~~  
~~mem~~

milli  
micro etc

Pg 50





FDE

R1, R2, R3, R4, R5

ADD

~~Disable B~~

① PC out, ~~ADD A~~ PASS THRU A

MAR in, READ, ~~IR~~

Increment, WMFC

MDR out, ~~IR~~

IR in, DECODE

② R1 out A, R2 out B, R3 out C, ADD A, Q in

③ Q out, ADD B, Z in R4 out A

④ Z out, ADD A, Q in

⑤ Q out, R5 in, END

Bonus : 60-120 seconds to go through a deck

-4-  
-4-

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problem solving : logic

business

time mgmt

no excuses

teamwork

no instructor

fun