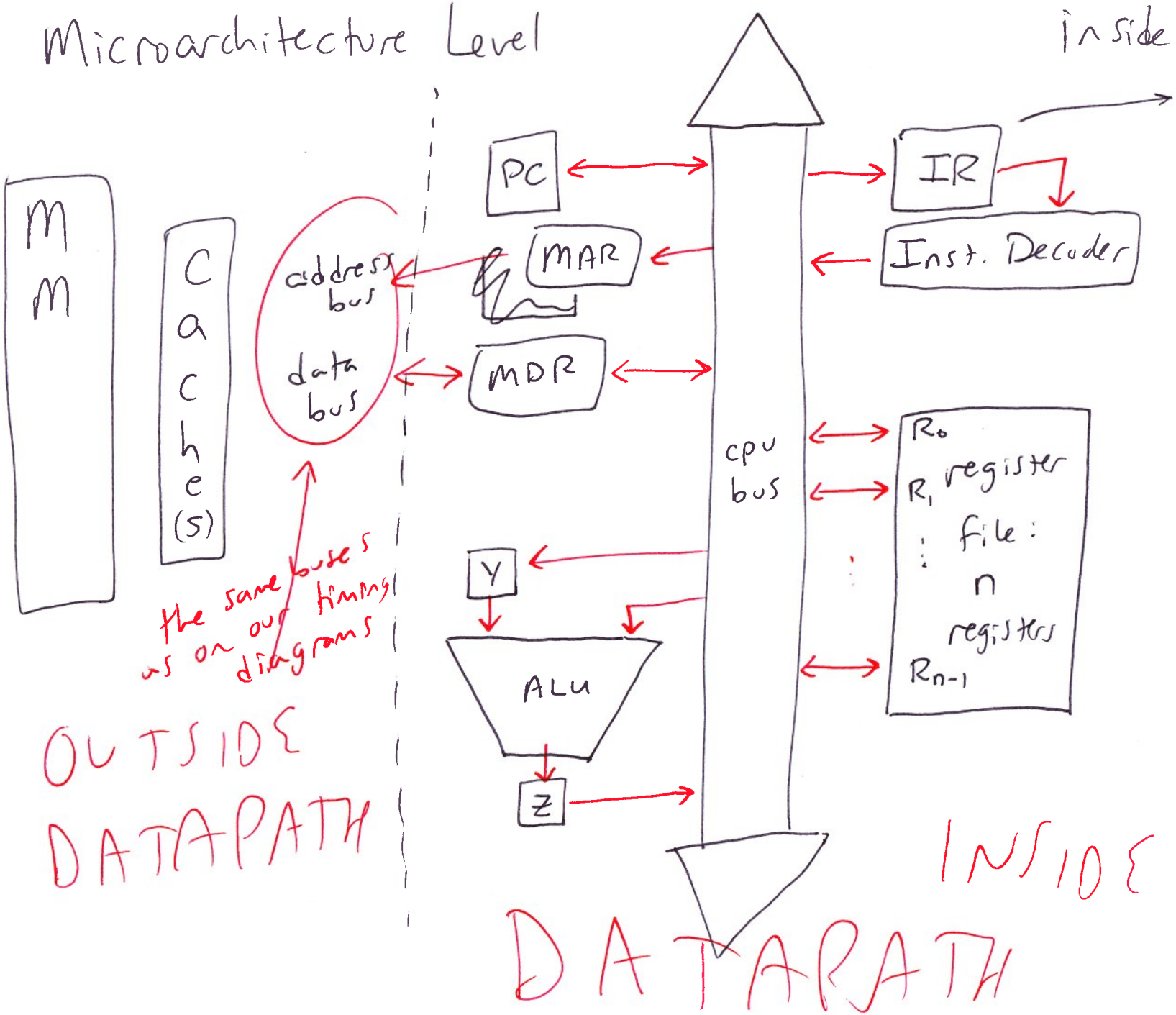
Microarchitecture Level



PC: program counter: special-purpose register that stores MM address of the next instruction to be FDE'd

CPU bus: only holds one word at a time
(per cycle)

registers are connected to the bus - some only read from the bus; others read/write from/to the bus.

we will make the best use of our time by interleaving processes

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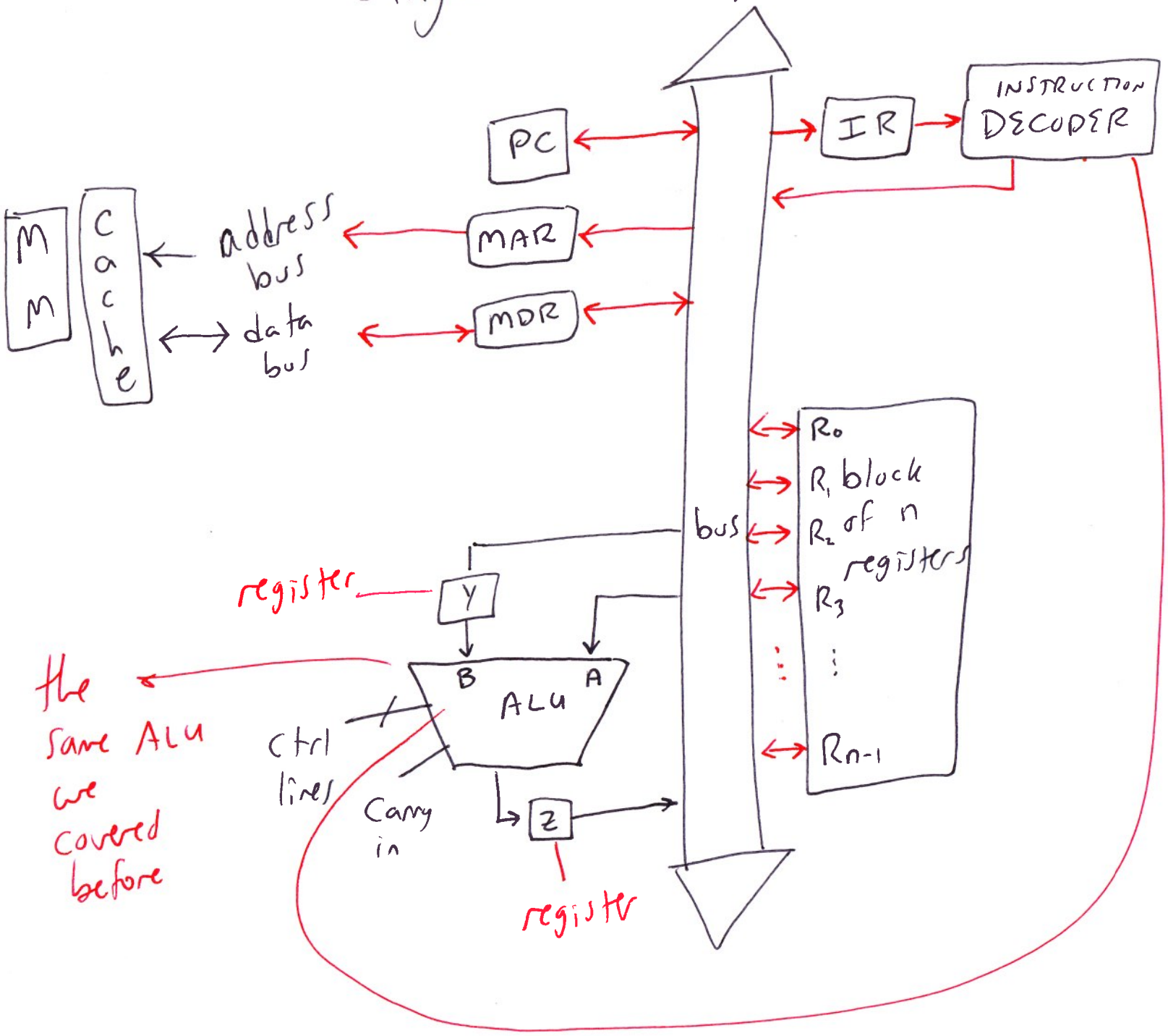
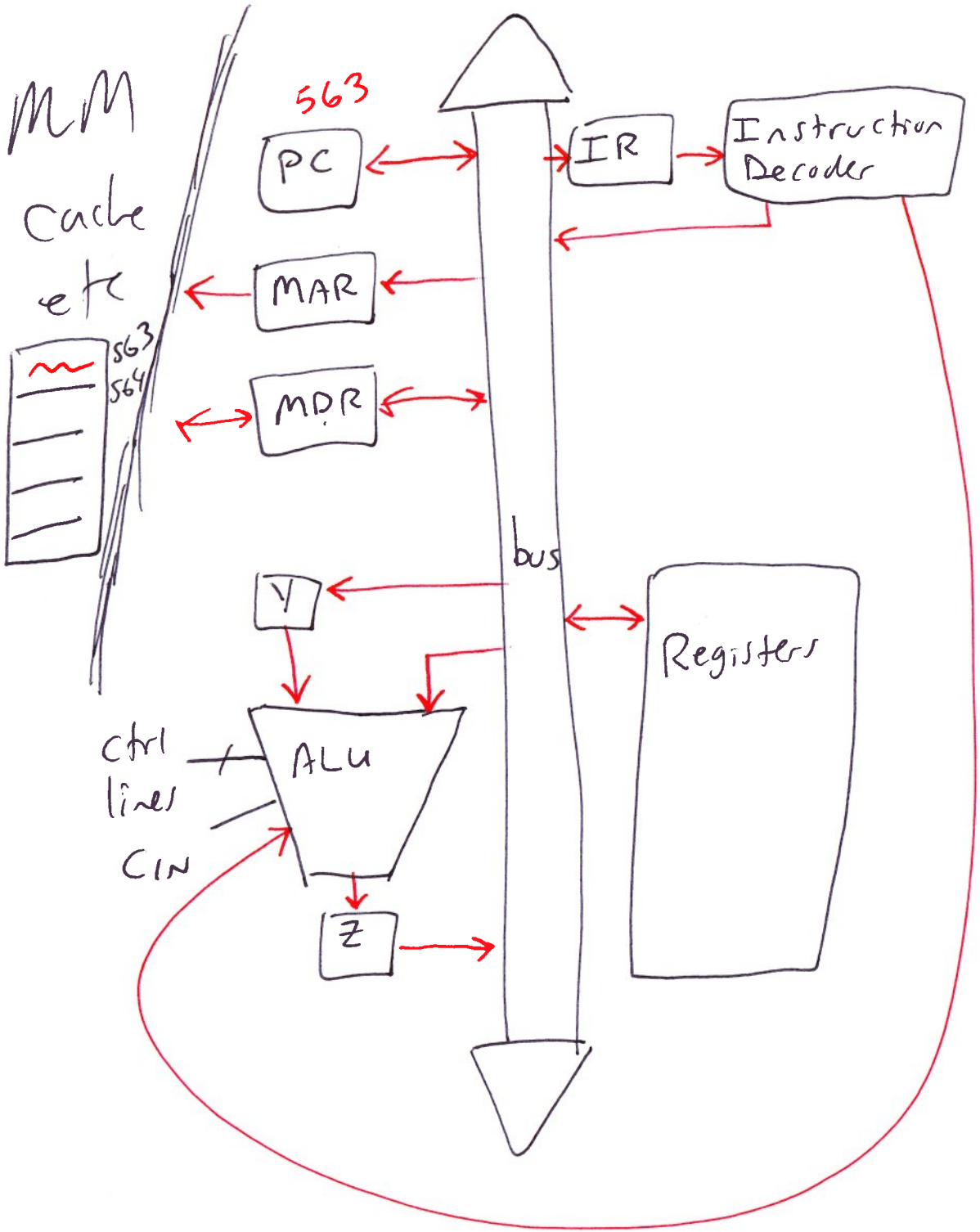
example:
- chores
- spaghetti

single-bus datapath





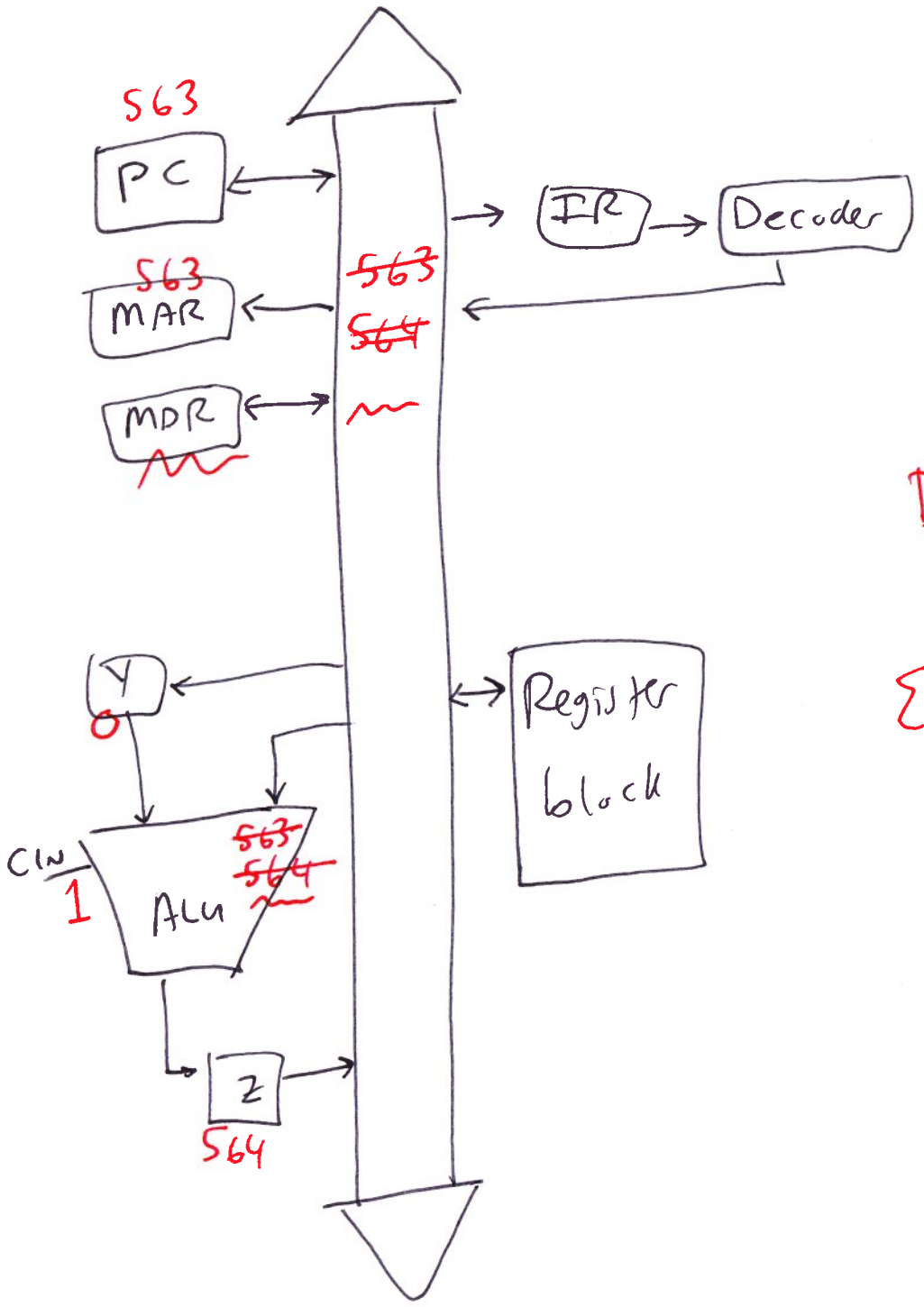
F D E an instruction

Pseudocode:

take 563 from PC — F
put into MAR
issue read
~~assert~~ assert memory request
wait
take word from MDR — D
put into IR, decode it,
do it — E

assume microprogram:

current
next



FDE: takes a while

F
1. PC_{OUT}, MAR_{IN}, READ, ~~WMFC~~,
~~MDR_{OUT}~~
CLR Y, Set $Carry_{IN}$, ADD, Z_{IN}
2. Z_{OUT}, PC_{IN}, WMFC

D
3. MDR_{OUT}, IR_{IN}, DECODE

E

Fetch + Decode for 1-bus datapath.

1. PC_{OUT}, MAR_{IN}, READ, ~~WMFC~~,
   CLEAR Y, SET C-IN ON ALU, ADD, Z_{IN}
2. Z_{OUT}, PC_{IN}, WMFC
3. MDR_{OUT}, IR_{IN}, DECODE

MICROCODE