Midterm   Wed Feb 22

330 - 530

Ne1 - 331

- label parity bits
- use units of measure
- label all gates

"Ok" : improvement
needed for
midterm

No multiple choice

No calculator

Everything but the timing diagrams

Memorize: - SR latch → Flip Flop

     - SI units   milli, micro

     - 1 GHz ⟷ 1 nsec/cycle

       100 MHz ⟷ 10 nsec/cycle

       50 MHz ⟷ 20 nsec/cycle

     - $2^{31} = 2^1 \times 2^{30} = 2G$

Review

- 6 levels of computer
   + 5 interfaces

- definitions:

   - translation / comp

   - Hamming distance

   - latency / BW

   - pipeline

   - locality

Big Ideas

- Hamming
- FDE cycle + pipelines
- disk drive reading
- mux: TT, SoP, word problems
-

  D Q

  ᗡCK

- 6-levels
-

⋆ diagrams
  math
  definitions

Home Reading

- SSD
- Endian
- Van Neumann
- student-led lectures⟍
                       ↘ - mux
                         - bit shifter
                         - 1 bit ALU
                         - edge trigger
                         - adders

Little ideas

- one-bit ALU
- 4×3 memory

Bonus:

How long does it take to read a disk with ~~10,000~~ **2000** cylinders, each containing ~~four~~ **five** tracks of ~~2048~~ **4096** sectors? First, all the sectors of track 0 are to be read starting at sector 0, then all the sectors of track 1 starting at sector 0, and so on. The ~~rotation time is 10~~ **30msec** msec, and a seek takes ~~1 msec~~ **speed is 3000 RPM** between adjacent cylinders and ~~20 msec~~ **4 msec** for the worst case. Switching between tracks of a cylinder can be done instantaneously.

$\equiv \dfrac{20\,msec}{rot}$

① find track 0 on platter 0

$$\frac{0 + 30ms}{2} = 15\,msec \quad (\text{on avg})$$

② wait for sector 0: $\dfrac{20\,msec}{2} = 10\,msec \ (\text{on avg})$

③ Read that track back-to-back ($\times 5$):

$$5 \times 20\,msec = 100\,msec$$

④ Move to next (adjacent) cylinder: 4 msec

⑤ wait for $20 - 4 = 16\,msec$ for sector 0

→ Repeat $\times 2000$

⑥ minus 20 msec (no need to move after the final read)

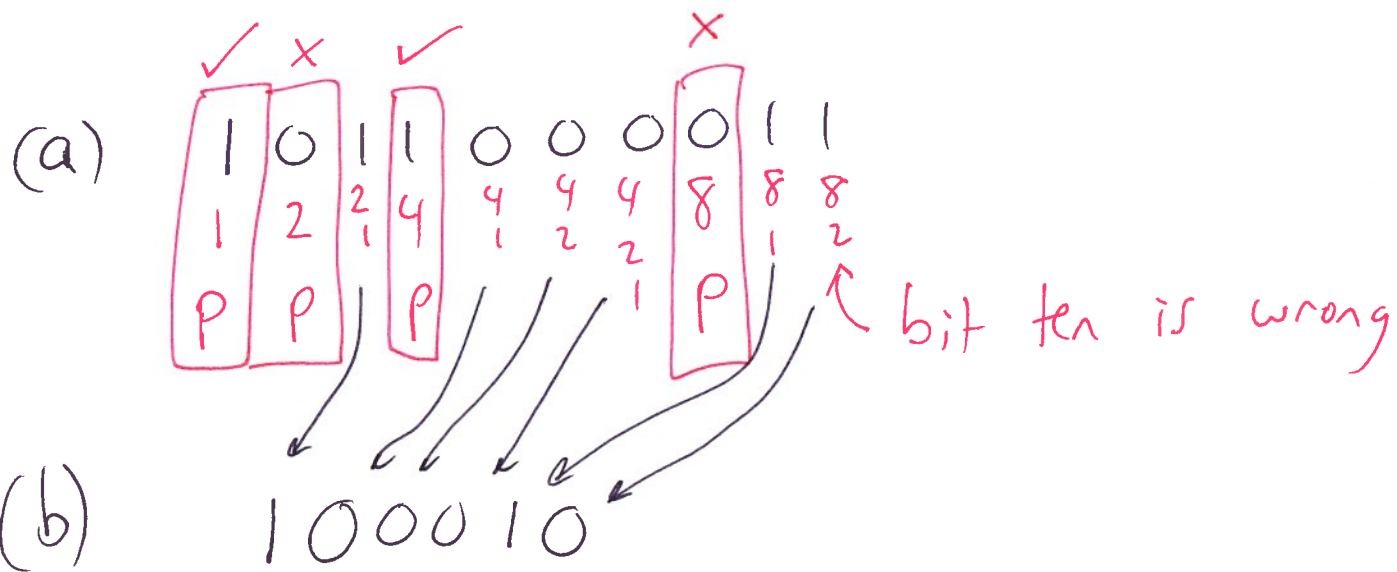$$= 15 + 10 + (100 + 4 + 16) \times 2000 - 20 = \boxed{240.005\,sec}$$

The following Hamming Codeword was made using (odd) parity.

(a) are there errors? where?

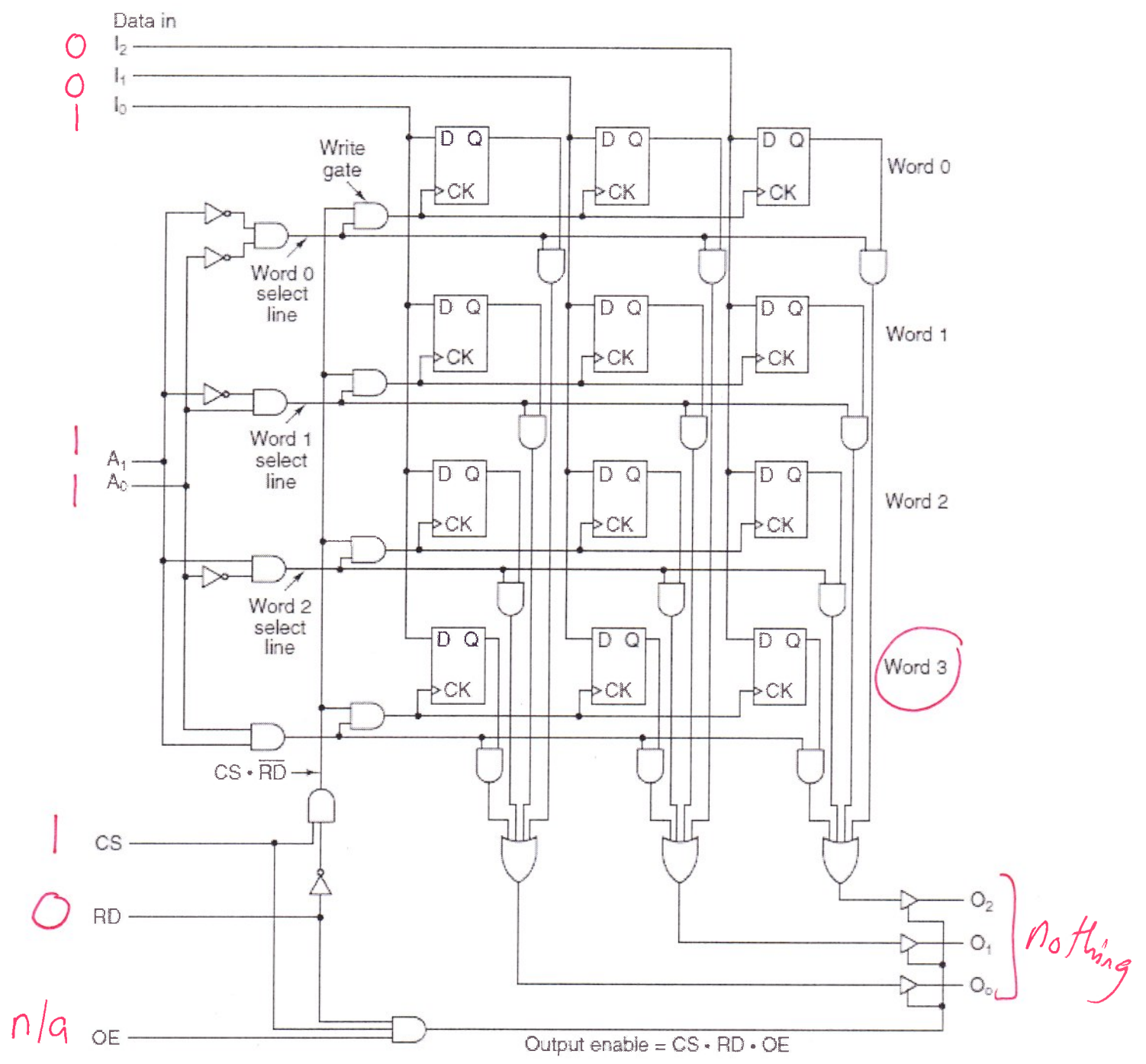(b) what was the original data word supposed to be?

1011 000011

(a)

1 0 1 1 0 0 0 0 1 1

bit ten is wrong

(b) 100010

What is the latency and band width
of a pipeline that has seven stages
that take the following amounts of time:

$2000\,\mu sec$, $2\,msec$, $0.004\,sec$, $1\,msec$, $3\,msec$, $2\,msec$, and $1000\,\mu sec$?

(a) latency: $15\,msec/instruction$

(b) bandwidth: $\dfrac{1\ instr}{4\,msec}$ $\Rightarrow$ $250\ instr/sec$

4 + 3 memory

Data in

I_2 — 0

I_1 — 0

I_0 — 1

Write gate

Word 0 select line

Word 0

Word 1 select line

Word 1

A_1 — 1
A_0 — 1

Word 2 select line

Word 2

Word 3

$CS \cdot \overline{RD} \rightarrow$

CS — 1

RD — 0

OE — n/a

Output enable = $CS \cdot RD \cdot OE$

O_2
O_1 } nothing
O_0

What are all the inputs and outputs *required* to write 100 into word 3?

1-bit ALU

Logical unit

Carry in n/a

O
INVA
O A
O ENA
1

O B
1 ENB

AB

A + B   OR

B̄

Output O

Sum

Enable
lines

O F₀

OR

| F₁
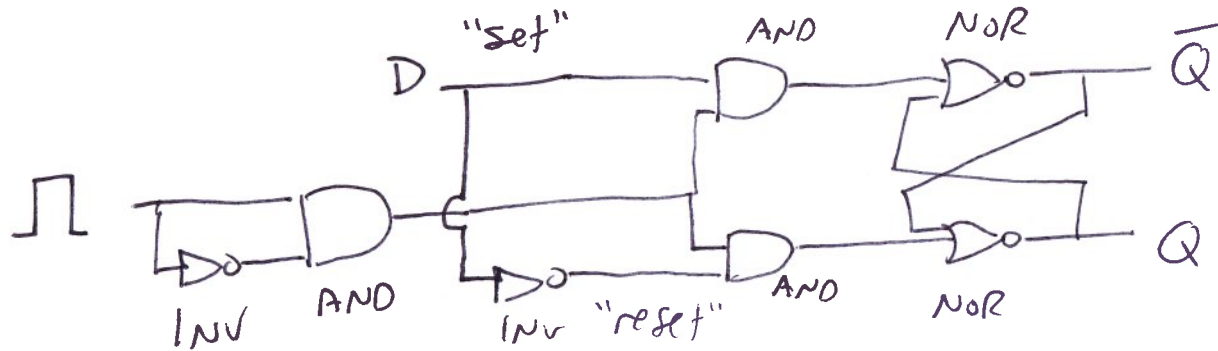
Decoder

Full
adder

Carry out n/a
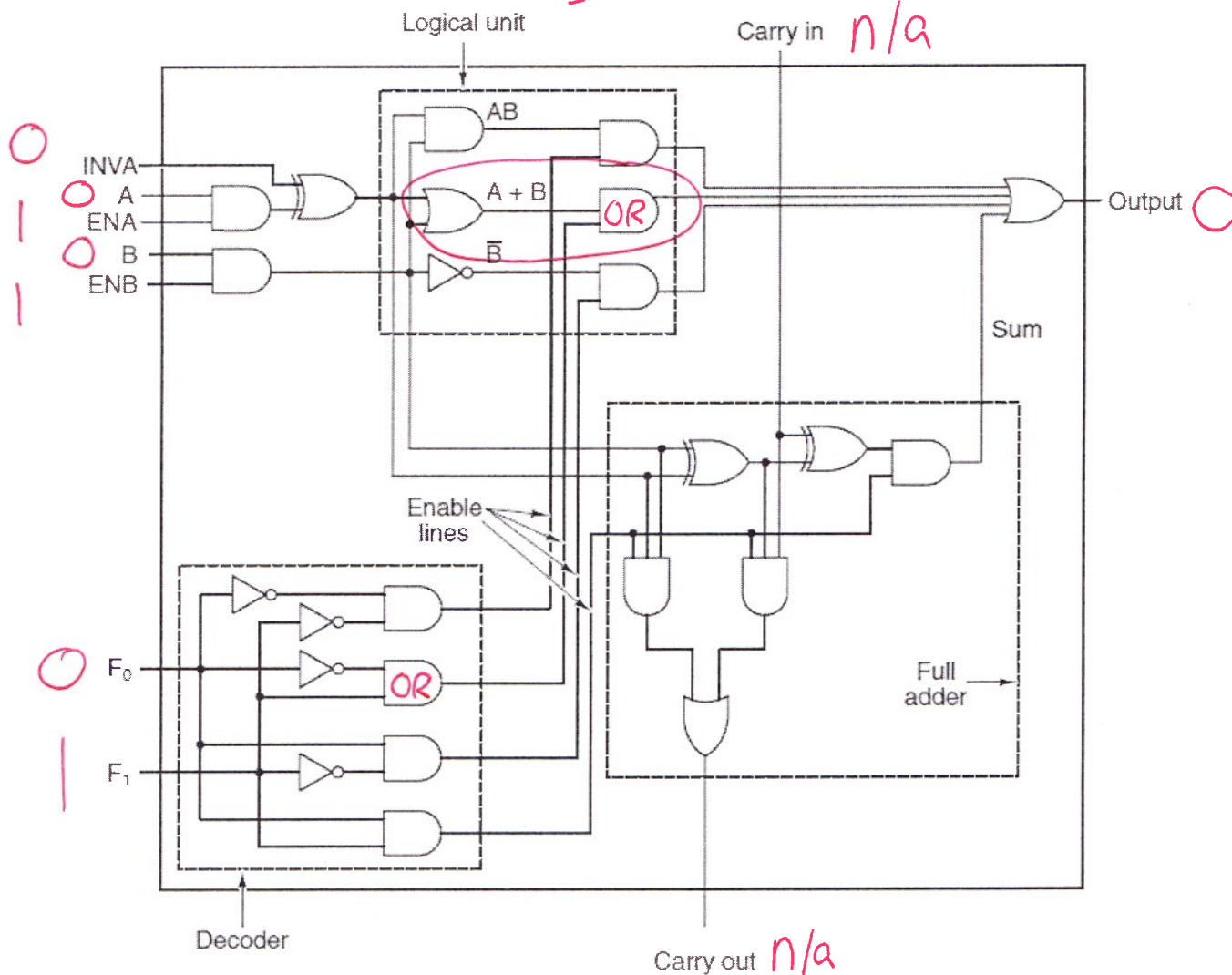
What are all the inputs and outputs required
to perform the operation "O or O"?
              A   B

(a) Draw ~~the~~ a D flipflop
(rising-edge-triggered 1-bit memory)

(b) Draw the 6-level computer + its 5 interfaces

$$\dfrac{Kn^2}{m^2}$$

5 PO
  COMPILER
4 ASM
  ASSEMBLER
3 OS
  PARTIAL INTERPRETER
2 ISA
  INTERPRETER
1 MA
  HARDWARE
0 DLL