4.1.3 Definition of the EE1002 and EE1002A Serial Presence Detect (SPD) EEPROMS

1. SCOPE

This standard defines the specifications of interface parameters, signaling protocols, and features for Serial Presence Detect (SPD) EEPROMs as used for memory module applications.

The purpose is to provide a standard for the EE1002 and EE1002A SPD logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation EE1002 refers to the part of the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2. DEVICE STANDARD

2.1 Description

The EE1002 is a 256-byte EEPROM device is designed for a range of supply voltages ranging from 1.8 V to 3.3 V nominal. The EE1002A is a similar device with a more restricted supply voltage of 3.3 V nominal only but with higher peak performance characteristics. Both devices are intended to interface to I^2C buses which have multiple devices on a shared bus, and must be uniquely addressed on this bus.

Features summary:

- Permanent and Reversible Software Data Protection for Lower 128 Bytes
- Two Wire I²C Serial Interface
- Up to 100 kHz Transfer Rate below 2.2 V
- Up to 400 kHz Transfer Rate at or above 2.2 V
- EE1002: 1.7 to 3.6 V Single Supply Voltage
- EE1002A: 3.0 to 3.6 V Single Supply Voltage
- Byte and Page Write (up to 16 Bytes)
- Random and Sequential Read modes
- Self-Timed Write Cycle
- Schmitt trigger on bus inputs
- Noise filter on bus inputs
- Automatic Address Incrementing
- Packages: PSON-8, TSSOP-8, MLP-8, SOIC-8, MSOP-8

The EE1002 is a 2 Kbit serial EEPROM memory able to lock permanently the data in its first half (from location 0x00 to 0x7F). This facility has been designed specifically for use in DRAM DIMMs (dual interline memory modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

The first half of the memory area can be write-protected using two different software write protection mechanisms. By sending the device a specific sequence, the first 128 bytes of the memory become write protected: permanently or resetable. In addition, the device allows the entire memory area to be write protected, using the WC# input (for example by tieing this input to V_{DDSPD}).

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 256x8 bits.

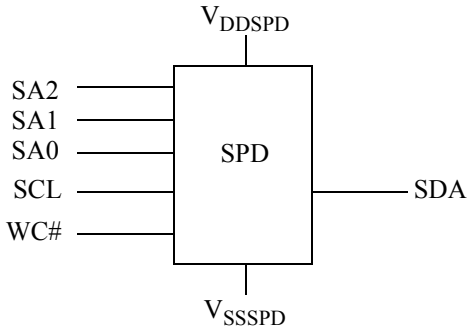


Figure 1 — Device Diagram

2.2 Device Interface

I^2C uses a two wire serial interface, comprising a bi-directional data line and a clock line. The device carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition to access the memory area and a second Device Type Identifier Code (0110) to define the protection. These codes are used together with the voltage level applied on the three chip enable inputs (SA2, SA1, SA0).

The device behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and
R/W# bit (as described in Table 2 on page 6), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

EE1002 family devices shall not initiate clock stretching, which is an optional I^2C bus feature.

2.3 Device Pin Definition

Table 1 — Pin Description for EE1002 and EE1002A

Pin #	Pin Name	Definition
1	SA0	Chip enable
2	SA1	Chip enable
3	SA2	Chip enable
4	V_{SSSPD}	Ground
5	SDA	Serial data
6	SCL	Serial clock
7	WC#	Write control
8	V_{DDSPD}	Supply voltage

2.4 Pin Functional Description

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DDSPD}. (Figure 2 on page 4 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{DDSPD}. (Figure 2 on page 4 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (SA0, SA1, SA2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. In the end application, SA0, SA1 and SA2 must be directly (not through a pull-up or pull-down resistor) connected to V_{DDSPD} or V_{SSSPD} to establish the Device Select Code. When these inputs are not connected, an internal pull-down circuitry makes (SA0, SA1, SA2) = (0, 0, 0).

The SA0 input is used to detect the V_{HV} voltage, when decoding an SWP or CWP instruction. Refer to Table 2 on page 6 for decode details.

Write Control (WC#)

This input signal is provided for protecting the contents of the whole memory from inadvertent write operations. Write Control (WC#) is used to enable (when driven Low) or disable (when driven High) write instructions to the entire memory area or to the Protection Register.

When Write Control (WC#) is tied Low or left unconnected, the write protection of the first half of the memory is determined by the status of the Protection Register.

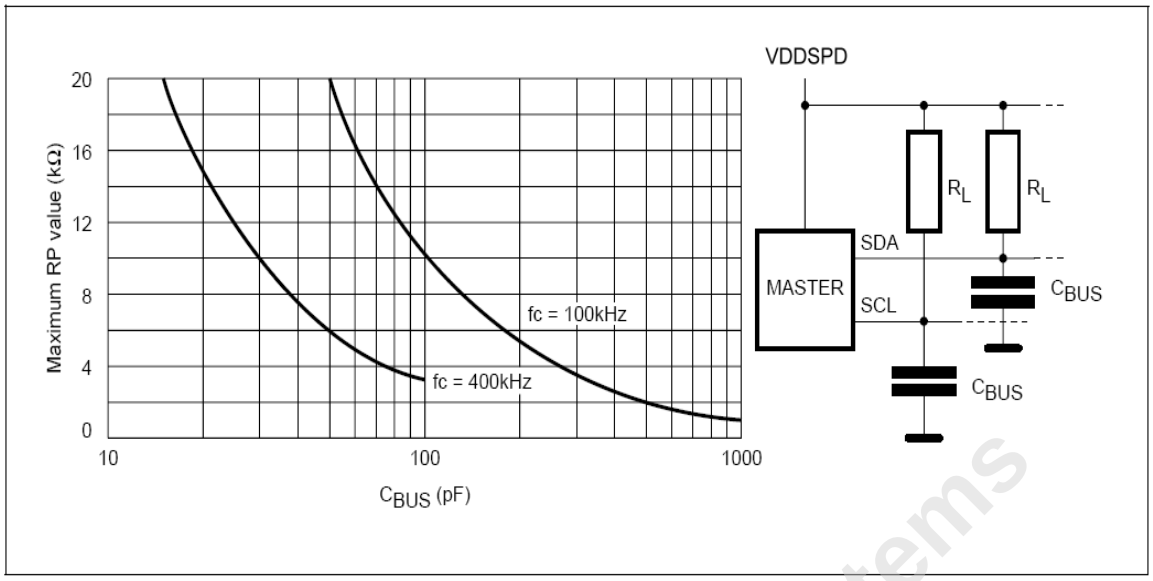


Figure 2 — Maximum R_L Value Versus Bus Capacitance (C_{BUS}) for an I^2C Bus

2.5 Device Reset and Initialization

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included.

At Power-up (phase during which V_{DDSPD} is lower than V_{DDSPD}min but increases continuously), the device will not respond to any instruction until V_{DDSPD} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{DDSPD} operating voltage defined in the DC AND AC PARAMETERS tables). Once V_{DDSPD} has passed the POR threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DDSPD} voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At Power-down (phase during which V_{DDSPD} decreases continuously), as soon as V_{DDSPD} drops from the normal operating voltage below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

2.6 Device Operation

The device supports the I^2C protocol. This is summarized in Table 3 on page 5. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The memory device is always a slave in all communication.

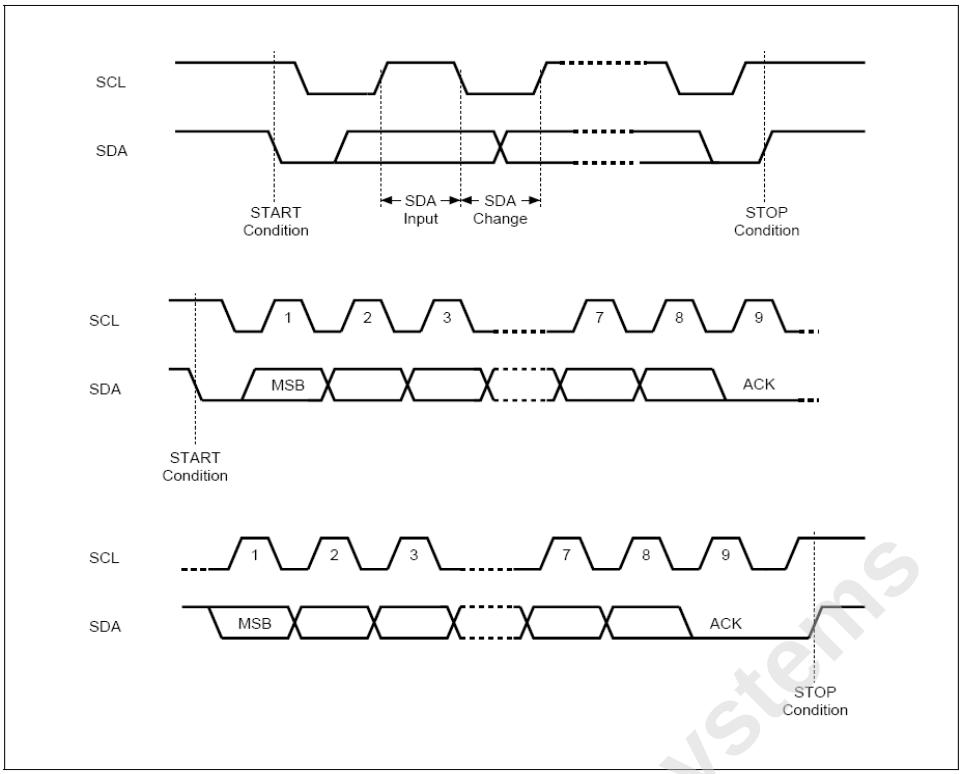


Figure 3 — I^2C Bus Protocol

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2 on page 6 (on Serial Data (SDA), most significant bit first).

Table 2 — Device Select Code

Memory Area Select Code (two arrays)[2]	Chip Enable Signals			Device Type Identifier				Chip Enable Bits			R/W#
				b7[1]	b6	b5	b4	b3	b2	b1	b0
	SA2	SA1	SA0	1	0	1	0	SA2	SA1	SA0	R/W#
Set Write Protection (SWP)	V_{SSSPD}	V_{SSSPD}	V_{HV}	0	1	1	0	0	0	1	0
Clear Write Protection (CWP)	V_{SSSPD}	V_{DDSPD}	V_{HV}					0	1	1	0
Permanently Set Write Protection (PSWP)[2]	SA2	SA1	SA0					SA2	SA1	SA0	0
Read SWP	V_{SSSPD}	V_{SSSPD}	V_{HV}					0	0	1	1
Read PSWP[2]	SA2	SA1	SA0					SA2	SA1	SA0	1

Note 1: The most significant bit, b7, is sent first.
Note 2: SA0, SA1, and SA2 are compared against the respective external pins on the EE1002.

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (SA2, SA1, SA0). To address the memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings, it is 0110b.

Up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on the Chip Enable (SA0, SA1, SA2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (SA0, SA1, SA2) inputs.

The 8th bit is the Read/Write bit (R/W#). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Standby mode.

Table 3 — Operating Modes

Mode	R/W# Bit	WC#	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, R/W# = 1
Random Address Read	0	X	1	START, Device Select, R/W# = 0, Address
	1	X		reSTART, Device Select, R/W# = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R/W# = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, R/W# = 0

Note 1: X = V_{IL} or V_{IH}.

2.7 Software Write Protect

The EE1002 has a hardware write-protection feature, using the Write Control (WC#) signal. This signal can be driven High or Low, and must be held constant for the whole instruction sequence. When Write Control (WC#) is held High, the whole memory array (addresses 0x00 to 0xFF) is write protected. When Write Control (WC#) is held Low, the write protection of the memory array is dependent on whether software write-protection has been set.

Software write-protection allows the bottom half of the memory area (addresses 0x00 to 0x7F) to be write protected irrespective of subsequent states of the Write Control (WC#) signal.

Software write-protection is handled by three instructions:

- SWP: Set Write Protection
- CWP: Clear Write Protection
- PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

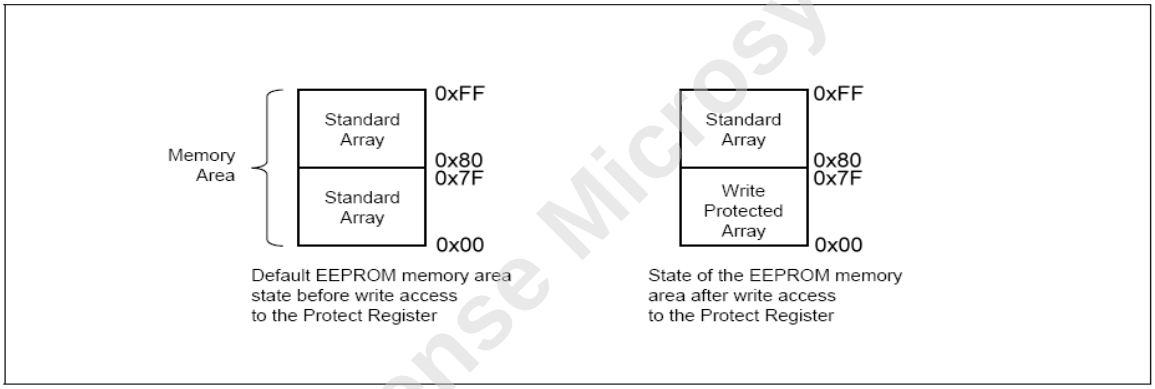


Figure 4 — Result of Setting the Write Protection

SWP and CWP

If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different Device Type Identifier (as shown in Table 2 on page 6). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all "Don't Care" (Figure 5 on page 8). Another difference is that the voltage, V_{HV}, must be applied on the SA0 pin, and specific logical levels must be applied on the other two (SA1 and SA2, as shown in Table 2 on page 6).

PSWP

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device, and regardless the state of Write Control (WC#). Also, once the PSWP instruction has been

successfully executed, the EE1002 no longer acknowledges any instruction (with a Device Type Identifier of 0110) to access the write-protection settings.

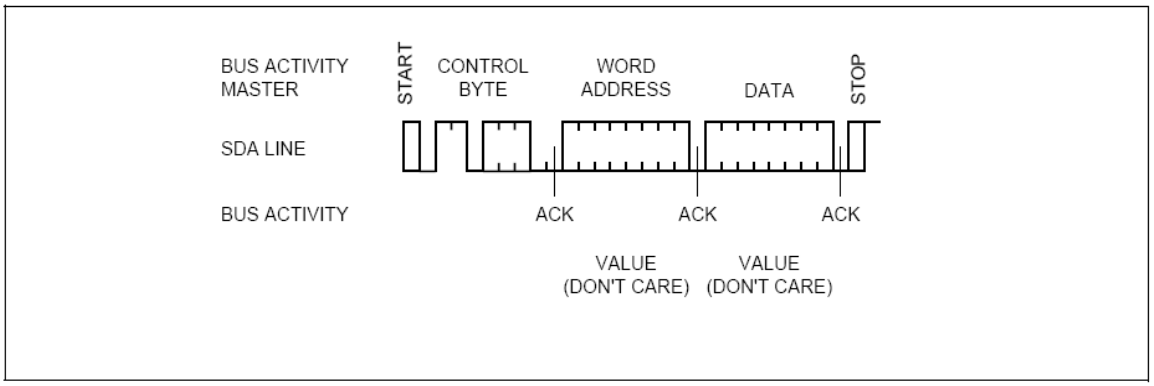


Figure 5 — Setting the Write Protection

Reading Write Protection Status

The status of software write protection can be determined using these instructions:

- Read SWP: Read Write Protection Status
- Read PSWP: Read Permanently Set Write Protection Status

Read SWP

The controller issues a Read SWP command. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck.

Read PSWP

The controller issues a Read PSWP command. If Permanent Software Write Protection has not been set, the device replies to the data byte with an Ack. If Permanent Software Write Protection has been set, the device replies to the data byte with a NoAck.

2.8 Write Operations

Following a Start condition the bus master sends a Device Select Code with the R/W# bit reset to 0. The device acknowledges this, as shown in Table 6 on page 9, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

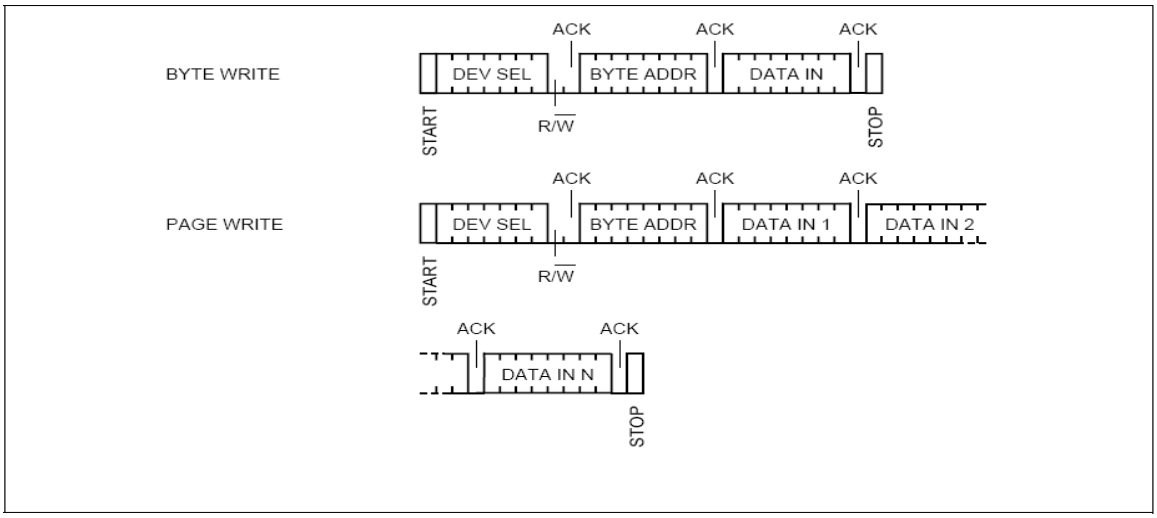


Figure 6 — Write Mode Sequences in a Non-Write Protected Area

Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 6 on page 9.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control (WC#) is Low. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

2.9 Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 13 on page 18, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 7 on page 10, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

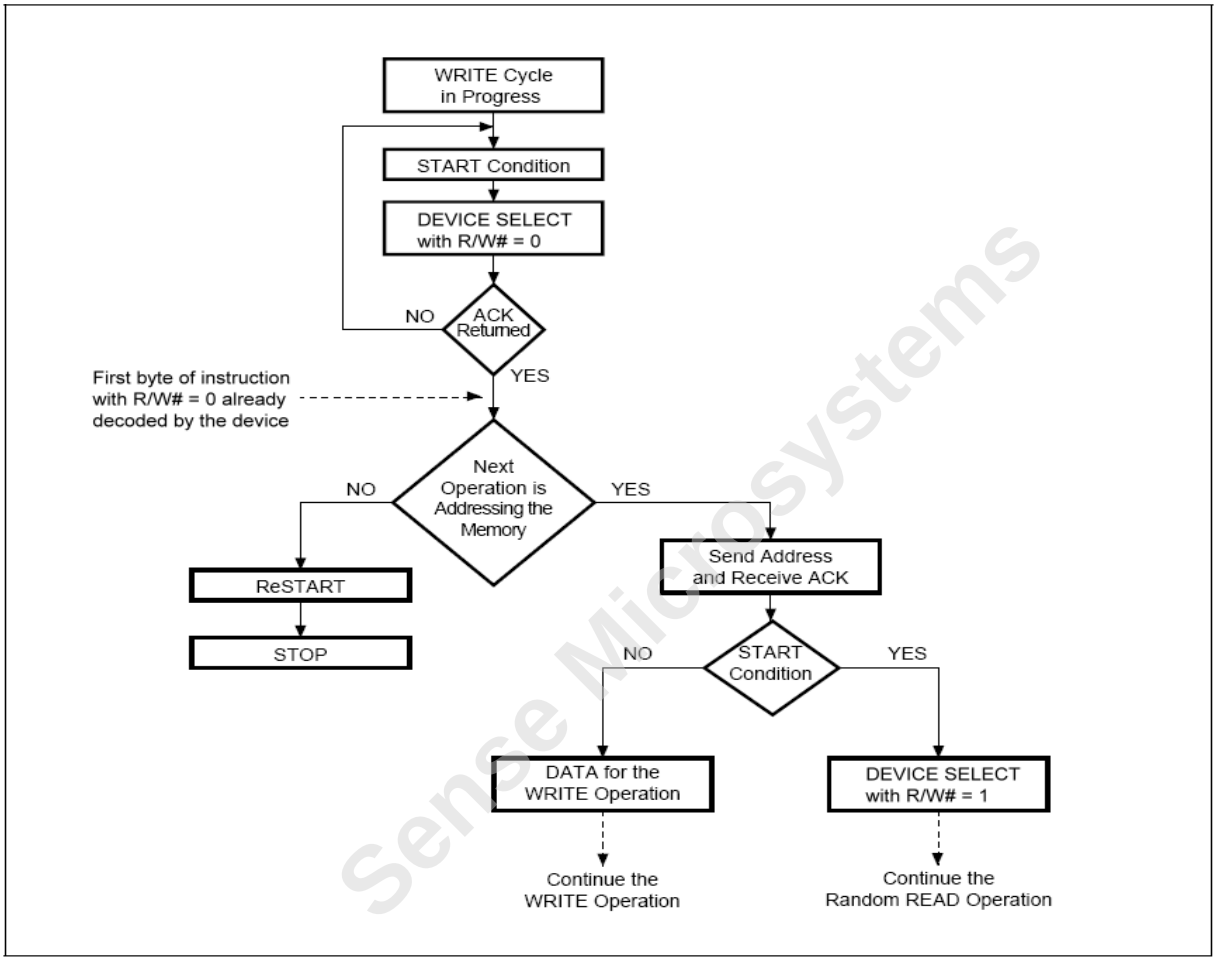


Figure 7 — Write Cycle Polling Flowchart Using ACK

2.10 Read Operations

Read operations are performed independently of whether hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

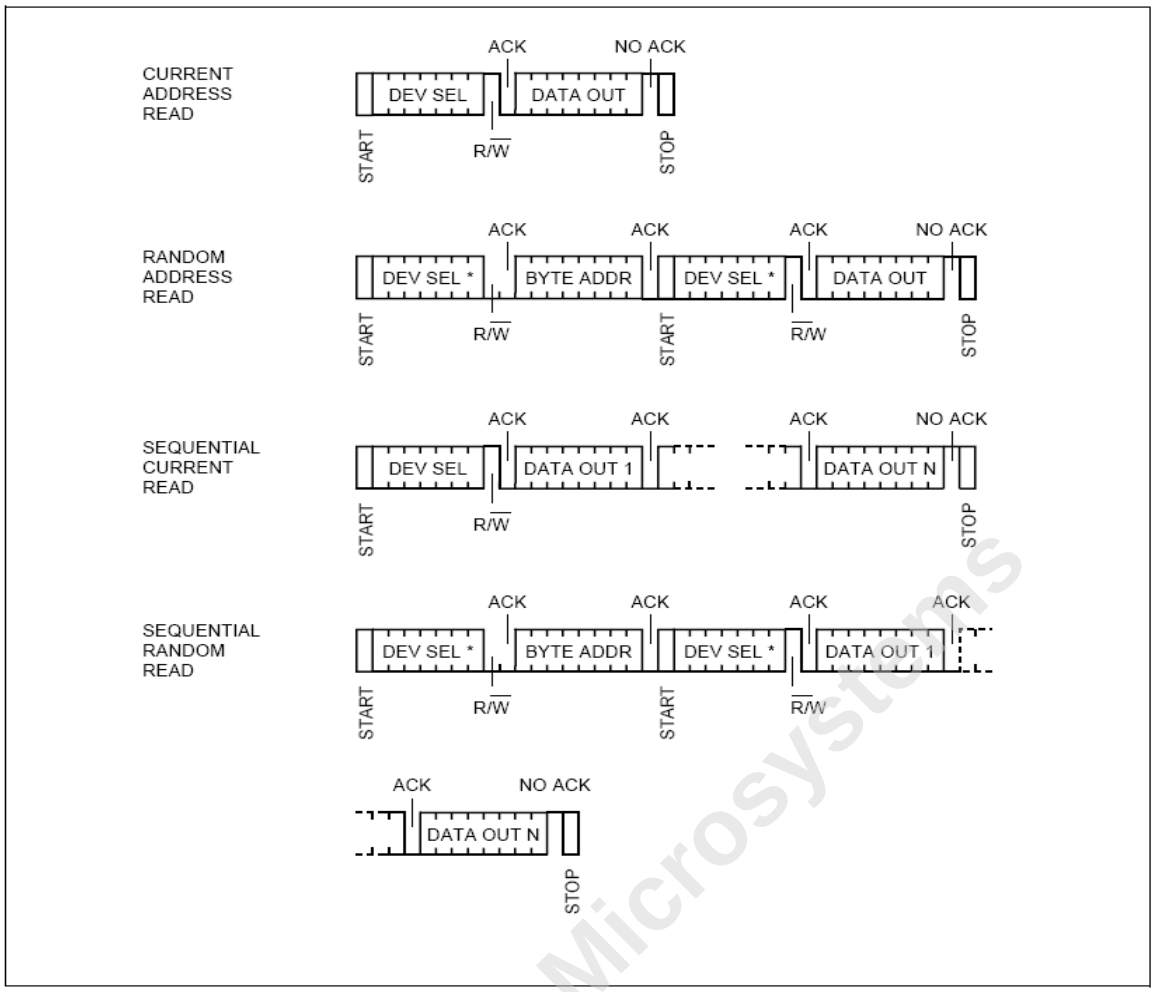


Figure 8 — Read Mode Sequences

Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 8 on page 11) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R/W# bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/W# bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 8 on page 11, without acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the

next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 8 on page 11.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

Table 4 — Acknowledge When Writing Data or Defining Write Protection (Instructions with R/W# bit = 0)

Status	WC#	Instruction	Ack	Address	Ack	Data byte	Ack	Write Cycle (t_W)
Permanently protected	x	PSWP or CWP	NoAck	Not significant	NoAck	Not significant	NoAck	No
		SWP[2]	Ack or NoAck	Not significant	Ack or NoAck	Not significant	Ack or NoAck	Yes
		Page or byte write in lower 128 bytes	Ack	Address	Ack	Data	Ack or NoAck[1]	Yes
Protected with SWP	0	SWP	NoAck	Not significant	NoAck	Not significant	NoAck	No
		CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
		PSWP	Ack	Not significant	Ack	Not significant	Ack	Yes
		Page or byte write in lower 128 bytes	Ack	Address	Ack	Data	Ack or NoAck[1]	Yes
	1	SWP	NoAck	Not significant	NoAck	Not significant	NoAck	No
		CWP	Ack	Not significant	Ack	Not significant	NoAck	No
		PSWP	Ack	Not significant	Ack	Not significant	NoAck	No
		Page or byte write	Ack	Address	Ack	Data	NoAck	No
Not protected	0	PSWP, SWP, or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
		Page or byte write	Ack	Address	Ack	Data	Ack	Yes
	1	PSWP, SWP, or CWP	Ack	Not significant	Ack	Not significant	NoAck	No
		Page or byte write	Ack	Address	Ack	Data	NoAck	No

1. Both implementations exist in the industry. Software must accept either return code.
2. Response codes and required write cycle delay T_W may depend on the previous status of SWP protection.

Table 5 — Acknowledge When Reading the Write Protection (Instructions with R/W# bit = 1)

PSWP Status	SWP Status	Instruction	ACK	Address	ACK	Data byte	ACK
Set	X	Read PSWP	NoAck	Not significant	NoAck	Not significant	NoAck
Not Set	X	Read PSWP	Ack	Not significant	NoAck	Not significant	NoAck
Set	Set	Read SWP	NoAck	Not significant	NoAck	Not significant	NoAck
Set	Not Set	Read SWP[1]	Ack or NoAck	Not significant	Ack or NoAck	Not significant	Ack or NoAck
Not Set	Set	Read SWP	NoAck	Not significant	NoAck	Not significant	NoAck
Not Set	Not Set	Read SWP	Ack	Not significant	NoAck	Not significant	NoAck

Note: X = Set or Not Set.

1. Both Ack or NoAck response codes to this command exist in the industry. Software must accept either return code.

2.11 Initial Device State

The device is delivered with all bits in the memory array set to '1' (each byte contains 0xFF).

2.12 Use in a Memory Module

In the Dual Inline Memory Module (DIMM) application, the EE1002 is soldered directly onto the printed circuit module. The three Chip Enable inputs (SA0, SA1, SA2) must be connected to V_{SSSPD} or V_{DDSPD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see Table 6 on page 13). The pull-up resistors needed for normal behavior of the I^2C bus are connected on the I^2C bus of the mother-board.

The Write Control (WC#) of the EE1002 can be left unconnected. However, connecting it to V_{SSSPD} is recommended, to maintain full read and write access.

Table 6 — Unique Addressing of SPDs in DIMM Applications

DIMM Position	SA2	SA1	SA0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Note: 0 = V_{SSSPD}, 1 = V_{DDSPD}

2.13 Programming the EE1002

The situations in which the EE1002 is programmed can be considered under two headings:

- when the DIMM is isolated (not inserted on the PCB motherboard)
- when the DIMM is inserted on the PCB motherboard

DIMM Isolated

With specific programming equipment, it is possible to define the EE1002 content, using Byte and Page Write instructions, and its write-protection using the SWP and CWP instructions. To issue the SWP and CWP instructions, the DIMM must be inserted in the application-specific slot where the SA0 signal can be driven to V_{HV} during the whole instruction. This programming step is mainly intended for use by DIMM makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the lower 128 Bytes, and finally to set permanently the write-protection with the PSWP instruction.

DIMM Inserted in the Application Mother Board

As the final application cannot drive the SA0 pin to V_{HV}, the only possible action is to freeze the write-protection with the PSWP instruction.

Table 4 on page 12 and Table 5 on page 13 show how the Ack bits can be used to identify the write-protection status.

2.14 Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 7 — Absolute Maximum Ratings for EE1002 and EE1002A

Symbol	Parameter	Min	Max	Units
T_{STG}	Storage temperature	-65	150	°C
V_{IO}	Input or output range, SA0	-0.50	10.0	V
	Input or output range, other pins	-0.50	4.3	V
V_{DDSPD}	Supply voltage	-0.5	4.3	V

2.15 DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8 — Operating Conditions for EE1002 and EE1002A

Symbol	Parameter	EE1002		EE1002A		Units
		Min	Max	Min	Max	
V_{DDSPD}	Supply Voltage	1.7	3.6	3.0	3.6	V
T_C	Case operating temperature	0	95	0	95	°C

Table 9 — AC Measurement Conditions for EE1002 and EE1002A

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2 * V_{DDSPD} to 0.8 * V_{DDSPD}		V
	Input and output timing reference levels	0.3 * V_{DDSPD} to 0.7 * V_{DDSPD}		V

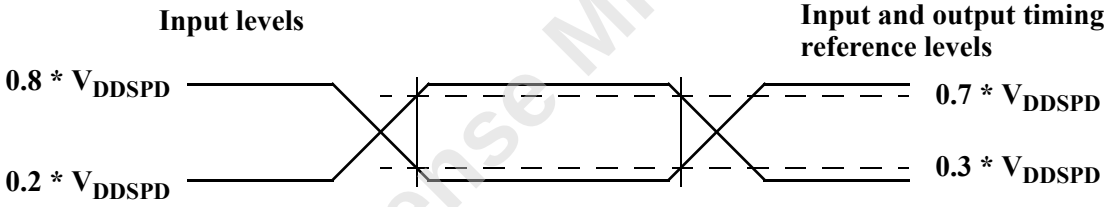


Figure 9 — AC Measurement I/O Waveform

Table 10 — Input Parameters for EE1002 and EE1002A

Symbol	Parameter[1,2]	Test Condition	Min	Max	Units
C_{IN}	Input capacitance (SDA)	--	--	8	pF
C_{IN}	Input capacitance (other pins)	--	--	6	pF
Z_{EIL}	Ei (SA0, SA1, SA2) input impedance	$V_{IN} < 0.3 * V_{DDSPD}$	30	--	kΩ
Z_{EIH}	Ei (SA0, SA1, SA2) input impedance	$V_{IN} > 0.7 * V_{DDSPD}$	800	--	kΩ
Z_{WCL}	WC# input impedance	$V_{IN} < 0.3 * V_{DDSPD}$	5	--	kΩ
Z_{WCH}	WC# input impedance	$V_{IN} > 0.7 * V_{DDSPD}$	500	--	kΩ
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	Single glitch, f ≤ 100 KHz	--	--	ns
		Single glitch, f > 100 KHz	0	50	

Note 1: T_A = 25 °C, f = 400 kHz
Note 2: Verified by design and characterization, not necessarily tested on all devices

DC Characteristics are listed separately for the wide voltage range EE1002 and the restricted voltage range EE1002A.

Table 11 — DC Characteristics for EE1002

Symbol	Parameter	Test Condition (in addition to those in Table 8 on page 15)	Min	Max	Units
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}	--	±2	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SSSPD}$ or V_{DDSPD}, SDA in Hi-Z	--	±2	µA
I_{DD}	Supply current	V_{DDSPD} = 1.7 V, f_C = 100 kHz (rise/fall time < 30 ns)	--	1	mA
I_{DD1}	Standby Supply current	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, V_{DDSPD} = 3.6 V	--	1	µA
		$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, V_{DDSPD} = 1.7 V	--	0.5	µA
V_{IL}	Input low voltage (SCL, SDA, WC#)	--	-0.45	0.3 * V_{DDSPD}	V
V_{IH}	Input high voltage (SCL, SDA, WC#)	--	0.7 * V_{DDSPD}	V_{DDSPD} + 1	V
V_{HV}	SA0 high voltage	$V_{HV} - V_{DDSPD} \geq 4.8$ V	7	10	V
V_{OL}	Output low voltage	IOL = 2.1 mA, 2.2 V ≤ V_{DDSPD} ≤ 3.6 V	--	0.4	V
		IOL = 0.7 mA, V_{DDSPD} = 1.7 V	--	0.2	V
V_{HYST}[1]	Input hysteresis	V_{DDSPD} < 2.2V	0.10 * V_{DDSPD}	--	V
		$V_{DDSPD} \geq$ 2.2V	0.05 * V_{DDSPD}	--	V

Notes:
1. Optional.

Table 12 — DC Characteristics for EE1002A

Symbol	Parameter	Test Condition (in addition to those in Table 8 on page 15)	Min	Max	Units
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}	--	±2	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SSSPD}$ or V_{DDSPD}, SDA in Hi-Z	--	±2	µA
I_{DD}	Supply current	$V_{DDSPD} = 3.0$ V, $f_C = 400$ kHz (rise/fall time < 30 ns)	--	TBD	mA
I_{DD1}	Standby Supply current	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, $V_{DDSPD} = 3.6$ V	--	1	µA
V_{IL}	Input low voltage (SCL, SDA, WC#)	--	-0.45	$0.3 * V_{DDSPD}$	V
V_{IH}	Input high voltage (SCL, SDA, WC#)	--	$0.7 * V_{DDSPD}$	$V_{DDSPD} + 1$	V
V_{HV}	SA0 high voltage	$V_{HV} - V_{DDSPD} \geq 4.8$ V	7	10	V
V_{OL}	Output low voltage	IOL = 2.1 mA, $3.0 \text{ V} \leq V_{DDSPD} \leq 3.6$ V	--	0.4	V
		IOL = 0.7 mA, $V_{DDSPD} = 3.0$ V	--	0.2	V

Table 13 — AC Characteristics for EE1002 and EE1002A

		$V_{DDSPD} < 2.2$ V[4]		$V_{DDSPD} \geq 2.2$ V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{SCL}	Clock frequency	10	100	10	400	kHz
t_{HIGH}	Clock pulse width high time	4000	--	600	--	ns
t_{LOW}[6]	Clock pulse width low time	4700	--	1300	--	ns
t_R[2]	SDA rise time	--	1000	20	300	ns
t_F[2]	SDA fall time	--	300	20	300	ns
$t_{SU:DAT}$	Data in setup time	250	--	100	--	ns
$t_{HD:DI}$	Data in hold time	0	--	0	--	ns
$t_{HD:DAT}$[5]	Data out hold time	200	3450	200	900	ns
$t_{SU:STA}$[1]	Start condition setup time	4700	--	600	--	ns
$t_{HD:STA}$	Start condition hold time	4000	--	600	--	ns
$t_{SU:STO}$	Stop condition setup time	4000	--	600	--	ns
t_{BUF}	Time between Stop Condition and next Start Condition	4700	--	1300	--	ns
t_W	Write time	--	10	--	10	ms

Note 1: For a reSTART condition, or following a write cycle
Note 2: Guaranteed by design and characterization, not necessarily tested
Note 3: To avoid spurious START and STOP conditions, a minimum delay is placed between falling edge of SCL and the falling or rising edge of SDA
Note 4: V_{DDSPD} below 3.0 V only supported on EE1002, not on EE1002A.
Note 5: This specification may conflict with SMBus timing specifications.
Note 6: EE1002 family devices shall not initiate clock stretching, which is an optional I^2C bus feature.
Note 7: EE1002 family devices are not required to support the SMBus timeout feature.

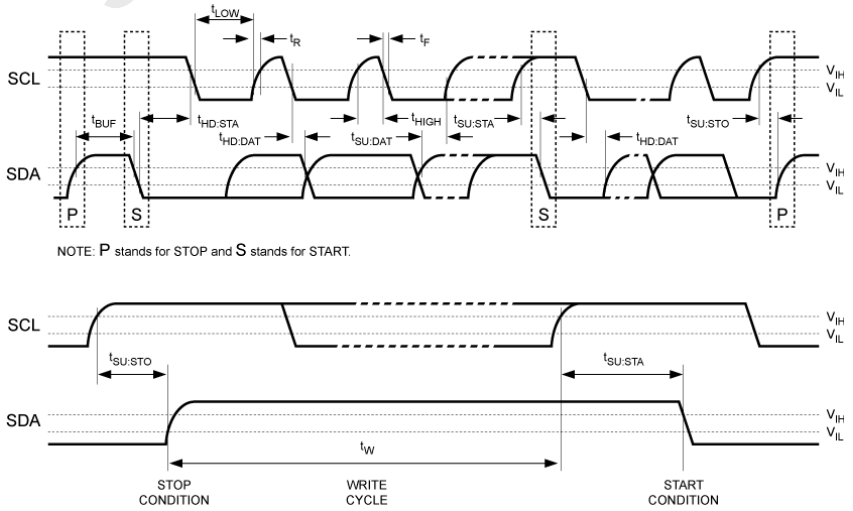


Figure 10 — AC Waveforms

3. PACKAGING OPTIONS

PSON-8. 8-lead plastic small outline no lead package outline (MO-229; 2x3 mm = variation V/WCED-3, 3x3 mm = variation V/WEED-7)

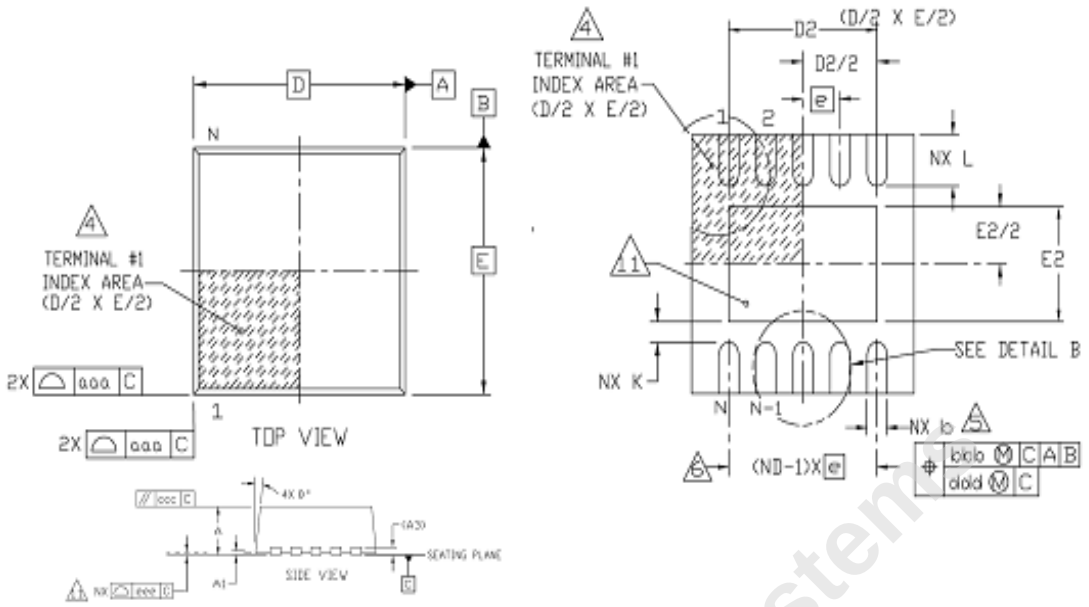
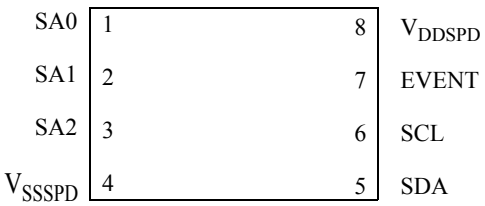


Figure 11 — PSON-8 Package Outline

Table 14 — PSON-8 Critical Package Dimensions

Symbol	Min	Typ	Max	Units	Notes
A	>0.80	0.90	1.00	mm	Var. V
A	0.70	0.75	0.80	mm	Var. W
D	--	2.00	--	mm	Basic, Var. V/ WCED-3
D	--	3.00	--	mm	Basic, Var. V/ WEED-7
D2	1.20	--	1.60	mm	
E	--	3.00	--	mm	Basic
E2	1.20	--	1.60	mm	
L	0.30	--	0.45	mm	
K	0.20	--	--	mm	
N	8			Leads	

Device Pinout



TSSOP-8 8-lead thin shrink small outline package outline

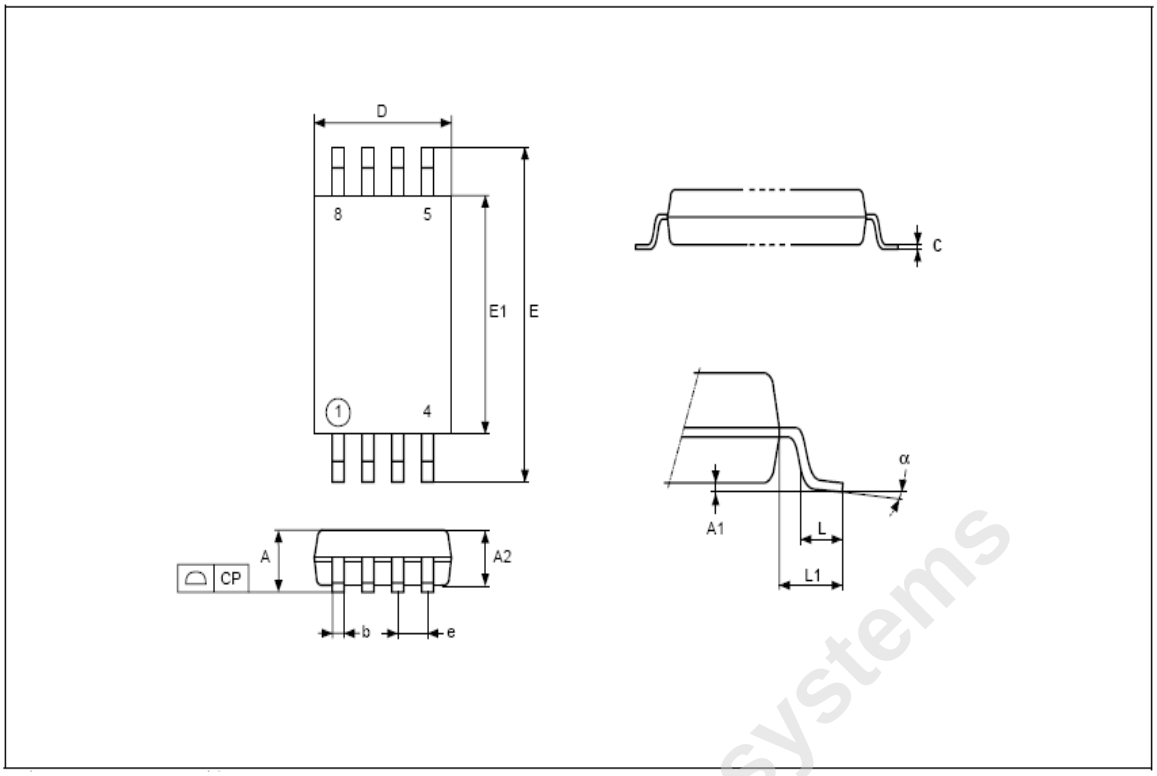
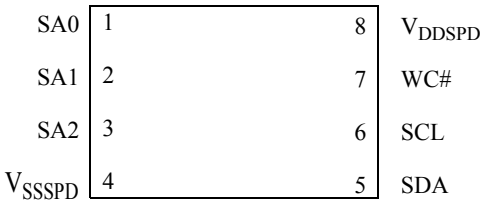


Figure 12 — TSSOP-8 Package Outline

Table 15 — TSSOP-8 Package Dimensions

Symbol	Min	Typ	Max	Units
A	--	--	1.20	mm
A1	0.50	--	0.15	mm
A2	0.80	1.00	1.05	mm
b	0.19	--	0.30	mm
c	0.09	--	0.20	mm
CP	--	--	1.00	mm
D	2.90	3.00	3.10	mm
e	--	0.65	--	mm
E	6.20	6.40	6.60	mm
E1	4.30	4.40	4.50	mm
L	0.45	0.60	0.75	mm
L1	--	1.00	--	mm
α	0	--	8	degrees
N	8			Leads

Device Pinout



SOIC-8 8-lead ultra thin fine pitch dual flat package no lead 5x6 mm package outline

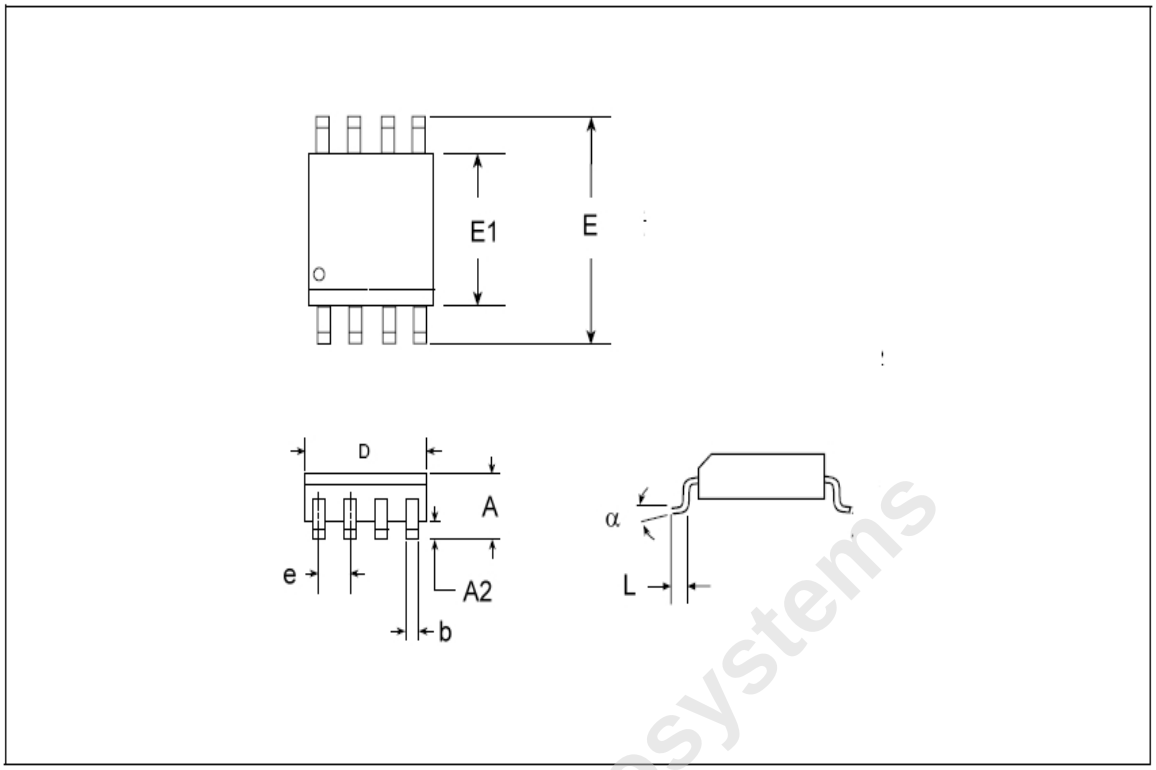
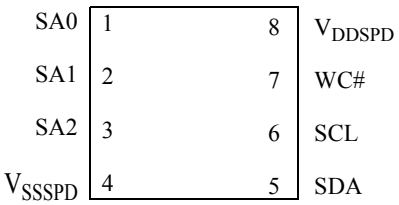


Figure 13 — SOIC-8 Package Outline

Table 16 — SOIC-8 Package Dimensions

Symbol	Min	Typ	Max	Units
A	1.35	1.55	1.75	mm
A2	0.10	--	0.25	mm
D	4.80	--	5.00	mm
E	5.80	6.00	6.20	mm
E1	3.80	--	4.00	mm
b	0.33	--	0.51	mm
e	--	1.27	--	mm
L	0.40	0.45	0.50	mm
α	0	--	8	degrees
N	8			Leads

Device Pinout



MSOP-8 8-lead micro small outline 3x3 mm package outline

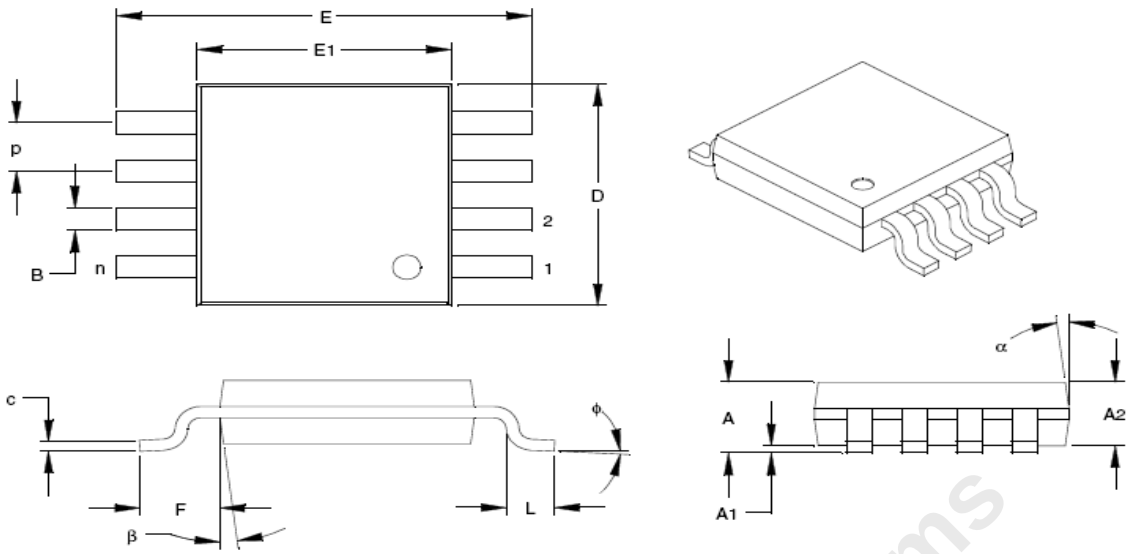
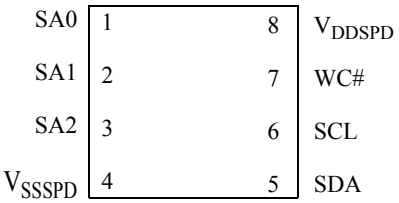


Figure 14 — MSOP-8 Package Outline

Table 17 — MSOP-8 Package Dimensions

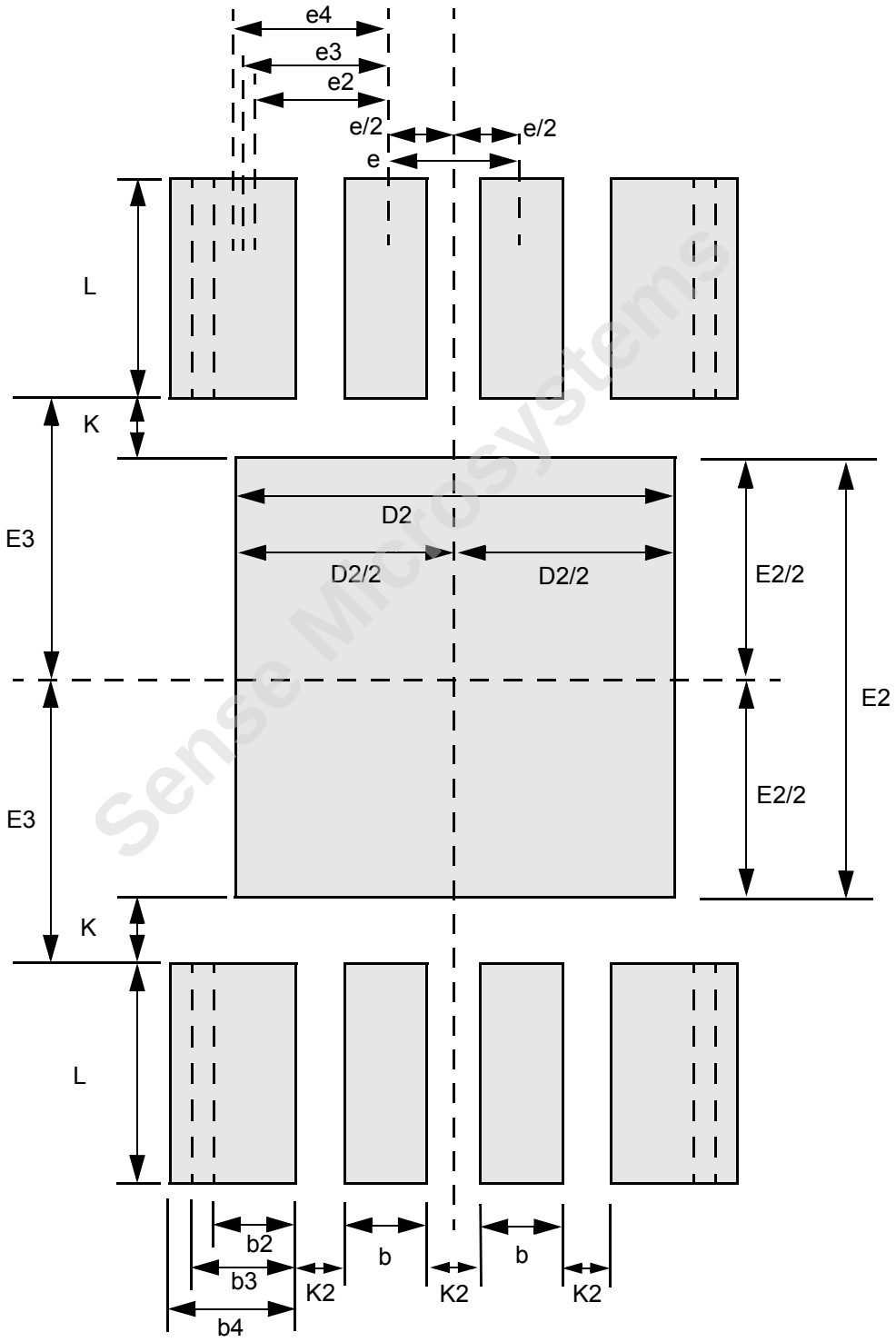
Symbol	Min	Typ	Max	Units
A	--	--	1.10	mm
A1	0	--	0.15	mm
E	--	4.90	--	mm
E1	--	3.00	--	mm
D	--	3.00	--	mm
L	0.40	0.60	0.80	mm
F	--	0.95	--	mm
c	0.08	--	0.23	mm
B	0.22	--	0.40	mm
Φ	0	--	8	degrees
α	0	--	8	degrees
β	5	--	15	degrees
n	8			Leads

Device Pinout



SPD Common Landing Pattern

The common landing pattern recommendations for the PSON packaged SPD (EE1002 compatible) or SPD with Thermal Sensor (TSE2002 compatible) are parameterized to allow for routing design constraints. These apply to the use of devices following MO-229 variations
V/WCED-3 and V/WEED-7. The preferred implementation with wide corner pads enhances device centering during assembly, but two narrower options are defined for modules with tight routing requirements. This is included for reference only; please refer to JESD21C-4.1.2 for details.



The table lists three variations of landing pattern implementations, ranked as “Preferred”, “Intermediate”, and “Minimum Acceptable”.

TABLE 18. Parameters for SPD Common Landing Pattern

Parameter	Description	Dimension			Notes
		Min	Nom	Max	
D2	Heat paddle width	1.40	-	1.60	
E2	Heat paddle height	1.40	-	1.60	
E3	Heat paddle centerline to contact inner locus	1.00	-	1.05	
L	Contact length	0.70	-	0.80	
K	Heat paddle to contact keepout	0.20	-	-	
K2	Contact to contact keepout	0.20	-	-	
e	Contact centerline to contact centerline pitch for inner contacts	-	0.50	-	
b	Contact width for inner contacts	0.25	-	0.30	
e2	Landing pattern centerline to outer contact centerline, “minimum acceptable” option	-	0.50	-	1
b2	Corner contact width, “minimum acceptable” option	0.25	-	0.30	1
e3	Inner contact centerline to outer contact centerline, “intermediate” option	-	0.55	-	2
b3	Corner contact width, “intermediate” option	0.35	-	0.40	2
e4	Landing pattern centerline to outer contact centerline, “preferred” option	-	0.60	-	3
b4	Corner contact width, “preferred” option	0.45	-	0.50	3

Notes:
1. Minimum acceptable option to be used when routing prevents preferred or intermediate width contact.
2. Intermediate option to be used when routing prevents preferred width contact.
3. Preferred option to be used when possible.