AN 26.18

Configuration Options for the USB253x / USB3x13 / USB46x4

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INTRODUCTION

The SMBus slave interface can be used to customize the functionality of the USB253x / USB3x13 / USB46x4 hub. Through this interface, the SOC is able to control the digital and USB lines for internal testing, configure the Hub to function with the desired options when enumerating, and load custom firmware to fully unlock the features of the embedded processor. This functionality entails that some configuration registers are accessible only during the configuration stages, while others are accessible during runtime. Both sets of registers are detailed in this application note.

This document includes the following topics:

References

The following documents should be referenced when using this application note. Contact your Microchip representative for availability.

USB2532 Data Sheet

USB2533 Data Sheet

USB2534 Data Sheet

USB3613 Data Sheet

USB3813 Data Sheet

USB4604 Data Sheet

USB4624 Data Sheet

Protouch Configuration Tool

USB2530 Software Development Kit

System Management Bus Specification, Version 1.0

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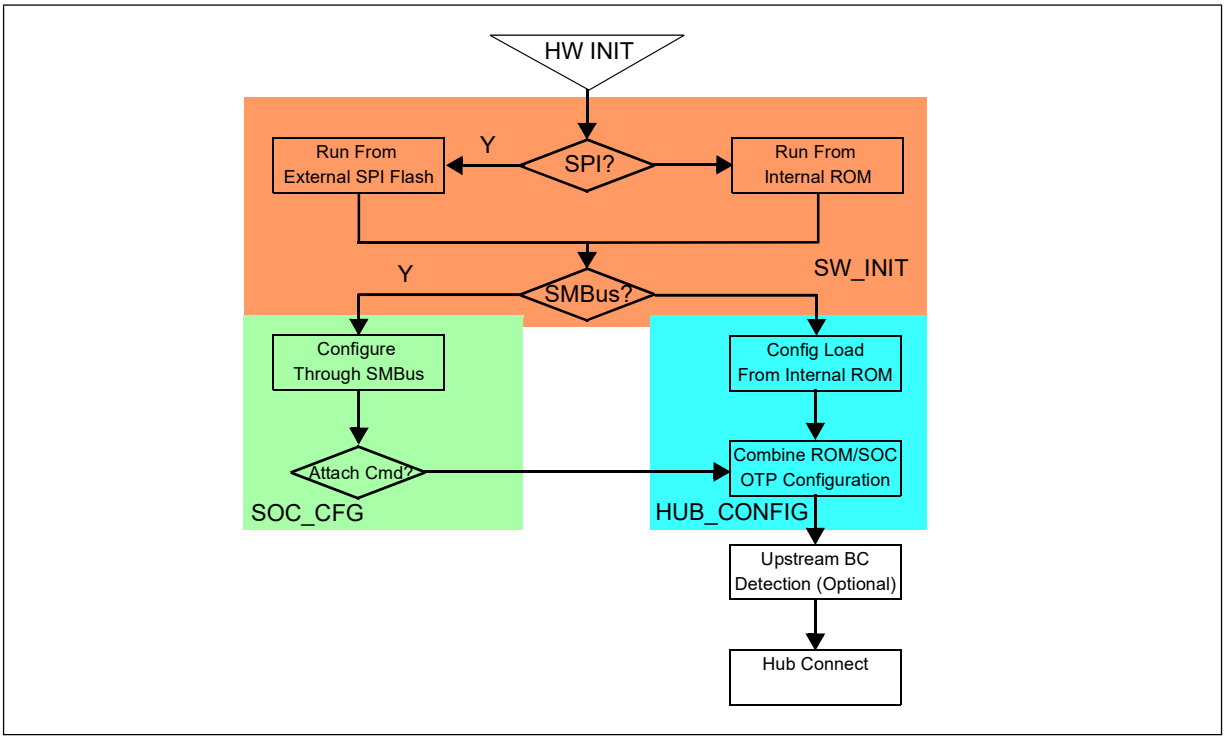
1.0 HUB OPERATIONAL MODE

1.1 Hub Configuration Stages

The Controller Hub is configured in three stages. The **SOC Configuration Stage** is executed through the SMBus interface. The hub also is configured from the internal OTP registers through the **Hub Configuration Stage** and finally during the **Hub Connect Stage**. The diagram below shows how these stages flow:

FIGURE 1: HUB OPERATIONAL MODE FLOWCHART



Note:	Because the OTP Configuration registers are loaded after the SOC_CFG stage, it is possible for configuration registers modified in the SOC_CFG stage to be overwritten in the HUB_CONFIG stage.

1.2 SMBus Protocol

The SMBus protocol is a flexible 2-pin serial protocol used for low speed communication between integrated circuits. The protocol consists of a SMBCLK pin generated by the SMBus Master and a bi-directional SMBDATA pin that can be driven by a Master or a Slave. The bus requires a pull-up resistor on both SMBCLK and SMBDATA to function. The hub configure the pins as Open/Drain buffers where the driver will either tristate the pin or drive the pin to ground. The input threshold for the high level ranges from 1.2V to 3.3V, allowing the Hub to communicate with a large sample of SOCs on the market. Refer to the System Management Bus Specification for more details on the timing specifications of the bus.

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2.0 SOC CONFIGURATION STAGE

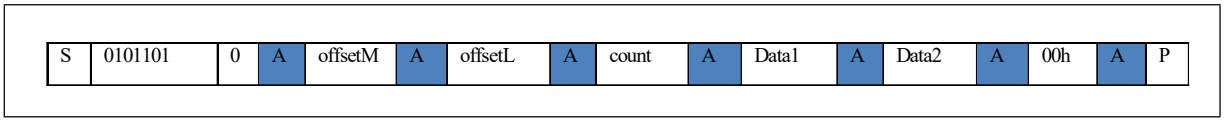
The first stage where the SMBus interface is active is the **SOC Configuration Stage**. In this stage, the SOC may modify any of the configuration settings to customize the Hub to their purposes. The SOC can configure the hub as Full Speed only, or have the Hub report a port as non-removable. The SOC can also disable a port entirely to conserve power. The hub can be addressed at the address ***2Dh*** and interprets the data bytes as shown in the following sub-sections:

Note:	If more than one hub is on the same SMBus, additional hubs may be held in reset while the initial hub is being configured.

2.1 SMBus Block Write

The SMBus block write consists of an Address+Direction(0) byte followed by the 16-bit memory address, split into two bytes. The address is used for special commands as well as a pointer to the hubs internal memory. After the address, the next byte of data is the count of data bytes that will follow, up to 128 bytes in a block. Finally, a write of 00h is used to terminate the write operation followed by the SMBus stop signal.

FIGURE 2: SMBUS BLOCK WRITE

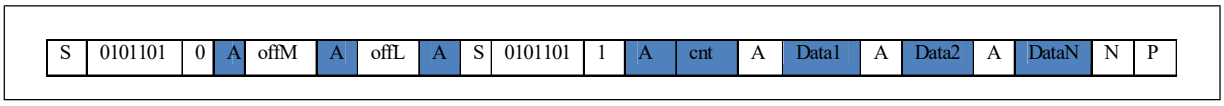


Note:	The 7-bit address of the hub is ***2Dh***. Or the first byte is ***5Ah*** for an SMBus Write.

2.2 SMBus Block Read

The SMBus block read consists of an Address+Direction(0) byte with the 16-bit memory address followed by a repeat Start signal and an Address+Direction(1) byte. The hub will then start to output the count (128 bytes) and the contents of the internal registers starting at the 16-bit address specified.

FIGURE 3: SMBUS BLOCK READ



Note:	The 7-bit address of the hub is ***2Dh.*** Or the first byte is ***5Ah*** for a write and ***5Bh*** for a read.

2.3 Special Commands

There are special commands that can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the configuration registers, or simply reset the device. The commands consist of the 16-bit command followed by a 00h byte to terminate the command.

TABLE 1: SPECIAL SMBUS COMMANDS

Operation	OPCODE	Description
Configuration Register Access	9937h	Read and Write Configuration Registers
USB Attach	AA55h	Exit SOC_CONFIG and Enter HUB_CONFIG Stage
OTP Program	9933h	Permanently program configuration commands to the OTP
OTP Read	9934h	Read the values of the OTP register

Note:	OTP Program and OTP Read commands reference data starting at configuration register 4800h.

2.4 Accessing Configuration Registers

The Configuration Register Access command allows the SMBus Master to read or write to the internal registers of the hub. When the Configuration Register Access command is sent, the hub will interpret the memory starting at offset 00h as follows:

TABLE 2: MEMORY FORMAT FOR CONFIGURATION REGISTER ACCESS

RAM Address	Description	Notes
0000h	Direction	0 = Register Write, 1 = Register Read.
0001h	Data Length	Number of bytes to Read/Write when executing the command.
0002h	Configuration Address MSB	The upper byte of the 16-bit configuration register address.
0003h	Configuration Address LSB	The lower byte of the 16-bit configuration register address.
0004h	Data1	The first byte of data to write to or read from the Configuration Address.
0004h+N	DataN	The Nth byte of data to write to or read from the Configuration Address, N is equal to the Data Length.

2.4.1 CONFIGURATION REGISTER WRITE EXAMPLE

To write to a configuration register, there are two steps that must to be followed:

1. Write data to the memory.
2. Execute the special Configuration Register Access command.

The following example shows how the SMBus messages will be formatted to set the VID of the hub to a custom value of 1234h.

1. Write data to the memory of the hub:

TABLE 3: EXAMPLE SMBUS WRITE COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	06h	Number of bytes to write to memory.
4	00h	Write Configuration Register.
5	02h	Writing two data bytes.
6	30h	VID is in register **30**00h.
7	00h	VID is in register 30**00**h.
8	34h	LSB of Vendor ID 12**34**h.
9	12h	MSB of Vendor ID **12**34h.

2. Execute the Configuration Register Access command:

TABLE 4: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit.
1	99h	Command **99**37h.
2	37h	Command 99**37**h.
3	00h	Command Completion.

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2.4.2 CONFIGURATION REGISTER READ EXAMPLE

Reading configuration registers is a three stage process:

1. Write data to the memory.
2. Execute the Configuration Register Access command.
3. Read data from the memory.

The following example shows how to read the Charger Detection register to determine what type of charger the hub has connected to:

1. Write data to the memory of the hub:

TABLE 5: EXAMPLE SMBUS WRITE COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	04h	Number of bytes to write to memory.
4	01h	Read Configuration Register.
5	01h	Reading one data bytes.
6	30h	BC Detect is in register **30**E2h.
7	E2h	BC Detect is in register 30**E2**h.

2. Execute the Configuration Register Access command:

TABLE 6: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit.
1	99h	Command **99**37h.
2	37h	Command 99**37**h.
3	00h	Command Completion.

3. Read back data starting at memory offset 04h, which is where the Data byte starts:

TABLE 7: EXAMPLE SMBUS READ COMMAND

Byte	Value	Comments
0	5Ah	Address plus Write bit.
1	00h	Memory Address **00**04h.
2	04h	Memory Address 00**04**h.
3	5Bh	Address plus Read bit.
4	80h	Device sends 128 bytes of data.
5	56h	Charging Downstream Port Detected.

Note: Although the device can send out 128 bytes of memory data, it isn't necessary to read the entire set; the SMBus Master can send a stop at any time.

2.5 Configuration Registers

Below is the list of configuration registers and their address.

TABLE 8: CONFIGURATION REGISTER MEMORY MAP

ADDR	R/W	Name	Function	
0806h	R/W	LED0_PIO0_CTL1	LED0/PIO0 Register 1	
0807h	R/W	LED0_PIO0_CTL2	LED0/PIO0 Register 2	
0808h	R/W	LED1_PIO1_CTL1	LED1/PIO1 Register 1	
0809h	R/W	LED1_PIO1_CTL2	LED1/PIO1 Register 2	
080Ah	R/W	UTIL_CONFIG1	Utility Configuration Register 1	
082Dh	R/W	PIO_16_23_PD	PIO 16-23 Pull-Down Register	PIO Pin Numbers
082Eh	R/W	PIO_8_15_PD	PIO 8-15 Pull-Down Register	
082Fh	R/W	PIO_0_7_PD	PIO 0-7 Pull-Down Register	
0831h	R/W	PIO_16_23_DIR	PIO 16-23 Direction Register	
0832h	R/W	PIO_8_15_DIR	PIO 8-15 Direction Register	
0833h	R/W	PIO_0_7_DIR	PIO 0-7 Direction Register	
0835h	R/W	PIO_16_23_OUT	PIO 16-23 Output Register	
0836h	R/W	PIO_8_15_OUT	PIO 8-15 Output Register	
0837h	R/W	PIO_0_7_OUT	PIO 0-7 Output Register	
0839h	R/W	PIO_16_23_IN	PIO 16-23 Input Register	
083Ah	R/W	PIO_8_15_IN	PIO 8-15 Input Register	
083Bh	R/W	PIO_0_7_IN	PIO 0-7 Input Register	
083Dh	R/W	PIO_16_23_PU	PIO 16-23 Pull Up Register	
083Eh	R/W	PIO_8_15_PU	PIO 8-15 Pull Up Register	
083Fh	R/W	PIO_0_7_PU	PIO 0-7 Pull Up Register	
092Eh	R/W	PIO_40_47_PD	PIO 40-47 Pull Down Register	
0932h	R/W	PIO_40_47_DIR	PIO 40-47 Direction Register	
0936h	R/W	PIO_40_47_OUT	PIO 40-47 Output Register	
093Ah	R/W	PIO_40_47_IN	PIO 40-47 Input Register	
093Eh	R/W	PIO_40_47_PU	PIO 40-47 Pull Up Register	
0954h	R/W	I2C_CTL	Vendor ID LSB	
3000h	R/W	VIDL	Vendor ID LSB	
3001h	R/W	VIDM	Vendor ID MSB	
3002h	R/W	PIDL	Product ID LSB	
3003h	R/W	PIDM	Product ID MSB	
3004h	R/W	DIDL	Device ID LSB	
3005h	R/W	DIDM	Device ID MSB	
3006h	R/W	HUB_CFG1	Hub Configuration Data Byte 1	
3007h	R/W	HUB_CFG2	Hub Configuration Data Byte 2	
3008h	R/W	HUB_CFG3	Hub Configuration Data Byte 3	
3009h	R/W	NRD	Non-Removable Device	
300Ah	R/W	PDS	Port Disable for Self Powered Operation	
300Bh	R/W	PDB	Port Disable for Bus Powered Operation	
300Ch	R/W	MAXPS	Max Power For Self Powered Operation	
300Dh	R/W	MAXPB	Max Power For Bus Powered Operation	
300Eh	R/W	HCMCS	Max Current For Self Powered Operation	
300Fh	R/W	HCMCB	Max Current For Bus Powered Operation	

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TABLE 8: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function
3010h	R/W	PWRT	Power-On Time Register
3011h	R/W	LANG_ID_H	Language ID High Register
3012h	R/W	LANG_ID_L	Language ID Low Register
3013h	R/W	MFR_STR_LEN	Manufacturer String Length Register
3014h	R/W	PRD_STR_LEN	Product String Length Register
3015h	R/W	SER_STR_LEN	Serial String Length Register
3016h-30CFh	R/W	STRINGS	Manufacturer + Product + Serial Strings
30E2h	R/W	UP_BC_DET	Battery Charger Detection Register
30E3h	R/W	UP_CUST_BC_CTL	Upstream Custom Battery Charger Control
30E4h	R	UP_CUST_BC_STAT	Upstream Custom Battery Charger Status
30E5h	R	PORT_PWR_STAT	Port Power Status
30E6h	R	OCS_STAT	Over Current Status
30E8h	R/W	SP_INT_STATUS	Serial Port Interrupt Status
30E9h	R/W	SP_INT_MSK	Serial Port Interrupt Mask
30ECh	R/W	BC_CHG_MODE	Upstream Battery Charger Mode Register
30EDh	R/W	BC_CHG_DET_MSK	Charge Detect Mask Register
30EEh	R/W	CFGP	Configure Portable Hub Register
30FAh	R/W	PRTSP	Hub Port Swap Register
30FBh	R/W	HUB_PRT_REMAP_12	Hub Port Remap12 Register
30FCh	R/W	HUB_PRT_REMAP_34	Hub Port Remap34 Register
30FDh	R/W	HUB_CTRL_REMAP	HUB Controller Remap Register
30FFh	R/W	STCD	Hub Status/Command Register
3104h	R/W	USB2_HUB_CTL	USB2 Hub Control
3108h	R/W	USB2_BCDUSB_M	USB2 Version Number MSB
3109h	R/W	USB2_BCDUSB_L	USB2 Version Number LSB
3114h	R/W	USB2_BOS_LEN	USB2 BOS Descriptor Length
3120h	R/W	USB2_BOS_ARRAY	USB2 BOS Descriptor Array
318Bh	R/W	PSELSUSP	OCS Port Select Register
318Eh	R/W	CONNECTCFG	Connect Configuration Register
3191h	R/W	GLOBAL_RESUME	Global Resume Timing Register 3
3192h	R/W	GLOBAL_RESUME	Global Resume Timing Register 2
3193h	R/W	GLOBAL_RESUME	Global Resume Timing Register 1
31FFh	R/W	STCD	Remap of 30FFh
3C00h	R/W	PORT_CFG_SEL_1	PORT1 Port power select
3C04h	R/W	PORT_CFG_SEL_2	PORT2 Port power select
3C08h	R/W	PORT_CFG_SEL_3	PORT3 Port power select
3C0Ch	R/W	PORT_CFG_SEL_4	PORT4 Port power select
3C20h	R/W	USB_OCS_SEL_1	USB Port1 OCS Source Select
3C24h	R/W	USB_OCS_SEL_2	USB Port2 OCS Source Select
3C28h	R/W	USB_OCS_SEL_3	USB Port 3 OCS Source Select
3C2Ch	R/W	USB_OCS_SEL_4	USB Port 4 OCS Source Select
3C40h	R/W	VBUS_PASS_THRU	USB Port 4 OCS Source Select
3C51h	R/W	INT_N_BYPASS	INT_N_Bypass Control
3C52h	R/W	SUSP_SEL	SUSPEND Select

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TABLE 8: CONFIGURATION REGISTER MEMORY MAP (CONTINUED)

ADDR	R/W	Name	Function
4130h	R/W	INTERNAL_PORT	Internal Hub Controller Enumeration Control
413Ch	R/W	BC_CFG_P1	Port 1 Battery Charging Configuration
413Dh	R/W	BC_CFG_P2	Port 2 Battery Charging Configuration
413Eh	R/W	BC_CFG_P3	Port 3 Battery Charging Configuration
413Fh	R/W	BC_CFG_P4	Port 4 Battery Charging Configuration
4194h-4292h	R/W	HUB_CON_STRING (255 bytes)	Hub Controller string descriptor formatted as per the USB specification string descriptor requirements. Includes language ID, manufacturer, and product strings.
42ACh	R/W	bcdUSB	Hub Controller USB Specification version LSB
42ADh	R/W		Hub Controller USB Specification version MSB
42B2h	R/W	idVendor	Hub Controller VID LSB
42B3h	R/W		Hub Controller VID MSB
42B4h	R/W	idProduct	Hub Controller PID LSB
42B5h	R/W		Hub Controller PID MSB
42B6h	R/W	bcdDevice	Hub Controller Device BCD LSB
42B7h	R/W		Hub Controller Device BCD MSB
42B8h	R/W	iManufacturer	Hub Controller Manufacturer string index (00-disable, 01-enable)
42B9h	R/W	iProduct	Hub Controller Product string index (00-disable, 02-enable)
60CAh	R/W	HS_UP_BOOST	USB Upstream Boost Register
60CCh	R/W	HS_UP_SENSE	USB Upstream VariSense Register
6141h	R/W	HSIC_UP_CTL	HSIC Upstream Control Register
64CAh	R/W	HS_P1_BOOST	USB Port 1 Boost Register
64CCh	R/W	HS_P1_SENSE	USB Port 1 VariSense Register
6541h	R/W	HSIC_P1_CTL	HSIC Port 1 Control Register
6643h	R/W	HSIC_P1_CFG	HSIC Port 1 Configuration Register
68CAh	R/W	HS_UP_BOOST	USB Port 2 Boost Register
68CCh	R/W	HS_UP_SENSE	USB Port 2 VariSense Register
6941h	R/W	HSIC_P2_CTL	HSIC Port 2 Control Register
6A43h	R/W	HSIC_P2_CFG	HSIC Port 2 Configuration Register
6CCAh	R/W	HS_P3_BOOST	USB Port 3 Boost Register
6CCCh	R/W	HS_P3_SENSE	USB Port 3 Varisense Register
6D41h	R/W	HSIC_P3_CTL	HSIC Port 3 Control Register
6E43h	R/W	HSIC_P3_CFG	HSIC Port 3 Configuration Register
70CAh	R/W	HS_P4_BOOST	USB Port 4 Boost Register
70CCh	R/W	HS_P4_SENSE	USB Port 4 Varisense Register
7141h	R/W	HSIC_P4_CTL	HSIC Port 4 Control Register
7243h	R/W	HSIC_P4_CFG	HSIC Port 4 Configuration Register

Note: Status registers do not have a default value because the status can change depending on system conditions.

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2.5.1 DEFAULT VALUES

The default values of the registers will vary based on the catalog part number. Below are the default values for each part:

TABLE 9: REGISTER DEFAULT VALUES

ADDR	USB2532	USB2533	USB2534	USB3613	USB3813	USB4604	USB4624
0806h	00h	00h	00h	00h	00h	00h	00h
0807h	00h	00h	00h	00h	00h	00h	00h
0808h	00h	00h	00h	00h	00h	00h	00h
0809h	00h	00h	00h	00h	00h	00h	00h
080Ah	00h	00h	00h	00h	00h	00h	00h
082Dh	00h	00h	00h	00h	00h	00h	00h
082Eh	07h	07h	07h	47h	47h	07h	07h
082Fh	3Bh	3Bh	3Bh	3Bh	3Bh	3Bh	3Bh
0831h	00h	00h	00h	00h	00h	00h	00h
0832h	00h	00h	00h	00h	00h	00h	00h
0833h	00h	00h	00h	00h	00h	00h	00h
0835h	00h	00h	00h	00h	00h	00h	00h
0836h	0Fh	0Fh	0Fh	0Fh	0Fh	0Fh	0Fh
0837h	00h	00h	00h	00h	00h	00h	00h
0839h	1Fh	1Fh	1Fh	1Fh	1Fh	1Eh	1Eh
083Ah	05h	05h	05h	01h	01h	00h	00h
083Bh	3Ch	3Ch	3Ch	FCh	FCh	04h	04h
083Dh	1Eh	1Eh	1Eh	00h	00h	1Eh	1Eh
083Eh	00h	00h	00h	00h	00h	00h	00h
083Fh	00h	00h	00h	00h	00h	00h	00h
092Eh	00h	00h	00h	00h	00h	00h	00h
0932h	00h	00h	00h	00h	00h	00h	00h
0936h	00h	00h	00h	00h	00h	00h	00h
093Ah	3Eh	3Eh	3Eh	20h	20h	3Eh	3Eh
093Eh	00h	00h	00h	00h	00h	00h	00h
3000h	24h	24h	24h	24h	24h	24h	24h
3001h	04h	04h	04h	04h	04h	04h	04h
3002h	34h	34h	34h	13h	13h	04h	24h
3003h	25h	25h	25h	36h	38h	46h	46h
3004h	16h	16h	16h	16h	16h	16h	16h
3005h	01h	01h	01h	01h	01h	01h	01h
3006h	9Bh	9Bh	9Bh	98h	98h	9Bh	9Bh
3007h	22h	22h	22h	20h	20h	20h	20h
3008h	08h	08h	08h	08h	08h	08h	08h
3009h	0Eh	0Eh	0Eh	00h	00h	00h	00h
300Ah	00h	00h	00h	10h	10h	00h	00h
300Bh	00h	00h	00h	10h	10h	00h	00h
300Ch	01h	01h	01h	01h	01h	01h	01h
300Dh	50h	50h	50h	50h	50h	50h	50h
300Eh	01h	01h	01h	01h	01h	01h	01h
300Fh	50h	50h	50h	50h	50h	50h	50h
3010h	32h	32h	32h	32h	32h	32h	32h

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TABLE 9: REGISTER DEFAULT VALUES (CONTINUED)

ADDR	USB2532	USB2533	USB2534	USB3613	USB3813	USB4604	USB4624
3011h	00h	00h	00h	00h	00h	00h	00h
3012h	00h	00h	00h	00h	00h	00h	00h
3013h	00h	00h	00h	00h	00h	00h	00h
3014h	00h	00h	00h	00h	00h	00h	00h
3015h	00h	00h	00h	00h	00h	00h	00h
3016h-30CFh	00h	00h	00h	00h	00h	00h	00h
30E2h	02h	02h	02h	02h	70h	02h	02h
30E3h	00h	00h	00h	00h	00h	00h	00h
30E4h	00h	00h	00h	00h	00h	00h	00h
30E5h	00h	00h	00h	00h	00h	00h	00h
30E6h	00h	00h	00h	00h	00h	00h	00h
30E8h	00h	00h	00h	00h	00h	00h	00h
30E9h	00h	00h	00h	00h	00h	00h	00h
30ECh	00h	00h	00h	0Ch	0Ch	00h	00h
30EDh	00h	00h	00h	00h	00h	00h	00h
30EEh	00h	00h	00h	00h	00h	00h	00h
30FAh	00h	00h	00h	00h	00h	00h	00h
30FBh	21h	21h	21h	21h	21h	21h	21h
30FCh	43h	43h	43h	03h	03h	43h	43h
30FFh	00h	00h	00h	00h	00h	00h	00h
3104h	00h	00h	00h	00h	00h	00h	00h
3108h	02h	02h	02h	02h	02h	02h	02h
3109h	01h	01h	01h	01h	01h	01h	01h
318Bh	00h	00h	00h	00h	00h	00h	00h
318Eh	80h	80h	80h	80h	80h	80h	80h
3191h	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch	0Ch
3192h	D2h	D2h	D2h	D2h	D2h	D2h	D2h
3193h	90h	90h	90h	90h	90h	90h	90h
31FFh	00h	00h	00h	00h	00h	00h	00h
3C51h	00h	00h	00h	00h	00h	00h	00h
4130h	00h	00h	00h	00h	00h	00h	00h
413Ch	Note 2-1	Note 2-1	Note 2-1	Note 2-1	N/A	Note 2-1	N/A
413Dh	Note 2-1	Note 2-1	Note 2-1	Note 2-1	Note 2-1	Note 2-1	N/A
413Eh	N/A	Note 2-1	Note 2-1	N/A	Note 2-1	Note 2-1	Note 2-1
413Fh	N/A	N/A	Note 2-1	N/A	N/A	Note 2-1	Note 2-1
42B2h	00h	00h	00h	00h	00h	00h	00h
42B3h	00h	00h	00h	00h	00h	00h	00h
42B4h	00h	00h	00h	00h	00h	00h	00h
42B5h	00h	00h	00h	00h	00h	00h	00h
42B6h	00h	00h	00h	00h	00h	00h	00h
42B7h	00h	00h	00h	00h	00h	00h	00h
60CAh	00h	00h	00h	00h	00h	00h	00h
60CCh	00h	00h	00h	00h	00h	00h	00h
6141h	02h	02h	02h	06h	02h	06h	06h

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TABLE 9: REGISTER DEFAULT VALUES (CONTINUED)

ADDR	USB2532	USB2533	USB2534	USB3613	USB3813	USB4604	USB4624
64CAh	00h	00h	00h	00h	00h	00h	00h
64CCh	00h	00h	00h	10h	00h	00h	00h
6541h	02h	02h	02h	02h	06h	02h	06h
6643h	00h	00h	00h	00h	00h	00h	00h
68CAh	00h	00h	00h	00h	00h	00h	00h
68CCh	00h	00h	00h	00h	00h	00h	00h
6941h	02h	02h	02h	02h	02h	02h	06h
6A43h	00h	00h	00h	00h	00h	00h	00h
6CCAh	00h	00h	00h	00h	00h	00h	00h
6CCCh	00h	00h	00h	00h	00h	00h	00h
6D41h	02h	02h	02h	06h	02h	02h	02h
6E43h	00h	00h	00h	00h	00h	00h	00h
70CAh	00h	00h	00h	00h	00h	00h	00h
70CCh	00h	00h	00h	00h	00h	00h	00h
7141h	02h	02h	02h	02h	02h	02h	02h
7243h	00h	00h	00h	00h	00h	00h	00h

Note 2-1 Default value of D3h when BC_EN strap is enabled, otherwise 00h.

Note: Some registers may contain values that reflect the state of the external pins, so the default vale may be different than what is listed.

2.5.2 REGISTER DEFINITIONS

2.5.2.1 PIO Control

Different catalog part numbers will have different PIO pins exposed for control. Below is a chart of the digital pins used for control and their corresponding pin numbers on the USB253x and USB46x4 products. Be aware that if the pin is used as a PIO, the default functionality will be lost. Because of this, the Hub must be configured to account for the change in functionality. For example, to free up the Port Power and OCS pins, the hub can be configured in Ganged mode in register 3006h.

TABLE 10: PIO PIN NUMBERS

Pin Name	PIO	USB(8)46x4 Pin	USB253x Pin	Requirements
SUSPEND/LED0	PIO0	14	11	LED0_PIO_CTL2[0]=0, CONNECT_CFG[1]=0, SUSP_SEL[0]=0
SOF/LED1	PIO1	13	NA	LED1_PIO_CTL2[0]=0, CONNECT_CFG[1]=0, UTIL_CONFIG1[7]=0
SCL/SMBCLK	PIO2	33	N/A	I2C_CTL[1:0]=00
PIO3	PIO3	22	NA	
SPI_CLK	PIO4	27	NA	UTIL_CONFIG1[2]=1
SPI_DO/SPI_SPD_SEL	PIO5	26	NA	UTIL_CONFIG1[2]=1
PIO8	PIO8	23	NA	
SPI_DI	PIO9	24	NA	UTIL_CONFIG1[3:2]=01
PIO10	PIO10	34	NA	
VBUS_DET	PIO16	36	27	VBUS_PASS_THRU[0]=0
OCS1	PIO17	16	13	USB_OCS_SEL_1[3:0]=0000 or HUB_CFG1[2:1]=00 or HUB_CFG1[2]=1

TABLE 10: PIO PIN NUMBERS (CONTINUED)

OCS2	PIO18	20	17	USB_OCS_SEL_2[3:0]=0000 or HUB_CFG1[2:1]=00 or HUB_CFG1[2]=1
OCS3/UART_RX	PIO19	28	19	USB_OCS_SEL_3[3:0]=0000 or HUB_CFG1[2:1]=00 or HUB_CFG1[2]=1
OCS4/UART_TX	PIO20	30	21	USB_OCS_SEL_4[3:0]=0000 or HUB_CFG1[2:1]=00 or HUB_CFG1[2]=1
PRTPWR1	PIO41	15	12	PORT_CFG_SEL_1[5:0]=100000 or HUB_CFG1[0]=0
PRTPWR2	PIO42	19	16	PORT_CFG_SEL_2[5:0]=100000 or HUB_CFG1[0]=0
PRTPWR3	PIO43	21	18	PORT_CFG_SEL_3[5:0]=100000 or HUB_CFG1[0]=0
PRTPWR4	PIO44	29	20	PORT_CFG_SEL_4[5:0]=100000 or HUB_CFG1[0]=0
SDA/SMBDATA	PIO45	31	NA	I2C_CTL[1:0]=00

TABLE 11: LED0/PIO0 REGISTER 1

LED0_PIO0_CTL1 (0806h)			**LED0_PIO0 Control Register**
Bit	**Name**	**R/W**	**Description**
7	XNOR	R/W	This bit toggles the polarity of the LED output. It can be used to invert the polarity.
6	MODE	R/W	0 - Blink the LED. 1 - Breath the LED.
5:0	RATE	R/W	In Blink mode: This is the Blink Rate of LED in 50 ms increments. Duty cycle of 50%. Rate range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an active breadth in 500 ms increments.

Note: Breath mode modulates the pulse width of the output to slowly change the brightness of the connected LED. The LED will then slowly grow brighter and dimmer at the breath rate specified.

TABLE 12: LED0/PIO0 REGISTER 2

LED0_PIO0_CTL2 (0807h)			**LED0_PIO0 Control Register**
Bit	**Name**	**R/W**	**Description**
7:2	TRAILOFF_TIME	R/W	In Blink mode: Time the LED must continue blinking after LED_ON is turned off. TRAIL_TIME is in 50ms increments. Range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an sleeping in between breadths in 500 ms increments
1	LED_ON	R/W	If LED_ON is set, then start blinking or breathing this LED. Blink timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops when TRAIL_TIME expires. In Breath Mode: Breath timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops immediately.
0	LED_PIO	R/W	‘0’ = PIO0 ‘1’ = LED0

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TABLE 13: LED1/PIO1 REGISTER 1

LED1_PIO1_CTL1 (0808h)			LED1_PIO1 Control Register
Bit	**Name**	**R/W**	**Description**
7	XNOR	R/W	This bit toggles the polarity of the LED output. It can be used to invert the polarity.
6	MODE	R/W	0 - Blink the LED. 1 - Breath the LED.
5:0	RATE	R/W	In Blink mode: This is the Blink Rate of LED in 50 ms increments. Duty cycle of 50%. Rate range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an active breadth in 500 ms increments.

Note: Breath mode modulates the pulse width of the output to slowly change the brightness of the connected LED. The LED will then slowly grow brighter and dimmer at the breath rate specified.

TABLE 14: LED1/PIO1 REGISTER 2

LED1_PIO1_CTL2 (0809h)			LED1_PIO1 Control Register
Bit	**Name**	**R/W**	**Description**
7:2	TRAILOFF_TIME	R/W	In Blink mode: Time the LED must continue blinking after LED_ON is turned off. TRAIL_TIME is in 50ms increments. Range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an sleeping in between breadths in 500 ms increments
1	LED_ON	R/W	If LED_ON is set, then start blinking or breathing this LED. Blink timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops when TRAIL_TIME expires. In Breath Mode: Breath timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops immediately.
0	LED_PIO	R/W	‘0’ = PIO0 ‘1’ = LED0

TABLE 15: UTILITY CONFIGURATION REGISTER 1

UTIL_CONFIG1 (080Ah)			UTILITY CONFIGURATION REGISTER 1
Bit	**Name**	**R/W**	**Description**
7	SOF_ENABLE	R/W	When this bit is set, the SOF output is enabled. The GPIO attached to the pin is forced to be an input. The processor can monitor the bit on PIO1.
6	DEV_RESET	R/W	Setting this bit to “1”, sets all of the registers into a known state as specified in each register. This bit is cleared when the RESET process has completed.
5	TXD_SEL	R/W	When this bit is cleared to “0”, the internal PIO signal is routed to the TDO/LED/UART_TX pin. When this bit is set to “1”, internal UART_TX signal is routed to the TDO/LED/UART_TX pin. In Test Mode this bit is overridden.
4	Reserved	R/W	Always write to 0
3	RXD_SEL	R/W	When this bit is cleared to “0”, internal PIO signal is routed to the TDI/LED/UART_RX pin. When this bit is set to “1”, internal UART_RX signal is routed to the TDI/LED/UART_RX Pin.
2	SPI_MASTER_DIS	R/W	After reset the SPI interface is always enabled. If the firmware does not detect a SPI ROM externally, it sets this bit. This disables the SPI interface and enables PIO4 and PIO5.
1	Reserved	R/W	Always read 0.
0	HUB_RESUME_INHIBIT	R/W	‘0’ = Normal resume activity per the USB2.0 specification 1 = Alternate resume behavior is enabled per the descriptions in the previous section. Note: This bit has the same function as the HUB_CFG_3 bit 4. This bit is to enable the function from the USB host.

TABLE 16: PIO 16-23 PULL-DOWN REGISTER

PIO_16_23_PD (082Dh)			PIO 16-23 Pull Down Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:5	PIO[23:21]_PD	R/W	Reserved
4	PIO20_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
3	PIO19_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
2	PIO18_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
1	PIO17_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
0	PIO16_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.

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TABLE 17: PIO 8-15 PULL-DOWN REGISTER

PIO_8_15_PD (082Eh)			PIO 8-15 Pull Down Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:3	PIO[15:11]_PD	R/W	Reserved
2	PIO10_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
1	PIO9_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
0	PIO8_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.

TABLE 18: PIO 0-7 PULL-DOWN REGISTER

PIO_0_7_PD (082Fh)			PIO 0-7 Pull Down Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[7:6]_PD	R/W	Reserved
5	PIO5_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
4	PIO4_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
3	PIO3_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
2	PIO2_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
1	PIO1_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
0	PIO0_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.

TABLE 19: PIO 16-23 DIRECTION REGISTER

PIO_16_23_DIR (0831h)			PIO 16-23 Direction Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:5	PIO[23:21]_DIR	R/W	Reserved
4	PIO20_DIR	R/W	“0” = Input, “1” = Output.
3	PIO19_DIR	R/W	“0” = Input, “1” = Output.
2	PIO18_DIR	R/W	“0” = Input, “1” = Output.
1	PIO17_DIR	R/W	“0” = Input, “1” = Output.
0	PIO16_DIR	R/W	“0” = Input, “1” = Output.

TABLE 20: PIO 8-15 DIRECTION REGISTER

PIO_8_15_DIR (0832h)			PIO 8-15 Direction Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:3	PIO[15:11]_DIR	R/W	Reserved
2	PIO10_DIR	R/W	“0” = Input, “1” = Output.
1	PIO9_DIR	R/W	“0” = Input, “1” = Output.
0	PIO8_DIR	R/W	“0” = Input, “1” = Output.

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TABLE 21: PIO 0-7 DIRECTION REGISTER

PIO_0_7_DIR (0833h)			PIO 0-7 Direction Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[7:6]_DIR	R/W	Reserved
5	PIO5_DIR	R/W	“0” = Input, “1” = Output.
4	PIO4_DIR	R/W	“0” = Input, “1” = Output.
3	PIO3_DIR	R/W	“0” = Input, “1” = Output.
2	PIO2_DIR	R/W	“0” = Input, “1” = Output.
1	PIO1_DIR	R/W	“0” = Input, “1” = Output. [Note 2-3]
0	PIO0_DIR	R/W	“0” = Input, “1” = Output. [Note 2-2]

Note 2-2 LED_PIO bit in the LED0/PIO0 register must be set to 0 to use this bit.

Note 2-3 LED_PIO bit in the LED1/PIO1 register must be set to 0 to use this bit.

TABLE 22: PIO 16-23 OUTPUT REGISTER

PIO_16_23_OUT (0835h)			PIO 16-23 Output Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:5	PIO[23:21]_OUT	R/W	Reserved
4	PIO20_OUT	R/W	Output register data
3	PIO19_OUT	R/W	Output register data
2	PIO18_OUT	R/W	Output register data
1	PIO17_OUT	R/W	Output register data
0	PIO16_OUT	R/W	Output register data

TABLE 23: PIO 8-15 OUTPUT REGISTER

PIO_8_15_OUT (0836h)			PIO 8-15 Output Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:3	PIO[15:11]_OUT	R/W	Reserved
2	PIO10_OUT	R/W	Output register data
1	PIO9_OUT	R/W	Output register data
0	PIO8_OUT	R/W	Output register data

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TABLE 24: PIO 0-7 OUTPUT REGISTER

PIO_0_7_OUT (0837h)			PIO 0-7 Output Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[7:6]_OUT	R/W	Reserved
5	PIO5_OUT	R/W	Output register data
4	PIO4_OUT	R/W	Output register data
3	PIO3_OUT	R/W	Output register data
2	PIO2_OUT	R/W	Output register data
1	PIO1_OUT	R/W	Output register data
0	PIO0_OUT	R/W	Output register data

TABLE 25: PIO 16-23 INPUT REGISTER

PIO_16_23_IN (0839h)			PIO 16-23 Input Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:5	PIO[23:21]_IN	R/W	Reserved
4	PIO20_IN	R/W	Input buffer data
3	PIO19_IN	R/W	Input buffer data
2	PIO18_IN	R/W	Input buffer data
1	PIO17_IN	R/W	Input buffer data
0	PIO16_IN	R/W	Input buffer data

TABLE 26: PIO 8-15 INPUT REGISTER

PIO_8_15_IN (083Ah)			PIO 8-15 Input Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:3	PIO[15:11]_IN	R/W	Reserved
2	PIO10_IN	R/W	Input buffer data
1	PIO9_IN	R/W	Input buffer data
0	PIO8_IN	R/W	Input buffer data

TABLE 27: PIO 0-7 INPUT REGISTER

PIO_0_7_IN (083Bh)			PIO 0-7 Input Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[7:6]_IN	R/W	Reserved.
5	PIO5_IN	R/W	Input buffer data.
4	PIO4_IN	R/W	Input buffer data.
3	PIO3_IN	R/W	Input buffer data.
2	PIO2_IN	R/W	Input buffer data.
1	PIO1_IN	R/W	Input buffer data. [Note 2-5]
0	PIO0_IN	R/W	Input buffer data. [Note 2-4

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Note 2-4 Note 1: LED_PIO bit in the LED0/PIO0 register must be set to 0 to use this bit.

Note 2-5 Note 2: LED_PIO bit in the LED1/PIO1 register must be set to 0 to use this bit.

TABLE 28: PIO 16-23 PULL UP REGISTER

PIO_16_23_PU (083Dh)			**PIO 16-23 Pull Up Register** Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:5	PIO[23:21]_PU	R/W	Reserved
4	PIO20_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
3	PIO19_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
2	PIO18_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
1	PIO17_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
0	PIO16_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.

TABLE 29: PIO 8-15 PULL UP REGISTER

PIO_8_15_PU (083Eh)			**PIO 8-15 Pull Up Register** Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:3	PIO[15:11]_PD	R/W	Reserved
2	PIO10_PD	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
1	PIO9_PD	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
0	PIO8_PD	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.

TABLE 30: PIO 0-7 PULL UP REGISTER

PIO_0_7_PU (083Fh)			**PIO 0-7 Pull Up Register** Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[7:6]_PU	R/W	Reserved
5	PIO5_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
4	PIO4_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
3	PIO3_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
2	PIO2_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
1	PIO1_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor. [Note 2-7]
0	PIO0_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor. [Note 2-6]

Note 2-6 Note 1: LED_PIO bit in the LED0/PIO0 register must be set to 0 to use this bit.

Note 2-7 Note 2: LED_PIO bit in the LED1/PIO1 register must be set to 0 to use this bit.

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TABLE 31: PIO 40-47 PULL DOWN REGISTER

PIO_40_47_PD (092Eh)			PIO 40-47 Pull Down Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[47:46]_PD	R/W	Reserved
5	PIO45_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
4	PIO44_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
3	PIO43_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
2	PIO42_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
1	PIO41_PD	R/W	“0” = Disable pull-down resistor, “1” = Enable pull-down resistor.
0	PIO40_PD	R/W	Reserved

TABLE 32: PIO 40-47 DIRECTION REGISTER

PIO_40_47_DIR (0932h)			PIO 40-47 Direction Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[47:46]_DIR	R/W	Reserved
5	PIO45_DIR	R/W	“0” = Input, “1” = Output
4	PIO44_DIR	R/W	“0” = Input, “1” = Output
3	PIO43_DIR	R/W	“0” = Input, “1” = Output
2	PIO42_DIR	R/W	“0” = Input, “1” = Output
1	PIO41_DIR	R/W	“0” = Input, “1” = Output
0	PIO40_DIR	R/W	Reserved

TABLE 33: PIO 40-47 OUTPUT REGISTER

PIO_40_47_OUT (0936h)			PIO 40-47 Output Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[47:46]_OUT	R/W	Reserved
5	PIO45_OUT	R/W	Output register data.
4	PIO44_OUT	R/W	Output register data.
3	PIO43_OUT	R/W	Output register data.
2	PIO42_OUT	R/W	Output register data.
1	PIO41_OUT	R/W	Output register data.
0	PIO40_OUT	R/W	Reserved

Note: LED_PIO bit in the LED0/PIO0 register must be set to 0 to use this bit.
LED_PIO bit in the LED1/PIO1 register must be set to 0 to use this bit.

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TABLE 34: PIO 40-47 INPUT REGISTER

PIO_40_47_IN (093Ah)			PIO 40-47 Input Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[47:46]_IN	R/W	Reserved
5	PIO45_IN	R/W	Input buffer data.
4	PIO44_IN	R/W	Input buffer data.
3	PIO43_IN	R/W	Input buffer data.
2	PIO42_IN	R/W	Input buffer data.
1	PIO41_IN	R/W	Input buffer data.
0	PIO40_IN	R/W	Reserved

TABLE 35: PIO 40-47 PULL UP REGISTER

PIO_40_47_PU (093Eh)			PIO 40-47 Pull Up Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:6	PIO[47:46]_PU	R/W	Reserved
5	PIO45_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
4	PIO44_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
3	PIO43_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
2	PIO42_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
1	PIO41_PU	R/W	“0” = Disable pull-up resistor, “1” = Enable pull-up resistor.
0	PIO40_PU	R/W	Reserved

TABLE 36: I2C CONTROL REGISTER

I2C_CTL (0954h)			I2C Control Register Refer to PIO Pin Numbers for usable PIOs
Bit	**Name**	**R/W**	**Description**
7:2	PIO[47:46]_PU	R/W	Reserved
1	HW_I2C_EN	R/W	0=Disable external I2C, 1=Enable external I2C
0	I2C_EN	R/W	0=Disable core I2C, 1=Enable core I2C

2.5.2.2 Hub Enumeration and Functionality Registers

TABLE 37: VENDOR ID LSB

VIDL (3000h)			Vendor ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	VID_LSB	R/W	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Implementors Forum).

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TABLE 38: VENDOR ID MSB

VIDM (3001h)			Vendor ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	VID_MSB	R/W	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Implementors Forum).

TABLE 39: PRODUCT ID LSB

PIDL (3002h)			Product ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	PID_LSB	R/W	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product.

TABLE 40: PRODUCT ID MSB

PIDM (3003h)			Product ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	PID_MSB	R/W	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product.

TABLE 41: DEVICE ID LSB

DIDL (3004h)			Device ID LSB
Bit	**Name**	**R/W**	**Description**
7:0	DID_LSB	R/W	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

TABLE 42: DEVICE ID MSB

DIDM (3005h)			Device ID MSB
Bit	**Name**	**R/W**	**Description**
7:0	DID_MSB	R/W	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

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TABLE 43: HUB CONFIGURATION DATA BYTE 1

HUB_CFG1 (3006h)			Hub Configuration Data Byte 1
Bit	**Name**	**R/W**	**Description**
7	SELF_BUS_PWR	R/W	Self or Bus Power: Selects between Self- and Bus-Powered operation. The Hub is either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller). When configured as a Bus-Powered device, the Microchip Hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered Microchip Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available downstream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB2.0 specifications are not violated. When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500mA of current. 0 = Bus-Powered operation. 1 = Self-Powered operation.
6	VSM_DISABLE	R/W	0 = VSM Messaging is supported 1 = VSM Messaging is disabled When VSM is disabled, all vendor specific messaging to the hub endpoint will be ignored with no ill effect.
5	HS_DISABLE	R/W	High Speed Disable: Disables the capability to attach as either a High/Full-speed device, and forces attachment as Full-speed only i.e. (no High-Speed support). 0 = High-/Full-Speed. 1 = Full-Speed-Only (High-Speed disabled!)
4	MTT_ENABLE	R/W	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT) **Note:** The host may force Single-TT mode only. 0 = single TT for all ports. 1 = one TT per port (multiple TTs supported)
3	EOP_DISABLE	R/W	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in suspend. 0 = An EOP is generated at the EOF1 point if no traffic is detected. 1 = EOP generation at EOF1 is disabled **Note:** This is normal USB operation.
2:1	CURRENT_SNS	R/W	Over Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together). The OCS source select registers need to be updated to select the OCS ganged input. 01 = Individual port-by-port. 1x = Over current sensing not supported. (must only be used with Bus-Powered configurations.)

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TABLE 43: HUB CONFIGURATION DATA BYTE 1 (CONTINUED)

HUB_CFG1 (3006h)			Hub Configuration Data Byte 1
Bit	**Name**	**R/W**	**Description**
0	PORT_PWR	R/W	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching.

TABLE 44: HUB CONFIGURATION DATA BYTE 2

HUB_CFG2 (3007h)			HUB Configuration Byte 2
Bit	**Name**	**R/W**	**Description**
7	DYNAMIC	R/W	Dynamic Power Enable: Controls the ability of the Hub to automatically change from Self-Powered operation to Bus- Powered operation if the local power source is removed or is unavailable (and from Bus-Powered to Self-Powered if the local power source is restored). **Note:** If the local power source is available, the Hub will always switch to Self-Powered operation. When Dynamic Power switching is enabled, the Hub detects the availability of a local power source by monitoring the external LOCAL_PWR pin. If the Hub detects a change in power source availability, the Hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The Hub will then re-attach to the upstream port as either a Bus-Powered Hub (if local-power is unavailable) or a Self-Powered Hub (if local power is available). 0 = No Dynamic auto-switching. (pin becomes SUSP_IND.) and the hub controller will utilize the inverse of the SELF_BUS_PWR bit for 'Hub_Status_Field' bit '0' (local power source). 1 = Dynamic Auto-switching capable. (pin becomes LOCAL_PWR) and the hub controller will utilize the LOCAL_PWR pin for 'Hub_Status_Field' bit '0' (local power source).
6	Reserved	R/W	Reserved
5:4	OC_TIMER	R/W	Over Current Timer: Over Current Timer delay. This measures the minimum pulse width for which a pulse is considered valid. 00 = 50 ns 01 = 100 ns 10 = 200 ns 11 = 400 ns
3	COMPOUND	R/W	Compound Device: Allows the OEM to indicate that the Hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a “Non-Removable Device”. **Note:** When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 = No. 1 = Yes, Hub is part of a compound device.
2:0	Reserved	R/W	Always read ‘0’

TABLE 45: HUB CONFIGURATION DATA BYTE 3

HUB_CFG3 (3008h)			HUB Configuration Byte 3
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Reserved
3	PRTMAP_EN	R/W	Port Re-Mapping enable: Selects the method used by the hub to assign port numbers and disable ports. '0' = Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as Port 'n' on the hub is reported as Port 'n' to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. '1' = Port Re-Map mode. The mode enables remapping via the registers defined below. Disable the LPM to use this feature in USB2 Hub Control.
2:1	Reserved	R/W	Always read '0'
0	STRING_EN	R/W	Enables String Descriptor Support '0' = String Support Disabled '1' = String Support Enabled

TABLE 46: NON-REMOVABLE DEVICE

NRD (3009h)			HUB Non-removable Device
Bit	**Name**	**R/W**	**Description**
7:0	NR_DEVICE	R/W	Non-Removable Device: Indicates which port(s) include non- removable devices. '0' = port is removable, '1' = port is non-removable. Informs the Host if one of the active ports has a permanent device that is nondetachable from the Hub. **Note:** The device must provide its own descriptor data. When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable. Bit 7= Reserved Bit 6= Reserved Bit 5= 1; Port 5 non-removable. (UDC20) Bit 4= 1; Port 4 non-removable. Bit 3= 1; Port 3 non-removable. Bit 2= 1; Port 2 non-removable. Bit 1= 1; Port 1 non removable. Bit 0 is Reserved, always = '0'.

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TABLE 47: PORT DISABLE FOR SELF POWERED OPERATION

PDS (300Ah)			Port Disable for Self Powered Operation
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_SP	R/W	Port Disable Self-Powered: Disables 1 or more ports. '0' = port is available, '1' = port is disabled. During Self-Powered operation, when PRTMAP_EN = 1, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= 1; Port 4 is disabled. Bit 3= 1; Port 3 is disabled. Bit 2= 1; Port 2 is disabled. Bit 1= 1; Port 1 is disabled. Bit 0 is Reserved, always = '0'

TABLE 48: PORT DISABLE FOR BUS POWERED OPERATION

PDB (300Bh)			Port Disable for Bus Powered Operation
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_BP	R/W	Port Disable Bus-Powered: Disables 1 or more ports. '0' = port is available, '1' = port is disabled. During Bus-Powered operation, when PRTMAP_EN = 1, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= 1; Port 4 is disabled. Bit 3= 1; Port 3 is disabled. Bit 2= 1; Port 2 is disabled. Bit 1= 1; Port 1 is disabled. Bit 0 is Reserved, always = '0

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TABLE 49: MAX POWER FOR SELF POWERED OPERATION

MAXPS (300Ch)			Max Current for Self Powered Operation
Bit	**Name**	**R/W**	**Description**
7:0	MAX_PWR_SP	R/W	Max Power Self Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors. **Note:** The USB2.0 Specification does not permit this value to exceed 100mA

TABLE 50: MAX POWER FOR BUS POWERED OPERATION

MAXPB (300Dh)			Max Current for BUS Powered Operation
Bit	**Name**	**R/W**	**Description**
7:0	MAX_PWR_BP	R/W	Max Power Bus Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors.

TABLE 51: MAX CURRENT FOR SELF POWERED OPERATION

HCMCS (300Eh)			Hub Controller Max Current for Self Powered Operation
Bit	**Name**	**R/W**	**Description**
7:0	HC_MAX_C_SP	R/W	Hub Controller Max Current Self-Powered: Value in 1mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self- powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The USB2.0 Specification does not permit this value to exceed 100mA

TABLE 52: MAX CURRENT FOR BUS POWERED OPERATION

HCMCB (300Fh)			Hub Controller Max Current for Bus Powered Operation
Bit	**Name**	**R/W**	**Description**
7:0	HC_MAX_C_BP	R/W	Hub Controller Max Current Bus-Powered: Value in 1mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus- powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.

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TABLE 53: POWER-ON TIME REGISTER

PWRT (3010h)			Power On Time Register
Bit	**Name**	**R/W**	**Description**
7:0	POWER_ON_TIME	R/W	Power On Time: The length of time that is takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. System software uses this value to determine how long to wait before accessing a powered-on port.

TABLE 54: LANGUAGE ID HIGH REGISTER

LANG_ID_H (3011h)			Language ID High Register
Bit	**Name**	**R/W**	**Description**
7:0	LANG_ID_H	R/W	USB LANGUAGE ID (Upper 8 bits of a 16 bit ID field)

TABLE 55: LANGUAGE ID LOW REGISTER

LANG_ID_L (3012h)			Language ID Low Register
Bit	**Name**	**R/W**	**Description**
7:0	LANG_ID_L	R/W	USB LANGUAGE ID (Lower 8 bits of a 16 bit ID field)

TABLE 56: MANUFACTURER STRING LENGTH REGISTER

MFR_STR_LEN (3013h)			Manufacturer String Length Register
Bit	**Name**	**R/W**	**Description**
7:0	MFR_STR_LEN	R/W	Manufacturer String Length The sum of the values in MFR_STRL_LEN + PROD_STR_LEN + SER_STR_LEN must be less than or equal to the 93 character storage space devoted to strings in the hub.

TABLE 57: PRODUCT STRING LENGTH REGISTER

PRD_STR_LEN (3014h)			Product String Length Register
Bit	**Name**	**R/W**	**Description**
7:0	PRD_STR_LEN	R/W	Product String Length The sum of the values in MFR_STRL_LEN + PROD_STR_LEN + SER_STR_LEN must be less than or equal to the 93 character storage space devoted to strings in the hub.

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TABLE 58: SERIAL STRING LENGTH REGISTER

SER_STR_LEN (3015h)			Serial String Length Register
Bit	**Name**	**R/W**	**Description**
7:0	SER_STR_LEN	R/W	Serial String Length The sum of the values in MFR_STRL_LEN + PROD_STR_LEN + SER_STR_LEN must be less than or equal to the 93 character storage space devoted to strings in the hub.

TABLE 59: MANUFACTURER + PRODUCT + SERIAL STRINGS

STRINGS (3016h~30CFh)			Strings Storage
Bit	**Name**	**R/W**	**Description**
7:0	STRINGS	R/W	Manufacturer String, Product String, & Serial String. UNICODE UTF-16LE per USB 2.0 Specification The total maximum size of all strings combined must be less than or equal to 93 characters (186 Bytes). The string space may be allocated in any division desired, according to the sizes in the MFR_STR_LEN, PROD_STR_LEN, and SER_STR_LEN configuration registers. The Manufacturer String is stored first starting at address 16h and is allocated twice the number of bytes as specified in MFR_STR_LEN. The Product String is stored next in the next consecutive register address after the most significant byte allocated to the Manufacturer String. It is allocated twice the number of bytes as specified in PRD_STR_LEN. The Serial String is stored last starting at the next consecutive address after the most significant byte allocated to the Product String. It is allocated twice the number of bytes as specified in SER_STR_LEN. The most significant byte of the Serial String must be stored in the register no higher than address CFh which is the end of the 186 Byte address space allocated to string storage. The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering of your selected programming tools.

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TABLE 60: BATTERY CHARGER DETECTION REGISTER

UP_BC_DET (30E2h)			Upstream Battery Charging Register
Bit	**Name**	**R/W**	**Description**
7:5	CHARGER_TYPE	R/W	Read Only. This register indicates the result of the automatic charger detection. Values reported depend on EnhancedChrgDet setting in Battery Charger Mode Register. If EnhancedChrgDet=1 000 = Charger Detection is not complete. 001 = DCP - Dedicated Charger Port 010 = CDP – Charging Downstream Port 011 = SDP – Standard Downstream Port 100 = SE1 Low Current Charger 101 = SE1 High Current Charger 110 = SE1 Super High Current Charger 111 = Charger Detection Disabled If EnhancedChrgDet=0 000 = Charger Detection is not complete. 001 = DCP/CDP – Dedicated Charger or Charging Downstream Port 010 = Reserved 011 = SDP – Standard Downstream Port 100 = SE1 Low Current Charger 101 = SE1 High Current Charger 110 = SE1 Super High Current Charger 111 = Charger Detection Disabled
4	CHGDET_ COMPLETE	R	Indicates Charger Detection has been run and is completed. This bit is negated when START_BC_DET is asserted high.
3	Reserved	R/W	Reserved for debugging
2:1	CHG_DET[1:0]	R	Indicates encoded status of what chargers or status been detected according to the settings in the chgDetMask register. It can be used to determine what current can be drawn from the upstream USB port. 00 = No selected Chargers or Status identified 01 = 100ma (VBUS detect without enumeration) 10 = 500ma (Device enumerated, Standard Port Detected) 11 = 1000+ma (Charger detected) The actual current amount for the charger will be system dependent.
0	START_CHG_DET	R/W	Manually Initiates a USB battery charger detection sequence at the time of assertion. This bit must not be set while hub is in operation. Bit is cleared automatically when the manual battery charger detection sequence is completed. This bit may be asserted either by a serial port write, or by asserting the StartBChgDet input. 0 = Write: No Effect / Read: Battery Charger Detection Sequence Completed or not run. 1 = Write: Start Battery Charger Detection / Read: Battery Charger Detection Sequence is running

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TABLE 61: UPSTREAM CUSTOM BATTERY CHARGER CONTROL

UP_CUST_BC_CTL (30E3h)			Upstream Custom Battery Charging Control
Bit	**Name**	**R/W**	**Description**
7	I2CControl	R/W	When '1' the I2C control is enabled
6	DmPulldownEn	R/W	DM 15K pull down resistor enable
5	DpPulldownEn	R/W	DP 15K pull down resistor enable
4	IdatSinkEn	R/W	I_{DAT} current sink enable
3	HostChrgEn	R/W	When '1' the charger detection connections of DP and DM are swapped. The USB signal path is not reversed.
2	VdatSrcEn	R/W	V_{DAT} voltage source enable
1	ContactDetectEn	R/W	Contact Detect Current Source Enable
0	SeRxEn	R/W	Single Ended Receiver Enable

TABLE 62: UPSTREAM CUSTOM BATTERY CHARGER STATUS

UP_CUST_BC_STAT (30E4h)			Upstream Custom Battery Charging Status
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	RxHiCurr	R	DM high current SE1 charger output. A '1' indicates that the DM signal is 600mV higher than DP. The HostChrgEn bit will swap the DP
2	DmSeRx	R	DM Single Ended Receiver Status
1	DpSeRx	R	DP Single Ended Receiver Status
0	VdatDet	R	Indicates V_{DAT}_Det comparator output

TABLE 63: PORT POWER STATUS

PORT_PWR_STAT (30E5h)			Port Power Status
Bit	**Name**	**R/W**	**Description**
7	UDC20_SUSPEND	R	Suspend indicator for the UDC20
6:5	Reserved	R	Reserved
4:1	PRTPWR[4:1]	R	Optional status to SOC indicating that power to the downstream port was enabled by the USB Host for the specified port. Not required for an embedded application. This is a read-only status bit. Actual control over port power is implemented by the USB Host, OCS register and Downstream Battery Charging logic if enabled. 0 = USB Host has not enabled port to be powered or in downstream battery charging and corresponding OCS bit has been set. 1 = USB Host has enabled port to be powered
0	Reserved	R	Reserved

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TABLE 64: OVER CURRENT STATUS

OCS_STAT (30E6h)			Port Power Status
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4:1	OCS[4:1]	R	Optional control from SOC on indicating external current monitor indicating an over-current condition on the specified port for HUB status reporting to USB host. Also resets corresponding PRTPWR status register bit. Not required for an embedded application. 0 = No Over Current Condition 1 = Over Current Condition
0	Reserved	R	Reserved

TABLE 65: SERIAL PORT INTERRUPT STATUS

SP_INT_STATUS (30E8h)			Serial Port Interrupt Status
Bit	**Name**	**R/W**	**Description**
7	Interrupt	R/W	Read: 1 = INT_N pin has been asserted low due to unmasked interrupt 0 = INT_N pin has not been asserted low due to unmasked interrupt Write: 1 = No Effect – INT_N pin and register retains its current value 0 = Negate INT_N pin high
6:5	Reserved	R	Reserved
4	HubSuspInt	R/W	Read: 1 = Hub has entered USB suspend 0 = Hub has not entered USB suspend since last HubSuspInt reset Write: 1 = No Effect 0 = Negate HubSuspInt status low
3	HubCfgInt	R/W	Read: 1 = Hub has been configured by USB Host 0 = Hub has not been configured by USB Host since last HubConfInt reset Write: 1 = No Effect 0 = Negate HubConfInt status low
2	PrtPwrInt	R/W	Read: 1 = Port Power register has been updated 0 = Port Power register has not been updated since last PrtPwrInt reset Write: 1 = No Effect 0 = Negate PrtPwrInt status low
1	ChrgDetInt	R/W	Read: 1 = CHG_DET_N bit in Charger Detect Register has been asserted low 0 = CHG_DET_N bit has not been updated since last ChrgDetInt reset Write: 1 = No Effect 0 = Negate ChrgDetInt status low

TABLE 65: SERIAL PORT INTERRUPT STATUS (CONTINUED)

SP_INT_STATUS (30E8h)			Serial Port Interrupt Status
Bit	**Name**	**R/W**	**Description**
0	ChrgDetCompInt	R/W	Read: 1 = ChrgDetComplete bit in Charger Detect Register has been asserted high 0 = ChrgDetComplete bit in Charger Detect Register has not been updated since last ChrgDetCompInt reset Write: 1 = No Effect 0 = Negate ChrgDetCompInt status low

TABLE 66: SERIAL PORT INTERRUPT MASK

SP_INT_MSK (30E9h)			Serial Port Interrupt Mask
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	HubSuspMask	R/W	1 = INT pin is asserted when Hub enters suspend 0 = INT pin is not affected by Hub entering suspend
3	HubCfgMask	R/W	1 = INT pin is asserted when Hub configured by USB Host 0 = INT pin is not affected by Hub configuration event
2	PrtPwrMask	R/W	1 = INT pin is asserted when Port Power register has been updated by USB Host 0 = INT pin is not affected by Port Power register
1	ChrgDetMask	R/W	1 = INT pin is asserted when CHG_DET bit in Charger Detect Register is asserted 0 = INT_N pin is not affected by CHG_DET_N
0	ChgDetCompMask	R/W	1 = INT pin is asserted when ChrgDetComplete bit in Charger Detect Register is asserted high 0 = INT pin is not affected by ChrgDetComplete

TABLE 67: UPSTREAM BATTERY CHARGER MODE REGISTER

BC_CHG_MODE (30ECh)			Upstream Battery Charger M ode
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Reserved
5	HoldVdat	R/W	Dead Battery V_{DAT} Detect voltage source enable. 0 = The charger detection state machine will turn off the V_{DAT} Source at the end of the charger detection routine. 1 = The charger detection state machine leave V_{DAT} Source on during Hub.Connect stage when a SDP has been detected.
4	Reserved	R	Reserved
3	SE1ChrgDet	R/W	When enabled the charger detection routine will look for the attachment of an SE1 type charger.
2	EnhancedChrgDet	R/W	When enabled the charger detection routine will reverse V_{DAT} SRC to differentiate between a CDP and a DCP.
1:0	Reserved	R	Reserved

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TABLE 68: CHARGE DETECT MASK REGISTER

BC_CHG_DET_MSK (30EDh)			Charge Detect Mask
Bit	**Name**	**R/W**	**Description**
7	CONFIGURED	R/W	If this bit is set, it indicates that the hub is configured. The charge detect bits will indicate a 500mA source. This bit will have no effect on the charge detect bits if a battery charging source is detected.
6	CONNECTED	R/W	If this bit is set, it indicates that the hub is connected. Which means a VBUS was detected. The charge detect bits will indicate a 100mA source. This bit will have no effect on the charge detect bits if a battery charging source is detected, or the CONFIGURED bit is set.
5	SUSPENDED	R/W	This is a status that is set when the hub is in suspend. This bit has no effect on charge detect encoding.
4	SE1SMask	R/W	1= *battChg.chgDet* indicates status for this mask set met when a SE1 Super High Current Charger is detected 0= *battChg.chgDet* is not affected for this mask set by detection of a SE1 Super High Current Charger
3	SE1HMask	R/W	1 = *battChg.chgDet* indicates status for this mask set met when a SE1 High Current Charger is detected 0 = *battChg.chgDet* is not affected for this mask set by detection of a SE1 High Current Charger
2	SE1LMask	R/W	1 = *battChg.chgDet* indicates status for this mask set met when a SE1 Low Current Charger is detected 0 = *battChg.chgDet* is not affected for this mask set by detection of a SE1 Low Current Charger
1	CDPMask	R/W	1 = *battChg.chgDet* indicates status for this mask set met when a CDP Charger is detected 0 = *battChg.chgDet* is not affected for this mask set by detection of a CDP Charger This mask bit should only be enabled if EnhancedChrgDet in is asserted in Table 67, “Upstream Battery Charger Mode Register,” on page 32 because without it, the charger detection is unable to identify a CDP.
0	DCPMask	R/W	1 = *battChg.chgDet* indicates status for this mask set met when a DCP Charger is detected 0 = *battChg.chgDet* is not affected for this mask set by detection of a DCP Charger

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TABLE 69: CONFIGURE PORTABLE HUB REGISTER

CFGP (30EEh)			Portable Hub Configuration Register
Bit	**Name**	**R/W**	**Description**
7	ClkSusp		1 = Force device to run internal clock even during USB suspend (will cause device to violate USB suspend current limit - intended for test or self-powered applications which require use of serial port during USB session.) 0 = Allow device to gate off its internal clocks during suspend mode in order to meet USB suspend current requirements.
6	IntSusp		1 = INT_N pin function is a level sensitive USB suspend interrupt indication. Allows system to adjust current consumption to comply with USB specification limits when hub is in the USB suspend state. 0 = INT_N pin function retains event sensitive role of a general serial port interrupt. See the USB3813 data sheet or the USB3613 data sheet for more information.
5:1	DIS_PHY_CLK[5:1]	R/W	A ‘1’ disables the PHY clock it that bit position. Bit 5 - Downstream port 5 Bit 4 - Downstream port 4 Bit 3 - Downstream port 3 Bit 2 - Downstream port 2 Bit 1 - Downstream port 1
0	Reserved	R	Always read ‘0’

TABLE 70: HUB PORT SWAP REGISTER

HUB_PRT_SWAP (30FAh)			Hub Port Swap Register
Bit	**Name**	**R/W**	**Description**
7:0	PRT_SWAP	R/W	Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. ‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 4= ‘1’: Port 4 DP/DM is Swapped. Bit 3= ‘1’: Port 3 DP/DM is Swapped. Bit 2= ‘1’: Port 2 DP/DM is Swapped. Bit 1= ‘1’: Port 1 DP/DM is Swapped. Bit 0= ‘1’: Upstream Port DP/DM is Swapped

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TABLE 71: HUB PORT REMAP12 REGISTER

HUB_PRT_REMAP_12 (30FBh)			Hub Port 1-2 Remap
Bit	**Name**	**R/W**	**Description**
7:4	PRT_2_MAP	R/W	0000 - Physical Port 2 is disabled 0001 - Physical Port 2 is mapped to Logical Port 1 0010 - Physical Port 2 is mapped to Logical Port 2 0011 - Physical Port 2 is mapped to Logical Port 3 0100 - Physical Port 2 is mapped to Logical Port 4 0101 - Physical Port 2 is mapped to Logical Port 5 0110 - 1111 Reserved, will default to 0000 value
3:0	PRT_1_MAP	R/W	0000 - Physical Port 1 is disabled 0001 - Physical Port 1 is mapped to Logical Port 1 0010 - Physical Port 1 is mapped to Logical Port 2 0011 - Physical Port 1 is mapped to Logical Port 3 0100 - Physical Port 1 is mapped to Logical Port 4 0101 - Physical Port 1 is mapped to Logical Port 5 0110 - 1111 Reserved, will default to 0000 value

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CF_3 is set.

TABLE 72: HUB PORT REMAP34 REGISTER

HUB_PRT_REMAP_34 (30FCh)			Hub Port 3-4 Remap
Bit	**Name**	**R/W**	**Description**
7:4	PRT-4_MAP	R/W	0000 - Physical Port 4 is disabled 0001 - Physical Port 4 is mapped to Logical Port 1 0010 - Physical Port 4 is mapped to Logical Port 2 0011 - Physical Port 4 is mapped to Logical Port 3 0100 - Physical Port 4 is mapped to Logical Port 4 0101 - Physical Port 4 is mapped to Logical Port 5 0110 - 1111 Reserved, will default to 0000 value
3:0	PRT-3_MAP	R/W	0000 - Physical Port 3 is disabled 0001 - Physical Port 3 is mapped to Logical Port 1 0010 - Physical Port 3 is mapped to Logical Port 2 0011 - Physical Port 3 is mapped to Logical Port 3 0100 - Physical Port 3 is mapped to Logical Port 4 0101 - Physical Port 3 is mapped to Logical Port 5 0110 - 1111 Reserved, will default to 0000 value

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 73: HUB CONTROLLER REMAP REGISTER

HUB_CTRL_REMAP (30FDh)			Hub Controller Remap
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:0	HUB CTRL_MAP	R/W	0000 - Hub Controller is disabled 0001 - Hub Controller is mapped to Logical Port 1 0010 - Hub Controller is mapped to Logical Port 2 0011 - Hub Controller is mapped to Logical Port 3 0100 - Hub Controller is mapped to Logical Port 4 0101 - Hub Controller is mapped to Logical Port 5 0110 - 1111 Reserved, will default to 0000 value

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 74: HUB STATUS/COMMAND REGISTER

STCD (30FFh)			Hub Command and Status Register
Bit	**Name**	**R/W**	**Description**
7:5	PAGE_SEL	R/W	Select the accessible address space: 000 = Select registers in the Pg1 Space 010 = Select registers in the Pg2 Space 110 = Select registers in the Pg3 Space
4:3	Reserved	R/W	Reserved. Software must never write a ‘1’ to these bits.
2	INTFW_PW_DN	R/W	Disable the hub configuration register access by disabling the clock running its configuration space. 0 = Hub configuration register access is enabled and hub configuration clock is running. 1 = Hub configuration register access is disabled and hub configuration clock is stopped. **Note:** This bit is write once and is only cleared by assertion of the external RESET_N pin
1	RESET	R/W	Reset the internal memory back to nRESET assertion default settings. **Note:** During this reset, this bit is automatically cleared to its default value of 0. 0 = Normal Run/Idle State. 1 = Force a reset of the registers to their default state.
0	Reserved	R/W	Reserved

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TABLE 75: USB2 HUB CONTROL

USB2_HUB_CTL (3104h)			USB2 Hub Control
Bit	**Name**	**R/W**	**Description**
7:4	HIRD	R	Host Initiated Resume Duration. This is a direct read of the Host Initiated Resume Duration sent by the USB2 Host. This field indicates the minimum amount of time the host will drive the K-state during a resume. A value 0000b equals 50uS and each additional increment adds 75uS.
3:2	Reserved	R	Reserved for future use
1	LPM_DISABLE	R/W	Disables Link Power Management
0	Reserved	R	Reserved for future use

TABLE 76: USB2 VERSION NUMBER MSB

USB2_BCDUSB_M (3108h)			USB2 Version BCD
Bit	**Name**	**R/W**	**Description**
7:0	USBVCD[15:8]	R/W	USB Specification Release Number in BCD format. Default to USB 2.0 Support

TABLE 77: USB2 VERSION NUMBER LSB

USB2_BCDUSB_L (3109h)			USB2 Version BCD
Bit	**Name**	**R/W**	**Description**
7:0	USBVCD[7:0]	R/W	USB Specification Release Number in BCD format. Default to USB 2.0 Support

TABLE 78: USB2 BOS DESCRIPTOR LENGTH

USB2_BOS_LEN (3114h)			USB2 BOS Descriptor Length Register
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Always read ‘0’
5:0	BOS_DESC_LEN	R/W	Length of the BOS descriptor programmed into the BOS_DESC array minus one. For example 1Fh means a length of 32. A value of 0 means disabled.

TABLE 79: USB2 BOS DESCRIPTOR ARRAY

USB2_BOS_DESC (3120h-314Fh)			USB2 BOS Descriptor Array
Bit	**Name**	**R/W**	**Description**
47:0	BOS_DESC	R/W	This is a 48 byte array that contains the BOS descriptor.

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TABLE 80: OCS PORT SELECT REGISTER

PSEL (318Bh)			OCS Port Select Register (WLCSP package only)
Bit	**Name**	**R/W**	**Description**
7:6	APortSel	R/W	Specifies which downstream USB port is associated with the OCSA, PrtPwrA and OCSA pin functions. ‘00’ - Port 1 ‘01’ - Port 2 ‘10’ - Port 3 ‘11’ - Port 4
5:0	Reserved	R	Always read ‘0’

TABLE 81: CONNECT CONFIGURATION REGISTER

CONNECT_CFG (318Eh)			Connect Configuration Register
Bit	**Name**	**R/W**	**Description**
7	HIRD_TIMR_SEL	R/W	HIRD Timer selection register 0 - Use Alternate HIRD definition (up to 9.95ms) 1 - Use Original HIRD definition (up to 1.2ms)
6:2	Reserved	R	Reserved
1	EN_FLEX_MODE	R/W	If this is not set, normal hub operation is enabled, with separate port power and OCS control. If this bit is set, then FlexConnect mode is enabled.
0	FLEXCONNECT	R/W	FlexConnect Control. When asserted the USB253x / USB3x13 / USB46x4 changes it’s hub connections so that the Swap port (Physical Port 1) changes from it’s default behavior of a downstream port to an upstream port. The Flex Port (Physical port 0) transitions from an upstream port to a downstream port. ‘0’ - Flex Port = Up (Port 0) Swap Port= Down (Port 1) ‘1’ - Flex Port= Down (Port 1) Swap Port= Up (Port 0) This setting can be used to select whether the Flex Port is an upstream or downstream port. The Flex Port provides both an HSIC and D+/D- connection, so the OEM can select whether this flexibility is provided on the upstream or downstream port. Another application for this setting is to allow a dual-role device on the Swap Port to assume a host role and communicate directly with other downstream hub ports, or to communicate through the Flex Port to an exposed connector to an external device. If a “private” communication channel is desired between embedded devices, any externally exposed ports should be disabled. **Note:** All port-specific settings are specific to the logic port 0, 1, 2, 3. When *FlexConnect* is asserted these settings affect the newly assigned physical pin and PHY. Any settings which are specific to the physical Flex Port and Swap Port such as battery charger detection do not change with the setting in *FlexConnect*.

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TABLE 82: GLOBAL RESUME TIMING REGISTER 3

GLOBAL_RESUME_TIME3 (3191h)			Global Resume Timing Register 3
Bit	**Name**	**R/W**	**Description**
7:0	RESUME_TIME [23:16]	R/W	Timing for the global resume in 60Mhz clocks, must be programmed to 19ms or less.

TABLE 83: GLOBAL RESUME TIMING REGISTER 2

GLOBAL_RESUME_TIME2 (3192h)			Global Resume Timing Register 2
Bit	**Name**	**R/W**	**Description**
7:0	RESUME_TIME [15:8]	R/W	Timing for the global resume in 60Mhz clocks, must be programmed to 19ms or less.

TABLE 84: GLOBAL RESUME TIMING REGISTER 1

GLOBAL_RESUME_TIME1 (3193h)			Global Resume Timing Register 1
Bit	**Name**	**R/W**	**Description**
7:0	RESUME_TIME [0:7]	R/W	Timing for the global resume in 60Mhz clocks, must be programmed to 19ms or less.

TABLE 85: PORT1 PORT POWER SELECT

PORT_CFG_SEL_1 (3C00h)			Port 1 Power Select
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = The port power and overcurrent sense use separate pins. 1 = The port power and overcurrent sense use the same pin. In this mode the corresponding OCS pin cannot be used as GPIO.
6	Reserved	R/W	Always read ‘0’
5	DISABLED	R/W	0 = The port is enabled. 1 = The port is disabled.
4	PERMANENT	R/W	0 = The port has a removable device 1 = The port has a permanently attached device
3:0	PRT_SEL	R/W	This selects the source for the port 1 pin 0000b = Port power is disabled. 0001b = Source is USB2 port power. 0010b = Reserved. 0011b = Source is USB2 port power. 0100b = Port is on if designated GPIO is on All other values are reserved.

TABLE 86: PORT2 PORT POWER SELECT

PORT_CFG_SEL_2 (3C04h)			Port 2 Power Select
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = The port power and overcurrent sense use separate pins. 1 = The port power and overcurrent sense use the same pin. In this mode the corresponding OCS pin cannot be used as GPIO.
6	Reserved	R/W	Always read ‘0’
5	DISABLED	R/W	0 = The port is enabled. 1 = The port is disabled.
4	PERMANENT	R/W	0 = The port has a removable device 1 = The port has a permanently attached device
3:0	PRT_SEL	R/W	This selects the source for the port 1 pin 0000b = Port power is disabled. 0001b = Source is USB2 port power. 0010b = Reserved. 0011b = Source is USB2 port power. 0100b = Port is on if designated GPIO is on All other values are reserved.

TABLE 87: PORT3 PORT POWER SELECT

PORT_CFG_SEL_3 (3C08h)			Port 3 Power Select
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = The port power and overcurrent sense use separate pins. 1 = The port power and overcurrent sense use the same pin. In this mode the corresponding OCS pin cannot be used as GPIO.
6	Reserved	R/W	Always read ‘0’
5	DISABLED	R/W	0 = The port is enabled. 1 = The port is disabled.
4	PERMANENT	R/W	0 = The port has a removable device 1 = The port has a permanently attached device
3:0	PRT_SEL	R/W	This selects the source for the port 1 pin 0000b = Port power is disabled. 0001b = Source is USB2 port power. 0010b = Reserved. 0011b = Source is USB2 port power. 0100b = Port is on if designated GPIO is on All other values are reserved.

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TABLE 88: PORT4 PORT POWER SELECT

PORT_CFG_SEL_4 (3C0Ch)			Port 4 Power Select
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = The port power and overcurrent sense use separate pins. 1 = The port power and overcurrent sense use the same pin. In this mode the corresponding OCS pin cannot be used as GPIO.
6	Reserved	R/W	Always read ‘0’
5	DISABLED	R/W	0 = The port is enabled. 1 = The port is disabled.
4	PERMANENT	R/W	0 = The port has a removable device 1 = The port has a permanently attached device
3:0	PRT_SEL	R/W	This selects the source for the port 1 pin 0000b = Port power is disabled. 0001b = Source is USB2 port power. 0010b = Reserved. 0011b = Source is USB2 port power. 0100b = Port is on if designated GPIO is on All other values are reserved.

TABLE 89: USB PORT1 OCS SOURCE SELECT

USB_OCS_SEL_1 (3C20h)			Port 1 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read ‘0’
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for port 1 0000b = OCS is disabled. 0001b = OCS is enabled. All other values are reserved.

TABLE 90: USB PORT2 OCS SOURCE SELECT

USB_OCS_SEL_2 (3C24h)			Port 2 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read ‘0’
3:0	OCS_SEL	R/W	This selects the source for the OCS signal 0000b = OCS is disabled. 0001b = OCS is enabled. All other values are reserved.

TABLE 91: USB PORT 3 OCS SOURCE SELECT

USB_OCS_SEL_3 (3C28h)			Port 3 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read ‘0’
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for port 1 0000b = OCS is disabled. 0001b = OCS is enabled. All other values are reserved.

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TABLE 92: USB PORT 4 OCS SOURCE SELECT

USB_OCS_SEL_4 (3C2Ch)			Port 4 OCS Source Select
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read ‘0’
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for port 1 0000b = OCS is disabled. 0001b = OCS is enabled. All other values are reserved.

TABLE 93: VBUS PASS THROUGH

VBUS_PASS_THRU (3C40h)			VBUS Pass Through Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2	HUB_CONN_PASS_THRU	R/W	0=The HUB_CONNECT to USB Hub comes from device pin 1=The HUB_CONNECT is GPIO driven by processor PIO16
1	Reserved	R	Reserved
0	USB_PASS_THRU	R/W	0=VBUS to Hub comes from processor PIO32 1=VBUS to Hub comes from device pin

TABLE 94: INT_N_BYPASS CONTROL

INT_N_BYPASS (3C51h)			INT_N Bypass
Bit	**Name**	**R/W**	**Description**
7	Reserved	R/W	Reserved
6	INT_N_BYPASS	R/W	Route the SUSPEND signal directly to the SUSP_IND pin for the USB253x or the INT_N pin for the USB3x13.
5:2	Reserved	R	Reserved
1	SUSPEND	R	This is a direct read of the SUSPEND signal of the Hub.
0	INT_N	R	This is a direct read of the INT_N signal of the Hub.

TABLE 95: SUSPEND SELECT

SUSP_SEL (3C52h)			SUSPEND Select
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always read ‘0’
0	SUSPEND_SEL	R/W	0=PIO0 or LED0 routed to the SUSPEND/PIO0 pin 1=SUSPEND routed to the SUSPEND/PIO0 pin

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2.5.2.3 Additional Port Enumeration

The USB253x / USB3x13 / USB46x4 has an internal processor that enumerates as an additional port on the device. This port allows expanded options such as GPIO control, UART and I^2C communication and other enhancements. The enumeration of this port is controlled through register 4130h.

TABLE 96: INTERNAL HUB CONTROLLER ENUMERATION CONTROL

INTERNAL_PORT (4130h)			Internal Port Enumeration Control
Bit	**Name**	**R/W**	**Description**
7:2	Reserved	R/W	Reserved
1:0	PORT_ENUM	R/W	00b = Use default part number control. 01b = Always enable the internal Hub Controller enumeration. 10b = Always disable the internal Hub Controller enumeration. 11b = Reserved

2.5.2.4 Downstream Battery Charging Registers

When battery charging is enabled through SMBus or through the BC_EN strap option, the downstream ports can be configured to display multiple battery charging handshakes. The following registers configure the port for the unattached handshake. This handshake is used when the upstream port is not connected to a host, or if the host suspends the hub and nothing is connected to the downstream port and remote wakeup is disabled.

TABLE 97: PORT 1 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P1 (413Ch)			Port 1 Battery Charging Configuration
Bit	**Name**	**R/W**	**Description**
7:6	UCS_CLIM	R/W	When controlling the UCS1002 through I^2C this controls the current limit set point. 00b = 500mA 01b = 1000mA 10b = 1500mA 11b = 2000mA
5	DCP	R/W	When set this enables the Dedicated Charging Port mode defined by USB-IF
4:3	Reserved	R/W	Reserved
2	SE1_HC	R/W	When set this enables the SE1 High Current mode used by Apple devices to charge at 2A. Bit 1 must also be set.
1	SE1_EN	R/W	When set this enables the SE1 resistor dividers to be placed on the downstream port. Apple devices use these voltages to detect chargers.
0	BC_EN	R/W	This bit enables the battery charging support on this port.

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TABLE 98: PORT 2 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P2 (413Dh)			Port 2 Battery Charging Configuration
Bit	**Name**	**R/W**	**Description**
7:6	UCS_CLIM	R/W	When controlling the UCS1002 through I^2C this controls the current limit set point. 00b = 500mA 01b = 1000mA 10b = 1500mA 11b = 2000mA
5	DCP	R/W	When set this enables the Dedicated Charging Port mode defined by USB-IF
4:3	Reserved	R/W	Reserved
2	SE1_HC	R/W	When set this enables the SE1 High Current mode used by Apple devices to charge at 2A. Bit 1 must also be set.
1	SE1_EN	R/W	When set this enables the SE1 resistor dividers to be placed on the downstream port. Apple devices use these voltages to detect chargers.
0	BC_EN	R/W	This bit enables the battery charging support on this port.

TABLE 99: PORT 3 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P3 (413Eh)			Port 3 Battery Charging Configuration
Bit	**Name**	**R/W**	**Description**
7:6	UCS_CLIM	R/W	When controlling the UCS1002 through I^2C this controls the current limit set point. 00b = 500mA 01b = 1000mA 10b = 1500mA 11b = 2000mA
5	DCP	R/W	When set this enables the Dedicated Charging Port mode defined by USB-IF
4:3	Reserved	R/W	Reserved
2	SE1_HC	R/W	When set this enables the SE1 High Current mode used by Apple devices to charge at 2A. Bit 1 must also be set.
1	SE1_EN	R/W	When set this enables the SE1 resistor dividers to be placed on the downstream port. Apple devices use these voltages to detect chargers.
0	BC_EN	R/W	This bit enables the battery charging support on this port.

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TABLE 100: PORT 4 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P4 (413Fh)			Port 4 Battery Charging Configuration
Bit	**Name**	**R/W**	**Description**
7:6	UCS_CLIM	R/W	When controlling the UCS1002 through I^2C this controls the current limit set point. 00b = 500mA 01b = 1000mA 10b = 1500mA 11b = 2000mA
5	DCP	R/W	When set this enables the Dedicated Charging Port mode defined by USB-IF
4:3	Reserved	R/W	Reserved
2	SE1_HC	R/W	When set this enables the SE1 High Current mode used by Apple devices to charge at 2A. Bit 1 must also be set.
1	SE1_EN	R/W	When set this enables the SE1 resistor dividers to be placed on the downstream port. Apple devices use these voltages to detect chargers.
0	BC_EN	R/W	This bit enables the battery charging support on this port.

2.5.2.5 Port Control Registers

These registers control the analog signaling of specific ports. Although both HSIC and USB control registers are listed, please check the individual data sheets to see what registers apply to each specific product.

TABLE 101: USB UPSTREAM BOOST REGISTER

HS_UP_BOOST (60CAh)			USB Upstream Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

TABLE 102: USB UPSTREAM VARISENSE REGISTER

PHY_UP_SENSE (60CCh)			USB Upstream Varisense Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

TABLE 103: HSIC UPSTREAM CONTROL REGISTER

HSIC_UP_CTL (6141h)			HSIC Upstream Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Always read ‘0’
2	HSIC_DS_EN50	R/W	HSIC 50ohm Driver Enable (Data and Strobe). Selects the driver output impedance. 1'b0: 40ohm driver 1'b1: 50ohm driver.
1	HSIC_DS_SLEW_TUNE	R/W	HSIC Slew Tune (Data and Strobe). Reduces transmit slew rate on Data/Strobe by 30%. 1’b0: TX Slew boost disabled (Default) 1’b1: TX Slew boosted by 30%
0	HSIC_PIN_SWAP	R/W	HSIC Pin Swap

TABLE 104: USB PORT 1 BOOST REGISTER

HS_P1_BOOST (64CAh)			USB Port 1 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

TABLE 105: USB PORT 1 VARISENSE REGISTER

PHY_P1_SENSE (64CCh)			USB Port 1 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

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TABLE 106: HSIC PORT 1 CONTROL REGISTER

HSIC_P1_CTL (6541h)			HSIC Port 1 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Always read ‘0’
2	HSIC_DS_EN50	R/W	HSIC 50ohm Driver Enable (Data and Strobe). Selects the driver output impedance. 1'b0: 40ohm driver 1'b1: 50ohm driver.
1	HSIC_DS_SLEW_TUNE	R/W	HSIC Slew Tune (Data and Strobe). Reduces transmit slew rate on Data/Strobe by 30%. 1’b0: TX Slew boost disabled (Default) 1’b1: TX Slew boosted by 30%
0	HSIC_PIN_SWAP	R/W	HSIC Pin Swap

TABLE 107: HSIC PORT 1 CONFIGURATION REGISTER

HSIC_P1_CFG (6643h)			HSIC Port 1 Configuration
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always read ‘0’
0	PORT_POWER_MODE	R/W	1'b0: Bus keepers on DATA/STROBE are both driven to low when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller expects a CONNECT event from the device on subsequent re-enable of port power. 1'b1: Bus keepers on DATA/STROBE remains at IDLE state when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller does not expect a CONNECT event from the device on subsequent re-enable of port power.

TABLE 108: USB PORT 2 BOOST REGISTER

HS_P2_BOOST (68CAh)			USB Port 2 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

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TABLE 109: USB PORT 2 VARISENSE REGISTER

PHY_P2_SENSE (68CC)			USB Port 2 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	USB2_SQ_TUNE[2:0]	R/W	Squelch Tune 3'b000: Nominal 100mV Trip Point 3'b001: Decrease by 12.5mV 3'b010: Decrease by 25mV 3'b011: Decrease by 37.5mV 3'b100: Decrease by 50mV 3'b101: Decrease by 62.5mV 3'b110: Increase by 25mV 3'b111: Increase by 12.5mV

TABLE 110: HSIC PORT 2 CONTROL REGISTER

HSIC_P2_CTL (6941h)			HSIC Port 2 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Always read '0'
2	HSIC_DS_EN50	R/W	HSIC 50ohm Driver Enable (Data and Strobe). Selects the driver output impedance. 1'b0: 40ohm driver 1'b1: 50ohm driver.
1	HSIC_DS_SLEW_TUNE	R/W	HSIC Slew Tune (Data and Strobe). Reduces transmit slew rate on Data/Strobe by 30%. 1'b0: TX Slew boost disabled (Default) 1'b1: TX Slew boosted by 30%
0	HSIC_PIN_SWAP	R/W	HSIC Pin Swap

TABLE 111: HSIC PORT 2 CONFIGURATION REGISTER

HSIC_P2_CFG (6A43h)			HSIC Port 2 Configuration
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always read '0'
0	PORT_POWER_MODE	R/W	1'b0 : Bus keepers on DATA/STROBE are both driven to low when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller expects a CONNECT event from the device on subsequent re-enable of port power. 1'b1 : Bus keepers on DATA/STROBE remains at IDLE state when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller does not expect a CONNECT event from the device on subsequent re-enable of port power.

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TABLE 112: USB PORT 3 BOOST REGISTER

HS_P3_BOOST (6CCAh)			USB Port 3 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

TABLE 113: USB PORT 3 VARISENSE REGISTER

PHY_P3_SENSE (6CCCh)			USB Port 3 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	USB2_SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

TABLE 114: HSIC PORT 3 CONTROL REGISTER

HSIC_P3_CFG (6D41h)			HSIC Port 3 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Always read ‘0’
2	HSIC_DS_EN50	R/W	HSIC 50ohm Driver Enable (Data and Strobe). Selects the driver output impedance. 1'b0: 40ohm driver 1'b1: 50ohm driver.
1	HSIC_DS_SLEW_TUNE	R/W	HSIC Slew Tune Testbit (Data and Strobe). Reduces transmit slew rate on Data/Strobe by 30%. 1’b0: TX Slew boost disabled (Default) 1’b1: TX Slew boosted by 30%
0	HSIC_PIN_SWAP	R/W	HSIC Pin Swap

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TABLE 115: HSIC PORT 3 CONFIGURATION REGISTER

HSIC_P3_CFG (6E43h)			HSIC Port 3 Configuration
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always read ‘0’
0	PORT_POWER_MODE	R/W	1'b0 : Bus keepers on DATA/STROBE are both driven to low when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller expects a CONNECT event from the device on subsequent re-enable of port power. 1'b1 : Bus keepers on DATA/STROBE remains at IDLE state when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller does not expect a CONNECT event from the device on subsequent re-enable of port power.

TABLE 116: USB PORT 4 BOOST REGISTER

HS_P4_BOOST (70CAh)			USB Port 4 Boost Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

TABLE 117: USB PORT 4 VARISENSE REGISTER

PHY_P4_SENSE (70CCh)			USB Port 4 Varisense Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	USB2_SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

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TABLE 118: HSIC PORT 4 CONTROL REGISTER

HSIC_P4_CTL (7141h)			HSIC Port 4 Control Register
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Always read ‘0’
2	HSIC_DS_EN50	R/W	HSIC 50ohm Driver Enable (Data and Strobe). Selects the driver output impedance. 1'b0: 40ohm driver 1'b1: 50ohm driver.
1	HSIC_DS_SLEW_TUNE	R/W	HSIC Slew Tune Testbit (Data and Strobe). Reduces transmit slew rate on Data/Strobe by 30%. 1’b0: TX Slew boost disabled (Default) 1’b1: TX Slew boosted by 30%
0	HSIC_PIN_SWAP	R/W	HSIC Pin Swap

TABLE 119: HSIC PORT 4 CONFIGURATION REGISTER

HSIC_P4_CFG (7243h)			HSIC Port 4 Configuration Register
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always read ‘0’
0	PORT_POWER_MODE	R/W	1'b0 : Bus keepers on DATA/STROBE are both driven to low when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller expects a CONNECT event from the device on subsequent re-enable of port power. 1'b1 : Bus keepers on DATA/STROBE remains at IDLE state when HSIC host disables port power to downstream HSIC device. Downstream HSIC controller does not expect a CONNECT event from the device on subsequent re-enable of port power.

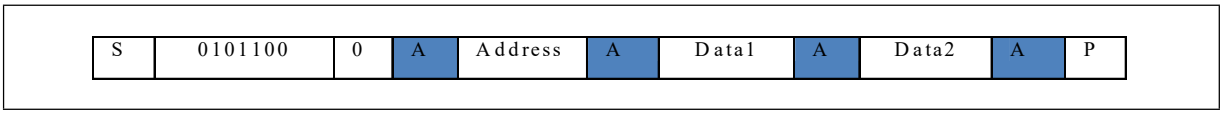
3.0 SMBUS RUN TIME ACCESSIBLE REGISTERS

After the hub enters the **Hub Connect Stage**, the SMBus protocol changes to allow faster access to a limited set of registers. These registers are accessed through an 8-bit address byte followed by the data. The address also changes from 2Dh to **2Ch**. An extended range of registers can be accessed through the SMBus Page Register.

3.1 SMBus Block Write

The SMBus block write consists of an Address+Direction(0) byte followed by the 8-bit memory address.

FIGURE 4: SMBUS BLOCK WRITE

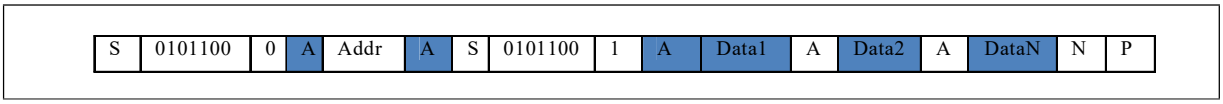


Note: The 7-bit address of the hub is ***2Ch***. Or the first byte is ***58h*** for an SMBus Write.

3.2 SMBus Block Read

The SMBus block read consists of an Address+Direction(0) byte with the 8-bit memory address followed by a repeat Start signal and an Address+Direction(1) byte. The hub will then start to output the contents of the internal registers starting at the 8-bit address specified.

FIGURE 5: SMBUS BLOCK READ



Note: The 7-bit address of the hub is ***2Ch***. Or the first byte is ***59h*** for an SMBus Read.

3.3 Run Time Registers

Table 3.1 provides a summary of the SMBus accessible run time registers. Each register is detailed in the subsequent tables.

3.4 Run Time SMBus Page Register

The following run time SMBus page register is located at FFh on page 1 and 2. This must be programmed to allow the SOC to page through different regions of the register space.

TABLE 120: SMBUS PAGE REGISTER

SMBUS_PAGE (FFh)			**SMBUS Page Register**
Bit	**Name**	**R/W**	**Description**
7:5	PAGE_SEL	R/W	Select the accessible address space: 000 = Select registers in the Pg1 Space 010 = Select registers in the Pg2 Space
5:0	Reserved	R	Reserved. **Note:** Software must never write a ‘1’ to these bits

Note: The SMBus page register must be configured to allow the SOC to access the proper register space.

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TABLE 121: SMBUS ACCESSIBLE RUN TIME REGISTERS

Name	ADDR	Description
UP_BC_DET	Pg1 E2h	Upstream Battery Charging Detection Control Register
UP_CUST_BC_CTL	Pg1 E3h	Upstream Custom Battery Charger Control Register
UP_CUST_BC_STAT	Pg1 E4h	Upstream Custom Battery Charger Status Register
PORT_PWR_STAT	Pg1 E5h	Port Power Status Register
OCS_STAT	Pg1 E6h	OCS Status Register
INT_STATUS	Pg1 E8h	Serial Port Interrupt Status Register
INT_MASK	Pg1 E9h	Serial Port Interrupt Mask Register
BC_CHG_MODE	Pg1 ECh	Upstream Battery Charger Mode Register
CHG_DET_MSK	Pg1 EDh	Charge Detect Mask Register
CFGP	Pg1 EEh	Configure Portable Hub Register
PSELSUSP	Pg2 8Bh	Port Select and Low-Power Suspend Register
CONNECT_CFG	Pg2 8Eh	Connect Configuration Register

3.4.1 REGISTER DEFINITIONS

3.4.1.1 Page 0 Registers

TABLE 122: UPSTREAM BATTERY CHARGING DETECTION CONTROL REGISTER

UP_BC_DET (PG1 E2h)			**Upstream Battery Charging Register**
Bit	**Name**	**R/W**	**Description**
7:5	CHARGER_TYPE	R/W	Read Only. This field indicates the result of the automatic charger detection. Values reported depend on EnhancedChrgDet bit setting in Upstream Battery Charger Mode Register. If EnhancedChrgDet = 1 000 = Charger Detection is not complete. 001 = DCP - Dedicated Charger Port 010 = CDP – Charging Downstream Port 011 = SDP – Standard Downstream Port 100 = SE1 Low Current Charger 101 = SE1 High Current Charger 110 = SE1 Super High Current Charger 111 = Charger Detection Disabled If EnhancedChrgDet = 0 000 = Charger Detection is not complete. 001 = DCP/CDP – Dedicated Charger or Charging Downstream Port 010 = Reserved 011 = SDP – Standard Downstream Port 100 = SE1 Low Current Charger 101 = SE1 High Current Charger 110 = SE1 Super High Current Charger 111 = Charger Detection Disabled
4	CHGDET_COMPLETE	R	Indicates Charger Detection has been run and is completed. This bit is negated when START_CHG_DET is asserted high.
3	Reserved	R/W	Reserved for debugging

TABLE 122: UPSTREAM BATTERY CHARGING DETECTION CONTROL REGISTER (CONTINUED)

UP_BC_DET (PG1 E2h)			Upstream Battery Charging Register
Bit	**Name**	**R/W**	**Description**
2:1	CHG_DET[1:0]	R	Indicates encoded status of what chargers or status has been detected according to the settings in the Charge Detect Mask Register. It can be used to determine what current can be drawn from the upstream USB port. 00 = No selected Chargers or Status identified 01 = 100ma (VBUS detect without enumeration) 10 = 500ma (Device enumerated, Set Config seen) 11 = 1000+ma (Charger detected) The actual current amount for the charger will be system dependent
0	START_CHG_DET	R/W	Manually Initiates a USB battery charger detection sequence at the time of assertion. This bit must not be set while hub is in operation. This bit is cleared automatically when the manual battery charger detection sequence is completed. 0 = Write: No Effect / Read: Battery Charger Detection Sequence Completed or not run. 1 = Write: Start Battery Charger Detection / Read: Battery Charger Detection Sequence is running

TABLE 123: UPSTREAM CUSTOM BATTERY CHARGER CONTROL REGISTER

UP_CUST_BC_CTL (PG1 E3h)			Upstream Custom Battery Charging Control
Bit	**Name**	**R/W**	**Description**
7	SMBControl	R/W	SMBus control 0: SMBus control disabled 1: SMBus control enabled
6	DmPulldownEn	R/W	DM 15K pull down resistor control 0: DM 15K pull down resistor disabled 1: DM 15K pull down resistor enabled
5	DpPulldownEn	R/W	DP 15K pull down resistor control 0: DP 15K pull down resistor disabled 1: DP 15K pull down resistor enabled
4	IdatSinkEn	R/W	Idat current sink control 0: Idat current sink disabled 1: Idat current sink enabled
3	HostChrgEn	R/W	Host charger detection swap control 0: Charger detection connections of DP and DM are not swapped (standard) 1: Charger detection connections of DP and DM are swapped. The USB signal path is not reversed.
2	VdatSrcEn	R/W	Vdat voltage source control 0: Vdat voltage source disabled 1: Vdat voltage source enabled

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TABLE 123: UPSTREAM CUSTOM BATTERY CHARGER CONTROL REGISTER (CONTINUED)

UP_CUST_BC_CTL (PG1 E3h)			Upstream Custom Battery Charging Control
Bit	**Name**	**R/W**	**Description**
1	ContactDetectEn	R/W	Contact detect current source control 0: Contact detect current source disabled 1: Contact detect current source enabled
0	SeRxEn	R/W	Single-ended receiver control 0: Single-ended receiver disabled 1: Single-ended receiver enabled

TABLE 124: UPSTREAM CUSTOM BATTERY CHARGER STATUS REGISTER

UP_CUST_BC_STAT (PG1 E4h)			Upstream Custom Battery Charging Status
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3	RxHiCurr	R	DM high current SE1 charger output 0: DM signal is not above the VSE_RXH threshold 1: DM signal is above the VSE_RXH threshold
2	DmSeRx	R	DM Single Ended Receiver Status
1	DpSeRx	R	DP Single Ended Receiver Status
0	VdatDet	R	Vdat detect 0: Vdat not detected 1: Vdat detect comparator output

TABLE 125: PORT POWER STATUS REGISTER

PORT_PWR_STAT (PG1 E5h)			Port Power Status
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4:1	PRTPWR[4:1]	R	Optional status to SOC indicating that power to the corresponding downstream port was enabled by the USB Host for the specified port. Not required for an embedded application. This is a read-only status bit. Actual control over port power is implemented by the USB Host, OCS Status Register and Downstream Battery Charging logic, if enabled. 0: USB Host has not enabled port to be powered or in downstream battery charging and corresponding OCS bit has been set 1: USB Host has enabled port to be powered
0	Reserved	R	Reserved

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TABLE 126: OCS STATUS REGISTER

OCS_STAT (PG1 E6h)			Port Power Status
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4:1	OCS[4:1]	R	Optional control from SOC that indicates an over-current condition on the corresponding port for HUB status reporting to USB host. Also resets corresponding PRTPWR status bit in the Port Power Status Register. Not required for an embedded application. 0: No Over Current Condition 1: Over Current Condition
0	Reserved	R	Reserved

TABLE 127: SERIAL PORT INTERRUPT STATUS REGISTER

SP_INT_STATUS (PG1 E8h)			Serial Port Interrupt Status (USB3813 and USB3613 Only)
Bit	**Name**	**R/W**	**Description**
7	Interrupt	R/W	Read: 0: INT_N pin has not been asserted low due to unmasked interrupt 1: INT_N pin has been asserted low due to unmasked interrupt Write: 0: Negate INT_N pin high 1: No Effect – INT_N pin and register retains its current value
6:5	Reserved	R	Reserved
4	HubSuspInt	R/W	Read: 0: Hub has not entered USB suspend since last HubSuspInt reset 1: Hub has entered USB suspend Write: 0: Negate HubSuspInt status low 1: No Effect
3	HubCfgInt	R/W	Read: 0: Hub has not been configured by the USB Host since last HubConfInt reset 1: Hub has been configured by the USB host Write: 0: Negate HubConfInt status low 1: No Effect
2	PrtPwrInt	R/W	Read: 0: Port Power Status has not been updated since last PrtPwrInt reset 1: Port Power Status has been updated Write: 0: Negate PrtPwrInt status low 1: No Effect
1	ChrgDetInt	R/W	Read: 0: Charge detect has not been updated since last ChrgDetInt reset 1: Charge detect as been updated CHG_DET_N bit in Charger Detect Register has been asserted low Write: 0: Negate ChrgDetInt status low 1: No Effect

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TABLE 127: SERIAL PORT INTERRUPT STATUS REGISTER (CONTINUED)

SP_INT_STATUS (PG1 E8h)			Serial Port Interrupt Status (USB3813 and USB3613 Only)
Bit	**Name**	**R/W**	**Description**
0	ChrgDetCompInt	R/W	Read: 0: Charge detection not completed since last ChrgDetCompInt reset 1: Charge detection completed ChrgDetComplete bit in Charger Detect Register has been asserted high Write: 0: Negate ChrgDetCompInt status low 1: No Effect

TABLE 128: SERIAL PORT INTERRUPT MASK REGISTER

SP_INT_MSK (PG1 E9h)			Serial Port Interrupt Mask (USB3813 and USB3613 Only)
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4	HubSuspMask	R/W	0 = INT_N pin is not affected by Hub entering suspend 1 = INT_N pin is asserted when Hub enters suspend
3	HubCfgMask	R/W	0 = INT_N pin is not affected by Hub configuration event 1 = INT_N pin is asserted when Hub configured by USB Host
2	PrtPwrMask	R/W	0 = INT_N pin is not affected by Port Power register 1 = INT_N pin is asserted when Port Power register has been updated by USB Host
1	ChrgDetMask	R/W	0 = INT_N pin is not affected by CHG_DET_N 1 = INT_N pin is asserted when CHG_DET bit in Charger Detect Register is asserted
0	ChgDetCompMask	R/W	0 = INT_N pin is not affected by ChrgDetComplete 1 = INT_N pin is asserted when ChrgDetComplete bit in Charger Detect Register is asserted high

TABLE 129: UPSTREAM BATTERY CHARGER MODE REGISTER

BC_CHG_MODE (PG1 ECh)			Upstream Battery Charger Mode
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Reserved
5	HoldVdat	R/W	Dead Battery Vdat Detect voltage source enable 0: The charger detection state machine will turn off the Vdat Source at the end of the charger detection routine. 1: The charger detection state machine leave Vdat Source on during Hub.Connect stage when a SDP has been detected.
4	Reserved	R	Reserved
3	SE1ChrgDet	R/W	SE1 type charger detection control 0: The charger detection routine will not look for the attachment of an SE1 type charger. 1: The charger detection routine will look for the attachment of an SE1 type charger.

TABLE 129: UPSTREAM BATTERY CHARGER MODE REGISTER (CONTINUED)

BC_CHG_MODE (PG1 ECh)			Upstream Battery Charger Mode
Bit	**Name**	**R/W**	**Description**
2	EnhancedChrgDet	R/W	Enhanced charge detect control 0: The charger detection routine will not reverse Vdat SRC to differentiate between a CDP and a DCP. 1: The charger detection routine will reverse Vdat SRC to differentiate between a CDP and a DCP.
1:0	Reserved	R	Reserved

TABLE 130: CHARGE DETECT MASK REGISTER

CHG_DET_MSK (PG1 EDh)			Charge Detect Mask
Bit	**Name**	**R/W**	**Description**
7	CONFIGURED	R/W	If this bit is set, it indicates that the hub is configured. The charge detect bits will indicate a 500mA source. This bit will have no effect on the charge detect bits if a battery charging source is detected.
6	CONNECTED	R/W	If this bit is set, it indicates that the hub is connected. Which means a VBUS was detected. The charge detect bits will indicate a 100mA source. This bit will have no effect on the charge detect bits if a battery charging source is detected, or the CONFIGURED bit is set.
5	SUSPENDED	R/W	This is a status that is set when the hub is in suspend. This bit has no effect on charge detect encoding.
4	SE1SMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a SE1 Super High Current Charger 1: *battChg.chgDet* indicates status for this mask set met when a SE1 Super High Current Charger is detected
3	SE1HMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a SE1 High Current Charger 1: *battChg.chgDet* indicates status for this mask set met when a SE1 High Current Charger is detected
2	SE1LMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a SE1 Low Current Charger 1: *battChg.chgDet* indicates status for this mask set met when a SE1 Low Current Charger is detected
1	CDPMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a CDP Charger 1: *battChg.chgDet* indicates status for this mask set met when a CDP Charger is detected This mask bit should only be enabled if EnhancedChrgDet is asserted in the Upstream Battery Charger Mode Register. Without it, the charger detection is unable to identify a CDP.
0	DCPMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a DCP Charger 1: *battChg.chgDet* indicates status for this mask set met when a DCP Charger is detected

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TABLE 131: CONFIGURE PORTABLE HUB REGISTER

CFGP (PG1 EEh)			Portable Hub Configuration Register
Bit	**Name**	**R/W**	**Description**
7	ClkSusp	R/W	0: Allow device to gate-off its internal clocks during suspend mode in order to meet USB suspend current requirements. 1: Force device to run internal clock even during USB suspend (will cause device to violate USB suspend current limit - intended for test or self-powered applications which require use of serial port during USB session.)
6	IntSusp	R/W	0: INT_N pin function retains event sensitive role of a general serial port interrupt. (USB3813/USB3613 Only) 1: INT_N pin function is a level sensitive USB suspend interrupt indication. Allows system to adjust current consumption to comply with USB specification limits when hub is in the USB suspend state.
5:1	DIS_PHY_CLK[5:1]	R/W	A ‘1’ disables the PHY clock of the corresponding port: Bit 5 - Downstream port 5 Bit 4 - Downstream port 4 Bit 3 - Downstream port 3 Bit 2 - Downstream port 2 Bit 1 - Downstream port 1
0	Reserved	R	Always read ‘0’

3.4.1.2 Page 2 Registers

TABLE 132: PORT SELECT AND LOW-POWER SUSPEND REGISTER

PSELSUSP (PG2 8Bh)			Port Select and Low Power Suspend Register
Bit	**Name**	**R/W**	**Description**
7:6	APortSel	R/W	Specifies which downstream USB port is associated with the OCSA, PRTPWRA and PrtPwrOCSA pin function. ‘00’ - Port 1 ‘01’ - Port 2 ‘10’ - Port 3 ‘11’ - Port 4
5:0	Reserved	R	Always read ‘0’

Note: This applies to the USB3813 and USB3613 part numbers only.

TABLE 133: CONNECT CONFIGURATION REGISTER

CONNECT_CFG (PG2 8Eh)			Connect Configuration Register
Bit	**Name**	**R/W**	**Description**
7	HIRD_TIMR_SEL	R/W	HIRD timer selection 0: Use alternate HIRD definition (up to 9.95mS) 1: Use original HIRD definition (up to 1.2mS)
6:3	Reserved	R	Reserved
1	EN_FLEX_MODE	R/W	Flex Connect mode enable 0: Flex Connect mode is disabled. (Normal hub operation with separate port power and OCS control) 1: Flex Connect mode is enabled
0	FLEXCONNECT	R/W	FlexConnect Control. When asserted the device changes its hub connections so that the Swap port (Physical Port 1) changes from it's default behavior of a downstream port to an upstream port. The Flex Port (Physical port 0) transitions from an upstream port to a downstream port. '0' - Flex Port = Upstream (Port 0) Swap Port= Downstream (Port 1) '1' - Flex Port= Downstream (Port 1) Swap Port= Upstream (Port 0) This setting can be used to select whether the Flex Port is an upstream or downstream port. Another application for this setting is to allow a dual-role device on the Swap Port to assume a host role and communicate directly with other downstream hub ports, or to communicate through the Flex Port to a exposed connector to an external device. If a "private" communication channel is desired between embedded devices, any externally exposed ports should be disabled. Note: All port-specific settings such as VSNS, prtSp, sDiscon are specific to the logic port 0, 1, 2, 3. When FLEXCONNECT is asserted, these settings affect the newly assigned physical pins and PHY. Any settings which are specific to the physical Flex Port and Swap Port such as battery charger detection do not change with the setting of FLEXCONNECT.

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4.0 OTP CONFIGURATION

The OTP registers can be programmed through the SMBus interface in the SOC_CONFIG Stage. The OTP registers are configured as a series of commands that will manipulate the configuration registers. These commands can be appended to each other, so multiple OTP programs can be executed at different times. The OTP registers can only be programmed once, so once all of the registers have been written to, no other changes can be made.

The entire list of configuration commands contained in the OTP Registers are executed during the HUB_CONFIG stage, when the OTP registers are loaded. These commands are stored in the OTP registers according to the structure detailed in Section 4.2.

4.1 Configuration Commands

The OTP structure contains multiple configuration commands that are used to manipulate the configuration registers before the hub enters the **Hub Connect Stage**. These can be used to change the default behavior of the hub during normal operation. The configuration commands contain the following structure:

4.1.1 SET_ADDRESS BYTE (80H)

The SET_ADDRESS byte is the first byte of any configuration command, it is always 80h.

4.1.2 ADDRESS BYTES (MSB, LSB)

The next two bytes after the SET_ADDRESS byte are the configuration register address that will be manipulated. Because the address is 16 bits long, this covers two bytes with the MSB coming first, then the LSB.

4.1.3 BIT COMMAND (FEH)

This is a command that will allow a register to be manipulated. This command must be followed by either a WRITE_-BYTE, SET_BIT, or CLEAR_BIT command, then the data length.

4.1.3.1 WRITE_BYTE (00h), SET_BIT (01h), or CLEAR_BIT (02h)

The WRITE_BYTE will replace the entire contents of the register with the new value.

The SET_BIT command will set every bit that is true in the following data. For example, if the data is 03h, then the SET_BIT command will cause only bits 0 and 1 to be set in the specified configuration register.

The CLEAR_BIT command will clear every bit that is true in the following data. For example, if the data is C0h, then the CLEAR_BIT command will cause only bits 6 and 7 to be cleared in the specified configuration register.

4.1.4 DATA LENGTH

This is the number of bytes that will be written sequentially to the configuration registers, starting at the Address specified in the previous bytes. Only data lengths of 0-127 bytes are valid.

4.1.5 DATA

The rest of the bytes are the data bytes that must correspond to the Data length byte. These are the actual values to be written, or bits to be manipulated. The Configuration Register address will increment with each byte.

Note:	The data bytes must be followed by either a STOP command or a SET_ADDRESS byte command to set or clear bits in another register. No other values are valid.

4.1.6 STOP (FFH)

After the desired configuration commands are complete the FFh byte confirms the termination of the command sequence.

4.1.7 EXAMPLE

If it was desired to have the hub start up in the Flexed state, the user would want to modify configuration register 318Eh. The other bits in this register should not be manipulated though, so the configuration command would be set up as follows:

TABLE 134: EXAMPLE CONFIGURATION COMMAND

Byte	Value	Comment
1	80h	SET_ADDRESS Byte command.
2	31h	Manipulating configuration register **31**8Eh.
3	8Eh	Manipulating configuration register 31**8E**h.
4	FEh	Bit command to manipulate just the bits.
5	01h	SET_BIT.
6	01h	Data length of 1 byte to manipulate.
7	01h	Only set the FLEXCONNECT bit in this register.
8	FFh	STOP command.

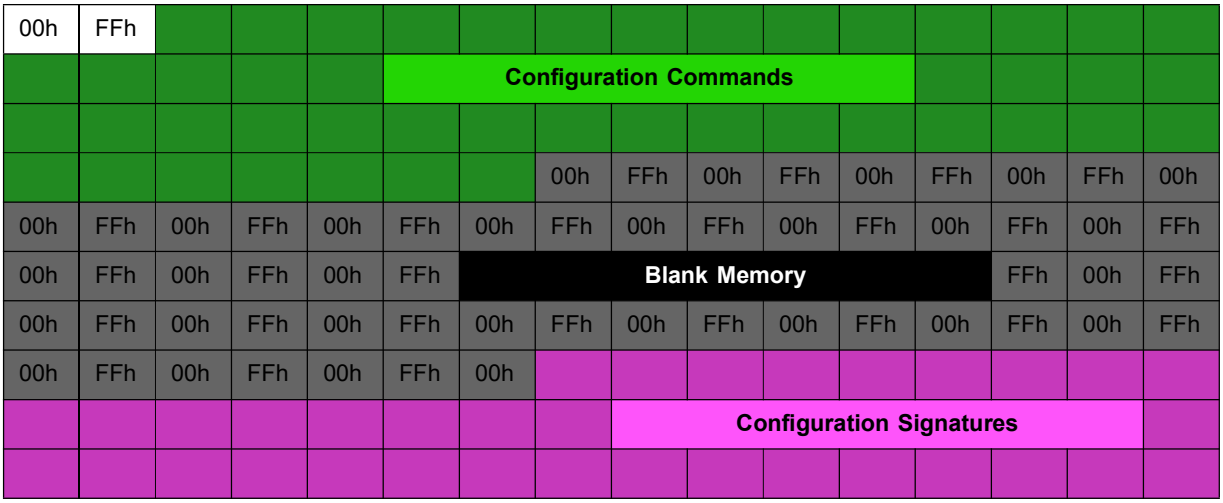
4.2 Reading OTP Data

Before any programming of the OTP data is done, the OTP data must first be read to confirm that enough space is available for the desired configuration commands.

To read the OTP data, send the OTP Read command **(9934h)** then read the configuration registers starting at address **4800h.** The OTP data is 2048 bytes of data.

The OTP data is broken up into three sections. The Configuration Command section, the Blank Memory section and the Command Signature section.

FIGURE 6: OTP DATA STRUCTURE



4.2.1 CONFIGURATION COMMAND SECTION

This section grows from the start of the OTP data. These are the commands that are appended every time an OTP Program command is sent through SMBus and can vary in length depending on how many configuration registers need to be manipulated.

4.2.2 BLANK MEMORY

This will cycle between 00h and FFh to show that is has not been written to yet.

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4.2.3 CONFIGURATION SIGNATURE

The Configuration Signature is automatically generated when the OTP data is programmed. This signature is always 8 bytes and is appended from the back of the OTP data every time the Program OTP Command is sent. This signature contains a checksum to confirm the configuration command was written correctly as well as information on where the configuration command is located and how long it is.

4.3 Programming OTP Data

To program the OTP data the following steps must to be followed:

1. Write the configuration command data starting at configuration register 4800h.
2. Write 03h to register 47FBh - This configures the hub to program the OTP registers.
3. Write the data length of the configuration command to register 47FFh - This tells the hub how much data will be programmed. If the data is longer than 256 bytes, register 47FEh is the MSB and register 47FFh is the LSB.
4. Send the OTP program command 9933h followed by 00h to confirm the command.

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5.0 USB CONFIGURATION

USB commands can be used to access Hub Controller registers. In addition, Microchip provides the USB2530 Software Development Kit to enable access to all the USB hub functionality.

5.1 USB Register Reads

For register reads the following USB SETUP packet is used:

TABLE 135: USB REGISTER READS SETUP PACKET

Setup Parameter	Value	Description
bmRequestType	0xC1	Device-to-host, vendor class, targeted to interface
bRequest	0x04	Register read command: CMD_REG_READ
wValue	Register Address	Valid Address Range: <0x0000> to <0xFFFF> [64KB]
wIndex	0x0000	Reserved
wLength	Data length	Length of data bytes to be retrieved

Command phase: Receive the setup packet with the parameters specified above

Data Phase:Send the data bytes of length wLength from the specified address.

5.2 USB Register Writes

For register writes the following USB SETUP packet is used:

TABLE 136: USB REGISTER WRITES SETUP PACKET

Setup Parameter	Value	Description
bmRequestType	0x41	Host-to-device, vendor class, targeted to interface
bRequest	0x03	Register write command: CMD_REG_WRITE
wValue	Register Address	Valid Address Range: <0x0000> to <0xFFFF> [64KB]
wIndex	0x0000	Reserved
wLength	Data Length	Length of data bytes to write

Command phase: Receives the setup packet with the parameters specified above

Data Phase: Receives wLenght data bytes and writes starting from the specified register address.

Status Phase: ACK - On successful completion of register write.

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APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
DS00001801C (11-20-15)	Trademarks page	Updated trademarks listing
	Worldwide Sales	Updated sales listing
	Table 2, “Memory Format for Configuration Register Access,” on page 4	Removed empty row.
	Table 32, “PIO 40-47 Direction Register,” on page 19	Updated: **Bit 7:6**: Updated name. **Bit 1** to **Bit 5**: Update descriptions.
DS00001801B (03-03-15)	Cover	Updated title
	Trademarks page	Updated trademarks listing
	Worldwide Sales	Updated sales listing
	All	Changed all hex value notation to “xxxxh” for consistency
	Table 8, “Configuration Register Memory Map,” on page 6	Added/updated registers: **080Ah-0954h**: PIO registers **3006h-3008h**: Updated Names **3016h-30CFh**: mfr./product/serial string registers **30FDh**: Hub controller remap register **3114h-3120h**: USB2.0 BOS descriptor registers **3C20h-3C40h**: USB OCS source select registers **3C52h**: SUSPEND Select register **4194h-4292h**: Hub controller string desc. registers **42ACh-42ADh**: USB spec. version registers **42B2h-42B3h**: Hub controller VID registers **42B4h-42B5h**: Hub controller PID registers **42B6h-42B7h**: Device BCD registers **42B8h**: Manufacturer string index register **42B9h**: Product string index register
	Table 9, “Register Default Values,” on page 9	Added default values for new registers (listed above)
	Table 10, “PIO Pin Numbers,” on page 11	Updated requirements column for PIO0, PIO17-PIO20, PIO41-PIO44
	Section 2.5.2, "Register Definitions," on page 11	Added register definitions for new registers (listed above)
	Section 2.5.2.1, "PIO Control," on page 11	Added additional information to PIO register descriptions
	Section 4.0, "OTP Configuration," on page 61	Added minor corrections
	Section 4.1.3, "Bit command (FEh)," on page 61	Updated description
	Section 4.1.3, "Bit command (FEh)," on page 61	Updated description
	Section 5.0, "USB Configuration," on page 64	Added new section
	Table 43, “Hub Configuration Data Byte 1,” on page 22, Table 44, “Hub Configuration Data Byte 2,” on page 23, Table 45, “Hub Configuration Data Byte 3,” on page 24	Added “HUB_” to name.

TABLE A-1: REVISION HISTORY (CONTINUED)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
DS00001801B (03-03-15) [continued]	Table 89, “USB Port1 OCS Source Select,” on page 41, Table 90, “USB Port2 OCS Source Select,” on page 41, Table 91, “USB Port 3 OCS Source Select,” on page 41, Table 92, “USB Port 4 OCS Source Select,” on page 42	Updated OCS_SEL field definitions.
	Table 93, “VBUS Pass Through,” on page 42	Updated description of HUB_CONN_PASS_THRU and USB_PASS_THRU bits.
DS00001801A (08-12-14)	REV A replaces previous SMSC version Rev. 0.8 (07-25-14)	
Rev. 0.8 (07-25-14)	Chapter 4	Added OTP Programming guidelines
Rev. 0.7 (06-07-13)	Document Release	

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