Ben Lancaster

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Experience

Senior CPU Design Engineer 2022 — Present
Arm Ltd - Processor Design Group *Cambridge, United Kingdom*

- Responsible for power/clock/reset design for all Arm Cortex A-class CPUs. Experience with CDC and RDC analysis.
- Specification and design of Cortex A-class CPUs for client and datacentre products.
- Design exploration for various new Armv9 architectural features (SME2, RME, GICv5).
- Rethinking microarchitecture across multiple clock and power domains to improve efficiency and performance.
- Extending CPU designs to support ASIL B/D (ISO 26262) for automotive and safety critical applications.
- Implementing Dual-Core Lock Step (DCLS) for fault detection across asynchronous crossings.

System IP Design Engineer 2019 — 2022
Arm Ltd - Interconnect Group *Cambridge, United Kingdom*

- Unit design lead for a System Level Cache product for the Memory System Filtering unit, Error reporting unit, and Performance Monitoring unit.
- L3 cache design with AMBA CHI and AXI5 interfaces, with qualify of service features and DRAM-aware controls.
- Team champion for pushing automation flows for generating synthesizable SystemVerilog RTL from machine-readable specifications.

Firmware Engineer, Intern 2015 — 2016
Spirent Communications - Satellite Positioning Group *Paignton, United Kingdom*

- Mixed-signal design for software-defined multi-frequency GNSS signal generators using Xilinx UltraScale FPGAs.
- Implemented algorithm for dynamic power attenuation/calibration using programmable DACs for consistent signal power.
- Experience using various test equipment (oscilloscopes, spectrum analysers, function generators, power meters).

Education

University of Leeds Leeds, United Kingdom
MSc (Eng) Embedded Systems - Electrical Engineering, 1st *2018 — 2019*

- Dissertation: Multi-core RISC SoC Design and Implementation for FPGAs | Deans List.
- Courses: FPGA Design for System-on-Chip, Digital Signal Processing for Communications, Embedded Systems, Signals and Systems, Control Systems, Microprocessor System Design.

University of Plymouth Plymouth, United Kingdom
BSc (Hons) Computer Science, 1st *2014 — 2018*

- Top Final Year Student, Best Final Project, Revell Research Systems Price.
- Final Project: Design of an FPGA soft-microprocessor and custom 16-bit RISC instruction set.

Projects

PCB development board for FPGA and Cortex-M0

- Designed a 2-layer printed circuit board for a Xilinx FPGA development kit to communicate with an STM32F0 TSSOP chip to provide software control and move software work loads to the FPGA. Features mutliple power supplies, I2C, in-circuit debugging header, and LEDs.

Custom programming language

- Designed a compiler and code generator for a C-like programming language that compiles into a custom instruction set that runs on an custom FPGA CPU. Supports functions, local variables, recursion, stack frames.

Skills

- **Hardware**: SystemVerilog, Digital design, Mixed signal design, CPU microarchitecture, Caches, PCB design.
- **Software**: Python, C, Perl.
- **Languages**: English (native), Spanish (C2)
- **Hobbies**: Running, Tennis, Sailing