Ben Lancaster

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EXPERIENCE

RTL Design Engineer **ARM Limited** **September 2019 – present**

- Design and verification of various Systems and Interconnect IP using SystemVerilog.
- IP requirements capture and specification.
- Programmers-view RTL for memory-mapped peripherals.
- Automation and rendering flows for generating RTL/UVM from machine-readable specifications.
- Physical implementation trials using Cadence and Synopsys tooling flows.
- Verification of AMBA protocols and other on-chip interfaces.

Firmware Engineer, Placement **Spirent Communications** **June 2016 – August 2017**

- Embedded programming on Xilinx MicroBlaze FPGAs and PIC16/24 microcontrollers.
- Implemented on-chip power levelling and calibration for GNSS RF signal generators.
- Controlling on-board fans, LEDs, EEPROM, and other peripherals with I2C and SMBus.
- Configuring, building, and maintaining Embedded Linux distributions using Yocto.
- Linux USB kernel driver development.

EDUCATION

MSc (Eng) Embedded Systems Engineering **University of Leeds** **2018-2019**

- 86%, Final Project: Multi-core RISC SoC Design and Implementation for FPGAs.
- Courses include: FPGA Design for System-on-Chip, Digital Signal Processing for Communications, Embedded Microprocessor System Design, Circuits, Medical Electronics and E-Health

BSc (Hons) Computer Science **University of Plymouth** **2014 – 2018**

- Top Final Year Student, Best Final Project, Revell Research Systems Price
- Final Project: FPGA-based 16-bit RISC soft-microprocessor (with IO & interrupts) and Compiler.
- First Class Honours with Certificate of Professional Industrial Experience.
- Courses: Digital Electronics, Embedded Systems and Compilers, Machine Vision, Parallel Computation.

OPEN-SOURCE PROJECTS & CONTRIBUTIONS

- Multi-core RISC System-on-Chip bendl/vmicro16 Up to 96 cores on Spartan-6 and Cyclone V FPGAs.
- 16-bit RISC soft-microprocessor bendl/prco304 An FPGA-based RISC soft-microprocessor written in Verilog, complete with Compiler and programming language.
- ARM Cortex M0 Processor Board bendl/armm0 A 2-layer board for the Minispartan6+ FPGA development kit. Features an STM32F0 TSSOP processor, dual power supplies, I2C, ICSP, and LEDs.

ADDITIONAL EXPERIENCE & AWARDS

- Top Final Year Student
- Best Final Project
- Dean's List 2015-2018 member
- Revell Research Systems Prize

TECHNOLOGIES

- Digital Design, CMOS, IC Design
- IP Integration
- Verilog, SystemVerilog
- Cadence, Xilinx/Altera FPGAs, Vivado/ISE, Quartus,
- C, C++, Python, Linux (user + kernel), Bash, Make, CUDA