Ben Lancaster

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EXPERIENCE

Arm - Central Engineering 2019 – present
RTL Design Engineer *United Kingdom*

- Worked on micro-architecture specification and RTL design of a fully-coherent System Level Cache for an upcoming 5nm IP targeting high-end smartphones.
- Responsible for the programming architecture, configuration register network, register block design, for distributing configuration registers throughout a design for an upcoming IP.
- Created automation and rendering flows for generating synthesisable SystemVerilog RTL from machine-readable specifications.
- Designed and implemented post-silicon debug features for MMU-700's Translation Buffer and Translation Control Unit compatible with Arm CoreSight ELA-600.
- Experience using physical implementations flows from Cadence to understand and improve design PPA.
- Experience implementing AMBA interfaces including CHI, AXI, and APB.

Spirent Communications 2016 - 2017
Firmware Engineer, Placement *United Kingdom*

- Using Xilinx Virtex UltraScale+/Spartan FPGAs for RF signal generation (UHF).
- Embedded C programming for Xilinx MicroBlaze and PIC16/24 micro-controllers.
- Controlling EEPROMs, LEDs, on-board fans, and other peripherals with I2C and SMBus.
- Configuring, building, and maintaining Embedded Linux distributions using Yocto.
- Linux USB and PCIe kernel driver development.

EDUCATION

University of Leeds 2018 – 2019
MSc (Eng) Embedded Systems Engineering *United Kingdom*

- 86%, Final Project: Multi-core RISC SoC Design and Implementation for FPGAs.
- Courses include: FPGA Design for System-on-Chip, Digital Signal Processing for Communications, Embedded Microprocessor System Design, Circuits, Medical Electronics and E-Health

University of Plymouth 2014 – 2018
BSc (Hons) Computer Science *United Kingdom*

- Top Final Year Student, Best Final Project, Revell Research Systems Price
- Final Project: FPGA-based 16-bit RISC soft-microprocessor (with IO & interrupts) and CFG Compiler
- Courses: Digital Electronics, Embedded Systems and Compilers, Machine Vision, Parallel Computation

ADDITIONAL EXPERIENCE & AWARDS

- Best Final Project
- Top Final Year Student
- Dean's List 2015-2018 member
- Revell Research Systems Prize

OPEN-SOURCE PROJECTS & CONTRIBUTIONS

- Multi-core RISC System-on-Chip. Can fit up to 96 cores on Spartan-6 and Cyclone V FPGAs.
- 16-bit RISC ISA and FPGA CPU. Written in Verilog, complete with Compiler for C-like programming language.
- Custom PCB with an ST Cortex M0 and debugging header. A 2-layer board for the Minispartan6+ FPGA development kit. Features an STM32F0 TSSOP processor, dual power supplies, I2C, ICSP, and LEDs.