數位電路設計 (Digital Circuit Design)

Lab2：組合電路之 HDL 模組撰寫與測試 (Writing and Testing the HDL Modules of Combinational Circuits)

1. 目標 (Goal)

在這次 Lab 中，我們希望同學們可以熟悉減法器以及 BCD 加法器的設計原理，以 **gate-level modeling**、**dataflow modeling**、**behavioral modeling** 等不同方式撰寫其 HDL 電路模組，並撰寫測試模組。分別模擬後，繳交模組檔案與波形圖。

The main purpose of this Lab Unit is to be familiar with the design of a binary substractor and BCD adder. Please write their HDL circuit modules by gate-level modeling, dataflow modeling, and behavioral modeling, and write the testbench for these circuit modules. After simulation, upload the files of the modules and the waveforms of the simulation results.

2. 撰寫 HDL 電路模組與測試模組（Design of the HDL Circuit Modules and Testbench)

A. **半減器(Half Substractor)**：設計一個半減器(half subtractor, HS)，有兩個輸入變數及兩個輸出變數。輸入變數為被減數 *x* 與減數 *y*；輸出變數為差值 *D* 與借位輸出 *B*。

Design a half subtractor (HS) which has 2 input variables and 2 output variables. The input variables are the minuend (被減數) ***x*** and the subtrahend (減數) ***y***, and the output variables produce the difference ***D*** and the borrow-out ***B***.

i. 請以 gate-level modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_half_sub_gate_level(output D, B, input x, y)，檔案則命名為 Lab2_half_sub_gatelevel.v。

Please write the Verilog circuit module in gate-level modeling. The circuit module and port list should be named as

Lab2_half_sub_gatelevel(output D, B, input x, y), and its file should be named as Lab2_half_sub_gatelevel.v .

ii. 請以 dataflow modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_half_sub_dataflow(output D, B, input x, y)，檔案則命名為 Lab2_half_sub_dataflow.v。

Please write the Verilog circuit module in dataflow modeling. The circuit module and port list should be named as Lab2_half_sub_dataflow(output D, B, input x, y), and its file should be named as Lab2_half_sub_dataflow.v .

iii. 請以 behavior modeling 方式撰寫其 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_half_sub_behavior (output D, B, input x, y)，檔案則命名為 Lab2_half_sub_behavior.v。

Please write the Verilog circuit module in behavior modeling. The circuit module and port list should be named as Lab2_half_sub_behavior (output D, B, input x, y), and its file should be named as Lab2_half_sub_behavior.v .

iv. 請撰寫一測試模組來測試上述三個以不同方式撰寫之半減器電路模組，請將此測試模組命名為 t_Lab2_half_sub，檔案則命名為 t_Lab2_half_sub.v

Please write a testbench to test the half-substractor circuit module which is described in three different way above. The testbench module should be named as t_Lab2_half_sub, and its file should be named as t_Lab2_half_sub.v

B. **全減器(Full Substractor)**：設計一個全減器(full subtractor, FS)，有三個輸入變數及兩個輸出變數。輸入變數為被減數 *x*、減數 *y*、及借位輸入 *z*；輸出變數為差值 *D* 與借位輸出 *B*。
Design a full subtractor (FS) which has 3 input variables and 2 output variables. The input variables are the minuend (被減數) ***x***, the subtrahend (減數) ***y***, and the borrow-in ***z***, and the output variables produce the difference ***D*** and the borrow-out ***B***.

i. 請利用 **2.A(i)**中的 gate-level 半減器來建構全減器。請撰寫出全減器

之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_full_sub(output D, B, input x, y, z)，檔案則命名為 Lab2_full_sub.v。
Please use the gate-level half-substractor designed in **2.A(i)** to construct the full-substractor. Plase write the HDL circuit module of the full-substractor. The circuit module and port list should be named as Lab2_full_sub(output D, B, input x, y, z), and its file should be named as Lab2_full_sub.v.

ii. 請撰寫全減器之測試模組，命名為 t_Lab2_full_sub，檔案則命名為 t_Lab2_full_sub.v。

Please write the testbench of the full-substractor. The testbench module should be named as t_Lab2_full_sub, and its file should be named as t_Lab2_full_sub.v.

C. **四位元漣波借位減法器(4-bit Ripple Borrow Subtractor, RBS)：**設計一個四位元漣波借位減法器，以產生兩個四位元二進位數字相減之結果。其輸入變數為四位元二進位被減數 ***X***、四位元二進位減數 ***Y***、及借位輸入 ***Bin***，輸出變數為四位元二進位差值 ***Diff*** 與借位輸出 ***Bout***。
Design a 4-bit binary subtractor which may produce the arithmetic difference of two 4-bit binary numbers. The input variables are the 4-bit binary minuend (被減數) ***X*** , the 4-bit subtrahend (減數) ***Y,*** and the borrow-in ***Bin***, and the output variables produce the 4-bit difference *Diff* and the borrow-out ***Bout***.

i. 利用 **2.B(i)** 中之全減器來建構此 4-bit Ripple Borrow Subtractor (RBS)。請撰寫出此 RBS 之 HDL 電路模組，模組名稱與 port list 請訂為 Lab2_ripple_borrow_4_bit_sub (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin)，檔案命名為 Lab2_ripple_borrow_4_bit_sub.v。

Please use the full substractor designed in **2.B(i)** to construct the 4-bit Ripple Borrow Subtractor (RBS). Please write the HDL circuit module of the RBS. The circuit module and port list should be named as Lab2_ripple_borrow_4_bit_sub (output [3:0] Diff, output Bout, input [3:0] X, Y, input Bin), and its file should be named as Lab2_ripple_borrow_4_bit_sub.v

ii. 請撰寫此 RBS 之測試模組，至少以下述六組測資測試之。請將此測試模組命名為 t_Lab2_ripple_borrow_4_bit_sub，檔案則命名為

t_Lab2_ripple_borrow_4_bit_sub.v。

Please write the testbench of the RBS in which at least six test data showed in the following figure should be included. The testbench module should be named as t_Lab2_ripple_borrow_4_bit_sub, and its file should be named as t_Lab2_ripple_borrow_4_bit_sub.v.

X	Y	Bin
1101	0101	0
1101	0101	1
0101	1101	0
0101	1101	1
0101	0101	0
1101	1101	1

D. **BCD 加法器(BCD Adder)**：設計一個可將兩個 BCD 數字及進位輸入相加的組合電路。其輸入變數為四位元 BCD 數字 ***A*** 與 ***B***，以及進位輸入 ***Cin***；輸出變數為四位元 BCD 和值 ***Sum*** 與進位輸出 ***Cout***。
Design a combinational circuit for the arithmetic addition of two decimal digits in BCD, together with an input carry. The input variables are the 4-bit BCD digits, ***A*** and ***B***, and the input carry ***Cin***, and the output variables are the 4-bit sum in BCD, ***Sum***, and the output carry, ***Cout***.

i. 請以 bevhavior modeling 方式撰寫 BCD 加法器之 HDL 電路模組，其模組名稱與 port list 請訂為 Lab2_BCD_adder_behavior (ouput [3:0] Sum, output Cout, input [3:0] A, B, input Cin)，檔案命名為 Lab2_BCD_adder_behavior.v。

Please write the HDL circuit module of BCD Adder in behavior modeling. The circuit module and port list should be named as Lab2_BCD_adder_behavior (ouput [3:0] Sum, output Cout, input [3:0] A, B, input Cin), and its file should be named as Lab2_BCD_adder_behavior.v .

ii. 請撰寫此 BCD adder 之測試模組，至少以下述六組測資測試之。請將此測試模組命名為 t_ Lab2_BCD_adder_behavior，檔案則命名為 t_Lab2_BCD_adder_behavior.v。

Please write the testbench of the BCD adder in which at least six test data showed in the following figure should be included. The testbench module should be named as t_ Lab2_BCD_adder_behavior, and its file should be named as t_Lab2_BCD_adder_behavior.v .

A	B	Cin
0100	0010	0
0100	0010	1
0101	0110	0
0101	0110	1
1001	0111	0
1001	0111	1

E. 注意事項 ：(Notes)

- 請用 ModelSim Student Edition 10.4a 做為開發環境。
  Develop your lab in ModelSim Student Edition 10.4.a.

- 請務必依照上述各項目之規定命名模組及檔案。
  Be sure to name the modules and files as described above.

- 禁止抄襲，違者(抄襲者與被抄襲者)以 0 分計算。
  Any assignment work by fraud will get a zero point.

- 助教會以其他測資去測試上述作業。
  TA will use similar Testbench modules with different test data to verify the correctness of your design of the Verilog circuit modules.

3. 作業及 HDL 模組繳交(Hand in)

A. 作業報告繳交：word 檔，命名為 Lab2_學號_姓名

包含下列項目：

(1) 2A iv (半減器) 之模擬結果波形圖，並說明三個以不同方式撰寫之半減器電路模組之波形圖是否有差異及是否正確。
(2) 2B ii (全減器) 之模擬結果波形圖，並說明是否正確。
(3) 2C ii (4-bit RBS) 之模擬結果波形圖，並說明是否正確。
(4) 2D ii (BCD 加法器) 之模擬結果波形圖，並說明是否正確。
(5) 心得與感想、及遭遇到的問題或困難

Hand in a word file, named Lab2_StudentID_Name , including the following items:

(1) Give the waveforms of the simulation results for the three modules of the half subtractor tested in 2A iv, and determine whether the waveforms are correct or not and explain the difference of the waveforms, if any.

(2) Give the waveform of the simulation results for the module of the full subtractor tested in 2B ii, and explain whether it is correct or not.

(3) Give the waveform of the simulation results for the module of the 4-bit RBS tested in 2C ii, and explain whether it is correct or not.

(4) Give the waveform of the simulation results of the six test data for the module of the BCD adder tested in 2D ii, and explain whether it is correct or not.

(5) Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

B. Verilog modules 檔案繳交：10 files

Lab2_half_sub_gatelevel.v、Lab2_half_sub_dataflow.v、
Lab2_half_sub_behavior.v、t_Lab2_half_sub.v、
Lab2_full_sub.v、t_Lab2_ full_sub.v、
Lab2_ripple_borrow_4_bit_sub.v、t_Lab2_ripple_borrow_4_bit_sub.v、
Lab2_BCD_adder_behavior.v、t_Lab2_BCD_adder_behavior.v

Hand in the following Verilog modules: 10 files

Lab2_half_sub_gatelevel.v, Lab2_half_sub_dataflow.v,
Lab2_half_sub_behavior.v, t_Lab2_half_sub.v,
Lab2_full_sub.v, t_Lab2_ full_sub.v,
Lab2_ripple_borrow_4_bit_sub.v, t_Lab2_ripple_borrow_4_bit_sub.v,
Lab2_BCD_adder_behavior.v, t_Lab2_BCD_adder_behavior.v

4. DEADLINE

- 本實驗單元為一人一組， 作業請上傳至 E3 平台。
  This lab unit is one student per group. Please upload your Lab Report (word file) and the corresponding HDL code (.v files) onto e-Campus platform.

- 作業繳交截止日期為 **5/11 (三) 23:59**。**逾期繳交，每遲交一天滿分少 10%；至多四天。**

  The deadline for handing in lab report and Verilog files is **May 11 (Wed.) 23:59**. **The grade of delayed submission will be 10% off for each day. Late hand-in is limited to four days at most.**

- 請將上述作業報告及 Verilog 電路模組與測試模組檔案(.v)全部壓縮成一個 **zip 檔** (禁止上傳 rar 檔或是其他檔案格式)，並以「Lab2_學號_姓名」的方式命名，如 ： 「Lab2_0416000_王大明」。

  Please compress the word file of lab report and the Verilog circuit modules and testbench described above all into one **zip** file (rar file or other format is not accepted), and name the zip file as "Lab2_StudentID_Name" , for example, "Lab2_0416000_Kent Chang"

- Demo 時間暫定為 **5/17 (二) & 5/19 (四) 6:00pm~9:30pm**，之後會再發公告通知大家上網填寫 Demo 時間表。

  The demo time is arranged at **2016/5/17 (Tue.) & 2016/5/19 (Thur.) 6:00PM~9:30PM** tentatively, and we will send an announcement to inform you to fill the Demo schedule online.

- 程式碼請勿抄襲別人或讓別人抄襲，經查證後此次 lab 總分一律以 0 分計算。

  Any assignment work by fraud will get a zero point