Instruction to FPGA working environment

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What is the FPGA ?

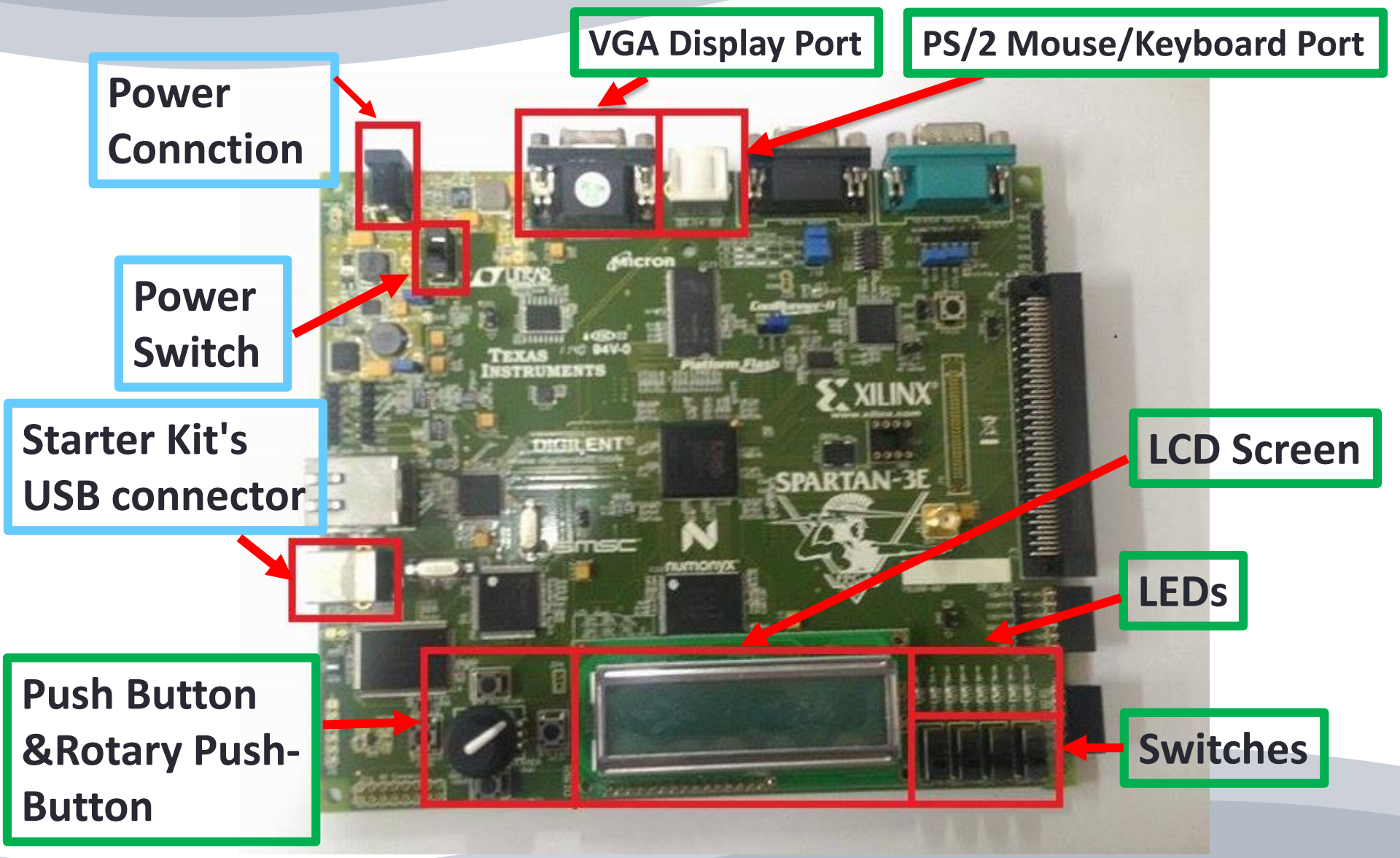
A **field-programmable gate array** (**FPGA**) is an integrated circuit . Engineers use FPGAs to implement and verify digital systems before production.

- **Advantage:**
  - Ability to re-program
  - Less debug cost
  - Lower engineering costs

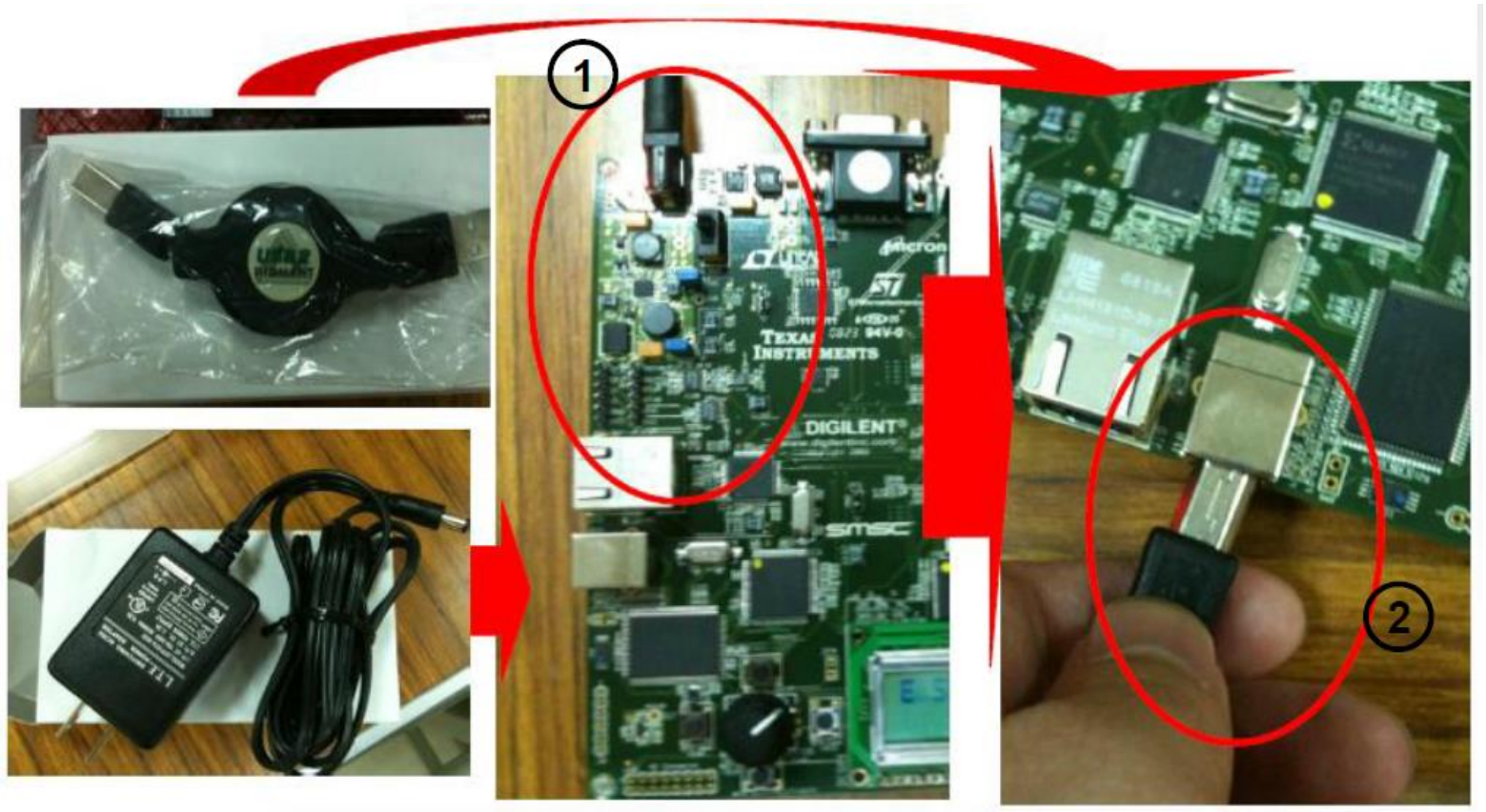
- **Shortcoming:**
  - Slower
  - Less energy efficient
  - Less functionality

Xilinx Spartan-3E Starter board

- **Family and Device:** Spartan-3E XC3S500E
- **On-Board Oscillator:** 50MHz
- **Key Components and Features**
  - 10/100 Ethernet PHY
  - Two 9-pin RS-232 Port
  - PS/2 Port
  - SMA clock input
  - Four slide switches
  - Eight discrete LEDs
  - Four push-button switches
  - VGA Display Port
  - 2-line, 16-character LCD screen


Power Connction
VGA Display Port
PS/2 Mouse/Keyboard Port
Power Switch
Starter Kit's USB connector
LCD Screen
LEDs
Push Button &Rotary Push-Button
Switches
TEXAS INSTRUMENTS
XILINX
DIGILENT
SPARTAN-3E

Installation



Attention

- **Avoid to touch the wires on the board which may cause static electricity.**
- **Always bind the wire by strap to avoid messing up the wires after use them.**

What is Xilinx ISE Design Suit

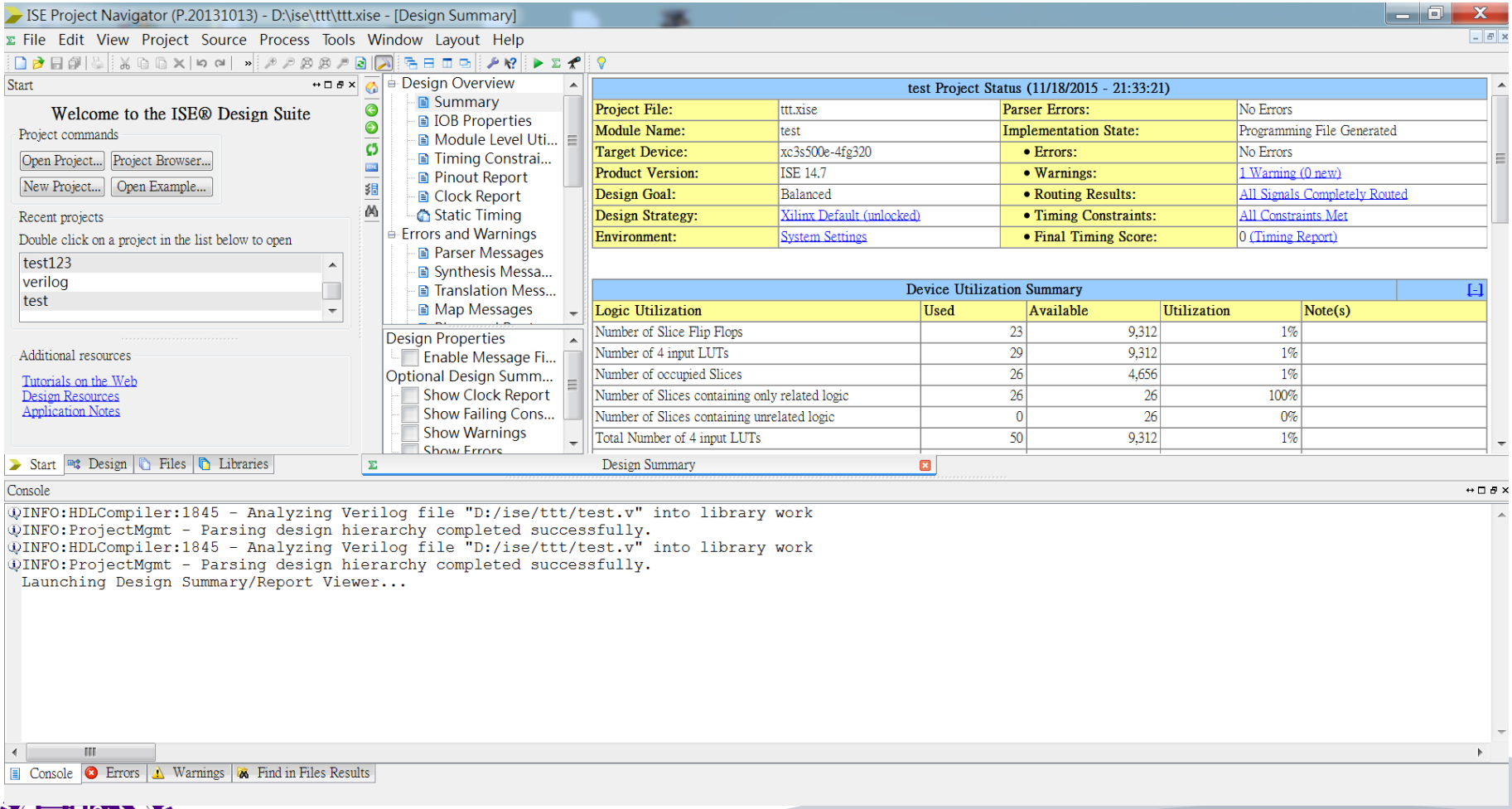
Xilinx ISE (**I**ntegrated **S**ynthesis **E**nvironment)

- ISE design suit is a software tool produced by Xilinx for synthesis and analysis of HDL designs.
- Developers can synthesize their designs , simulate the wave diagram ,and examine RTL diagram.
- Xilinx ISE Design Suit is a design environment for FPGA products.

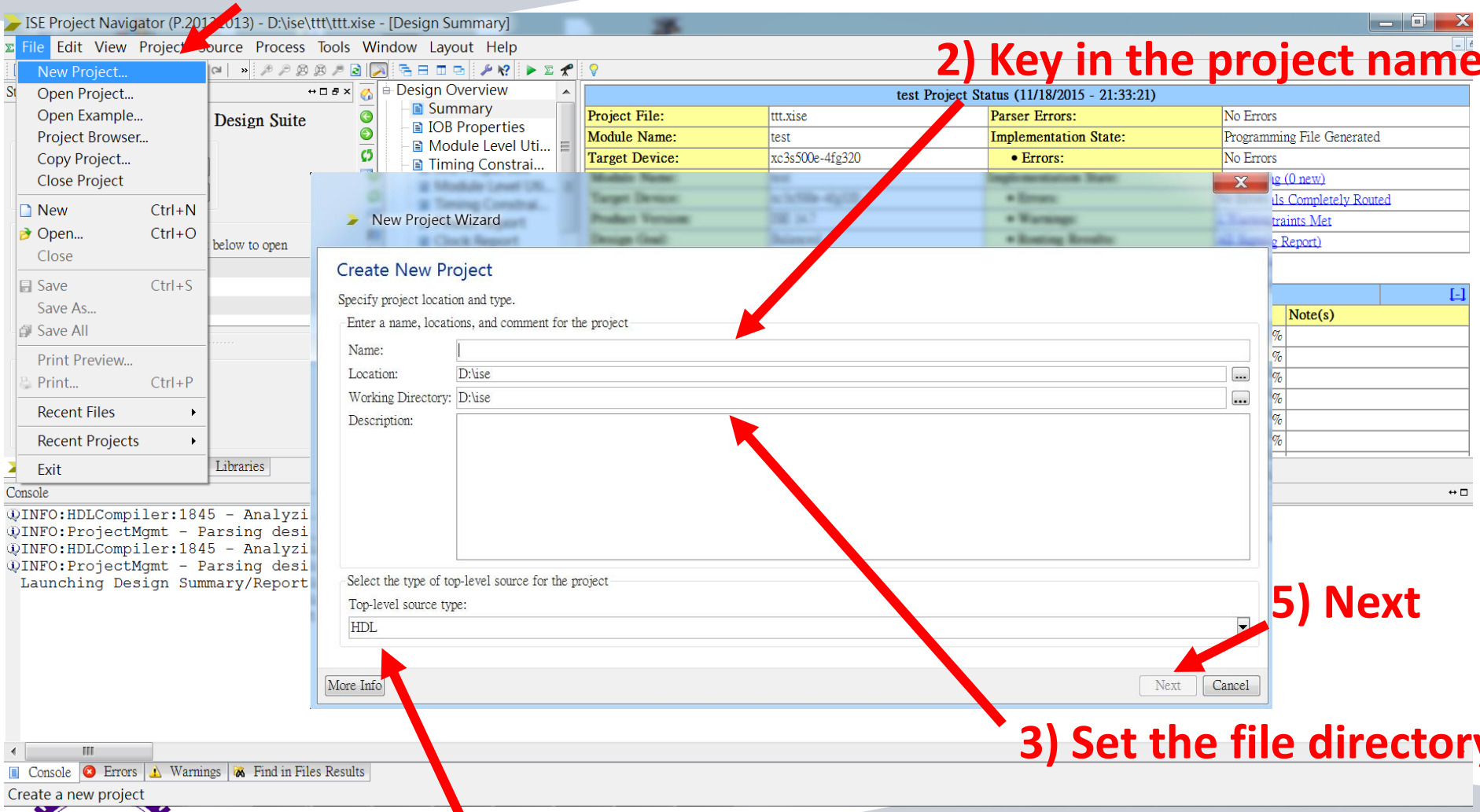
Open the Xilinx Project Navigator

First we start the Xilinx ISE software

Open the Xilinx Project Navigator



1) Creat a new project

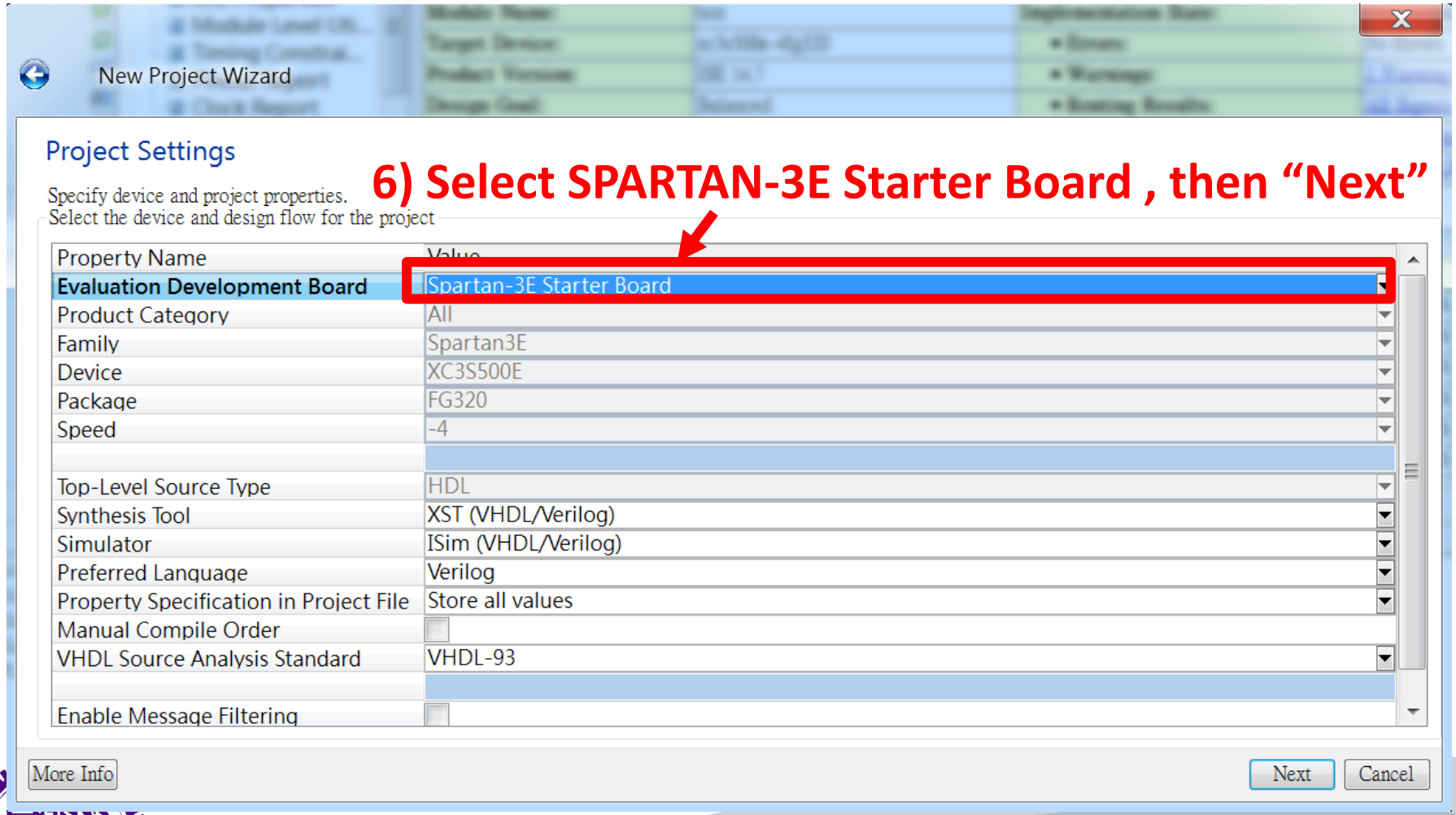


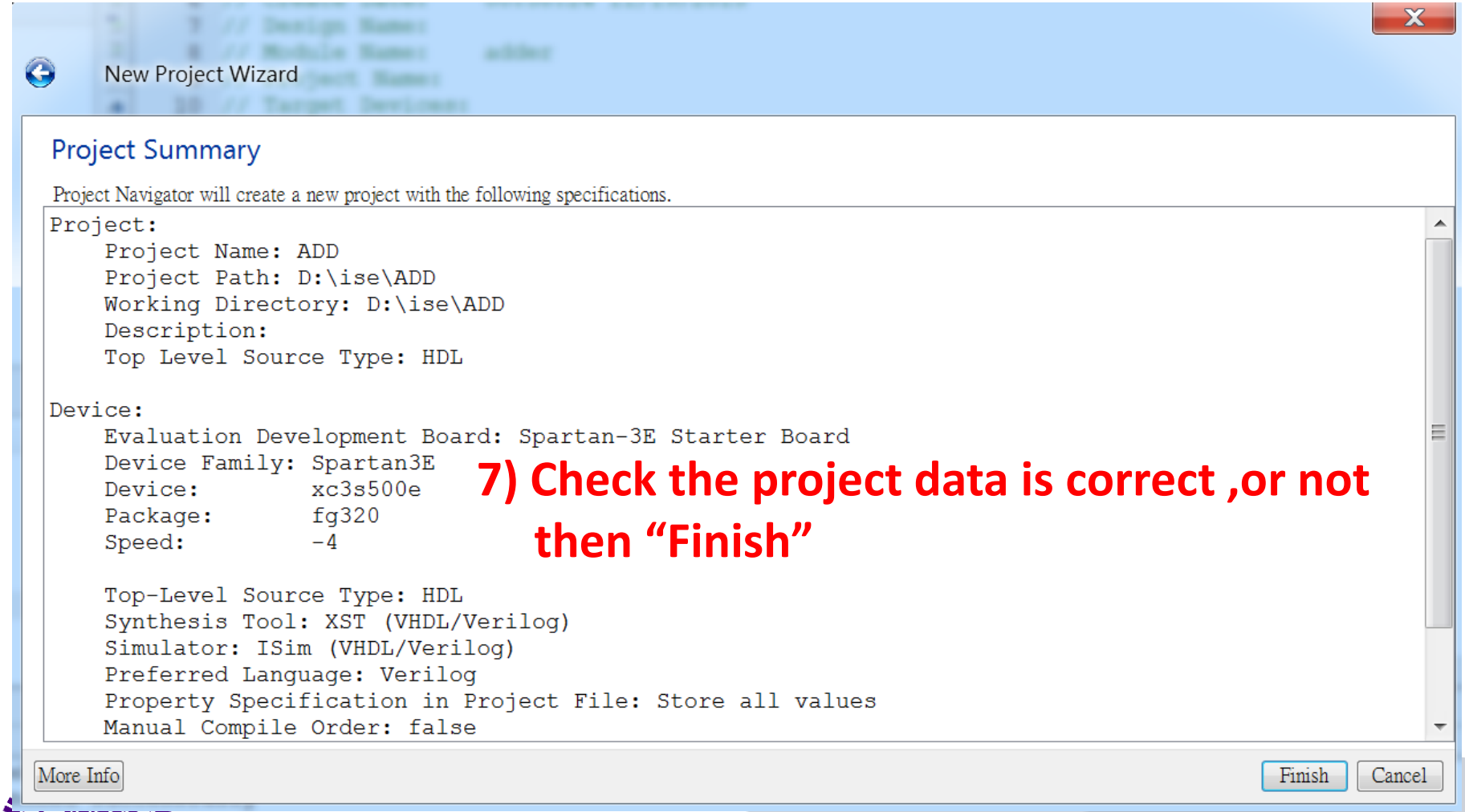
2) Key in the project name

3) Set the file directory

4) Select HDL

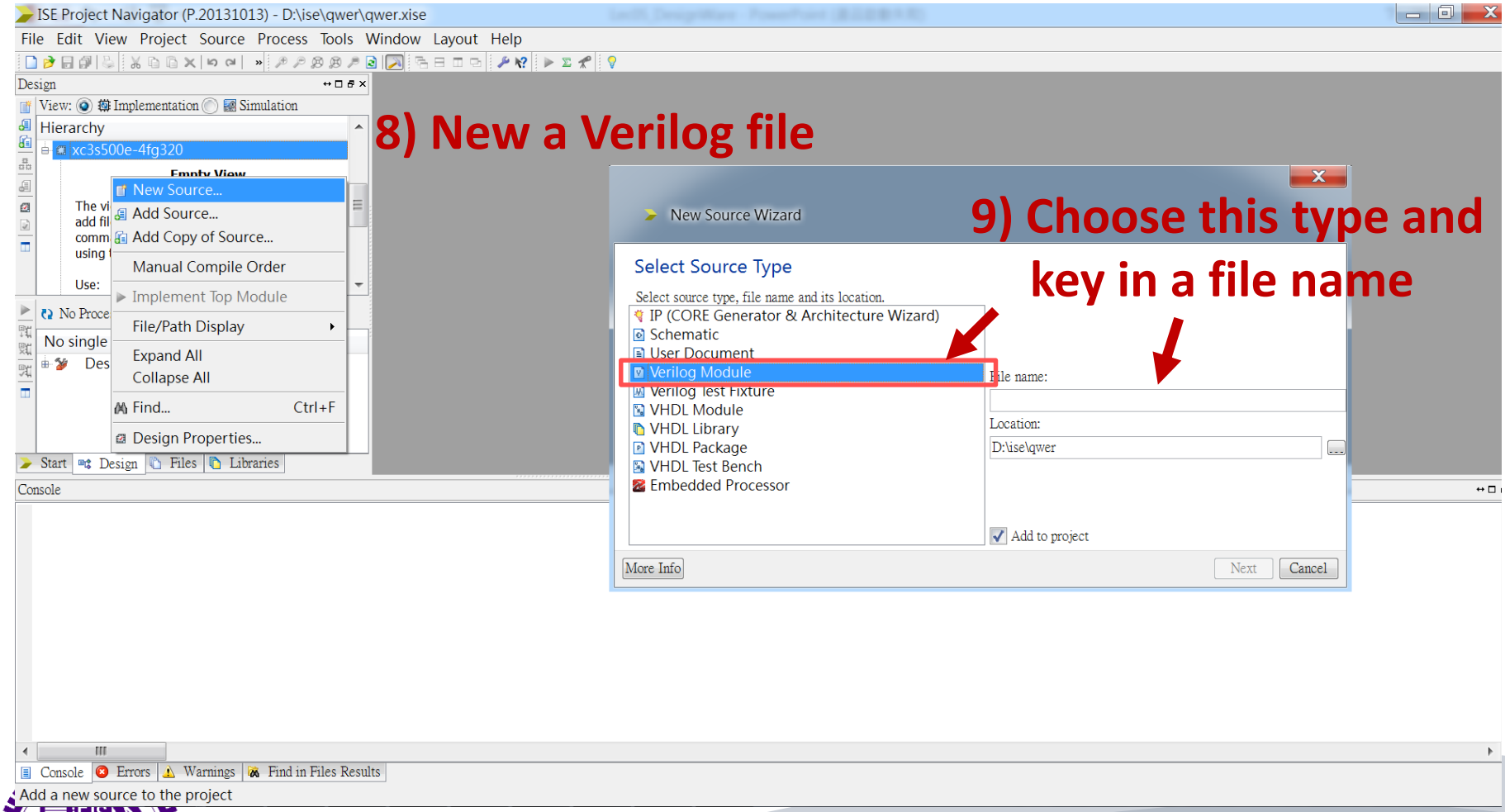
5) Next


New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
6) Select SPARTAN-3E Starter Board , then “Next”
Property Name
Value
Evaluation Development Board
Spartan-3E Starter Board
Product Category
All
Family
Spartan3E
Device
XC3S500E
Package
FG320
Speed
-4
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
Next
Cancel

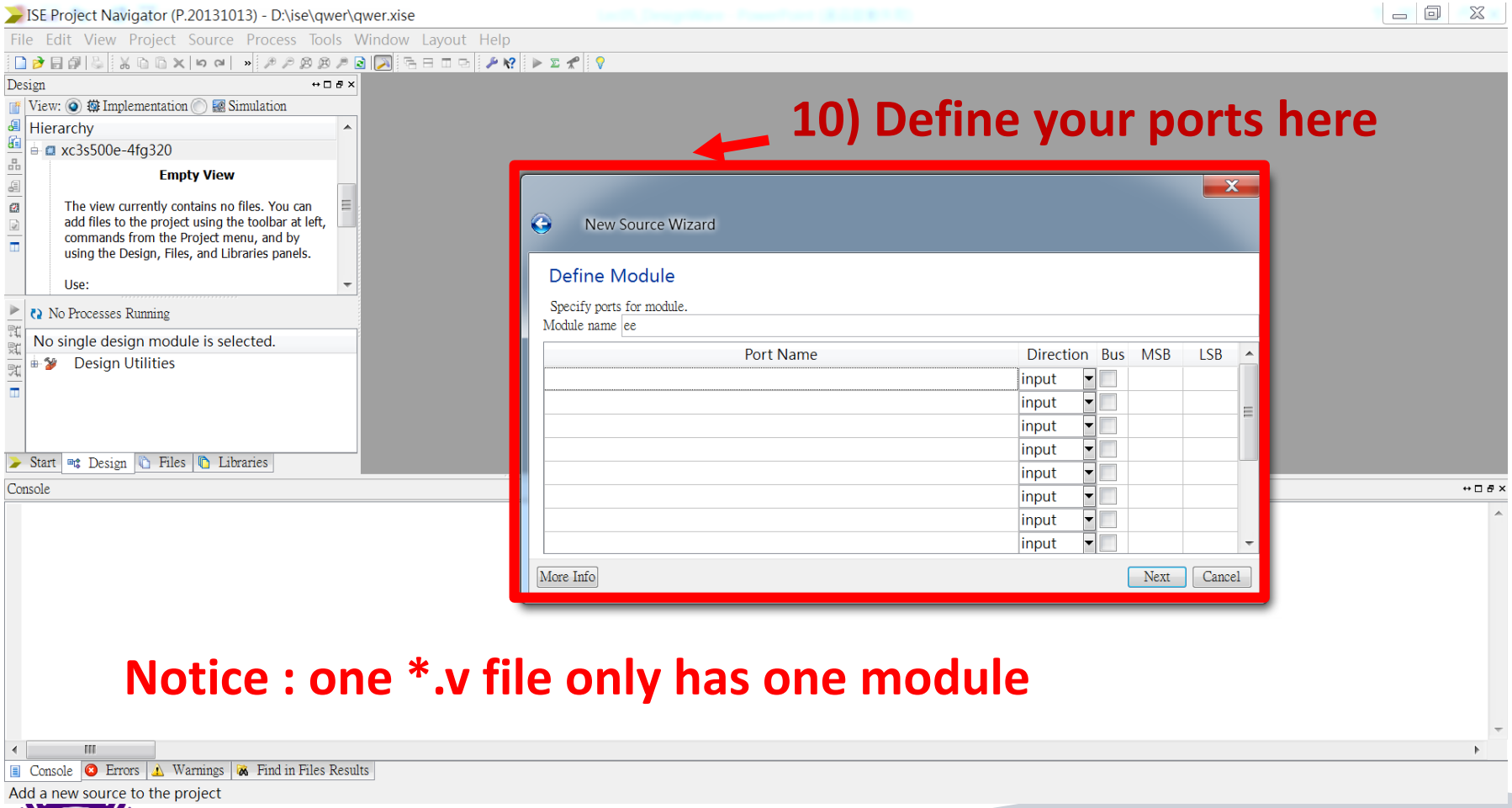


7) Check the project data is correct ,or not then “Finish”

New a source

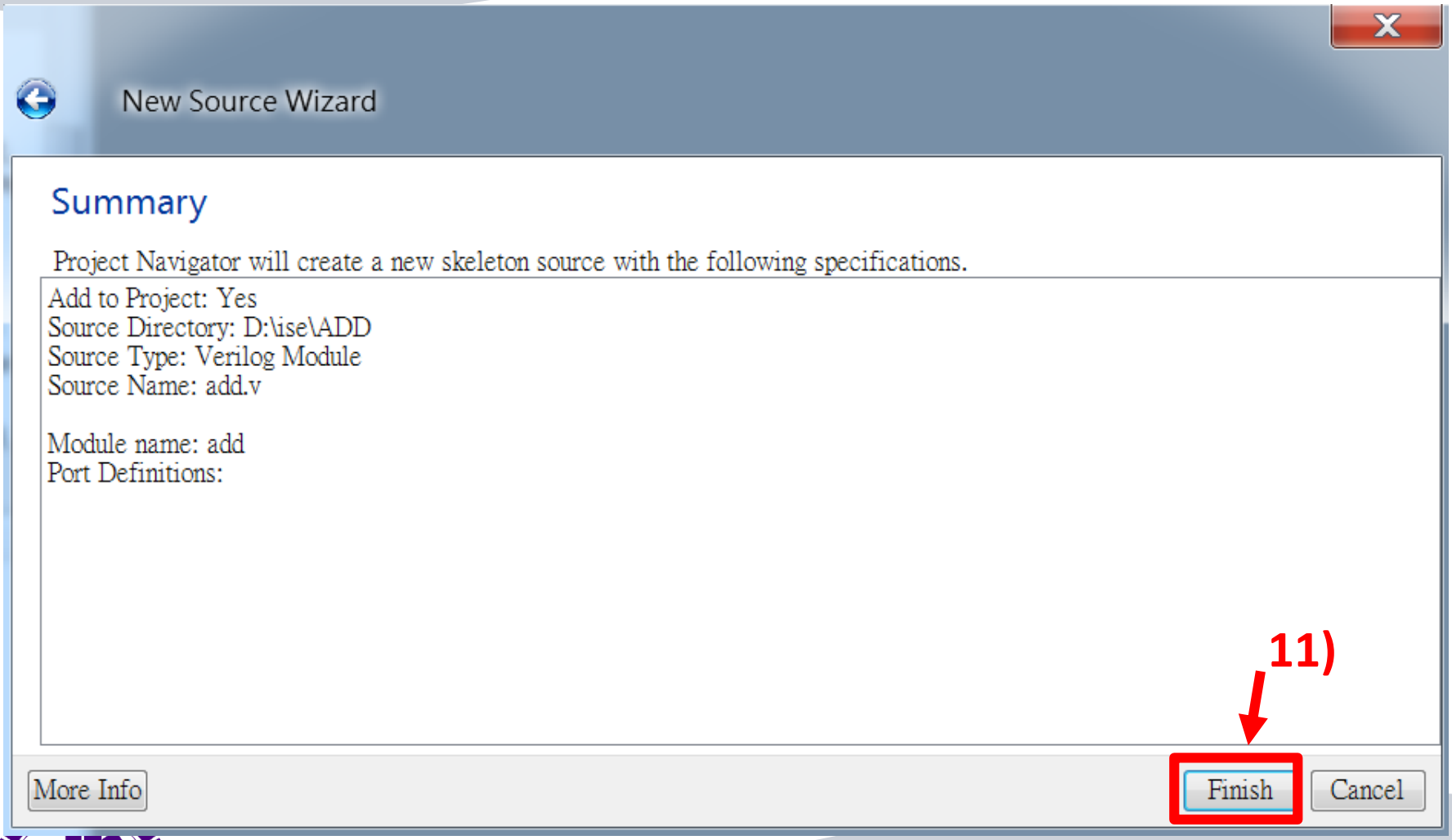

ISE Project Navigator (P.20131013) - D:\ise\qwer\qwer.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
xc3s500e-4fg320
New Source...
Add Source...
Add Copy of Source...
Manual Compile Order
Implement Top Module
File/Path Display
Expand All
Collapse All
Find... Ctrl+F
Design Properties...
Start Design Files Libraries
Console
Console Errors Warnings Find in Files Results
Add a new source to the project
8) New a Verilog file
New Source Wizard
Select Source Type
Select source type, file name and its location.
IP (CORE Generator & Architecture Wizard)
Schematic
User Document
Verilog Module
Verilog Test Fixture
VHDL Module
VHDL Library
VHDL Package
VHDL Test Bench
Embedded Processor
File name:
Location:
D:\ise\qwer
Add to project
More Info
Next
Cancel
9) Choose this type and key in a file name

New a source

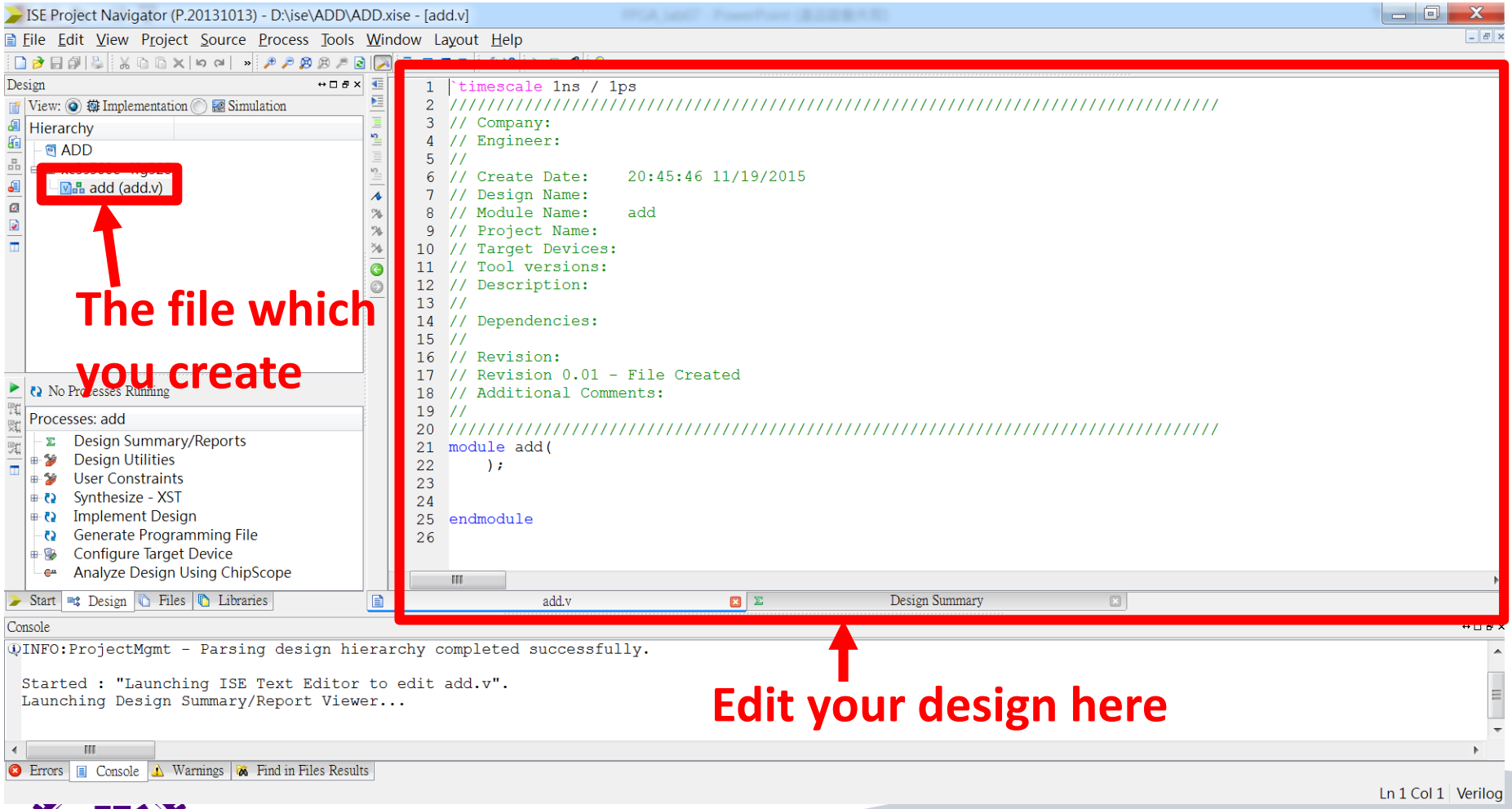


Notice : one *.v file only has one module

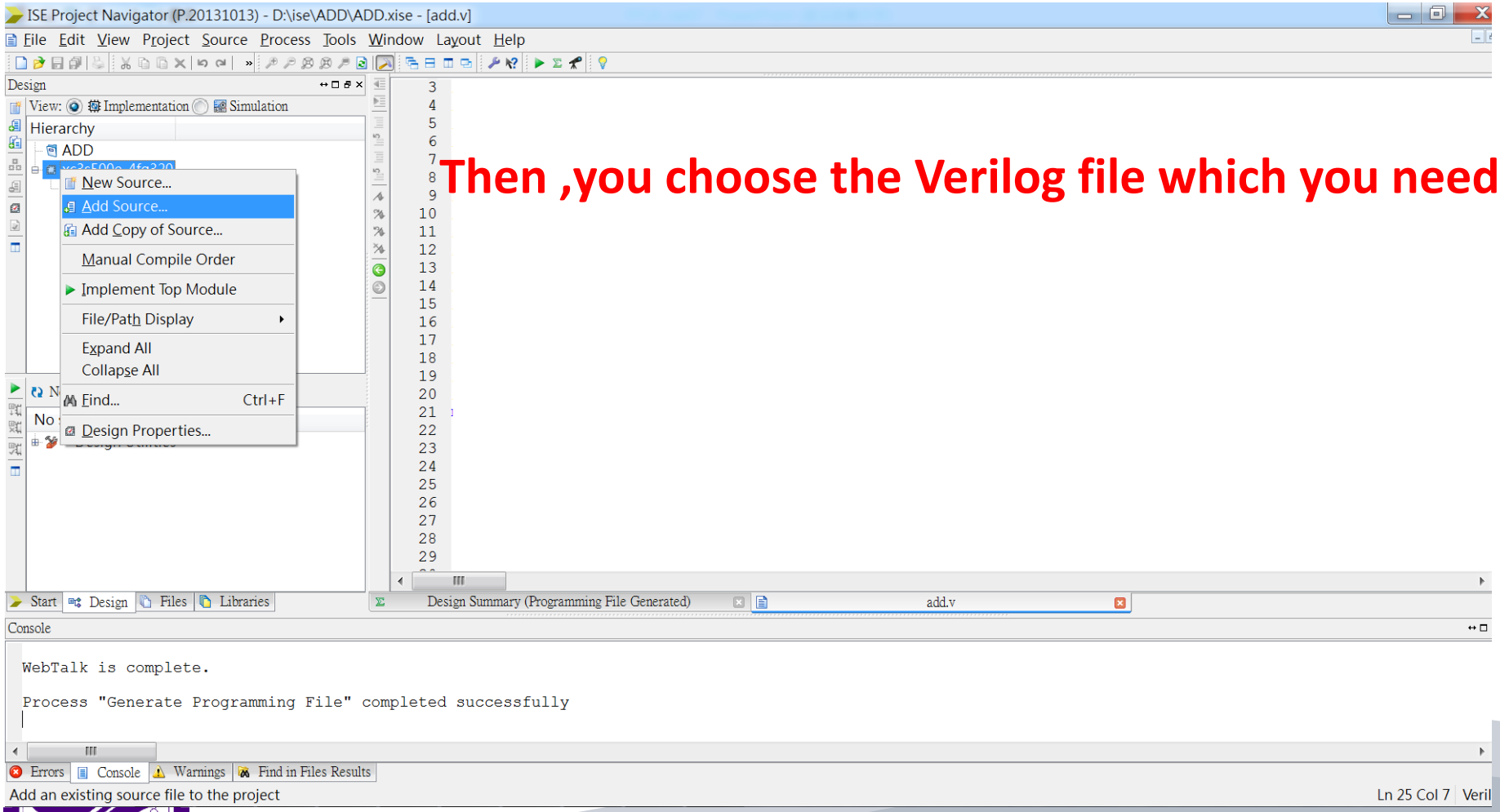
New a source


New Source Wizard
Summary
Project Navigator will create a new skeleton source with the following specifications.
Add to Project: Yes
Source Directory: D:\ise\ADD
Source Type: Verilog Module
Source Name: add.v
Module name: add
Port Definitions:
11)
More Info
Finish
Cancel

New a source

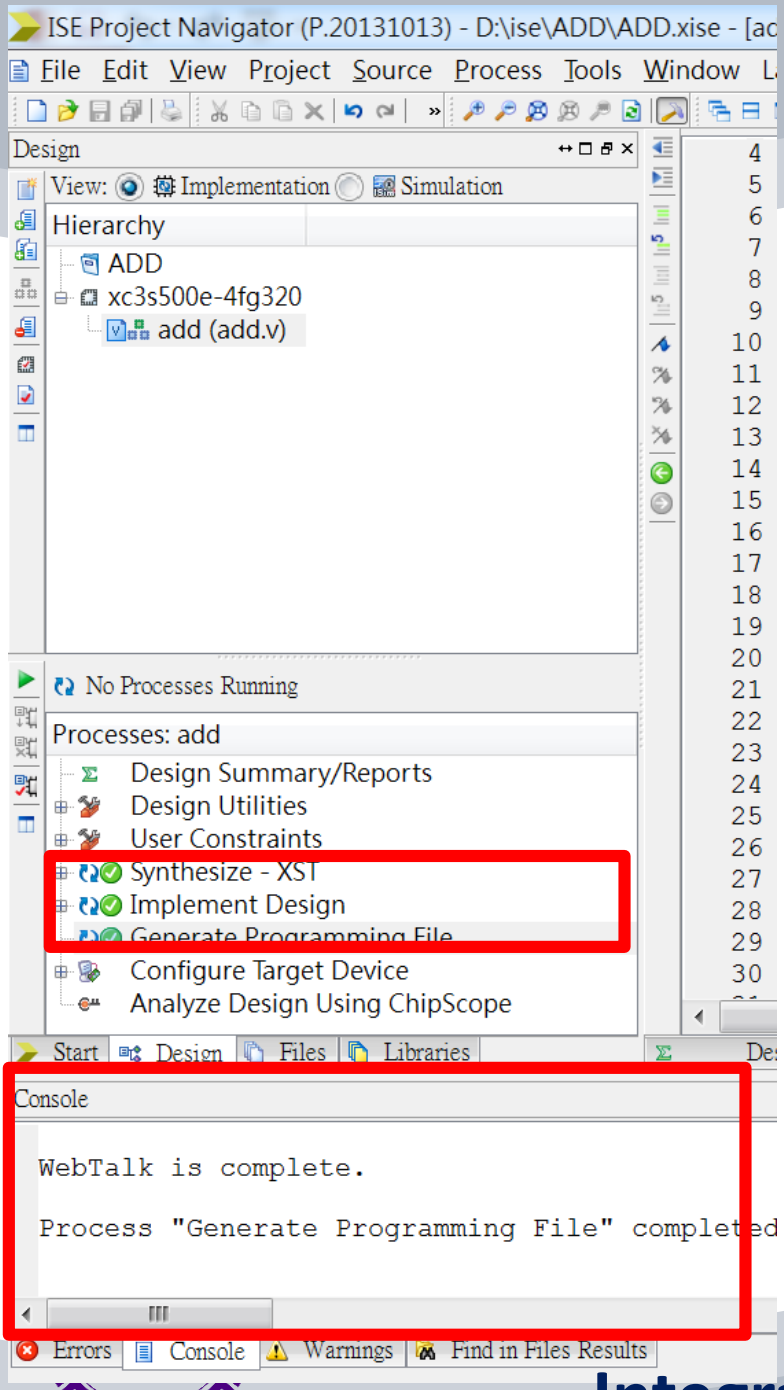

ISE Project Navigator (P.20131013) - D:\ise\ADD\ADD.xise - [add.v]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
ADD
add (add.v)
The file which you create
No Processes Running
Processes: add
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start Design Files Libraries
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 20:45:46 11/19/2015
7 // Design Name:
8 // Module Name: add
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module add(
22);
23
24
25 endmodule
26
add.v
Design Summary
Console
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit add.v".
Launching Design Summary/Report Viewer...
Errors Console Warnings Find in Files Results
Ln 1 Col 1 Verilog
Edit your design here

You can "**Add source**" if you have the Verilog file



Then ,you choose the Verilog file which you need.

Compile



- Double click “Synthesize - XST” for syntax checking
- Double click “Implement Design” for mapping connection file(.ucf) to your design and the platform
- There are four different icons for your design

 ->Warning

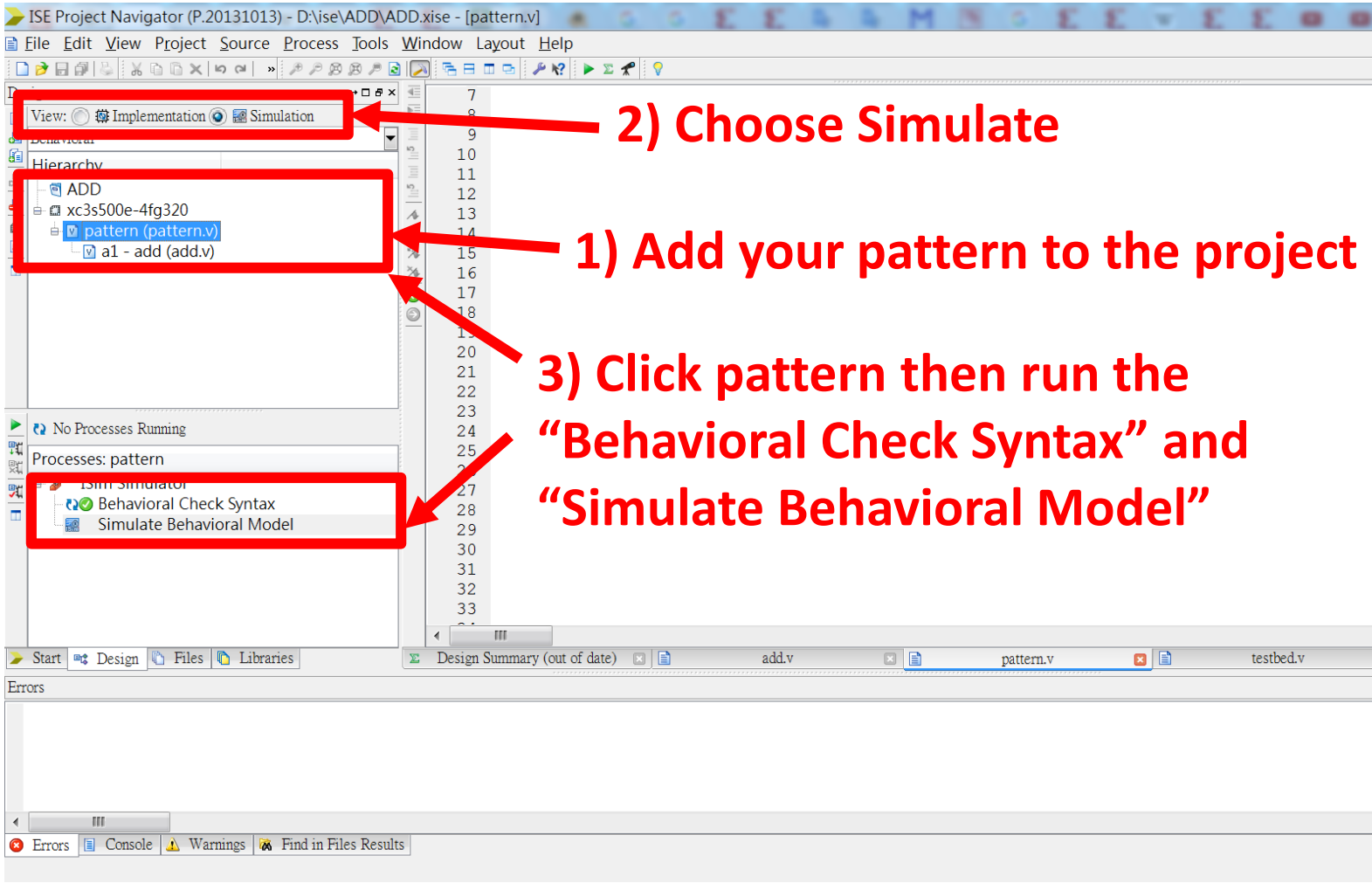
 ->your design is newer than before

 ->Error

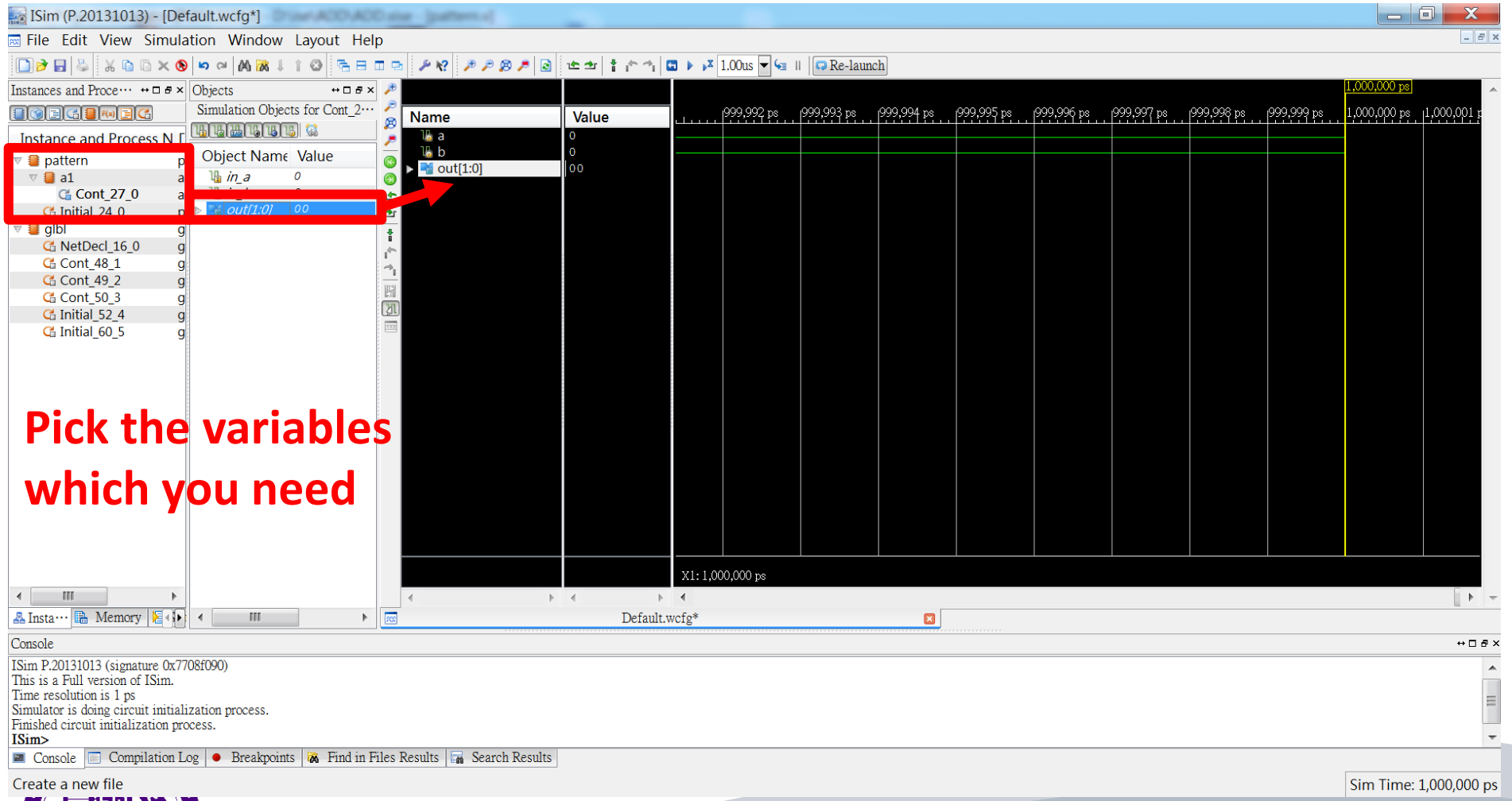
 ->Correct

- If your designs have errors, use the massages in the “Console Window” for debugging

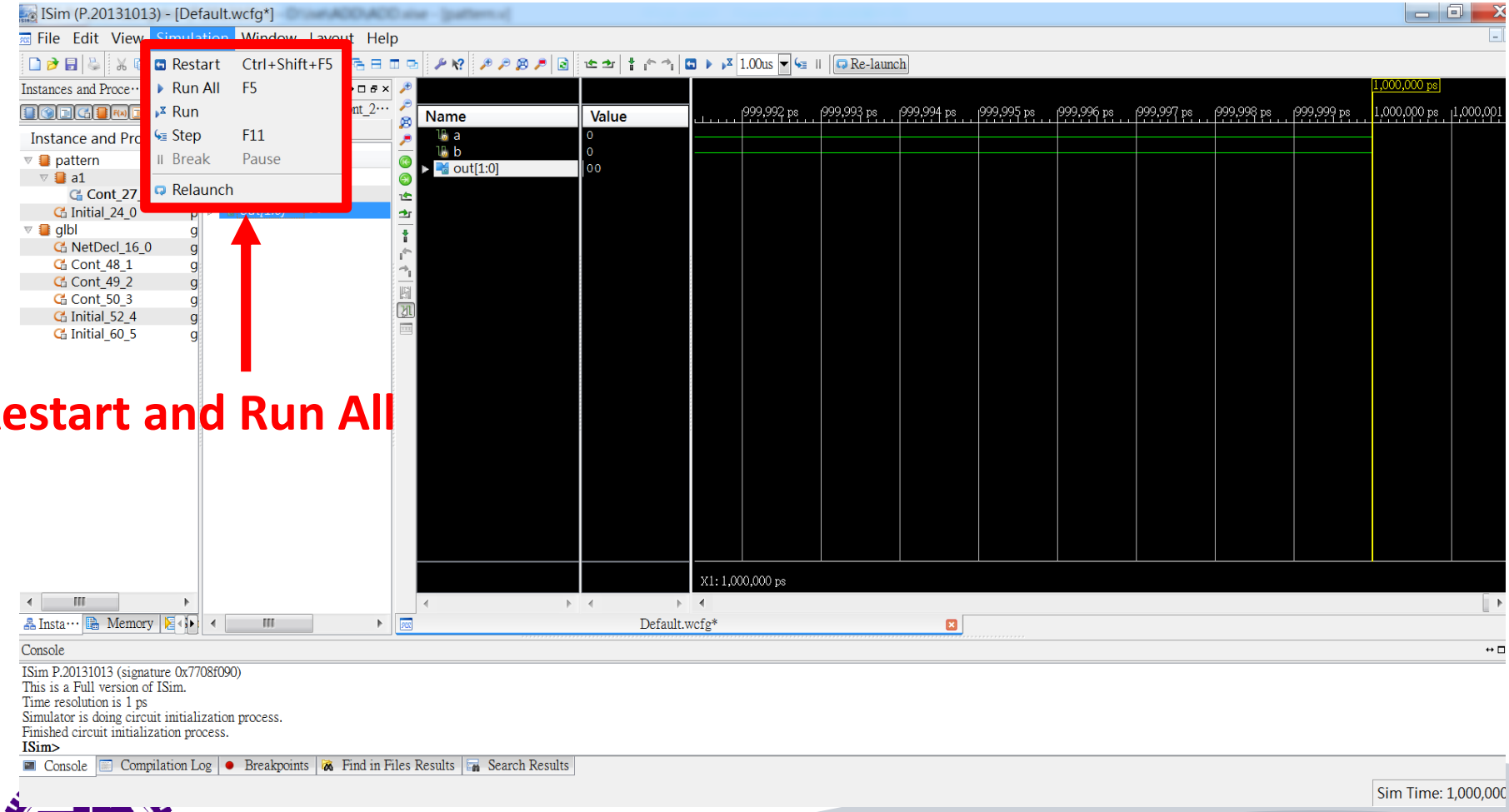
Add the pattern to simulate the design



Wave Diagram



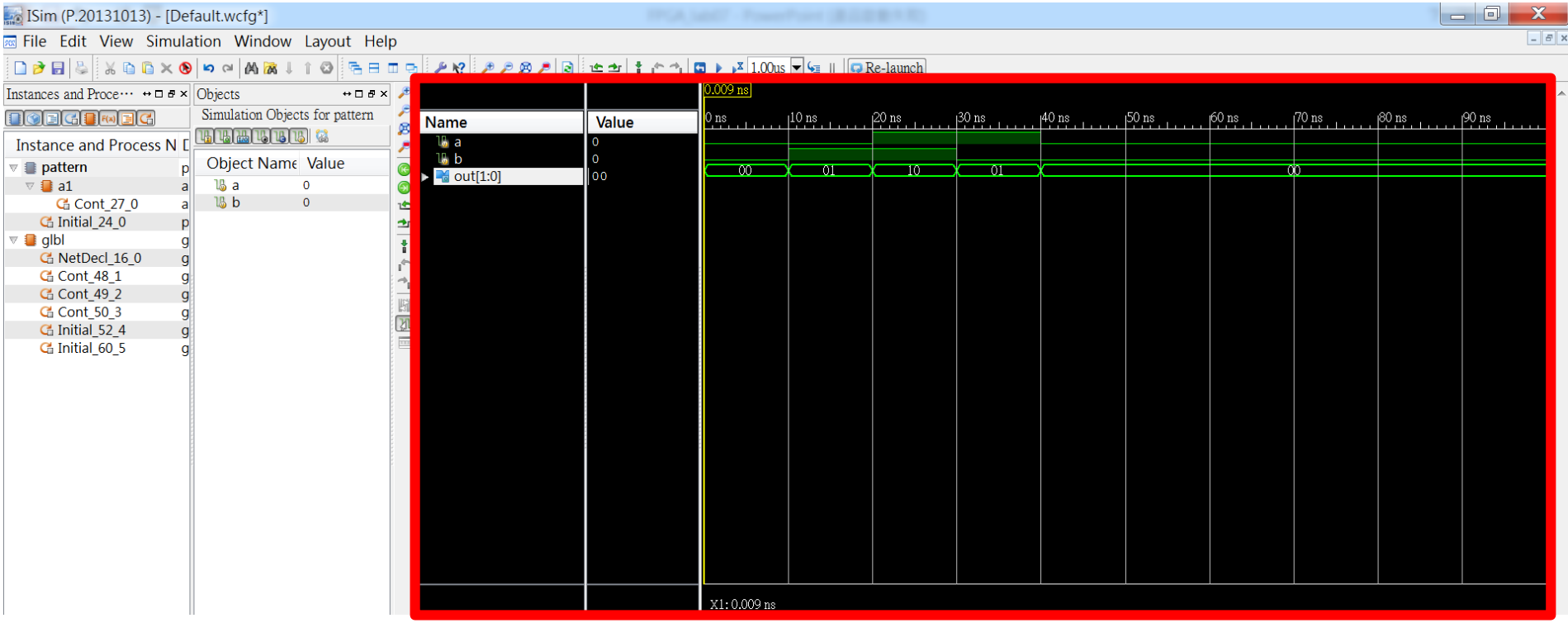
Wave Diagram



Restart and Run All

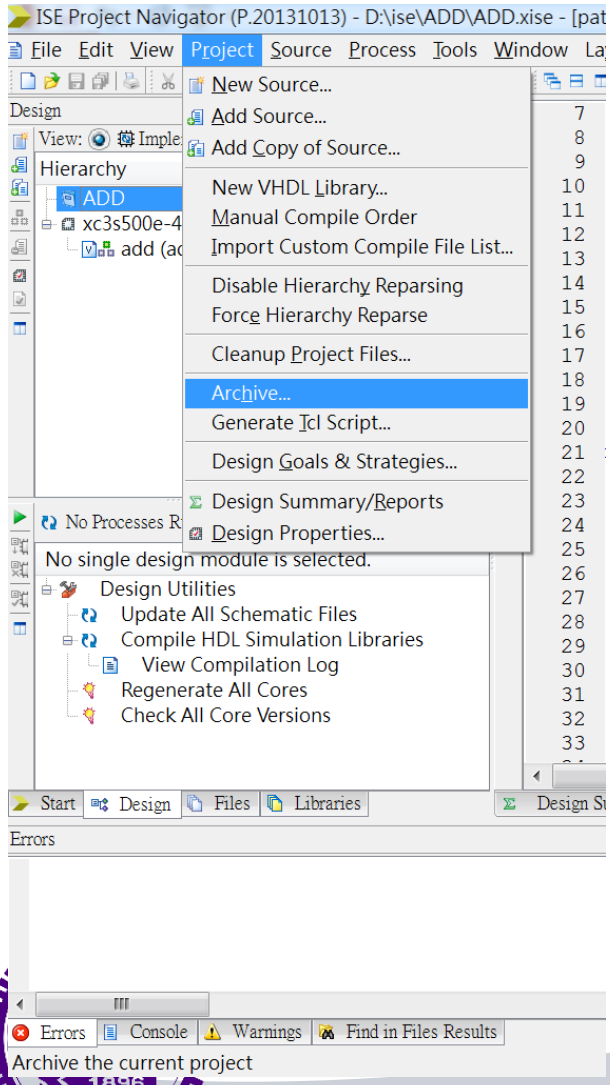
Wave Diagram

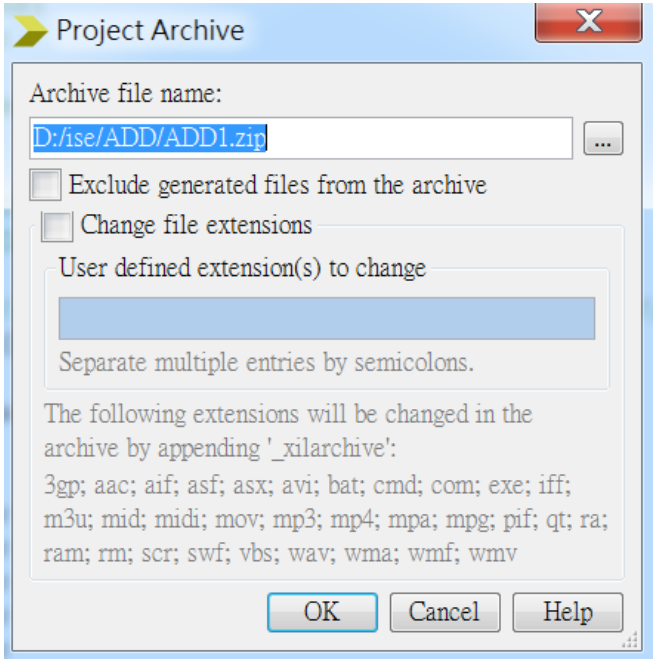
Wave Diagram



You get your wave

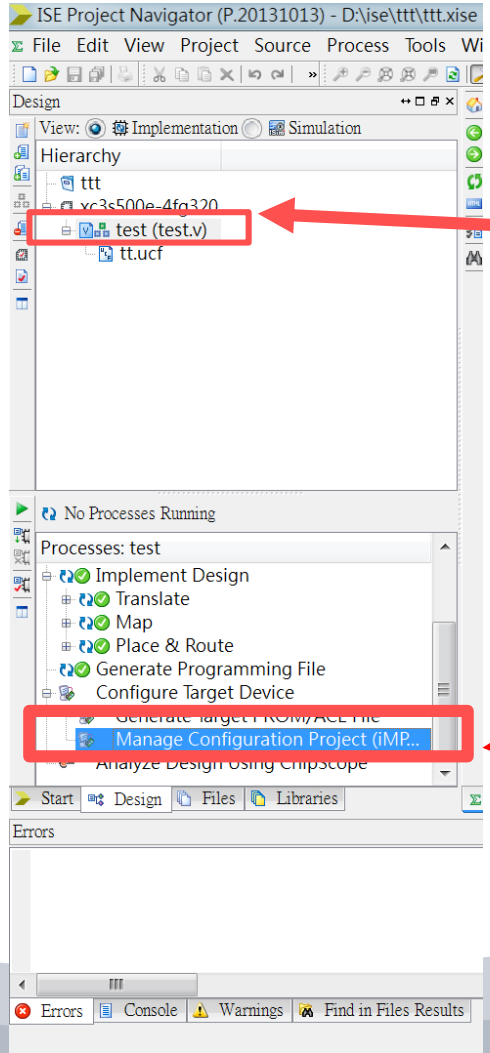
Archive


ISE Project Navigator (P.20131013) - D:\ise\ADD\ADD.xise - [pat
File Edit View Project Source Process Tools Window La
New Source...
Add Source...
Add Copy of Source...
New VHDL Library...
Manual Compile Order
Import Custom Compile File List...
Disable Hierarchy Reparsing
Force Hierarchy Reparse
Cleanup Project Files...
Archive...
Generate Tcl Script...
Design Goals & Strategies...
Design Summary/Reports
Design Properties...
Design
Hierarchy
ADD
xc3s500e-4
No single design module is selected.
Design Utilities
Update All Schematic Files
Compile HDL Simulation Libraries
View Compilation Log
Regenerate All Cores
Check All Core Versions
Start Design Files Libraries
Errors
Errors Console Warnings Find in Files Results
Archive the current project


Project Archive
Archive file name:
D:/ise/ADD/ADD1.zip
Exclude generated files from the archive
Change file extensions
User defined extension(s) to change
Separate multiple entries by semicolons.
The following extensions will be changed in the archive by appending '_xilarchive':
3gp; aac; aif; asf; asx; avi; bat; cmd; com; exe; iff; m3u; mid; midi; mov; mp3; mp4; mpa; mpg; pif; qt; ra; ram; rm; scr; swf; vbs; wav; wma; wmf; wmv
OK
Cancel
Help

Transplantation

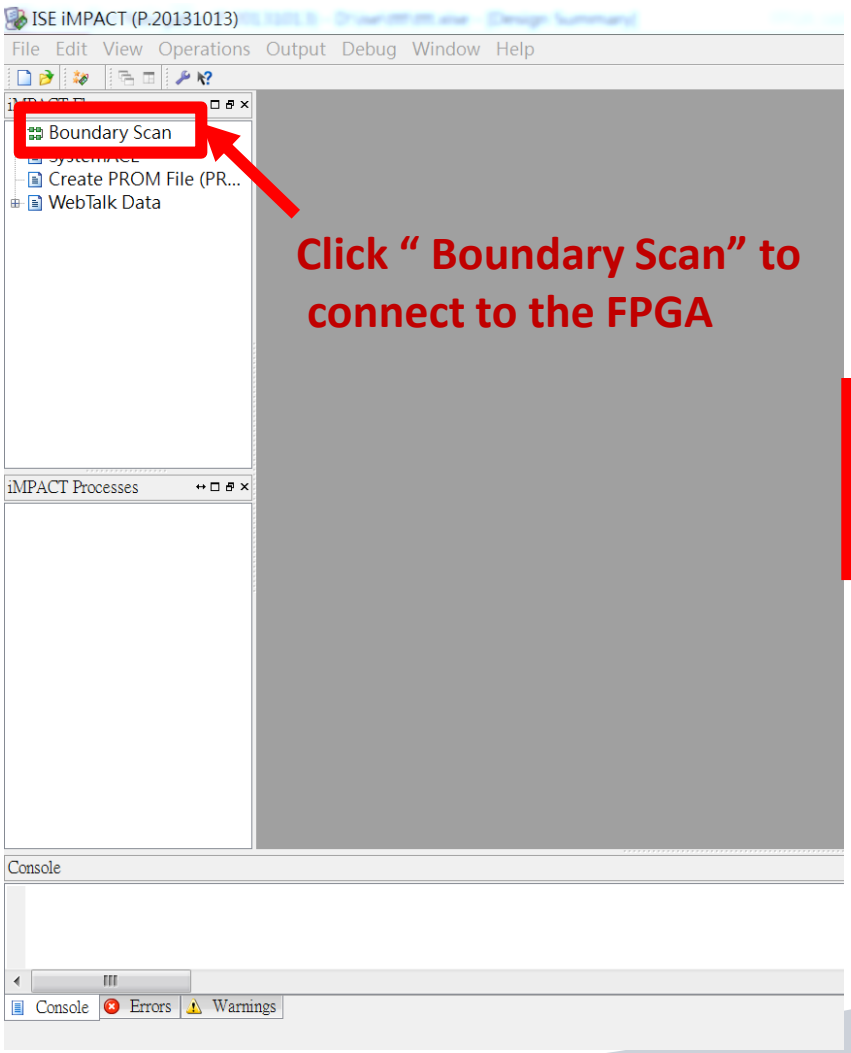
- After all your designs are correct, transplant your program file onto FPGA

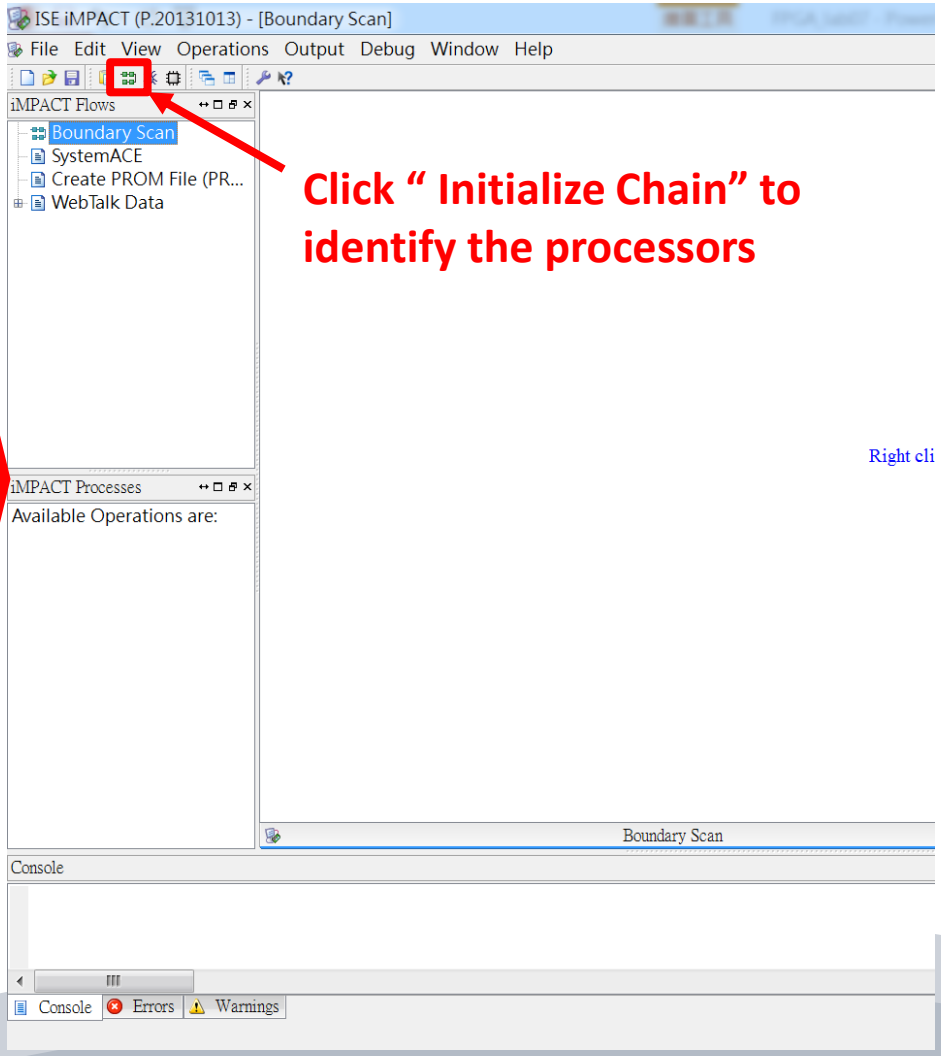


1) Select the top module of your design

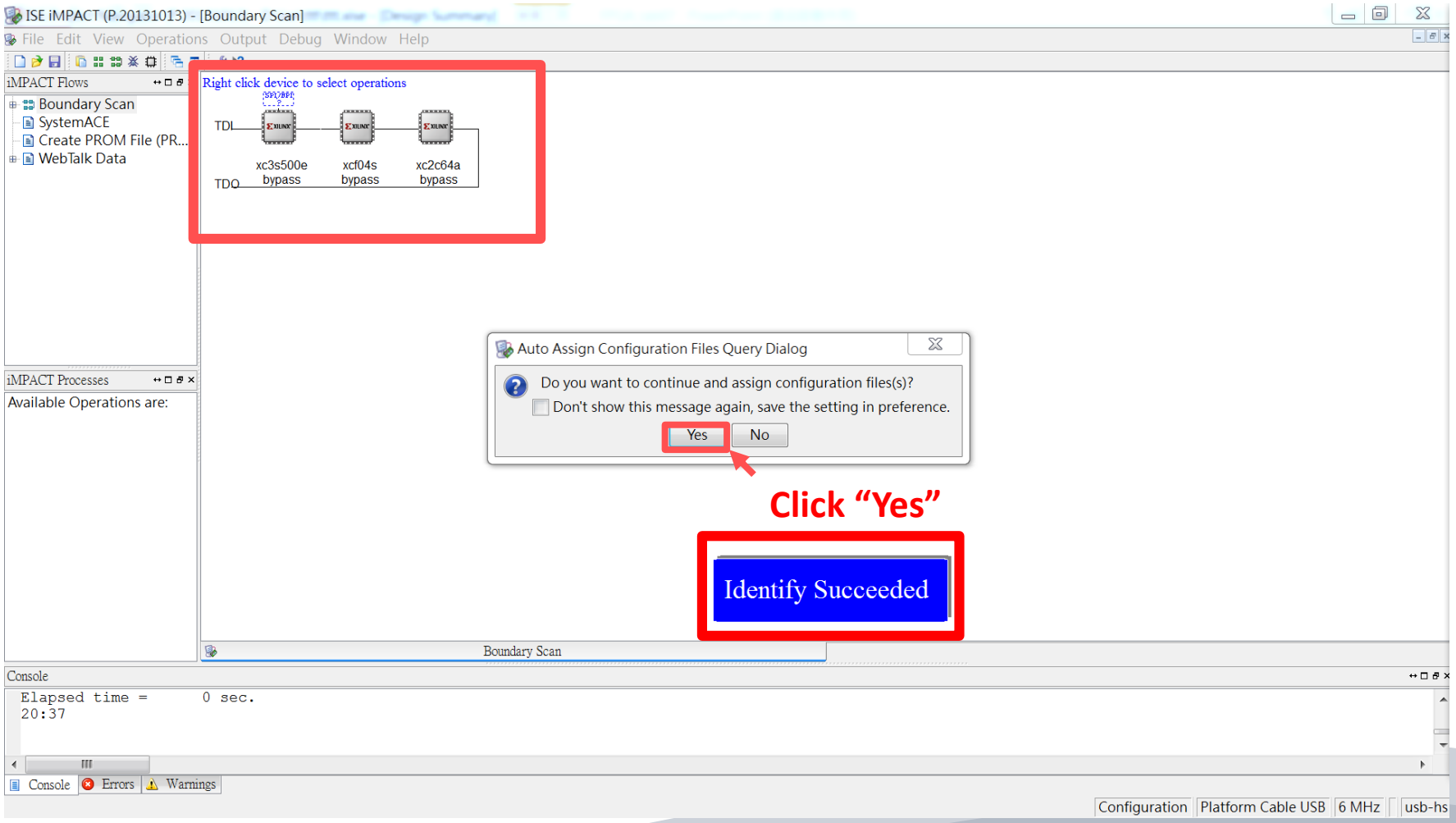
Double click “Manage Configuration Project(iMACT) ”to run generate programming file.

Transplantation





Transplantation



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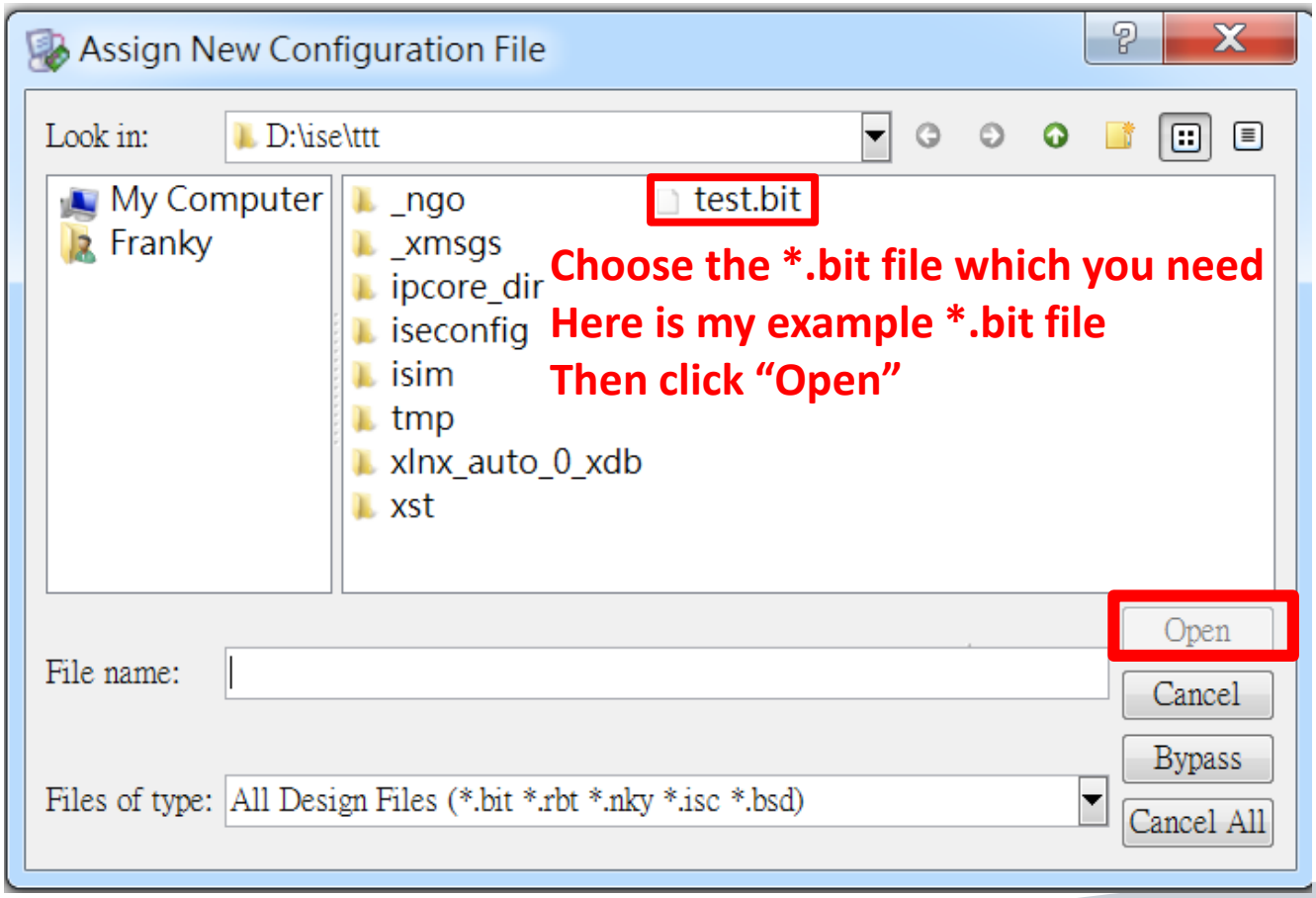
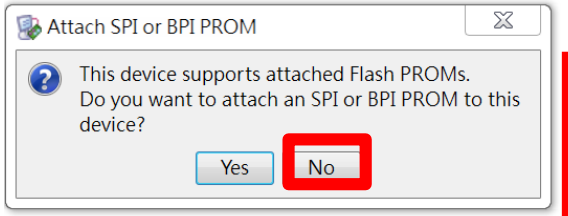
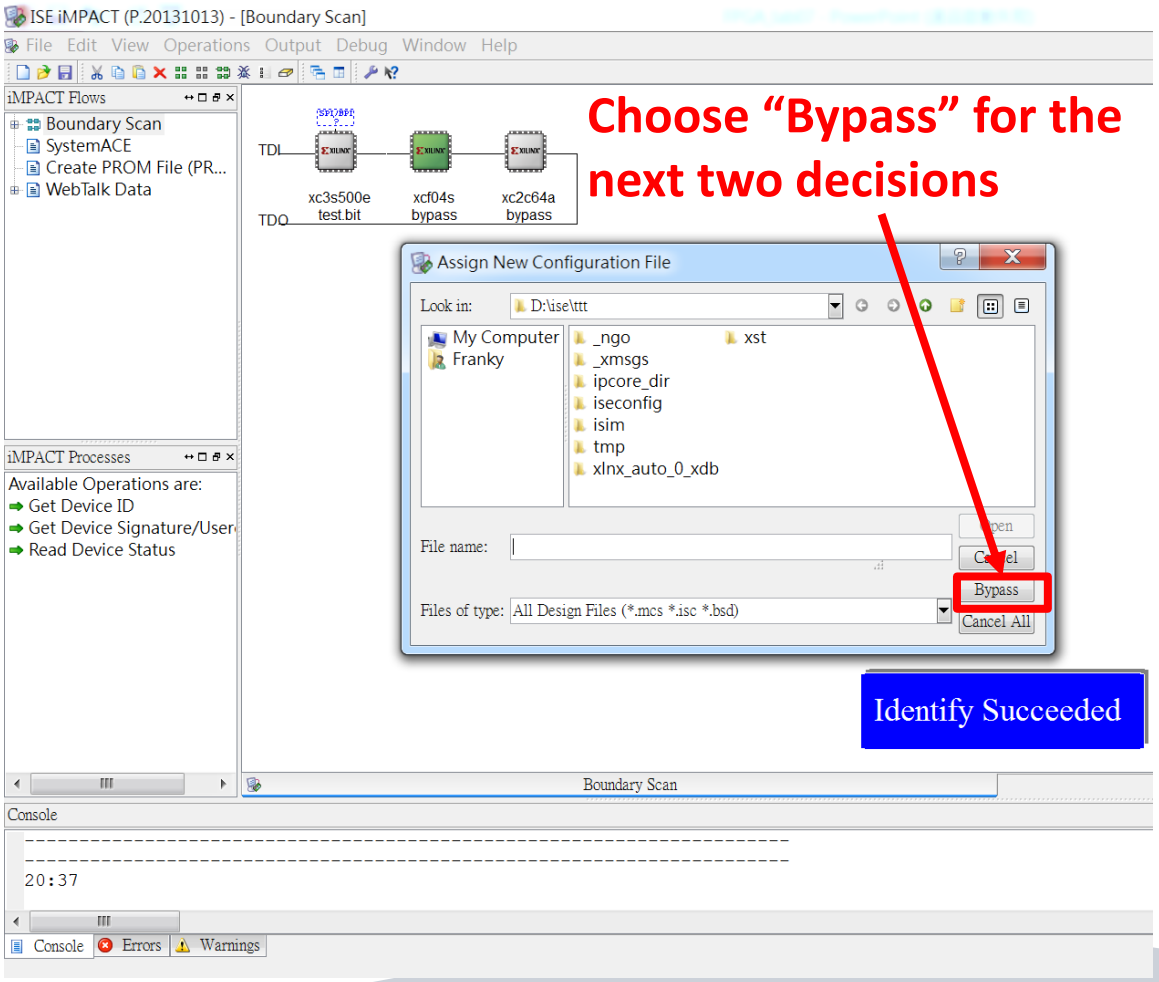


Transplantation





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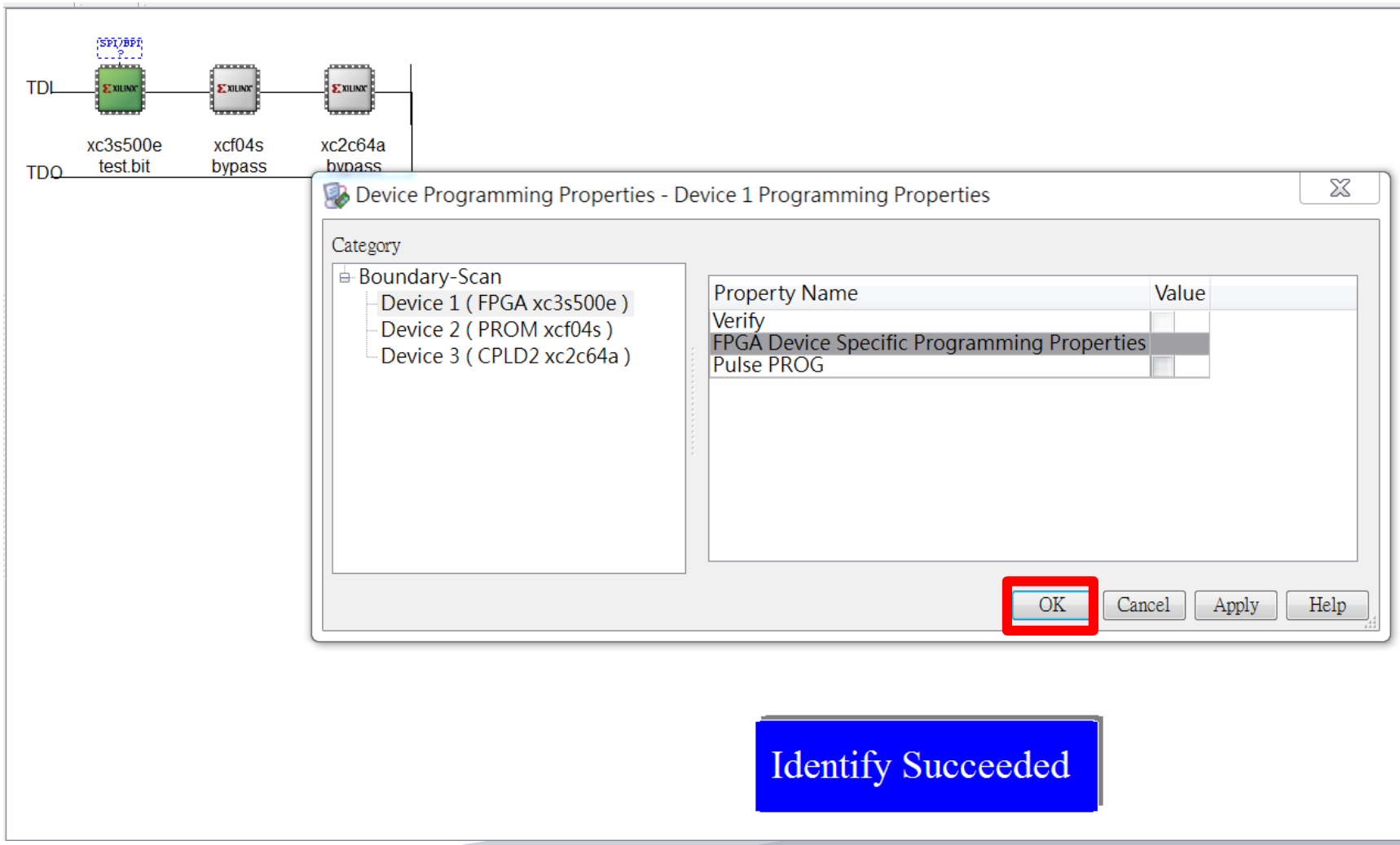
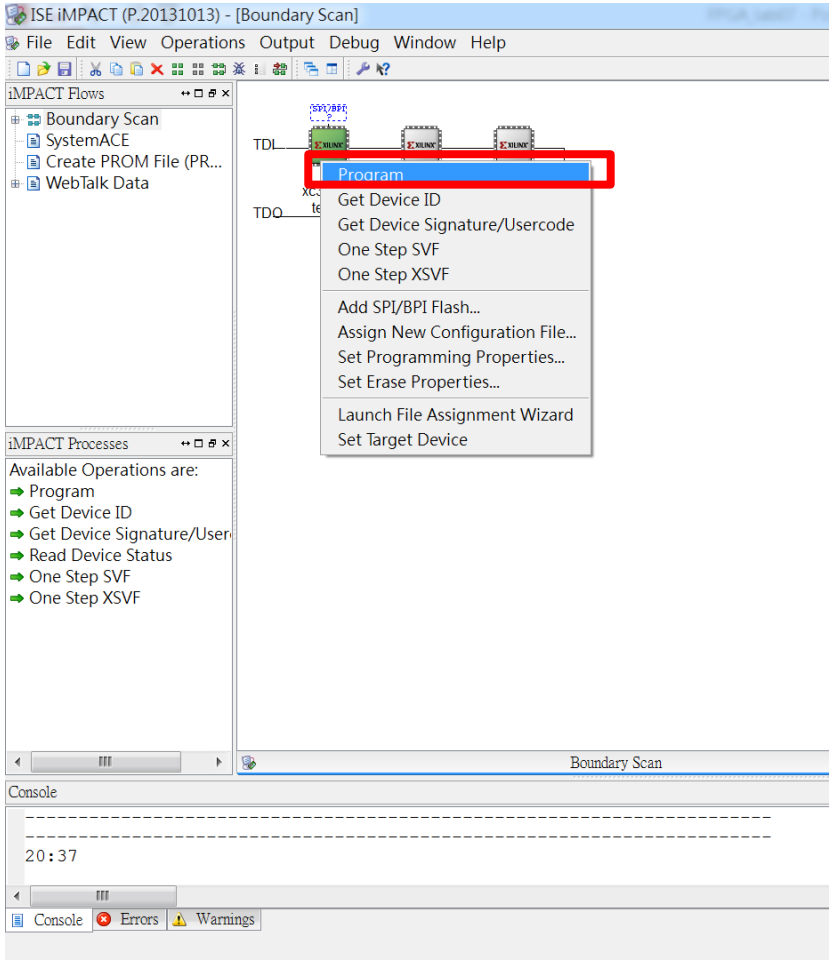
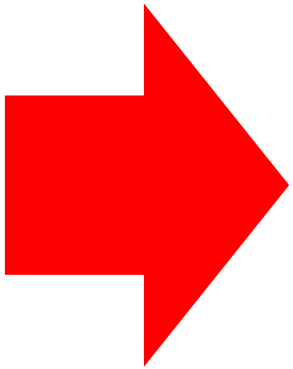
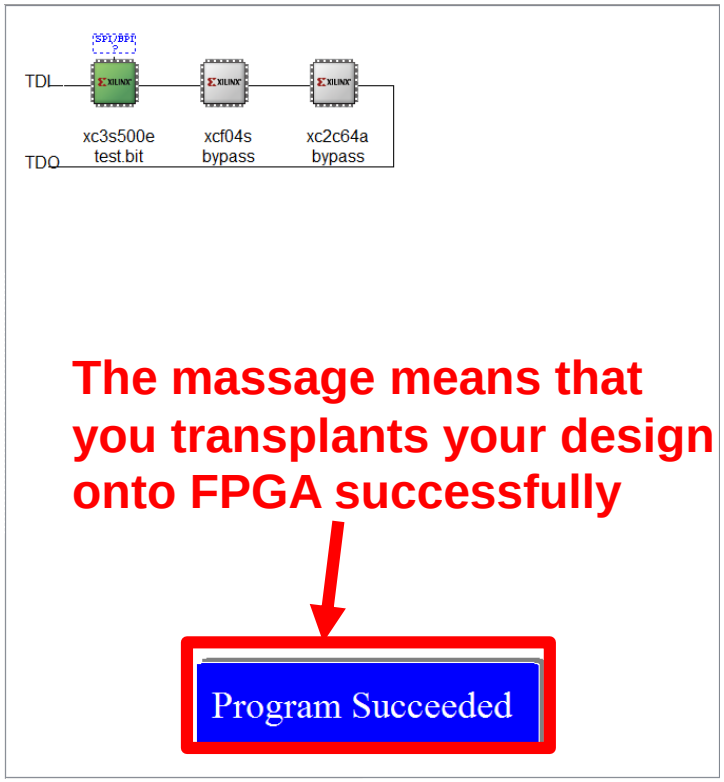


Transplantation







Thank You