NCTU-CS Digital System Lab.

Online Test (11/06)

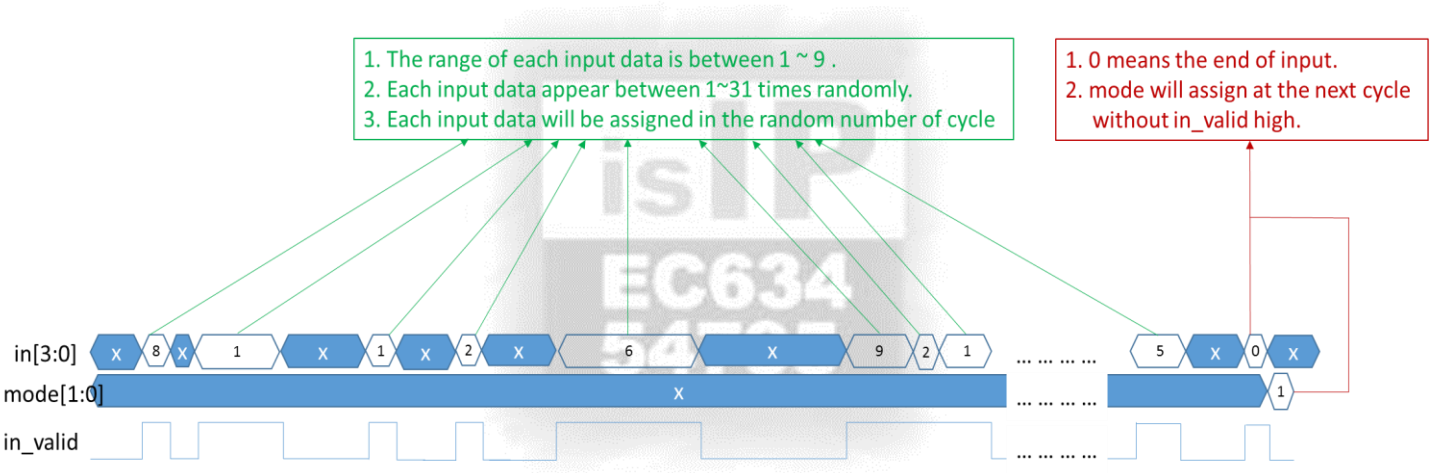
Data Preparation

1. Extract LAB data from TA's directory.
   % tar xvf ~2016dlabta02/Online_test1.tar

Design Description and Examples

Design three mode:

Input：



From **in[3:0]** channel, you will receive a large number of inputs in random cycles between each input data. And the total number of them are unknow but the range of each input data is 1~9. Each of them may appear 1~31 times. When you receive 0 in the end of input, we'll send **mode[1:0]** at the next cycle without in_valid high. You need to count the number 1~9 of each input data, and every number 1~9 appears between 1~31 times. According to mode, calculate your answer.

Mode 0：

Count each number 1~9 of input data, and every number of them is between 1~31 times.
Find the max times of number 1~9 after input data 1~9.

Ex :

1: 10 times 2: 5 times 3: 6 times 4: 28 times 5: 21 times

6: 2 times 7: 1 times 8: 30 times 9: 19 times

Output：

30

You should output 30 in 1 cycle.

Mode1:

Count each number 1~9 of input data, and every number of them is between 1~31 times.
Find the min times of number 1~9 after input data 1~9.

Ex :

1: 10 times 2: 5 times 3: 6 times 4: 28 times 5: 21 times

6: 2 times 7: 1 times 8: 30 times 9: 19 times

Output：

1

You should output 1 in 1 cycle.

Mode2:

Count each number 1~9 of input data, and every number of them is between 1~31 times.

Find the sum that numbers multiplied by its times of number 1~9 after input data 1~9.

Ex :

1: 10 times 2: 5 times 3: 6 times 4: 28 times 5: 21 times

6: 2 times 7: 1 times 8: 30 times 9: 19 times

Output：

1*10 + 2*5 + 3*6 + 4*28 + 5*21 + 6*2 + 7*1 +8*30 + 9*19

685

You should output 685 in 1 cycle.

Your goal is to compute these operations by above rules and output the correct answer.

Inputs

1. Input data for **in[3:0]** will be assign in **random** cycles while **in_ valid** is high.
2. **mode[1:0]** is valid at the next cycle of the ***end*** of input without **in_valid** high. (the next cycle when input data is 0)
3. All inputs will be changed at clock ***negative*** edge.
4. All signals are **unsigned** integer.

Input Signals	Bit Width	Description
clk	1	Clock, clock period = 4ns
rst_n	1	asynchronous active-low reset
in	4	the range of data is 1~9
in_valid	1	high when **in** is valid
mode	2	The function of mode: 0~2 discuss above

Outputs

1. Your answer should be output at **out[10:0]** in only **1 cycle** when **mode = 0, mode = 1, mode = 2**.
2. For **mode 0**, **out[10:0]** is unsigned integer.
3. For **mode 1**, **out[10:0]** is unsigned integer.
4. For **mode 2**, **out[10:0]** is unsigned integer.
5. **out_valid** should be low and **out** should be set to zero after initial reset.
6. **out_valid** should be set to high when output value is valid.
7. The latency of your design in each pattern should not be larger than 100 cycles.
8. All outputs are synchronized at clock ***positive*** edge.
9. Test pattern will check whether your answer is correct or not at clock **negative edge** when **out_valid** is high.

Output Signals	Bit Width	Description
out	11	output result
out_valid	1	high when **out** is valid

Specifications

1. Top module name : **Online_test1** (File name : **Online_test1.v**)
2. Input pins: **clk, rst_n, in_valid, in[3:0], mode[1:0]**.
3. Output pins: **out_valid, out[10:0]**.
4. **out_valid** should not be raised when **in_valid** is high (when **in** data is transferring).
5. It is **active-low asynchronous** reset.
6. The latency of your design in each pattern should not be larger than **100** cycles.
7. Grading policy:

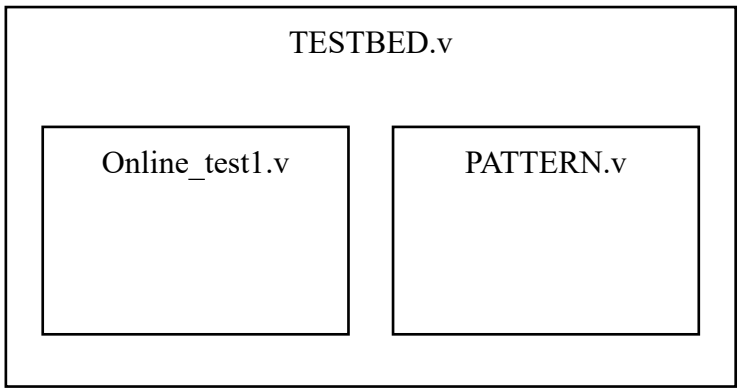
   Design: (01RTL, 02SYN, 03GATE) 70%

   Area: 10%

   Time: 10%

   Question: 10%

Block Diagram



Note

1. Simulation step:
   - Put your design in 01_RTL
   - Simulation to check design : ./01_run
   - Show wave to debug: nWave &
   - Go to folder 02_SYN/ and check synthesis：./01_run_dc
   - Go to folder 03_GATE/ and check s：./01_run.f
   - Clear up : ./09_clean_up
2. Please add your student ID and name to the file name of .v file before upload file on e3 platform:
   Online_test1_0556123_陳小明.v
3. Sample waveform: