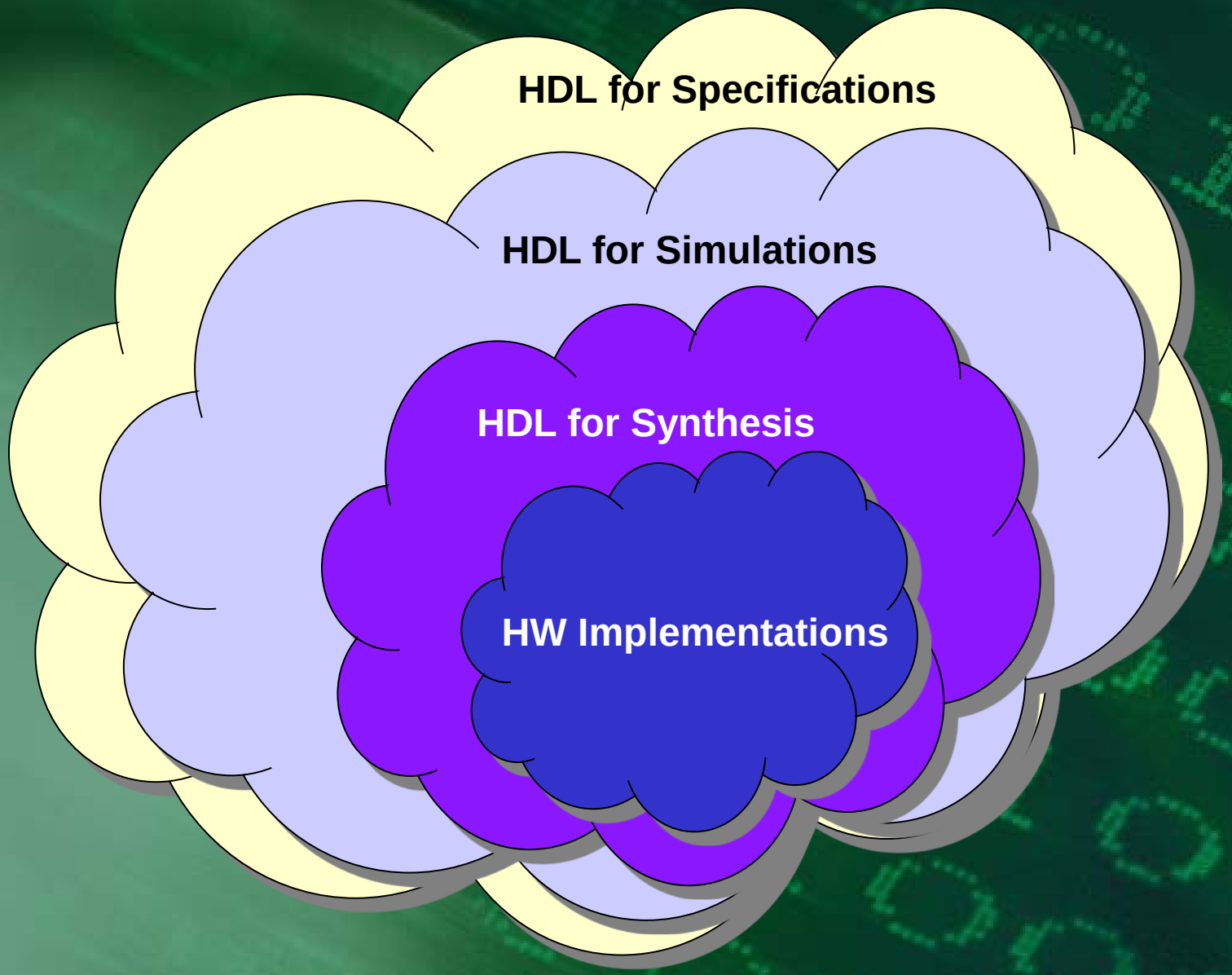
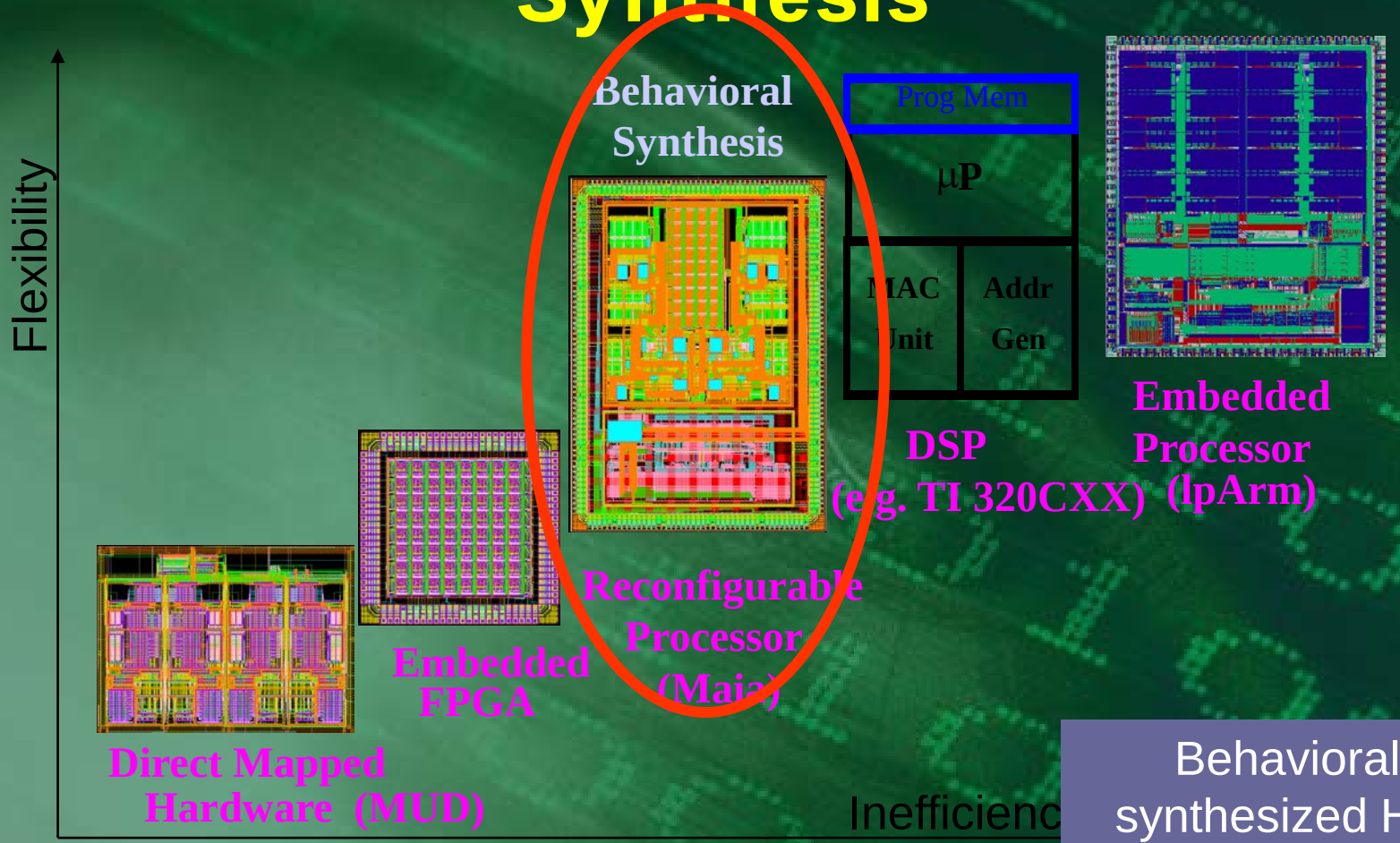
# Introduction to FPGA


HDL for Specifications
HDL for Simulations
HDL for Synthesis
HW Implementations

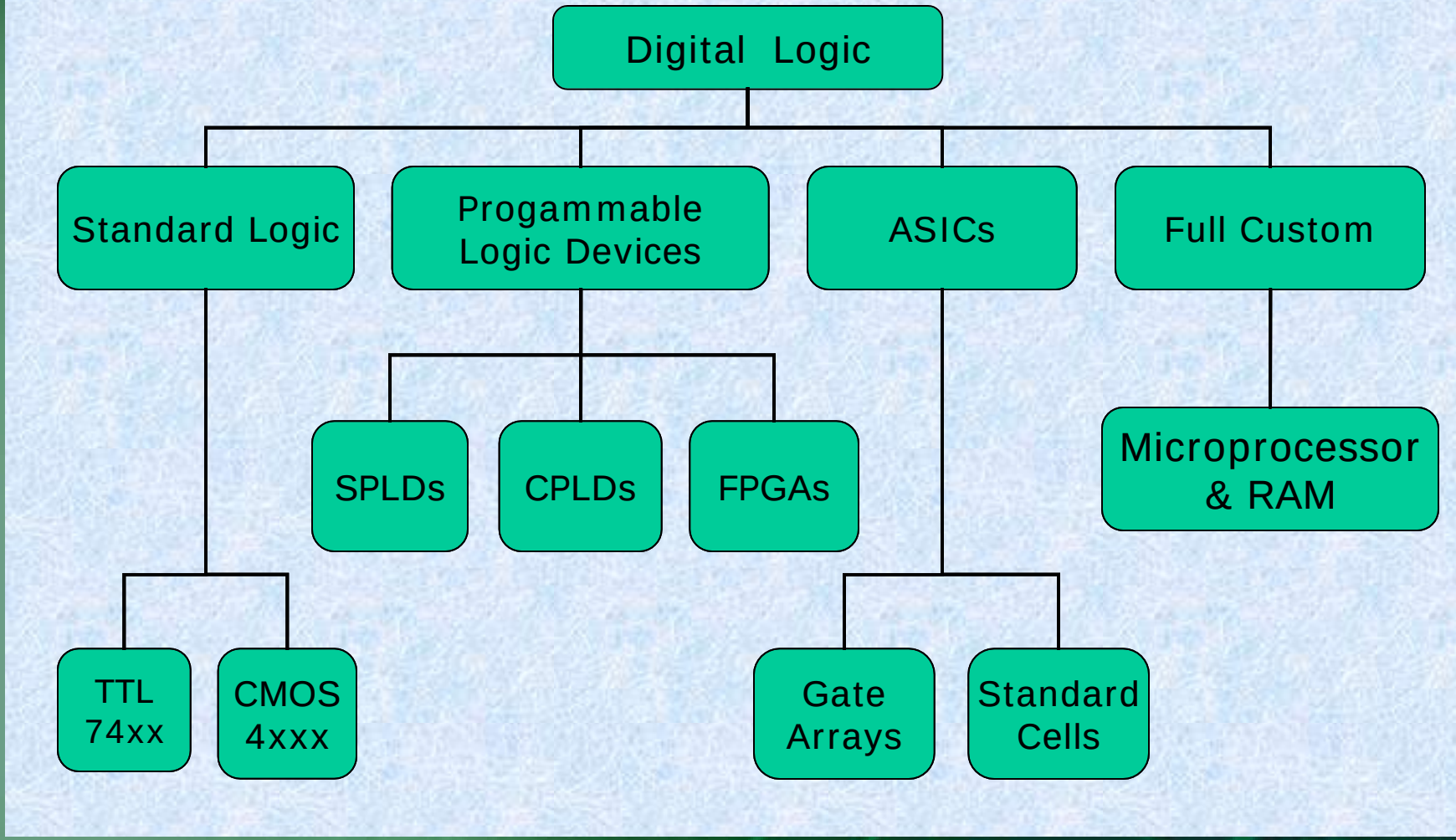
# Efficiency of Behavioral Synthesis




Behaviorally synthesized HW's tend to look like specialized processors.

**Note from CAD Developers:**
**Behavioral Synthesis would be more efficient if circuit designers didn't suck.**

# Classification



# What is FPGA ?

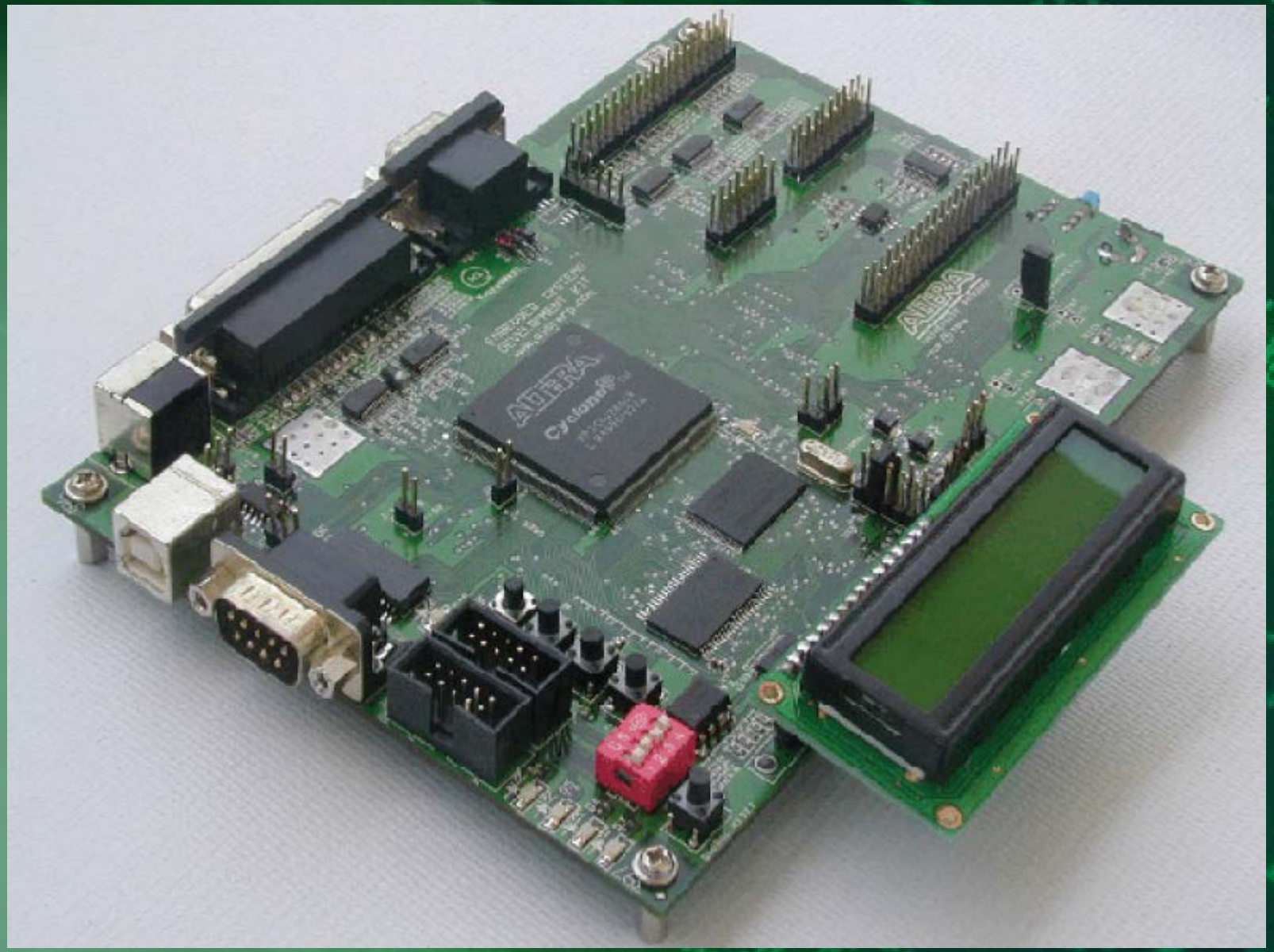
- Field Programmable Gate Array
- FPGA, CPLD, GAL, PAL ……
- Programmable
- Synthesizable

# Why needing FPGA ?

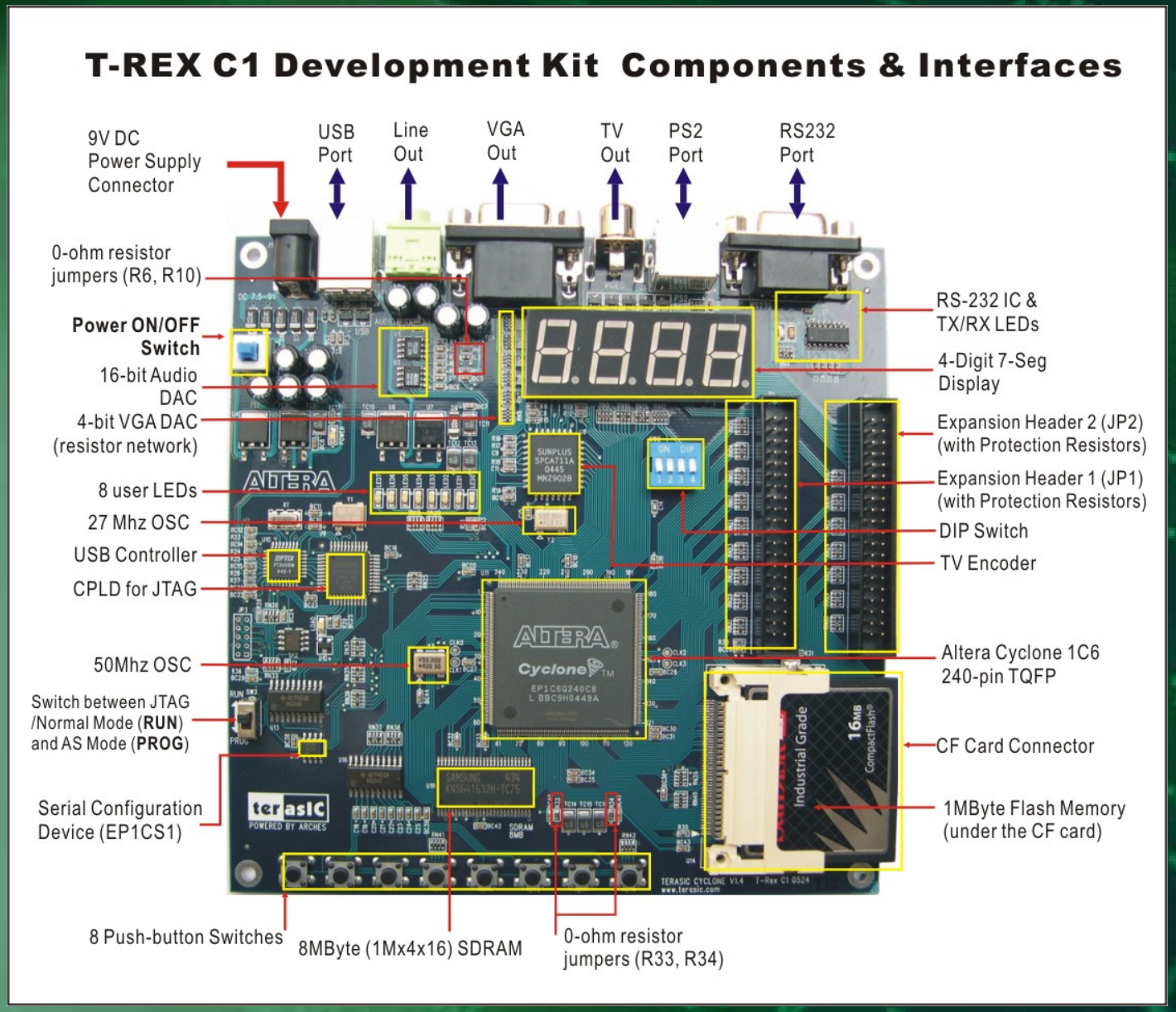
- An easy way to implement complex digital systems
- A simple and flexible way to debug a hardware design
- A quick way to evaluate designs to shorten the time-to-market costs
- A design verification before IC


TV/DTV
Setop Box
Image
USB
Host/Dev
DE2
Audio/MP3
terasIC
ALTERA
Ethernet
IrDA
RS232
Memory
SDRAM

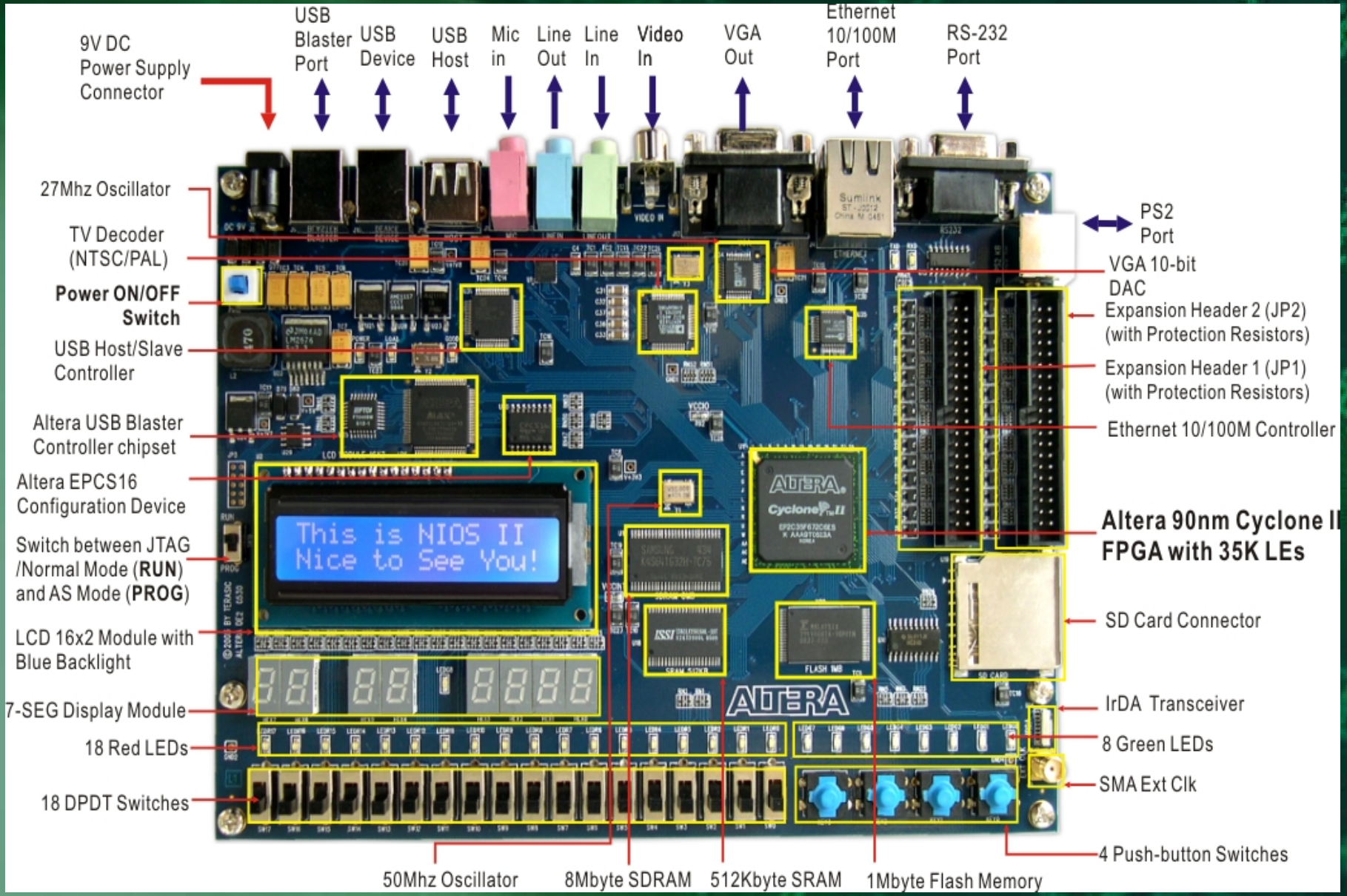
# Altera UP3 FPGA



# TR1 - Ideal for Undergrad Projects



# DE2 - Development and Educational Board II



# Design Supporting

- **Hardware design:**
  - **HDL : (Hardware Description Language)**
  - **Verilog HDL, VHDL, AHDL……**
- **Hardware/Software Co-Designs**
- **EDA Supporting**

- *PLD*

  **Programmable Logic Devices**

  – *PAL* **(Disappear)**

  **Programmable Array Logic. Fuse technology**

  – *GAL* **(Near to disappear)**

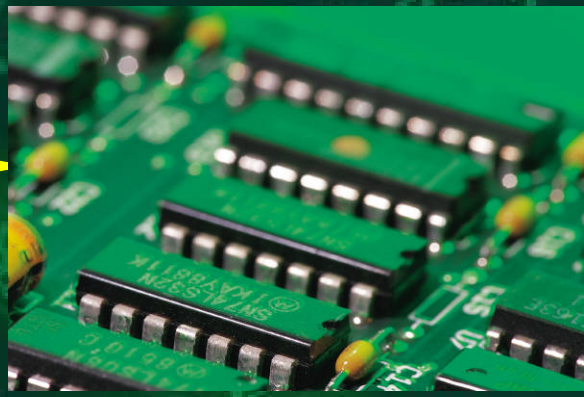
  **Generic Array Logic. $E^2$ technology**

  – *CPLD*

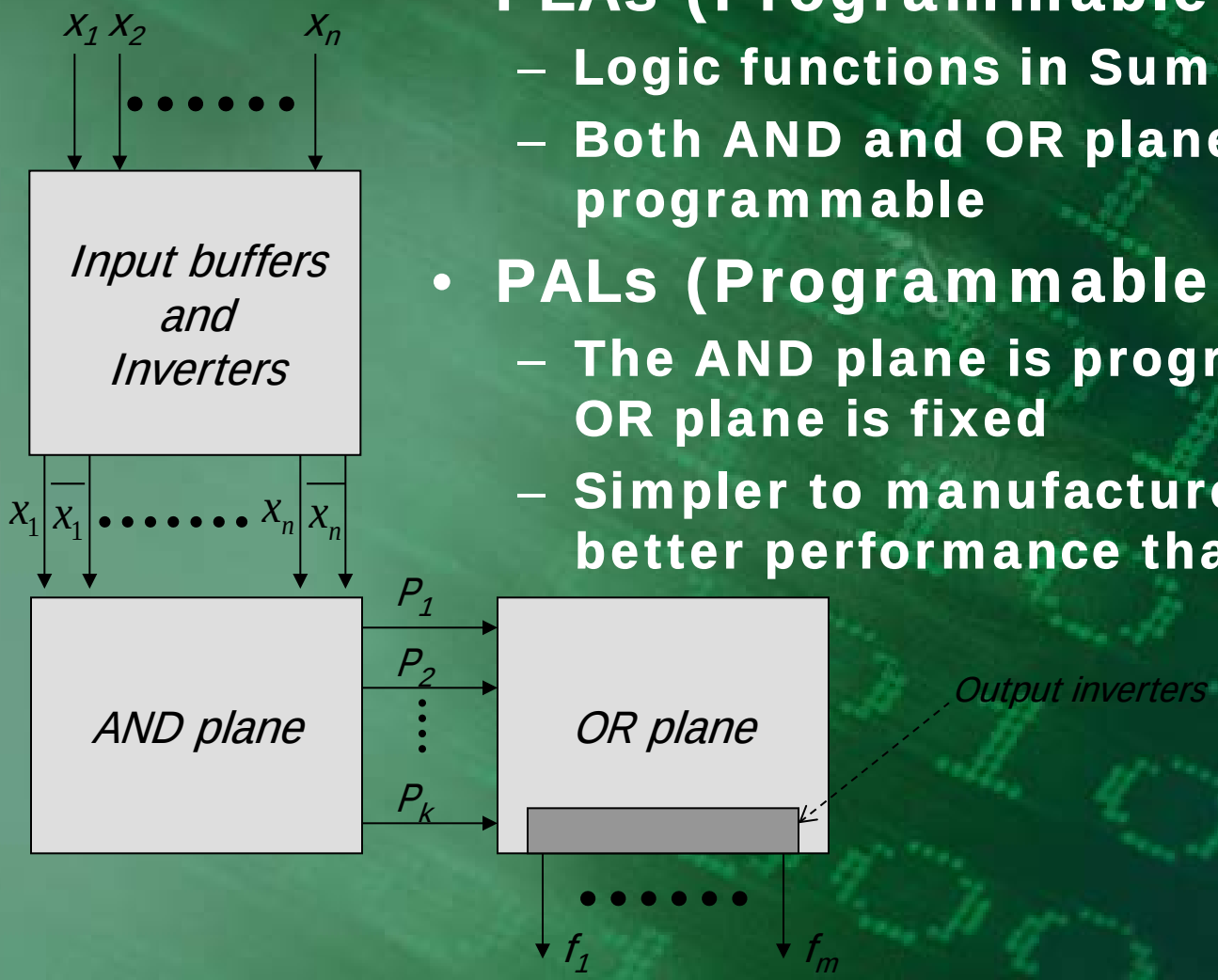
  **Complex PLD. $E^2$PROM or Flash technology**

  – *FPGA*

  **Field Programmable Gate Array. SRAM technology**

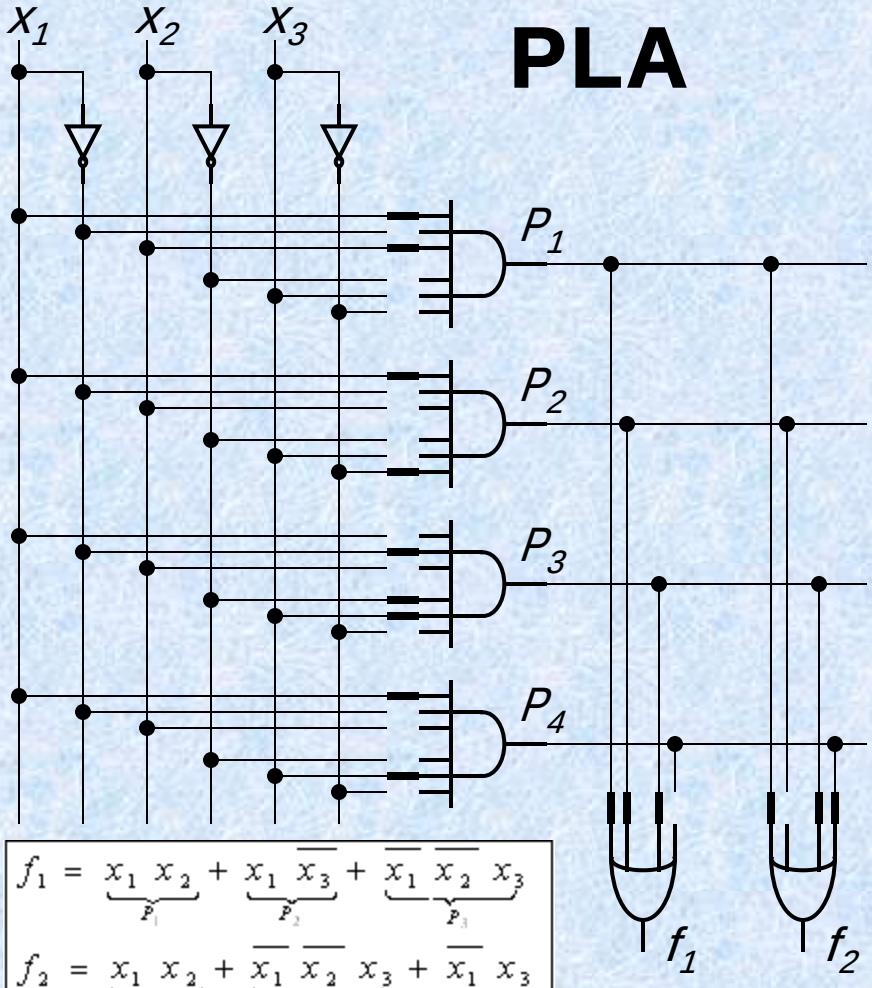


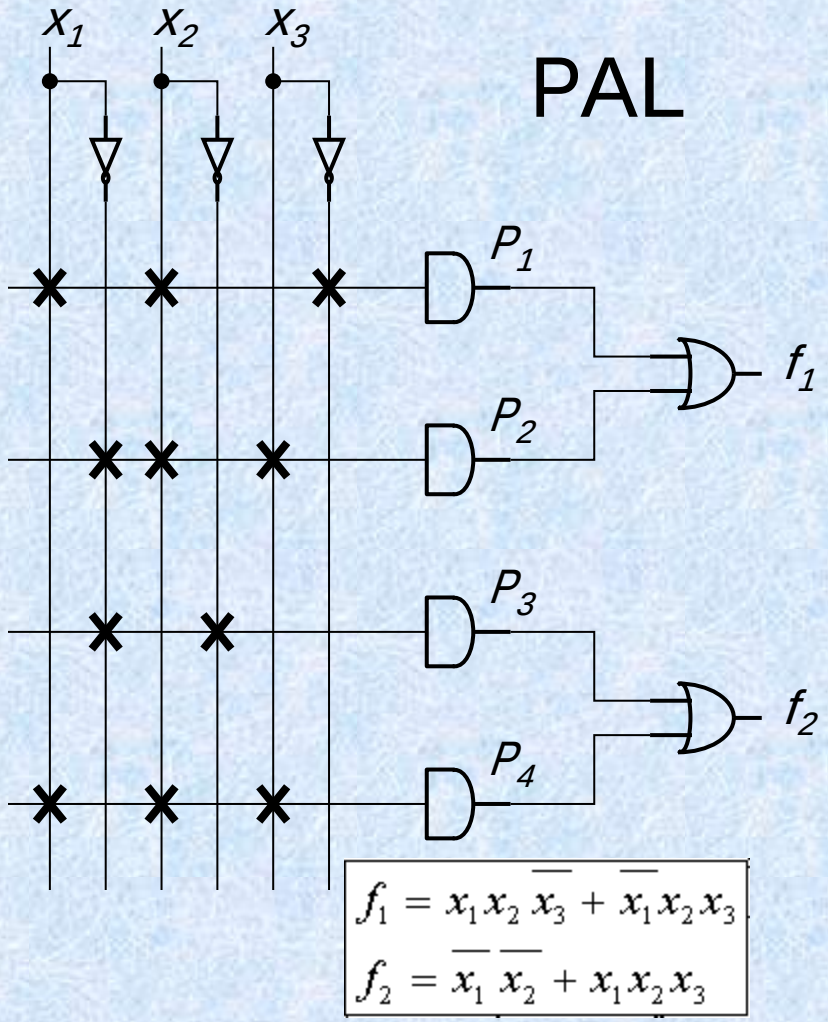
# SPLDs



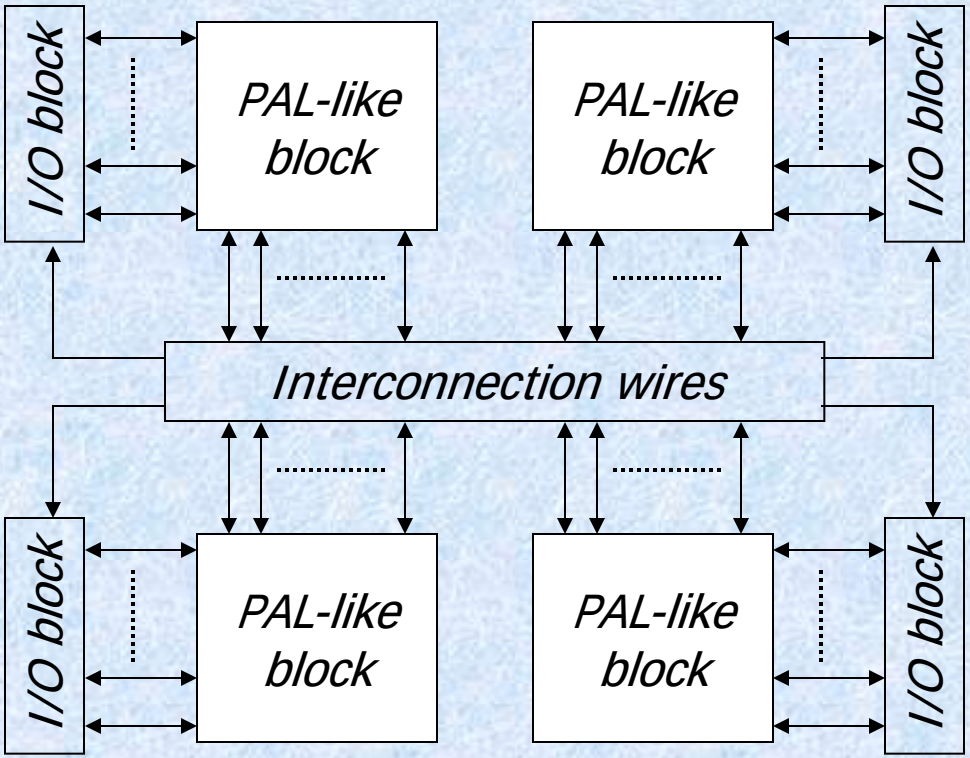

- **PLAs (Programmable Logic Arrays)**
  - **Logic functions in Sum Of Product form**
  - **Both AND and OR planes are programmable**
- **PALs (Programmable Array Logics)**
  - **The AND plane is programmable; the OR plane is fixed**
  - **Simpler to manufacture, less expensive, better performance than PLAs**

# SPLDs' Structure

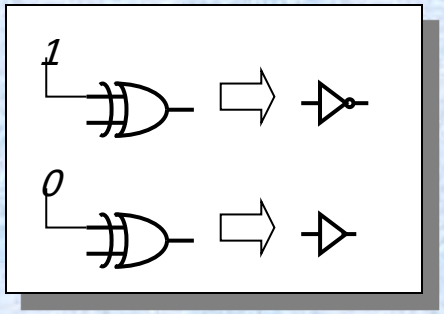


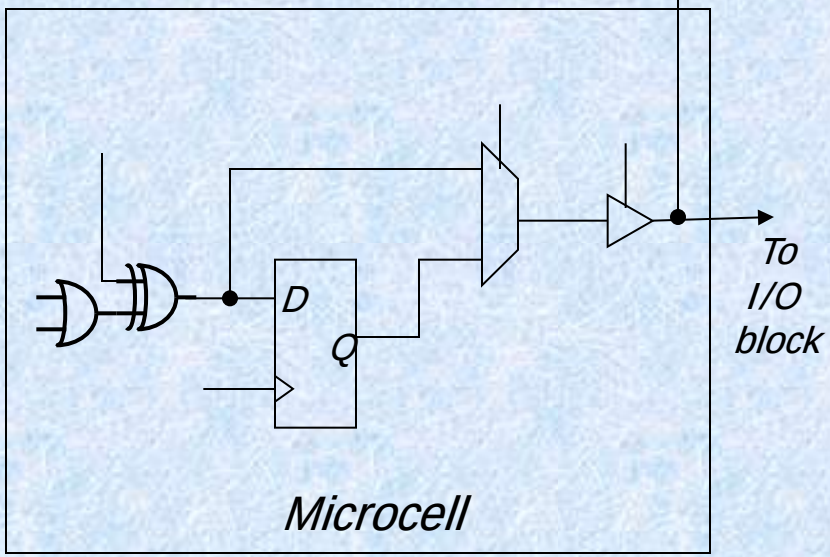



# CPLDs

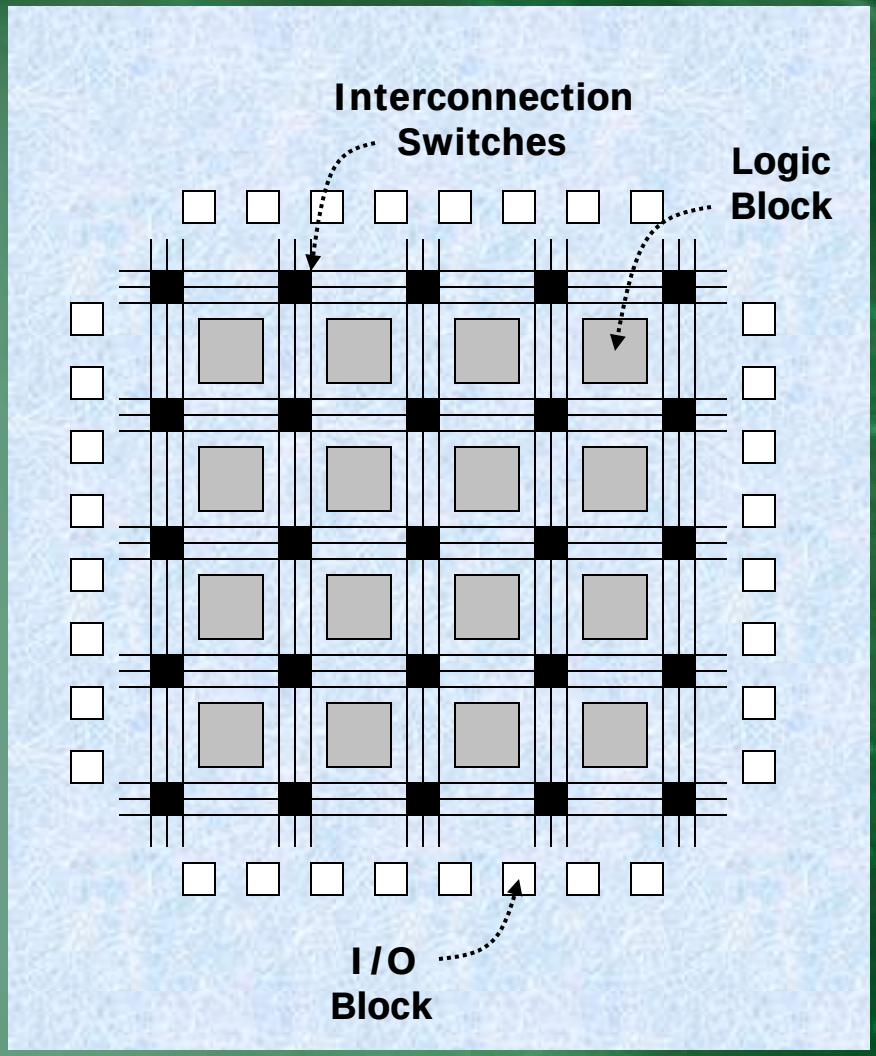



To implement multiple logic circuits



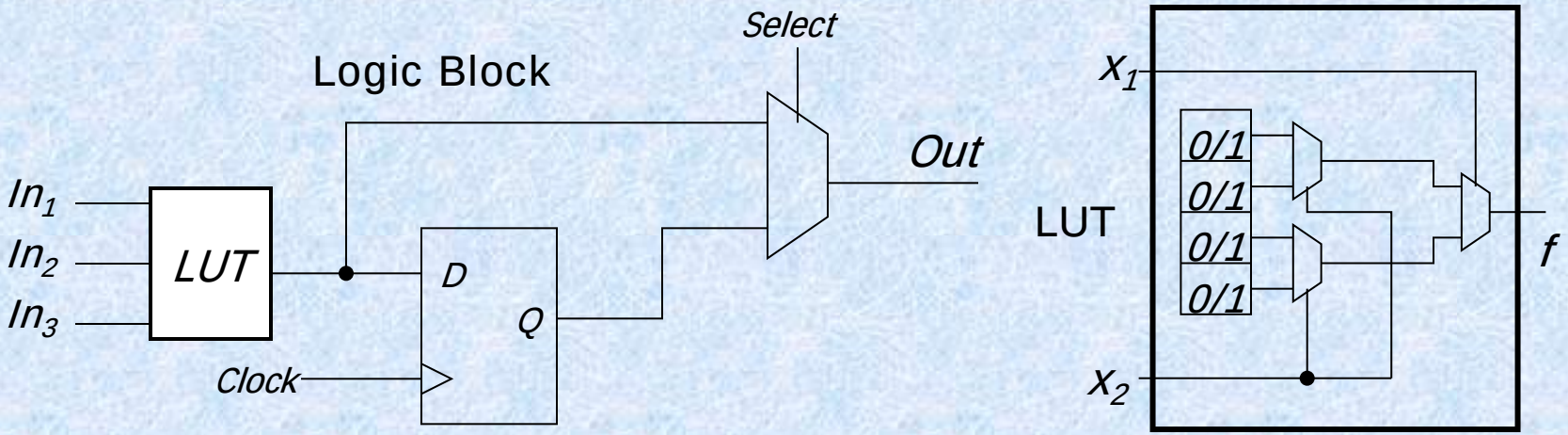



# FPGA



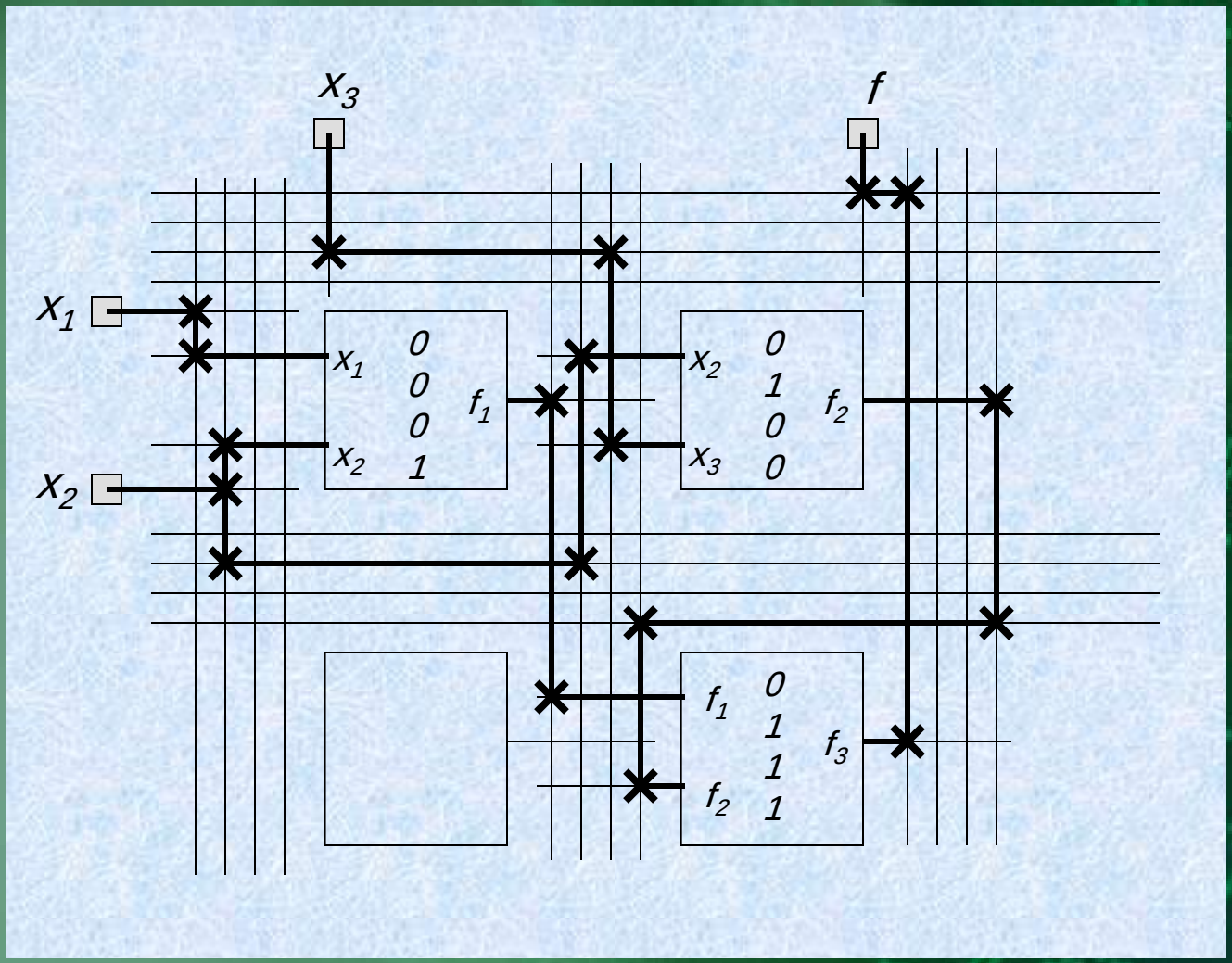

- FPGAs do not contain AND or OR planes
- Three elements:
  - Logic blocks
  - I/O blocks
  - Interconnection wires and switches

# FPGA Logic Block




- The storage cells in the LUTs in an FPGA are volatile
- Volatile: losing stored contents whenever the power is off
- Using PROM to hold data permanently
- The storage cells are loaded automatically from PROM when the chip is initialized

# Programming an FPGA




$$f_1 = x_1 x_2$$

$$f_2 = \overline{x_2} x_3$$

$$f = x_1 x_2 + \overline{x_2} x_3$$

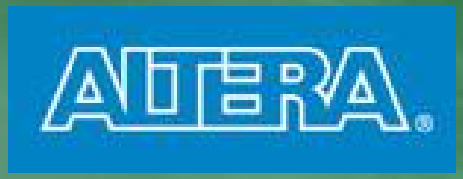
# Programming Technologies

- **Floating Gate Programming Technology**
- **SRAM Programming Technology**
- **Antifuse Programming Technology**

*In-System Programming (ISP) : performing the programming while the chip is still attached to its circuit board*

*JTAG (Boundary Scan):*
*A port added to FPGAs for testing purposes, as a means of downloading the design in the programmable device via serial port of a PC*

# The Main Producers







# Altera and Xilinx PLDs

- Altera
  - CPLD
    - MAX3000A – MAX7000
  - FPGA
    - Cyclone
    - Stratix - Stratix GX
    - APEX II - APEX 20K
    - Mercury
    - FLEX 10K
    - ACEX 1K



- Xilinx
  - CPLD
    - CoolRunner-II
    - CoolRunner XPLA3
    - XC9500 Series
  - FPGA
    - Rocket-PHY
    - Virtex - Virtex-II - Virtex-II Pro Series
    - Spartan-3,Spartan-IIE, Spartan-II, Spartan-XL, Spartan Seires