

# Instruction to FPGA working environment

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Integration System & Intellectual Property

# What is the FPGA ?

A **field-programmable gate array (FPGA)** is an integrated circuit . Engineers use FPGAs to implement and verify digital systems before production.

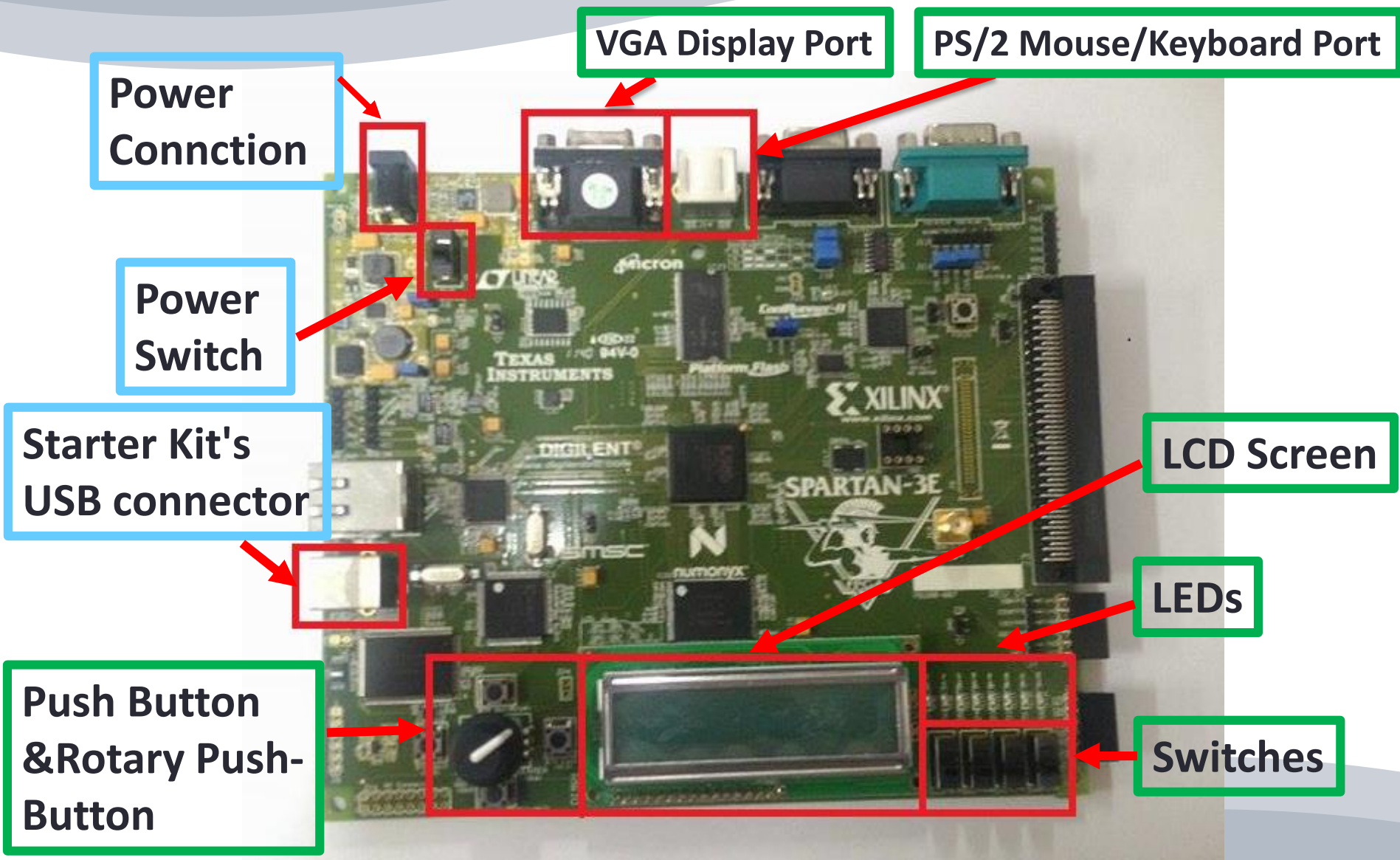
- **Advantage:**
  - Ability to re-program
  - Less debug cost
  - Lower engineering costs
- **Shortcoming:**
  - Slower
  - Less energy efficient
  - Less functionality



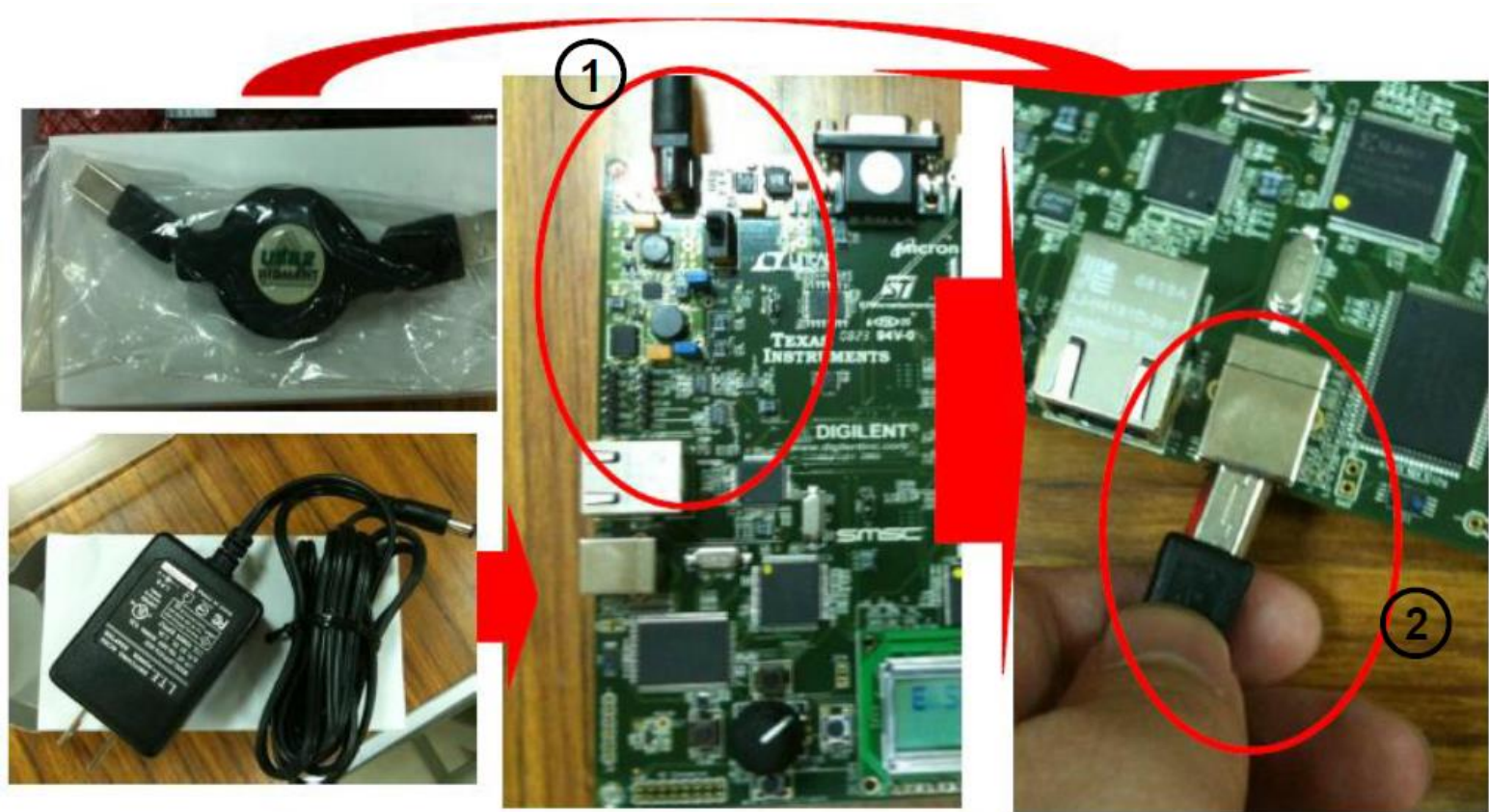
# Xilinx Spartan-3E Starter board

- **Family and Device:** Spartan-3E XC3S500E
- **On-Board Oscillator:** 50MHz
- **Key Components and Features**
  - \* 10/100 Ethernet PHY
  - \* Two 9-pin RS-232 Port
  - \* PS/2 Port
  - \* SMA clock input
  - \* Four slide switches
  - \* Eight discrete LEDs
  - \* Four push-button switches
  - \* VGA Display Port
  - \* 2-line, 16-character LCD screen





# Installation



# Attention

- **Avoid to touch the wires on the board which may cause static electricity.**
- **Always bind the wire by strap to avoid messing up the wires after use them.**



# What is Xilinx ISE Design Suit

## Xilinx ISE (Integrated Synthesis Environment)

- ISE design suit is a software tool produced by Xilinx for **synthesis** and **analysis** of HDL designs.
- Developers can synthesize their designs , simulate the wave diagram ,and examine RTL diagram.
- Xilinx ISE Design Suit is a design environment for FPGA products.





# Open the Xilinx Project Navigator

First we start the Xilinx ISE software





# Open the Xilinx Project Navigator

The screenshot shows the Xilinx ISE Project Navigator interface. The main window is titled "test Project Status (11/18/2015 - 21:33:21)". It contains a table with project details and a "Device Utilization Summary" table.

| test Project Status (11/18/2015 - 21:33:21) |   |                       |   |
|---|---|-----------------------|---|
| Project File:                               | ttt.xise                                  | Parser Errors:        | No Errors                                     |
| Module Name:                                | test                                      | Implementation State: | Programming File Generated                    |
| Target Device:                              | xc3s500e-4fg320                           | • Errors:             | No Errors                                     |
| Product Version:                            | ISE 14.7                                  | • Warnings:           | <a href="#">1 Warning (0 new)</a>             |
| Design Goal:                                | Balanced                                  | • Routing Results:    | <a href="#">All Signals Completely Routed</a> |
| Design Strategy:                            | <a href="#">Xilinx Default (unlocked)</a> | • Timing Constraints: | <a href="#">All Constraints Met</a>           |
| Environment:                                | <a href="#">System Settings</a>           | • Final Timing Score: | <a href="#">0 (Timing Report)</a>             |

| Device Utilization Summary                     |      |           |             |         |
|--|------|-----------|-------------|---------|
| Logic Utilization                              | Used | Available | Utilization | Note(s) |
| Number of Slice Flip Flops                     | 23   | 9,312     | 1%          |         |
| Number of 4 input LUTs                         | 29   | 9,312     | 1%          |         |
| Number of occupied Slices                      | 26   | 4,656     | 1%          |         |
| Number of Slices containing only related logic | 26   | 26        | 100%        |         |
| Number of Slices containing unrelated logic    | 0    | 26        | 0%          |         |
| Total Number of 4 input LUTs                   | 50   | 9,312     | 1%          |         |

The console window at the bottom shows the following logs:

```
INFO:HDLCompiler:1845 - Analyzing Verilog file "D:/ise/ttt/test.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
INFO:HDLCompiler:1845 - Analyzing Verilog file "D:/ise/ttt/test.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
```



# 1) Create a new project

ISE Project Navigator (P.2013.013) - D:\ise\ttt\ttt.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

New Project...  
Open Project...  
Open Example...  
Project Browser...  
Copy Project...  
Close Project

New Ctrl+N  
Open... Ctrl+O  
Close  
Save Ctrl+S  
Save As...  
Save All  
Print Preview...  
Print... Ctrl+P  
Recent Files  
Recent Projects  
Exit

Design Suite

Design Overview

Summary  
IOB Properties  
Module Level Util...  
Timing Constrai...

test Project Status (11/18/2015 - 21:33:21)

|                |                 |                       |                            |
|----------------|-----------------|-----------------------|----------------------------|
| Project File:  | ttt.xise        | Parser Errors:        | No Errors                  |
| Module Name:   | test            | Implementation State: | Programming File Generated |
| Target Device: | xc3s500e-4fg320 | Errors:               | No Errors                  |

New Project Wizard

Create New Project

Specify project location and type.  
Enter a name, locations, and comment for the project

Name:

Location:

Working Directory:

Description:

Select the type of top-level source for the project

Top-level source type:

More Info Next Cancel

Console

INFO:HDLCompiler:1845 - Analyzi  
INFO:ProjectMgmt - Parsing desi  
INFO:HDLCompiler:1845 - Analyzi  
INFO:ProjectMgmt - Parsing desi  
Launching Design Summary/Report

5) Next

3) Set the file directory

4) Select HDL

Create a new project



New Project Wizard

### Project Settings

Specify device and project properties.  
Select the device and design flow for the project

**6) Select SPARTAN-3E Starter Board , then "Next"**

| Property Name                          | Value                    |
|--|--------------------------|
| Evaluation Development Board           | Spartan-3E Starter Board |
| Product Category                       | All                      |
| Family                                 | Spartan3E                |
| Device                                 | XC3S500E                 |
| Package                                | FG320                    |
| Speed                                  | -4                       |
| Top-Level Source Type                  | HDL                      |
| Synthesis Tool                         | XST (VHDL/Verilog)       |
| Simulator                              | ISim (VHDL/Verilog)      |
| Preferred Language                     | Verilog                  |
| Property Specification in Project File | Store all values         |
| Manual Compile Order                   | <input type="checkbox"/> |
| VHDL Source Analysis Standard          | VHDL-93                  |
| Enable Message Filtering               | <input type="checkbox"/> |

More Info Next Cancel





## New Project Wizard



### Project Summary

Project Navigator will create a new project with the following specifications.

#### Project:

Project Name: ADD  
Project Path: D:\ise\ADD  
Working Directory: D:\ise\ADD  
Description:  
Top Level Source Type: HDL

#### Device:

Evaluation Development Board: Spartan-3E Starter Board  
Device Family: Spartan3E  
Device: xc3s500e  
Package: fg320  
Speed: -4

Top-Level Source Type: HDL  
Synthesis Tool: XST (VHDL/Verilog)  
Simulator: ISim (VHDL/Verilog)  
Preferred Language: Verilog  
Property Specification in Project File: Store all values  
Manual Compile Order: false

**7) Check the project data is correct ,or not  
then “Finish”**

More Info

Finish

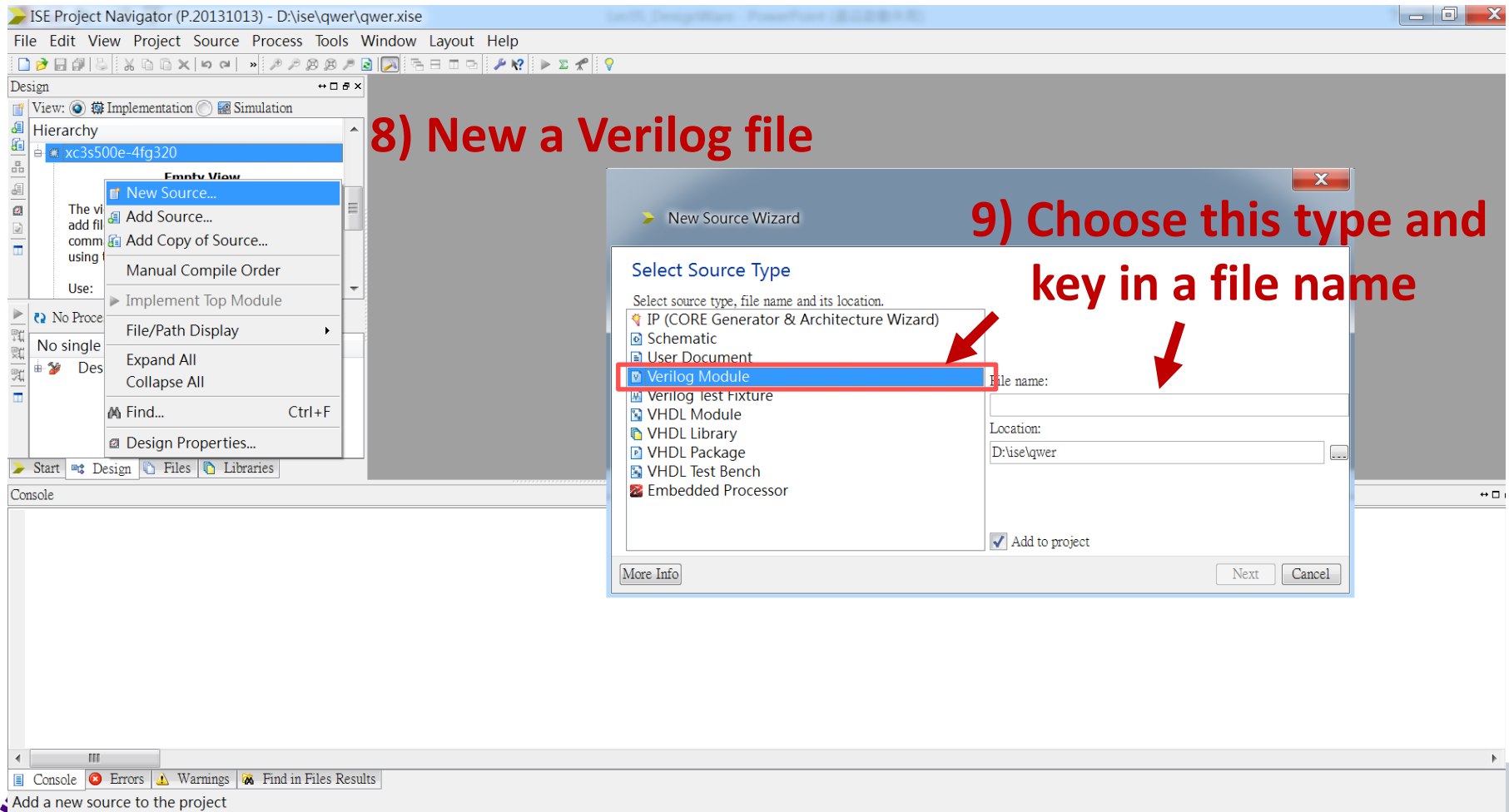
Cancel



# New a source

8) New a Verilog file

9) Choose this type and key in a file name



# New a source

ISE Project Navigator (P.20131013) - D:\ise\qwer\qwer.xise

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

xc3s500e-4fg320

Empty View

The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.

Use:

No Processes Running

No single design module is selected.

Design Utilities

Start Design Files Libraries

Console

Add a new source to the project

10) Define your ports here

New Source Wizard

Define Module

Specify ports for module.

Module name ee

| Port Name | Direction | Bus | MSB | LSB |
|-----------|-----------|-----|-----|-----|
|           | input     |     |     |     |
|           | input     |     |     |     |
|           | input     |     |     |     |
|           | input     |     |     |     |
|           | input     |     |     |     |
|           | input     |     |     |     |
|           | input     |     |     |     |

More Info Next Cancel

Notice : one \*.v file only has one module



# New a source





# New a source

The screenshot shows the ISE Project Navigator interface. In the left pane, the 'Hierarchy' view shows a project named 'ADD' with a sub-project 'add (add.v)' highlighted by a red box and a red arrow. Below this, the 'Processes' pane shows a list of tasks for 'add', including 'Design Summary/Reports', 'Design Utilities', 'User Constraints', 'Synthesize - XST', 'Implement Design', 'Generate Programming File', 'Configure Target Device', and 'Analyze Design Using ChipScope'. The main editor window displays the Verilog code for 'add.v', which is also highlighted by a red box. The code includes a timescale, comments, and a module definition. A red arrow points to the bottom of the editor window with the text 'Edit your design here'. The bottom status bar shows 'Ln 1 Col 1 | Verilog'.

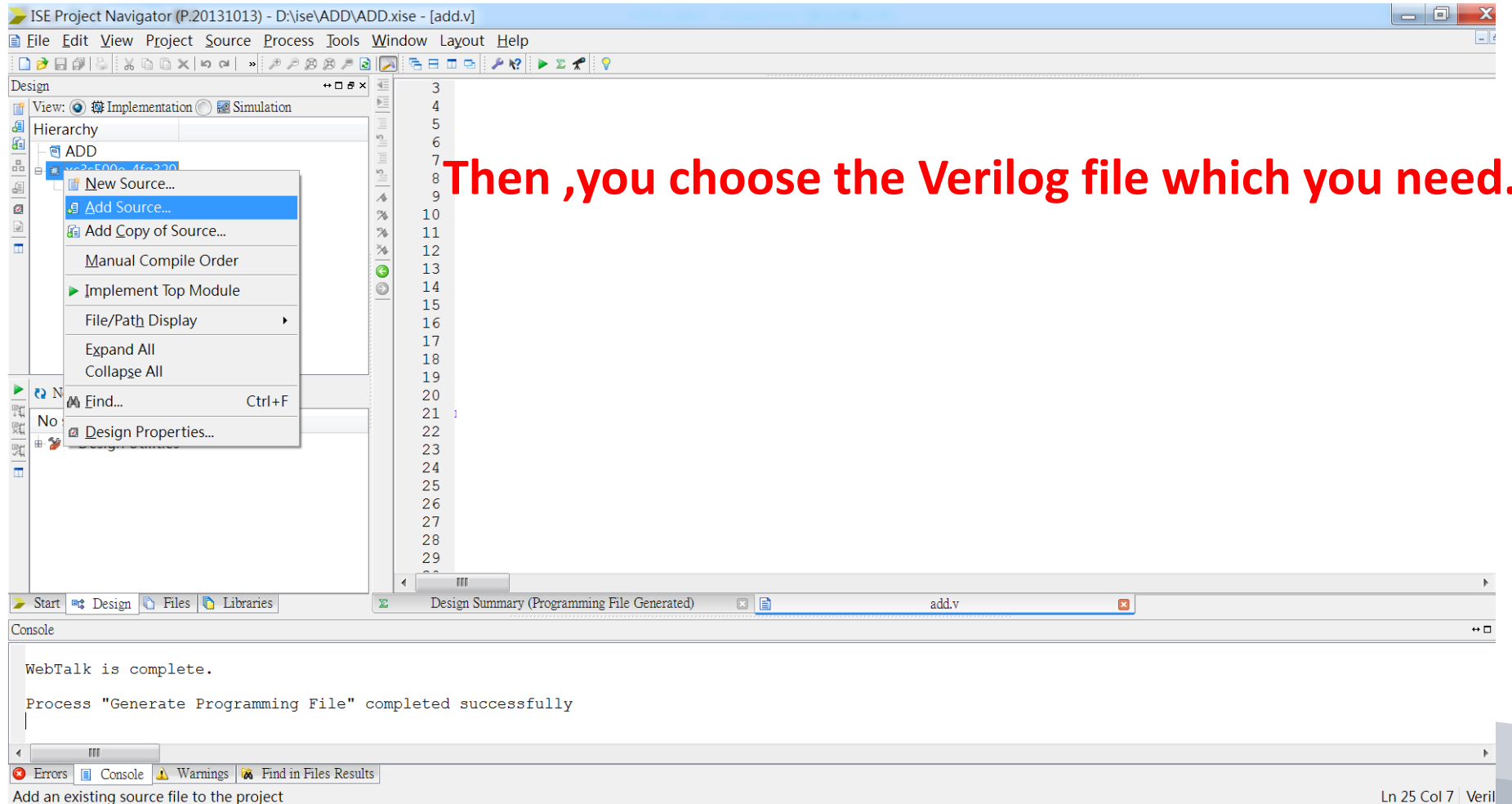
**The file which you create**

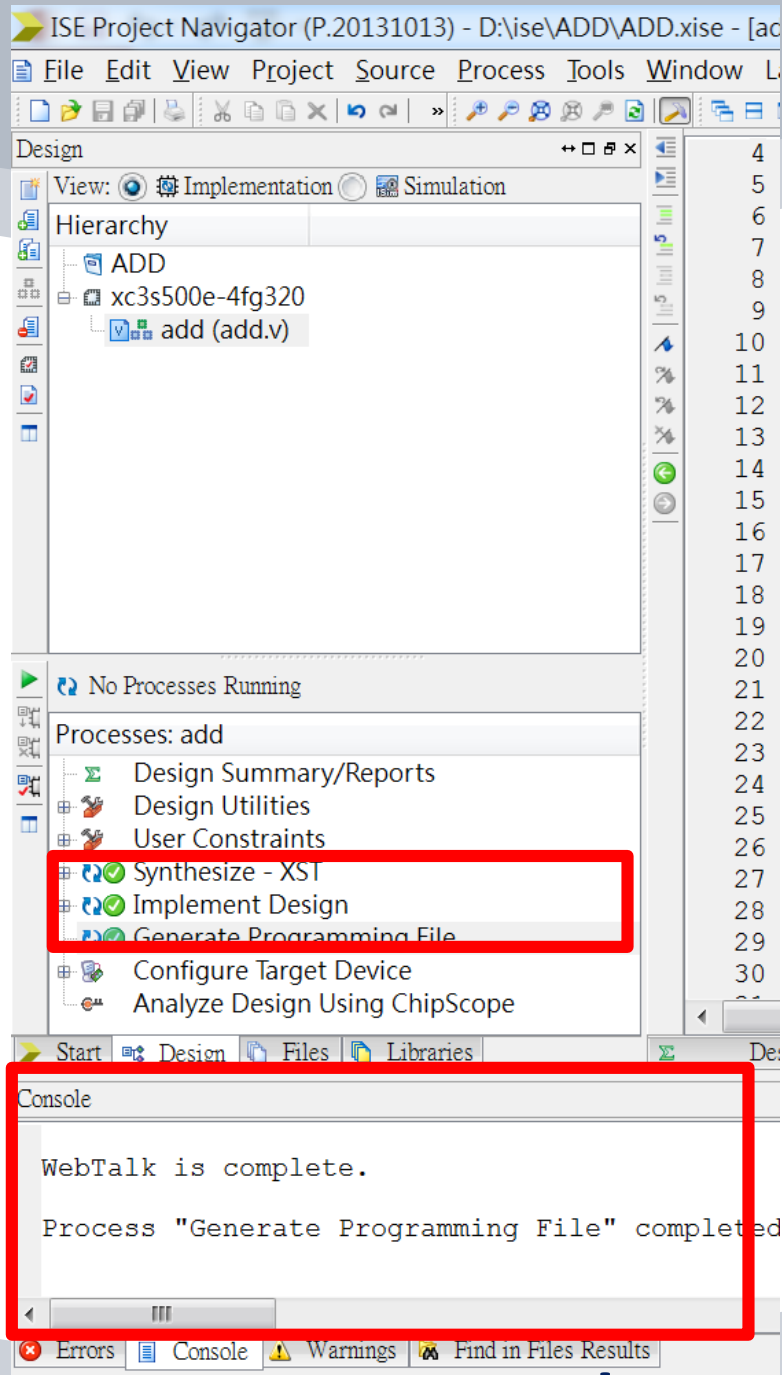
```
1 |`timescale 1ns / 1ps
2 |////////////////////////////////////
3 |// Company:
4 |// Engineer:
5 |//
6 |// Create Date:    20:45:46 11/19/2015
7 |// Design Name:
8 |// Module Name:    add
9 |// Project Name:
10 |// Target Devices:
11 |// Tool versions:
12 |// Description:
13 |//
14 |// Dependencies:
15 |//
16 |// Revision:
17 |// Revision 0.01 - File Created
18 |// Additional Comments:
19 |//
20 |////////////////////////////////////
21 |module add(
22 |    );
23 |
24 |
25 |endmodule
26 |
```

**Edit your design here**



# You can “Add source” if you have the Verilog file





# Compile

- Double click “Synthesize - XST” for syntax checking
- Double click “Implement Design” for mapping connection file(.ucf) to your design and the platform

- There are four different icons for your design



->Warning



->your design is newer than before



->Error



->Correct

- If your designs have errors, use the messages in the “Console Window” for debugging

# Add the pattern to simulate the design

The screenshot shows the Xilinx ISE Project Navigator interface. The 'View' dropdown at the top left is set to 'Simulation'. The 'Hierarchy' pane on the left shows the project structure: 'ADD' > 'xc3s500e-4fg320' > 'pattern (pattern.v)' > 'a1 - add (add.v)'. The 'Processes: pattern' pane at the bottom left shows the simulation process: 'ISIM Simulator' > 'Behavioral Check Syntax' > 'Simulate Behavioral Model'. The 'Errors' pane at the bottom is empty. The 'Design Summary' pane at the bottom right shows the design summary for 'add.v', 'pattern.v', and 'testbed.v'.

2) Choose Simulate

1) Add your pattern to the project

3) Click pattern then run the "Behavioral Check Syntax" and "Simulate Behavioral Model"



# Wave Diagram

The screenshot shows the ISim software interface. The top menu bar includes File, Edit, View, Simulation, Window, Layout, and Help. The main window is divided into several panes. On the left, the 'Instances and Process' pane lists simulation objects, with 'pattern' and 'a1' highlighted. A red box highlights the 'a1' object, and a red arrow points to the 'out[1:0]' value in the 'Value' column. The 'Value' column shows '0' for 'a' and 'b', and '00' for 'out[1:0]'. The 'Wave Diagram' pane on the right shows a timeline from 999,992 ps to 1,000,001 ps. The bottom status bar indicates 'Sim Time: 1,000,000 ps'.

**Pick the variables which you need**

Console  
ISim P.20131013 (signature 0x7708f090)  
This is a Full version of ISim.  
Time resolution is 1 ps  
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
ISim>

Console | Compilation Log | Breakpoints | Find in Files Results | Search Results

Create a new file

Sim Time: 1,000,000 ps



# Wave Diagram

The screenshot shows the ISim software interface. The 'Simulation' menu is open, highlighting 'Restart' (Ctrl+Shift+F5) and 'Run All' (F5). A red arrow points to the 'Restart' option. The wave diagram shows a signal 'out[1:0]' with a value of 00 at 1,000,000 ps. The console shows the simulation status: 'ISim P.20131013 (signature 0x7708f090) This is a Full version of ISim. Time resolution is 1 ps. Simulator is doing circuit initialization process. Finished circuit initialization process. ISim>'.

**Restart and Run All**

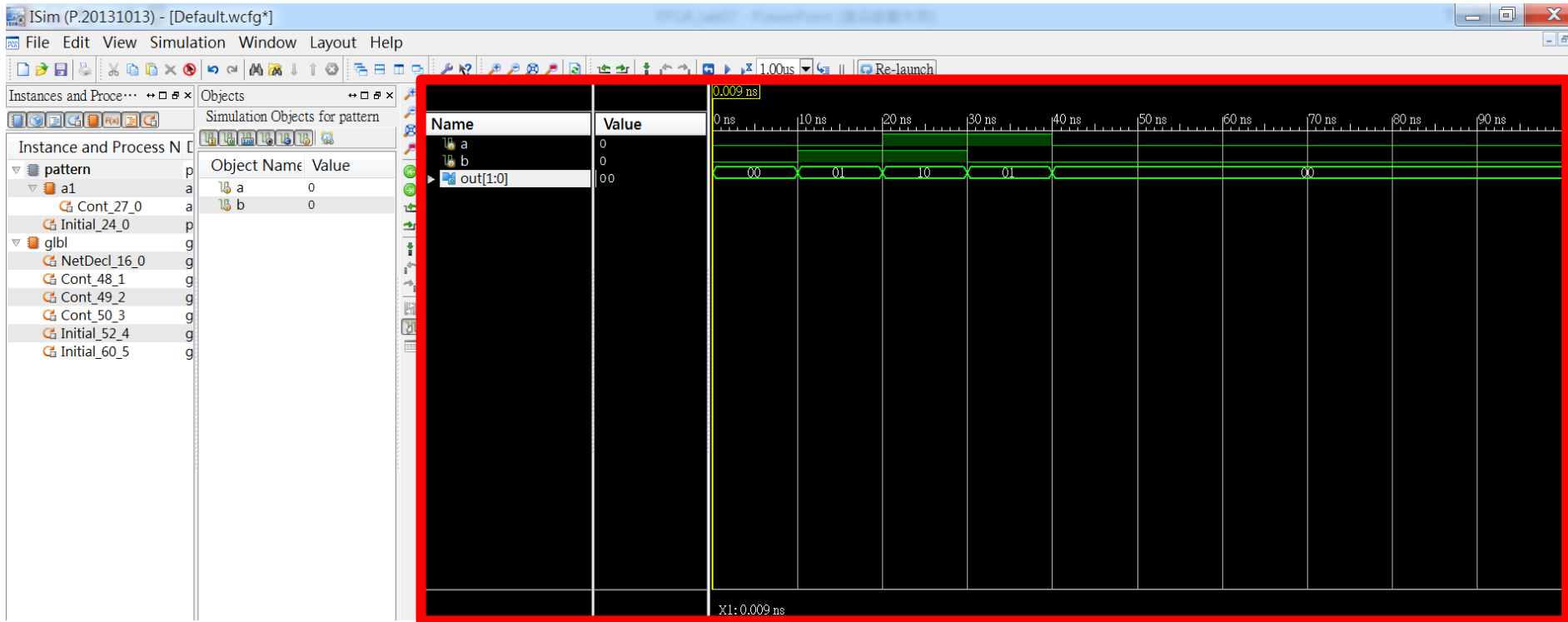


# Wave Diagram





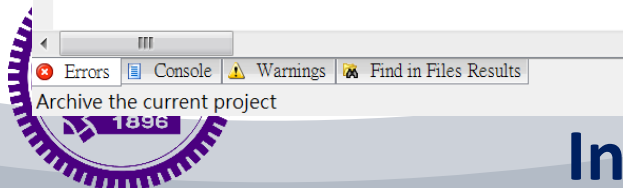
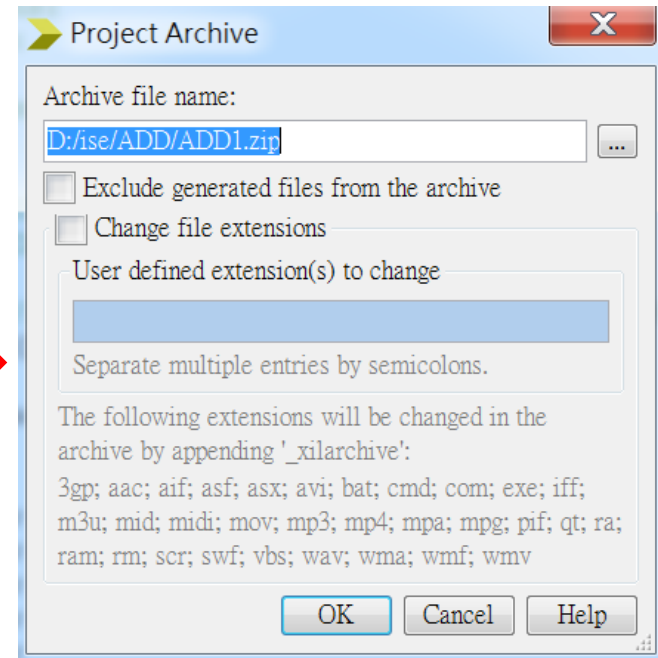
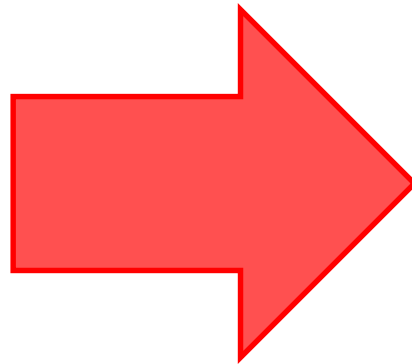
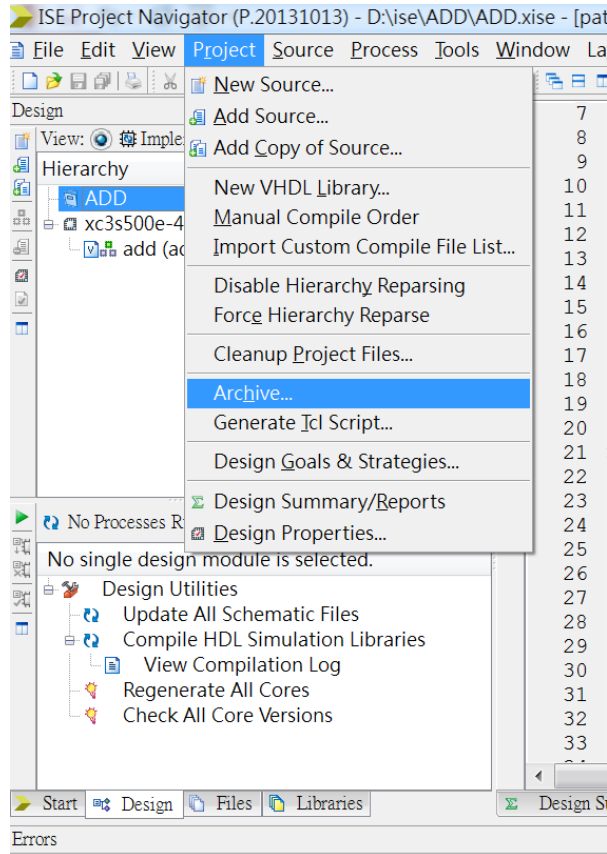
# Wave Diagram



**You get your wave**

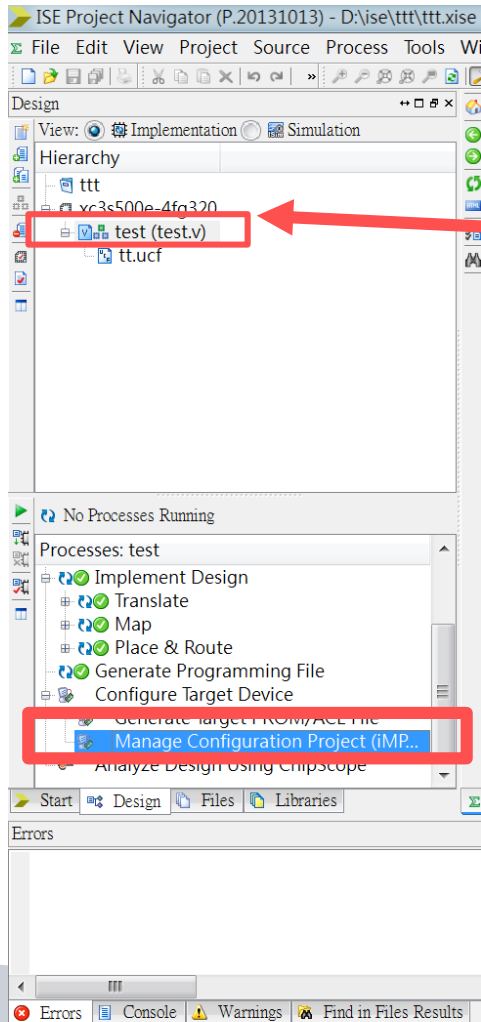


# Archive



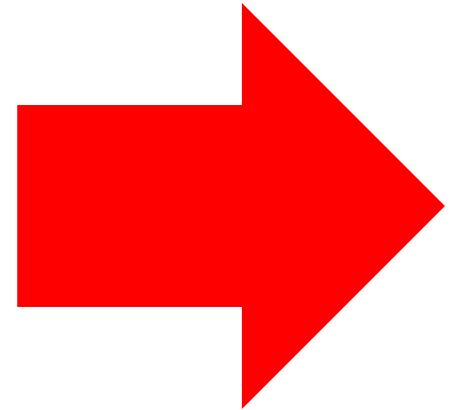
# Transplantation

- After **all your designs are correct**, transplant your program file onto FPGA

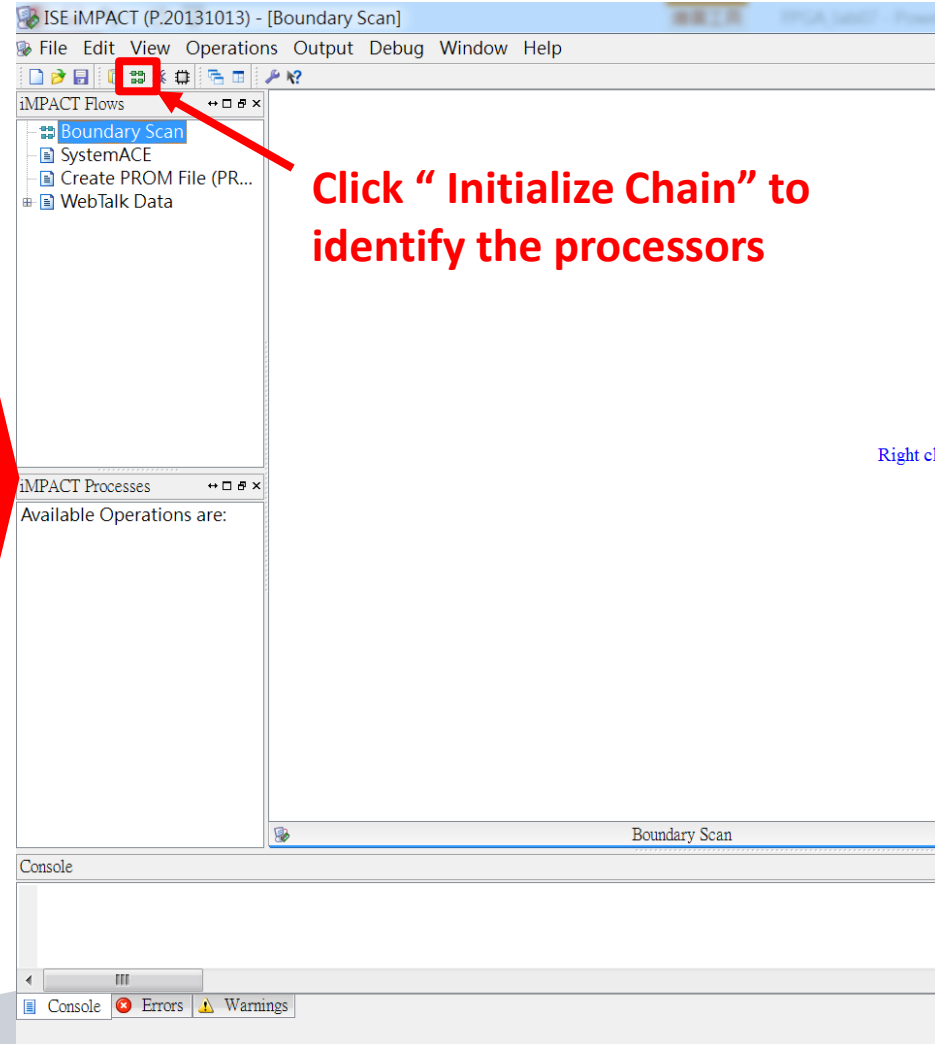
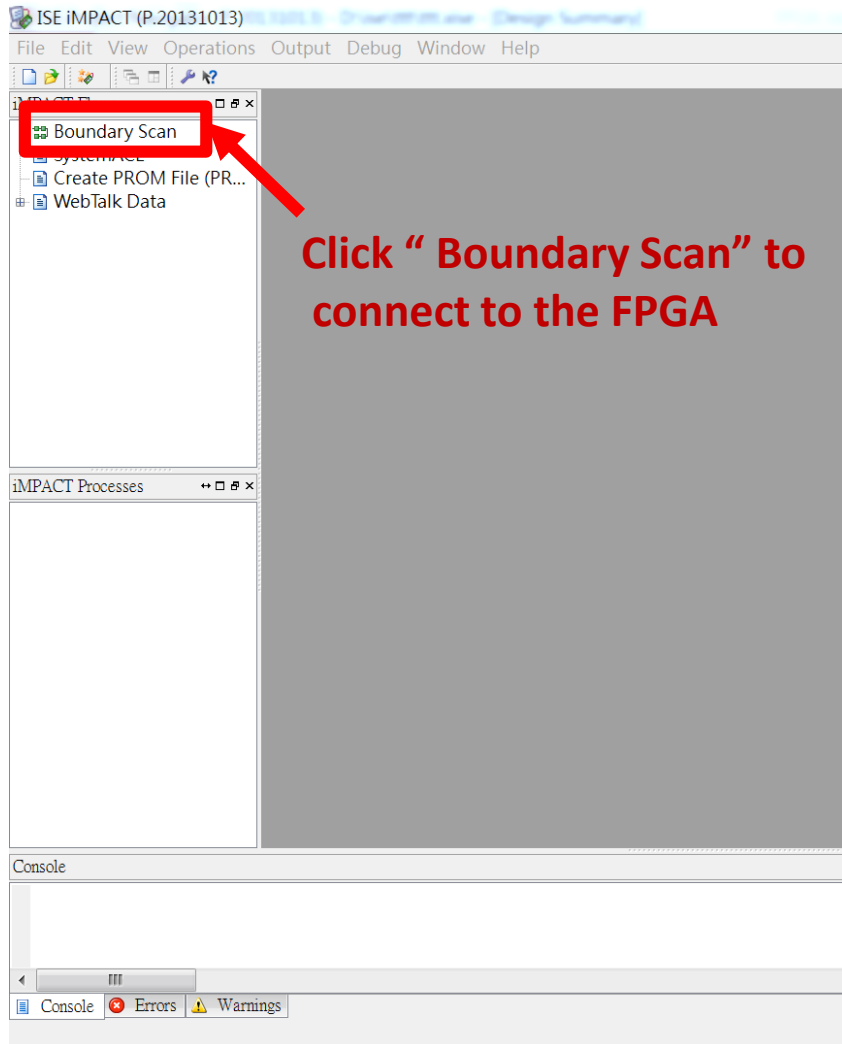


1) Select the top module of your design

Double click "Manage Configuration Project(iMACT)" to run generate programming file.

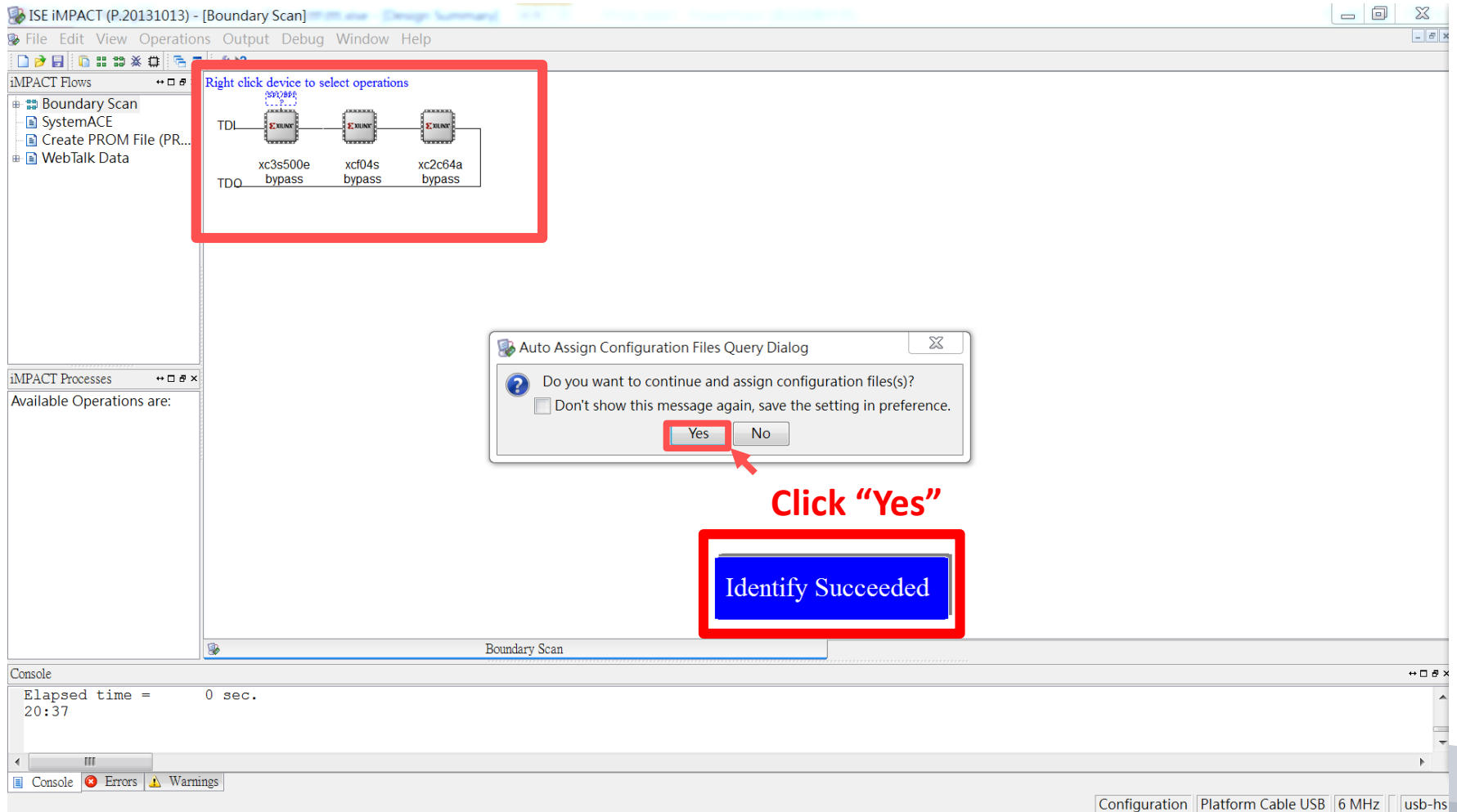


# Transplantation

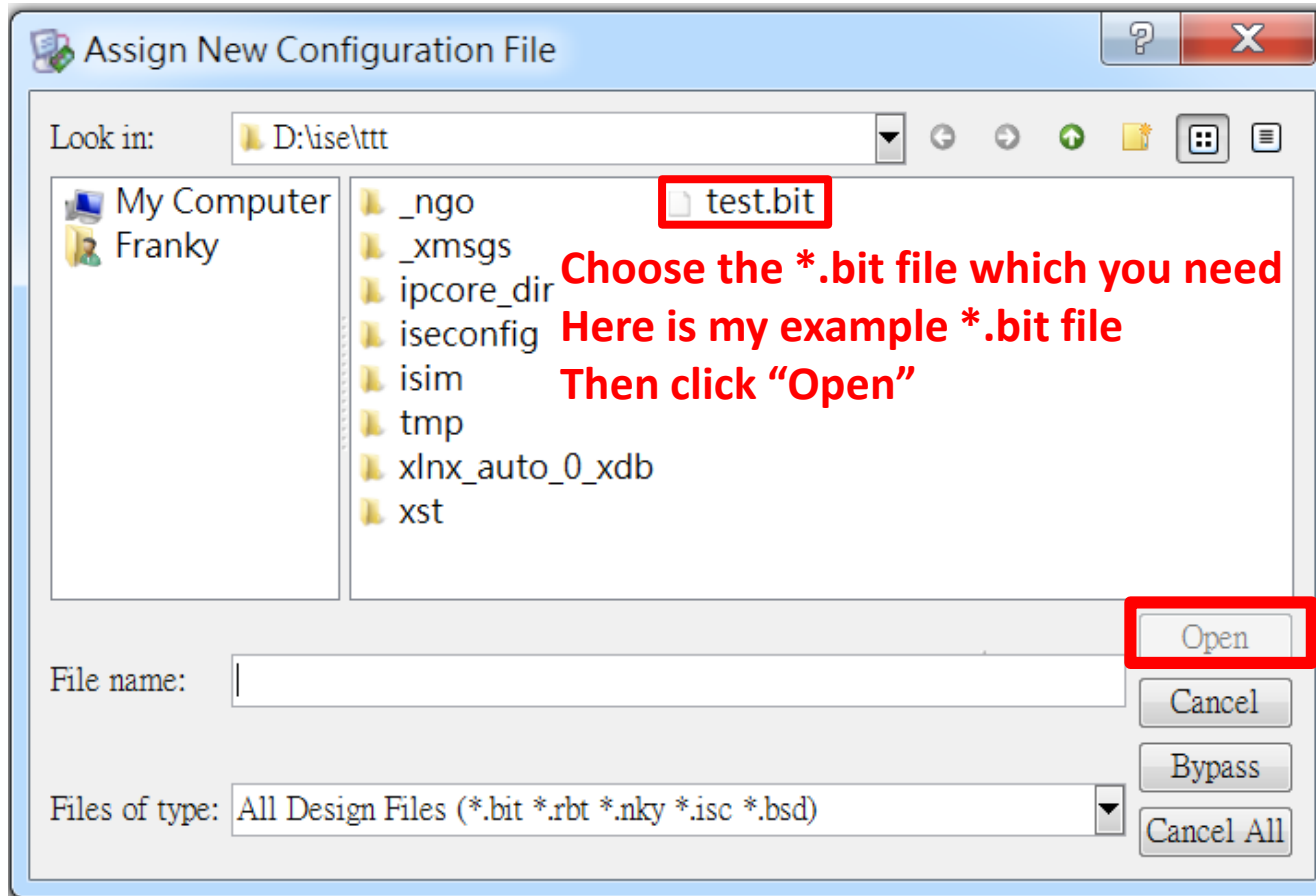


Right cli

# Transplantation



# Transplantation



# Transplantation

**Attach SPI or BPI PROM**

This device supports attached Flash PROMs. Do you want to attach an SPI or BPI PROM to this device?

Yes **No**

**Choose "Bypass" for the next two decisions**

**Assign New Configuration File**

Look in: D:\ise\lvt

My Computer Franky

- \_ngo
- \_xmsgs
- ipcore\_dir
- iseconfig
- isim
- tmp
- xlnx\_auto\_0\_xdb

File name:

Files of type: All Design Files (\*.mcs \*.isc \*.bsd)

**Bypass**

**Identify Succeeded**

ISE iMPACT (P.20131013) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

iMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PR...
- WebTalk Data

iMPACT Processes

Available Operations are:

- Get Device ID
- Get Device Signature/User
- Read Device Status

Boundary Scan

Console

20:37

Console Errors Warnings



# Transplantation

The diagram shows a JTAG chain with three devices: xc3s500e test.bit, xcf04s bypass, and xc2c64a bypass. The xc3s500e device is highlighted with a blue dashed box. The Device Programming Properties dialog box is open, showing the Boundary-Scan category and a list of devices. The 'FPGA Device Specific Programming Properties' table is visible, with the 'Verify' and 'Pulse PROG' rows highlighted. The 'OK' button is highlighted with a red box.

Diagram showing a JTAG chain configuration:

- TDL
- xc3s500e test.bit
- xcf04s bypass
- xc2c64a bypass
- TDQ

Device Programming Properties - Device 1 Programming Properties

Category

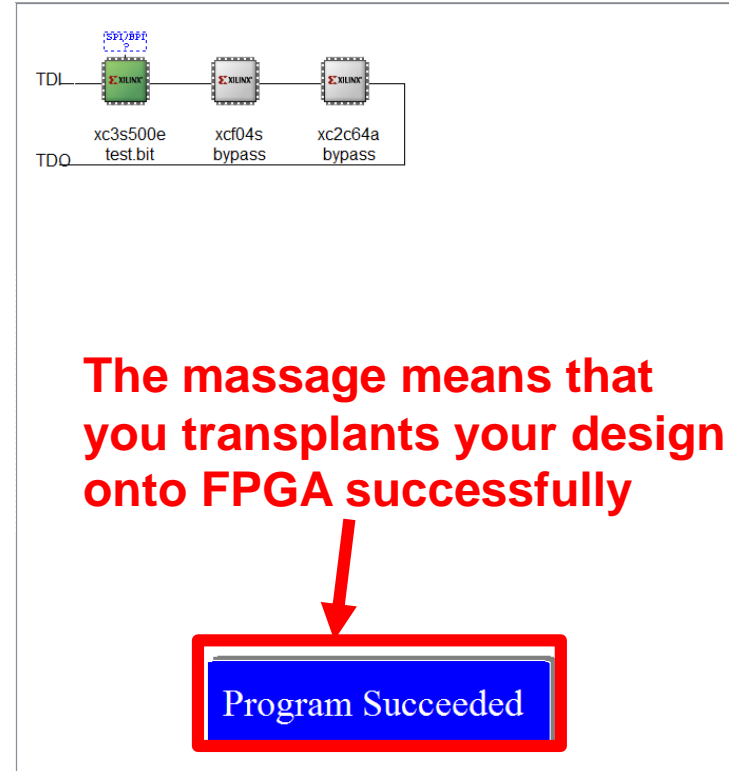
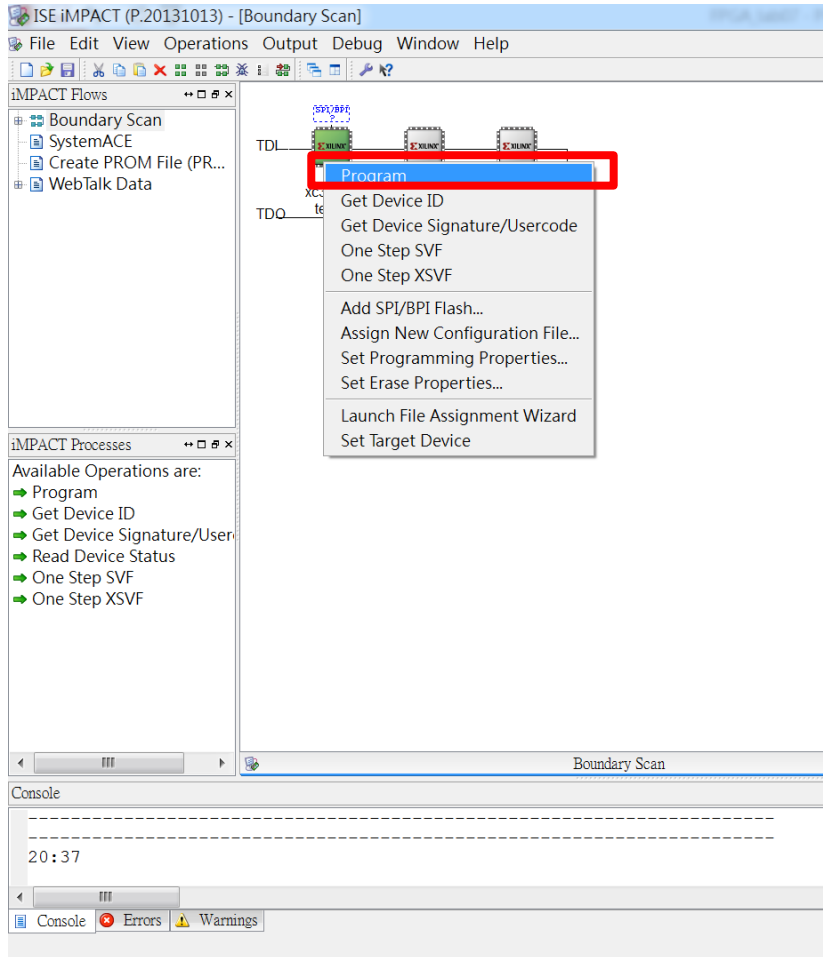
- Boundary-Scan
  - Device 1 ( FPGA xc3s500e )
  - Device 2 ( PROM xcf04s )
  - Device 3 ( CPLD2 xc2c64a )

| Property Name                               | Value                    |
|---|--------------------------|
| Verify                                      | <input type="checkbox"/> |
| FPGA Device Specific Programming Properties | <input type="checkbox"/> |
| Pulse PROG                                  | <input type="checkbox"/> |

OK Cancel Apply Help

Identify Succeeded

# Transplantation



# Thank You

