NCTU-CS DLab.

Lab07 (Led,Buttom,Switch,IP)

Design: Calculator

Data Preparation

Prepare following files by yourselves:
CAL.v
CAL.ucf

Design Description

You should design an easy calculator on the FPGA.
There are 4 buttons , 4 switchs, 8 LEDs will be used.

INPUT

Name	Location	Fuction
BTN_SOUTH	K17	Reset signal
BTN_WEST	D18	Square root
BTN_NORTH	V4	Multiplication
BTN_EAST	H13	Addition
SW0	L13	2^0
SW1	L14	2^1
SW2	H18	2^2
SW3	N17	2^3

OUTPUT

Name	Location	Fuction
LED0	F12	Specify as the answer[7:0] Ex. LED0 => answer[0]
LED1	E12	
LED2	E11	
LED3	F11	
LED4	C11	
LED5	D11	
LED6	E9	
LED7	F9	

First step:

We will use 4 switches to give you the input number

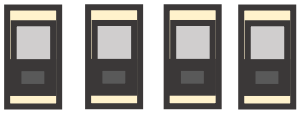
Second step:

According to the 4 buttoms，you should output the corresponding answer on LED.

And the answer should be stored for the next operand to calculate the answer.

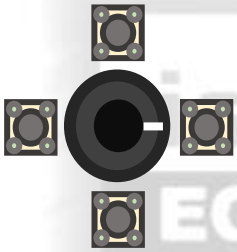
For example:

First step:



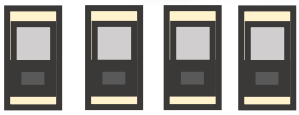
0 0 1 1 (3)

Second step:



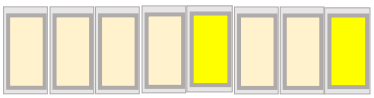
(add)East is pressed

Third step:



0 1 1 0 (6)

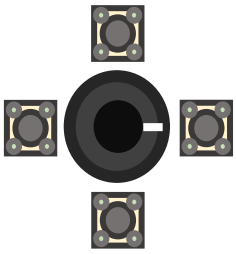
Forth step:



(9)

Fifth step:

(root)West is pressed



Sixth step:

 (3)

And so on…

Specification

1. All outputs are synchronized at clock positive edge.
2. It is asynchronous, active-high reset architecture.
3. Square root should use IP.
4. Reset means calculate restart.
5. All numbers are unsigned and integer.

Grading Policy

Function Validity: 80%

Questions: 20%