

CMOS INTRA-CHIP WIRELESS CLOCK DISTRIBUTION

By

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As the clock frequency and chip size of high-performance microprocessors increase, distributing clock signals across the chip becomes increasingly difficult due to increasing propagation delays and decreasing allowable clock skew. This dissertation presents the design, implementation, and demonstration of an intra-chip wireless clock distribution. The system consists of transmitters and receivers with on-chip antennas communicating via electromagnetic waves at the speed of light. A global clock signal is generated and broadcasted using a transmitting antenna. Clock receivers distributed throughout the chip detect the signal using on-chip antennas, amplify and divide it down to a local clock signal, and buffer and distribute the clock signals to the adjacent circuitry.

To synchronize all the receivers across the chip, a scheme using a transmitted global clock signal with 2-ns no transmission period and the programmable divider in receiver is proposed. The package (such as the heatsink) and on-chip metal structures can significantly affect the on-chip antenna characteristics. AlN, an insulator with high ther-

mal conductivity is used to reduce the heatsink effects and increase the antenna pair gain ~ 8dB. A general design guideline is also proposed to reduce the on-chip metal structures' impact on the antenna performance. In addition, thinning the lossy substrates to 100 μ m increases the gain of an on-chip antenna pair with 1.0 cm separation by ~15dB.

A broadband low noise amplifier (LNA) preceding the programmable divider and detector in the receiver is demonstrated using a 8-level-metal 130-nm CMOS process. It has 20 dB voltage gain at 20.6 GHz, 5.5 dB noise figure and 4 GHz 3-dB bandwidth.

An intra-chip wireless clock distribution system is successfully demonstrated using on-chip antenna pairs, a clock receiver, and a clock transmitter. With 0.26-mm separation between the antenna pair, the system is working between 17 GHz and 18.7 GHz. The peak-to-peak jitter of the whole system (excluding VCO in transmitter) is 5.4ps, or ~1.21% of a local clock period. The programming bits of the divider is also successfully demonstrated at 18 GHz. Because of the divider programmability, the maximum skew of this system should be less than 1/16 of a local clock period, which is 6.25% of a local clock period. Using an off-chip power amplifier which increases the transmitter output power from 4 to 11dBm, the system is demonstrated at 2.5-mm separation between the transmitting antenna and the receiver. These measurement results demonstrate the synchronization scheme of the intra-chip wireless clock distribution system, and indicate that wireless approach can be a practical for clock distribution option in the future microprocessors.

CHAPTER 1 INTRODUCTION

1.1 Clock Distribution Networks in Synchronous Digital Integrated Circuits

In a synchronous digital system, the clock signal is used to define a time reference for the movement of data within the system and to synchronize the flow of data signals among the synchronous data paths. The characteristics of clock signals are that they are typically loaded with the greatest fanout, travel over the longest distance, and have the highest frequency within the entire system. The demand for a higher speed microprocessor requires an increasing clock frequency. Transistor scaling enables the increase of the computation speed by shrinking the clock cycle time. However, the associated rise time of clock and the allowable time uncertainty of its arrival time (jitter and skew) must also be proportionally shrunken. This shrinking rise time, jitter and skew budgets necessitate the improvement on clock generation and distribution.

1.1.1 Conventional Clock Distribution Network

The most common and general approach to equipotential clock distribution is the buffered clock distribution trees [Fri01], where buffers are inserted at the clock source and along a clock path to amplify the clock signals degraded by the distributed interconnect impedance, and to isolate the local clock nets from upstream impedances (Figure 1-1). These buffers are a primary source of clock skew which is defined as the static differences in the arrival times of a clock signal measured between two or more distribution points

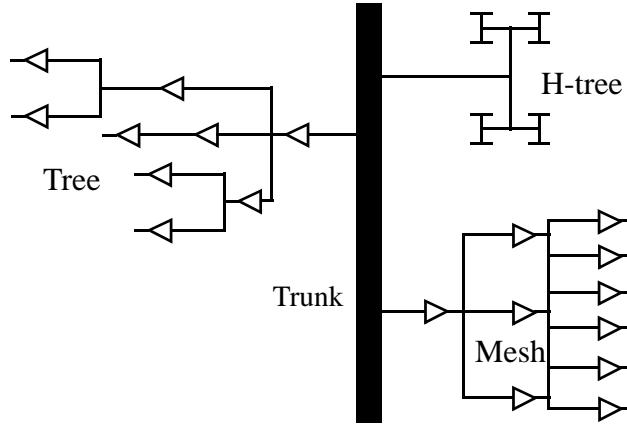


Figure 1-1 Common structures of clock distribution networks including a trunk, tree, mesh and H-tree.

within a clock distribution network. This is because the active device characteristics vary more than those of the passive device characteristics. To reduce static skew, a hierarchy of planar symmetric H-tree or X-tree structures shown in Figure 1-2 is used. By reducing the mismatch among the distributed interconnect and buffers[Bak86, Nek93], clock skew is reduced.

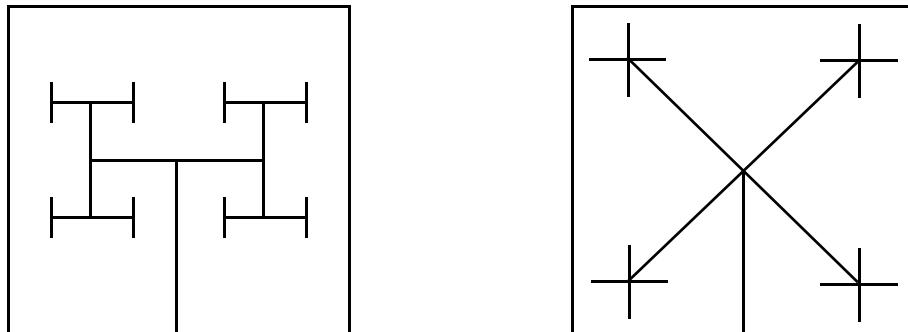


Figure 1-2 Symmetric H-tree and X-tree clock distribution networks.

Over the course of the past three decades, microprocessor clock frequency has increased from 108 kHz in 1971[Int75] to over 3.0 GHz at present [Del02]. According to the 2003 International Technology Roadmap for Semiconductors (ITRS), the global clock frequency will increase to 9.285 GHz in 2007 and 15.079 GHz in 2010, while the chip size

will increase to 17.6 mm x 17.6 mm. With this increasing global clock frequency and chip size, clocking large digital chips with a single high-frequency global clock is becoming a more and more difficult task using the conventional clock distribution technique mentioned above. There are three main challenges: reducing skew/jitter, limiting power consumption increase and mitigating the clock frequency limitation set by the dispersion associated with the interconnect resistance.

Skew and jitter are the two sources of timing uncertainty. As mentioned, skew represents the static difference in the arrival times of a clock signal as measured between two or more distribution points. Jitter represents the dynamic difference in the arrival time of the clock signal as measured at the same distribution point. Usually, 10% of a clock cycle is allocated for skew and jitter margin. With the gate scaling, the global wire delays stay approximately the same or increase due to the increase in chip size. On top of this, the increasing capacitive loading of the clock network further increases the delay. Because of this increased RC delay, a sharp edge at the input of such a wired system will have a much longer rise time at the destination, requiring more levels of buffering to build up adequate gain to achieve short rise time (slew time targets of generally no more than 10~20% of a

Table 1-1 2003 ITRS

Year	2007	2010
Physical Gate Length	25 nm	18 nm
Local Clock Frequency	9.285 GHz	15.079 GHz
uP Chip Size (mm ²)	310	310
Power Supply	0.8	0.7
Max. Power (uP), Heat Sink	189 W	218 W
Max. Number Wiring Levels	11	12

clock period). However, these buffers will increase the latency in the global clock network, and lead directly to the problems of uncompensated skew and jitter primarily due to the intra-chip variability and power supply noise coupling through buffers.

Clock distribution involves delivering a sharp clock edge to hundreds of thousands of static and dynamic latches which represent a capacitive load of several nanofarads. The power needed to charge and discharge this capacitance alone is $C \cdot V_{dd}^2 \cdot f$, where C represent the clock load capacitance and f is the clock frequency. With the clock frequency and capacitance increasing with each technology generation, offset only slightly by decreasing power supply voltages, the dynamic power dissipation associated with clock distribution is becoming an increasingly larger portion of the total power of a system. For example, in the Itanium processor [And02], the power required to switch a total of 7-nF of capacitance is 23 W.

The third challenge is the maximum clock frequency limitation caused by the dispersion associated with the interconnect resistance. In the conventional system, the clock signal is a square wave, including up to 7th harmonics. A non-zero interconnect resistance will cause the harmonics of the clock signal to travel at different velocities through the interconnect, resulting in an increase of the rise and fall times of the signal. These increases can ultimately limit the maximum frequency of the clock signal [Deu98].

To cope with the skew/jitter, power and dispersion challenges resulting from the 2003 ITRS requirements of higher clock frequency and larger chip size, numerous approaches to improve the clock distribution system have been proposed. To reduce the global clock skew, a closed-loop distribution network with active compensation is used to measure and adjust phase differences among clock signals reaching different portions of

the chip. In such a distribution network, active compensation (typically achieved through a delay-locked loop) can eliminate the majority of skew from the global clock signals, leaving jitter as the dominant limitation for clock performance [Gre00, Kur01, Tam00, Xan01] (see Table 1-2). The percentage of a clock period consumed by jitter is increasing with clock frequency due to the presence of higher power supply noise in increasingly complex microprocessors. This suggests that reducing skew alone is not adequate. Also, to reduce the power dissipation of clock distribution system, a clock network operating at half the power supply swing is proposed, reducing the power dissipated in the clock tree by 60% [Koj94]. However, this power reduction is at the cost of degraded speed performance. All these solutions are able to overcome the shortcoming of the conventional sys-

Table 1-2 Summary of High-performance Electrical Clock Distribution Networks Reported

Microprocessor	f_c (GHz)	L (μm)	Die Area (mm ²)	Global Wiring Distribution	Distribution Topology	Global Skew	P-P Jitter
Alpha 21364 [Xan01]	1.2	0.18	397	X-Tree, H-tree, Grid, Spine	CLAC	10.8%	N. A.
IA-64 [Tam00]	0.8	0.18	N. A.	H-Tree, Binary, Tree, Grid	CLAC	2.24%	N. A.
Pentium III [Gre00]	1.0	0.18	N. A.	N. A.	N. A.	3.5-7.0%	9.2%
Pentium IV [Kur01]	2.0/4.0	0.18	N. A.	Binary Tree	CLAC	3.2%	7.0%
Power PC [Hof00]	1.15	N. A.	N. A.	H-Tree, Grid	CL	1.72%	4.9%
Power 4 [Res02]	1.3	N. A.	N. A.	H-Tree, Grid	CL	3.25%	3.9%

CL--Closed Loop

CLAC--Closed Loop with Active Compensation

tem only in the near term. Therefore, new approaches for clocking must be investigated to develop approaches for future chips.

1.1.2 New Concepts of Clock Distribution Networks

To deliver the higher frequency global clock signal to a larger chip, new clock distribution concepts from novel architectures to alternative signaling media are proposed and being investigated. The list includes

- 1) a clock distribution system using distributed PLL [Gut00],
- 2) clock distribution using coupled standing-wave oscillators [Oma03],
- 3) resonant global clock distribution [Cha03],
- 4) low-power RF clock distribution [Ryu02],
- 5) optical clock system [Mul00, Tew97].
- 6) wireless clock distribution concept [O97].

In a clock network comprised of an array of distributed synchronized PLLs, independent oscillators generate the clock signal at multiple points across a chip [Gut00], and each oscillator distributes the clock to only a small section of the chip (“tile”) (Figure1-3). Phase detectors at the boundaries between tiles produce error signals that are summed by an amplifier in each tile and are used to adjust the frequency of node oscillator. With locally generated clocks (1.1 GHz ~1.3 GHz), there are no chip-length clock lines to couple in jitter, and the measured cycle-to-cycle jitter is less than 10 ps, which is ~1% of a clock cycle. Skew is introduced only by asymmetries in phase detectors, and measured to be 30 ps, ~3% of a clock period. Also, the local interconnect is much shorter, and the dispersion effects will be reduced. Another benefit of this system is that this network need not be regular. Because this proposed network has many nodes, the power and size con-

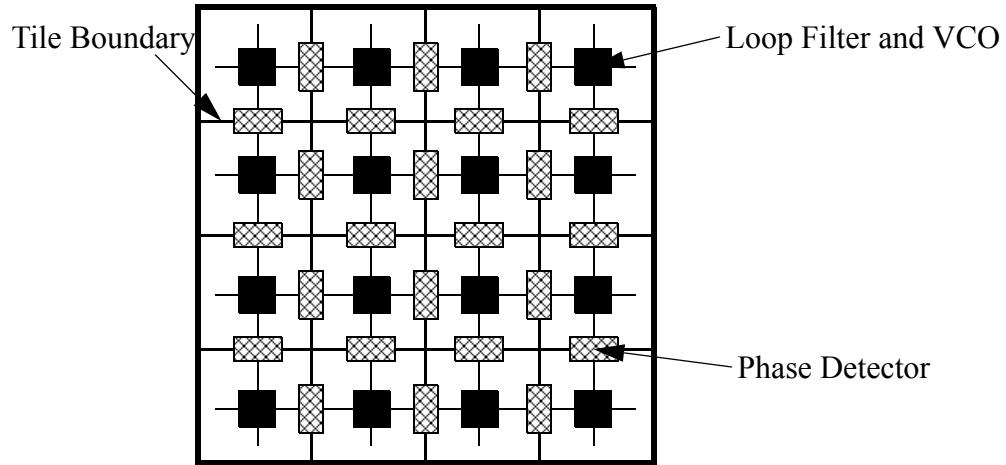


Figure 1-3 Distributed clocking network using distributed PLLs.

straints on each node need to be even more stringent. Although neither the power nor the area overhead of multiple PLL's is substantial compared to the cost of distributing the clock by conventional means, this system does not have power or area advantage over the conventional ones.

The global clock distribution system using coupled standing-wave oscillators (SWO) [Oma03] is shown in Figure 1-4. The clock network is comprised of SWO's cou-

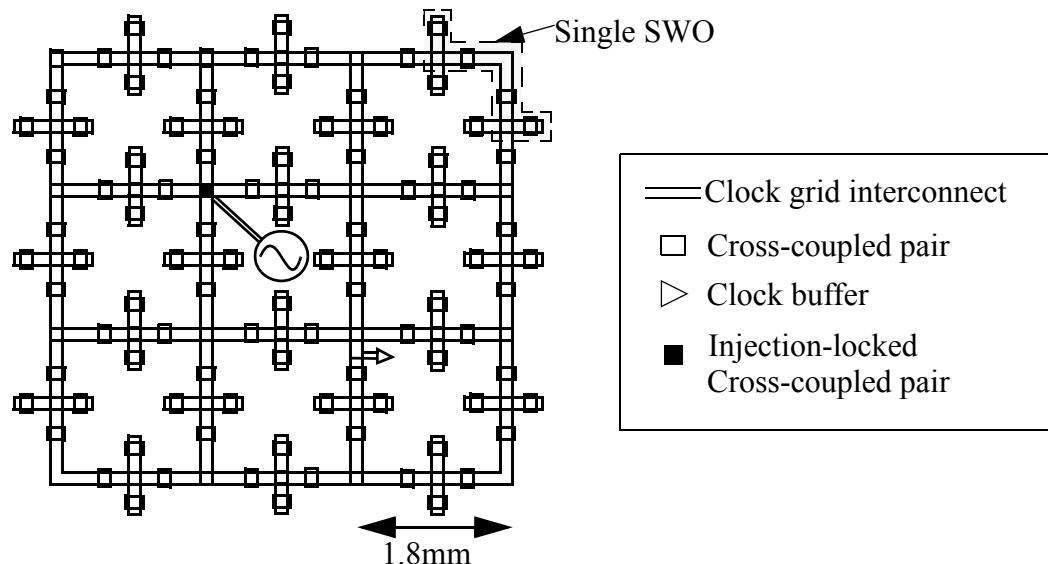


Figure 1-4 10-GHz standing-wave clock distribution network.

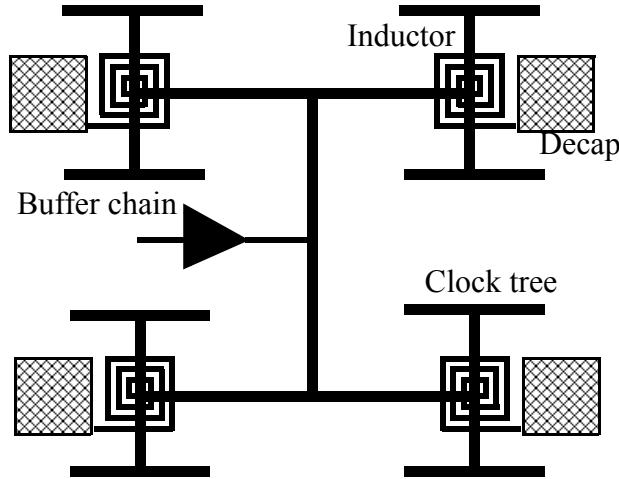


Figure 1-5 Resonant clock network consists of a buffer chain, spiral inductors and decoupling capacitors.

pled through clock grid interconnects. Within a grid of coupled oscillators, phase is averaged at each coupling point, so the phase differences among the SWO's are reduced by this averaging process. In this 10 GHz clock distribution system, for a 3 mm by 1 mm area, the measured skew is less than 4 ps and RMS jitter is 0.8 ps. Adding skew and jitter together is ~8.8% of a clock cycle. Because a sine wave is generated by the SWO's, dispersion effects are minimized. The limitation of this system is that it requires very regular clock network structures. Also, due to the large losses of on-chip interconnects, its power consumption is comparable to the conventional clock distribution system.

Another approach, the resonant global clock distribution system [Cha03] operates more like a conventional clock distribution, but the large clock capacitance is made to resonate with a set of on-chip inductors. This significantly reduces the power necessary to drive the grid (Figure 1-5). Also because of this dramatically reduced effective capacitance of the clock network, the number of gain stages and the associated latency (pipeline delay) required to drive the clock are reduced, resulting in a considerable improvement in skew and jitter. Such a resonant clock distribution benefits most from a sinusoidal clock,

which will also minimize the dispersion effects. In this paper, the total capacitance of the clock tree and mesh occupying an 2.5 mm by 2.5 mm area is assumed to be 9.5 pF, the on-chip inductor and decoupling capacitor should be 2.2 nH and 85.5 pF respectively for 1.1 GHz clock distribution. This 85.5 pF decoupling capacitor is too big for on-chip realization.

The RF clock distribution [Ryu02] consists of an RF clock transmitter and clock receivers including matching networks, RF amplifiers and an inverter chain as shown in Figure 1-6. The main benefit for this system is the lower power consumption through the use of a small voltage swing and elimination of the repeaters on the global clock grid. Since a single tone sine wave is used in the system, it reduces the dispersion effects. However, the voltage swing of the clock signal is small and the rise time of the clock signal is long compared to a digital signal with the same clock frequency. Therefore, the clock signal is more susceptible to common-mode supply noise, which induces jitter that is proportional to the rise time of the clock signal. Good common-mode rejection differential amplifiers are needed to reduce the common-mode induced jitter.

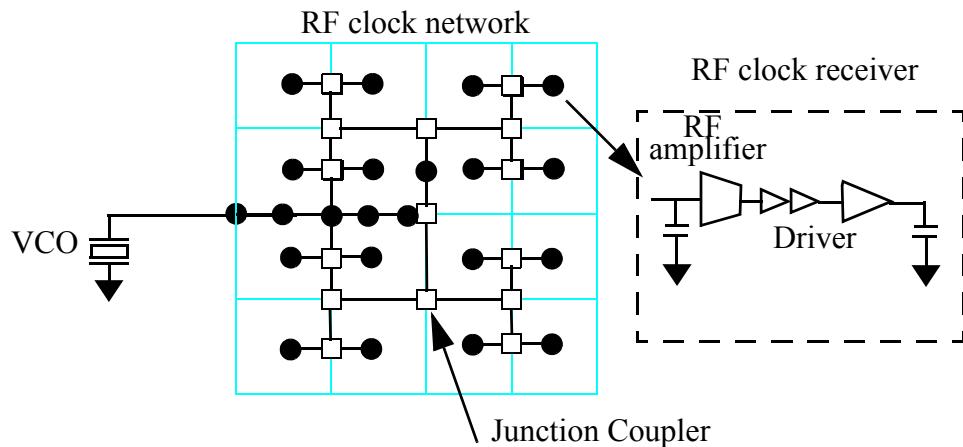


Figure 1-6 RF clock distribution.

At present, the most radical clock distribution option is the optical approach. In general, two different approaches exist for optical clock distribution, which are distinguishable based on the propagation medium between the photon source and chip level detectors: a) focused free-space [Tew97] and b) guided wave [Mul00] shown in Figure 1-7. Even though these optical methods have excellent signal integrity properties compared to the other methods previously discussed, the drawback of the optical clock distribution is that it is bulky, difficult to fabricate, expensive and not compatible to current CMOS technology.

1.2 Intra-chip Wireless Clock Distribution System

Another approach is the intra-chip wireless clock distribution system. It is an option proposed early on as an alternative to the optical and conventional clock distribution technique. Compared to the optical approach, it is a more practical technique that fits better to the CMOS technology. The basic concept is illustrated in Figure 1-8 [O97]. This intra-chip wireless clock distribution system has a transmitter in the center of the chip and

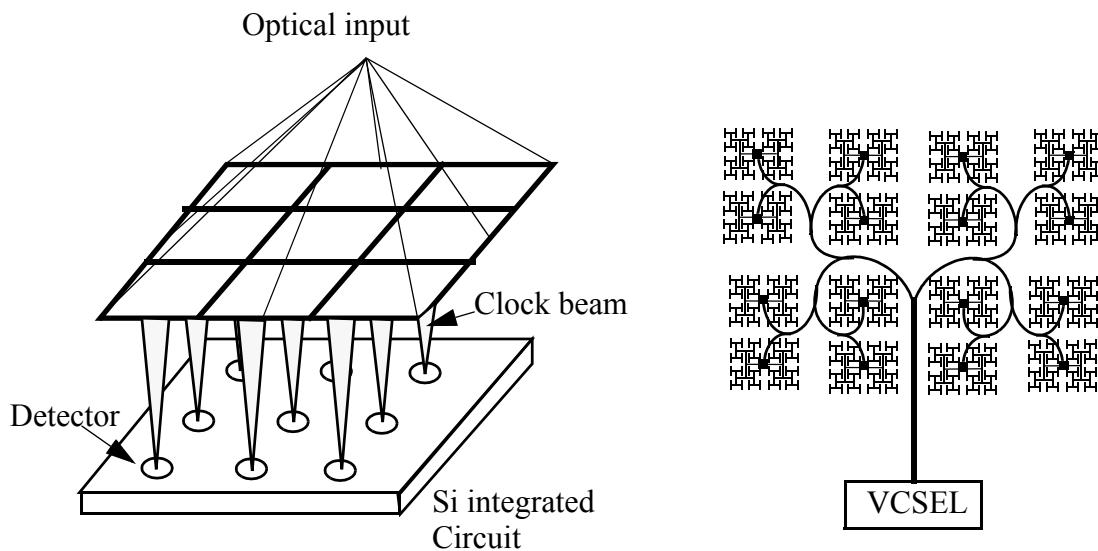
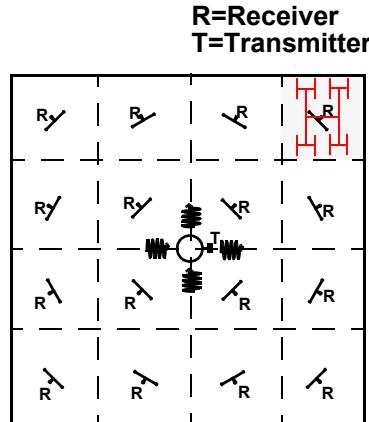


Figure 1-7 Focused free-space optical distribution and optical clock distribution using integrated optical waveguides.



Within an IC

Figure 1-8 The basic concept of the intra-chip wireless clock distribution system.

distributed receivers across the chip to receive the global clock and provide the local clock. The receiver is similar to that for the RF clock distribution system. The difference is that instead of using transmission lines, the wireless system uses on-chip antennas to transmit and receive the global clock signal.

In addition, to reduce the size of the on-chip antennas, a much higher global clock frequency (~20GHz) is generated by the transmitter and used as the global clock. Because of this, at the receiver side, the high frequency global clock is divided down to a lower frequency for local clocking. This higher global clock frequency provides a sharper edge (faster rise time) for the clock signal compared to that of the other RF approaches, and should lead to smaller jitter. The block diagram of a receiver in the wireless system is shown in Figure 1-9 [Flo99]. The receiver consists of an on-chip antenna, RF low noise

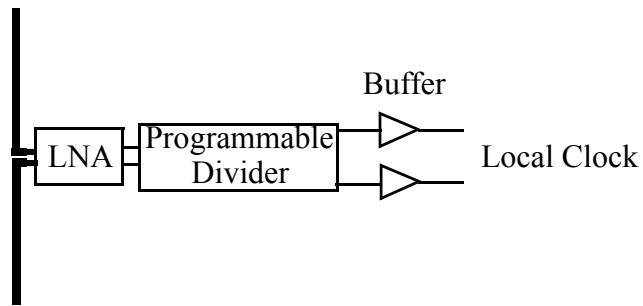


Figure 1-9 The block diagram of a receiver.

amplifier (LNA), and a divide-by-8 circuit with programmable delays, and buffers to drive the local clock trees.

The main advantages of this intra-chip wireless clock system are, first, the clock signal is propagated at the speed of light of propagation medium, which reduces the latency of the clock distribution system. This should make the static skew introduced by process variation and load mismatch easier to correct. Second, compared to a square wave clock, this single tone sine wave transmission has smaller bandwidth requirement which eliminates the need for a large number of repeaters, and replaces with receivers using tuned amplifier. Since the repeaters are broadband circuits, the gain will be lower than the narrow-band tuned amplifier in the receivers. Therefore, more stages of repeaters are needed, and the skew, jitter and power consumption associated with these repeaters should be worse than those caused by receivers. Also, this high frequency global clock signal (~8 times higher than local clock frequency) will have less noise effects on the local digital circuits and also affected less by the noise of the digital circuits, and should lead to better jitter performance. The reported peak-to-peak jitter of a receiver is 0.41% of a local clock cycle (925 MHz) [Dic02]. When surrounded with switching noise generators, the receiver peak-to-peak jitter increases to 3.63% of a local clock cycle. It should be possible to lower these by using guard rings or deep n-well. Third, this wireless system has no need for wired connection. This frees up the metal layers dedicated for wired connection. By year 2018, the circuits can operate above 100 GHz, and the area penalty associated with on-chip antennas will become smaller.

1.3 Design Challenges of the Intra-chip Wireless Clock Distribution System

The first challenge is that for a synchronous system, all the clocks should start at the same time and have the same clocking edges. Although the clock signal is propagated at the speed of light through the chip, it still arrives to varying points in the chip at different times due to varying distances to the transmitter and varying metal structures between the transmitter and receivers. This different arrival time of the transmitted signal will cause static skew. How to compensate the skew and start the distributed receivers at the same time are major design issues that must be solved to realize an intra-chip wireless clock distribution system.

The second challenge of this system is the on-chip antenna. The gain of this on-chip antenna can be significantly affected by the metal structures surrounding it, such as a heatsink, and the on-chip and package metal structures near the antenna. Mitigating the effects of heatsink and metal structures near the antenna is another critical challenge for developing a clock distribution system.

1.4 Overview of Dissertation

This dissertation focuses on the realization of an intra-chip wireless clock distribution system. This work focuses on the design and entire system feasibility evaluation by implementing and demonstrating a wireless clock distribution system.

In Chapter 2, a scheme for synchronizing the receivers distributed across a chip using an intra-chip wireless clock distribution system and the circuits realization are introduced. The circuit implementation and the measurement setup for system demonstration are also proposed in Chapter 2. Chapter 3 discusses the effects of package (such as the heatsink) and on-chip metal structures on the on-chip antenna characteristics. A general

design guideline to reduce the effects is proposed. In addition, thinning the lossy silicon substrate to increase the on-chip antenna gain is investigated. In Chapter 4, a broadband low noise amplifier (LNA) preceding the programmable divider and detector in the receiver is demonstrated. This broadband LNA has 20 dB voltage gain at 20.6 GHz, 5.5 dB noise figure and 4 GHz 3-dB bandwidth. This LNA has widest 3-dB bandwidth and the lowest power consumption among all the bulk CMOS LNAs that are working above 20 GHz.

Chapter 5 demonstrates the wireless clock distribution system using the UMC 130nm CMOS technology. Due to the lower antenna pair gain, the system is demonstrated with 0.26-mm separation between the transmitting and receiving antennas. The system operates between 17 GHz and 18.7 GHz. The peak-to-peak jitter of the whole system (excluding VCO in transmitter) is 5.4ps, or $\sim 1.21\%$ of a local clock period. The programming ability of the divider is also demonstrated successfully when the system is working at 18 GHz. Because of the divider programmability, the maximum skew of this system should be less than 1/16th of a local clock period, which is 6.25% of a local clock period. Adding the skew cause by intra-chip fabrication variation and temperature variation (10°C), the total skew is 7.6% of the local clock period. Using an off-chip power amplifier which increases the transmitter output power from 4dBm to 11dBm, the system is demonstrated at 2.5-mm separation between the transmitting antenna and the receiver. These measurement results demonstrate the synchronization scheme of the intra-chip wireless clock distribution system, and indicate that wireless approach can be practical.

Finally, Chapter 6 contains conclusions and summaries of this thesis and suggestions for future work.

CHAPTER 2 INTRA-CHIP WIRELESS CLOCK DISTRIBUTION SYSTEM

2.1 Introduction

As mentioned in Chapter 1, a transmitter at the center of a chip generates the high frequency global clock signal to synchronize the receivers distributed over the chip. Using on-chip antennas, receivers pick up the global clock signal and divide it down to provide the local clock signal. However, in this system the different distances between the transmitter and the receivers, and the different metal structures between transmitter and receivers, cause different time of flight to different receivers, that is, the transmitted signal arrives at different receivers at different times. This is a major source of static skew. To realize a practical clock system, techniques to compensate the static skew and to start the receivers at the same time are needed. The former works [Flo01, Flo02a] only demonstrated the wireless interconnect between a transmitter and the receivers.

This chapter concentrates on the synchronization scheme, which is used to start the receivers at the same time. To implement the scheme, the structures of the transmitter and receivers have to be modified and the requirement of this system is also changed. A characterization setup to demonstrate the synchronization between two receivers is also proposed in this chapter.

2.2 The Synchronization Scheme of the Intra-chip Wireless Clock Distribution

Shown in Figure 2-1 is the block diagram of a transmitter and a receiver. In the transmitter, a VCO generates a continuous 20-GHz sine wave and the output buffer ampli-

fies this signal. At the same time, the control circuit generates a 2-ns control signal to make the buffer output have 2-ns no clock transmission period. On the receiver side, the LNA amplifies this received signal, and feeds it into both the divider with programmable delays and the detector. As explained in Dong-Jun Yang's thesis [Yan04], the detector generates a pulse signal (INI) from this 2-ns no clock transmission period to control the programmable divider. At the rising edge of the INI, the divider loads the initialized value (the programmed delay). After receiving the INI signal falling edge, the divider starts counting down the programmed delay at the first crossing point of the clock signal, and then starts dividing. The programmed delay is used to compensate the static skew for different dividers.

In this synchronization scheme, the 2-ns no transmission period is critical. It is used to start up all the dividers at almost the same time. This scheme eliminates the need to transmit the control signal to different receivers through wired connection, simplifying routing easier. In addition, this synchronization scheme can easily be realized by just adding control circuits on the transmitter side and a detector on the receiver side with a minimal increase to the complexity. Since there is no wired connection between the transmitter

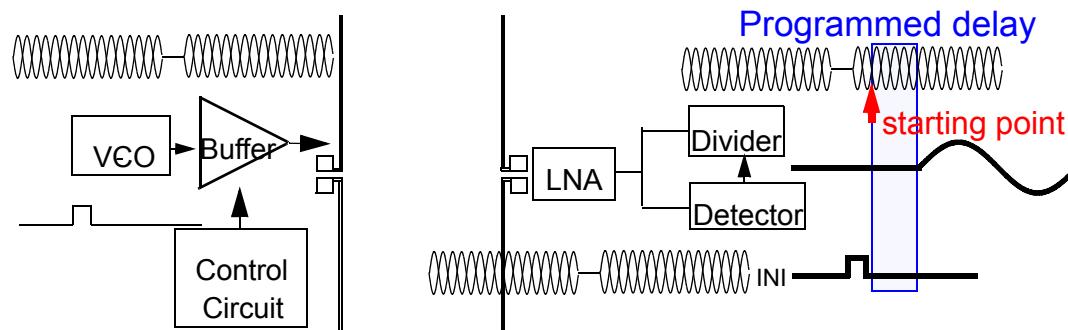


Figure 2-1 The block diagram of a transmitter and a receiver for the intra-chip wireless clock distribution system.

and receivers, the receivers can be placed anywhere on the chip. This provides flexibility for the system design.

The synchronization scheme can be further explained using Figure 2-2. Suppose there are two receivers located at different places of the chip, with different metal structures between the receivers and transmitter. Therefore, the transmitted signal will arrive at the two receivers at different times, which means there exists difference between the time of flight to the receivers. Thus, the two receivers INI signals are also generated at different times, and the two dividers start counting down the programmed delays at different times. However, two different delays for the two receivers can be generated to compensate this time of flight difference. Therefore after the counting down of the programmed delays, the two receivers start dividing at the same time, and the two receivers provide the synchronized clock to the local blocks.

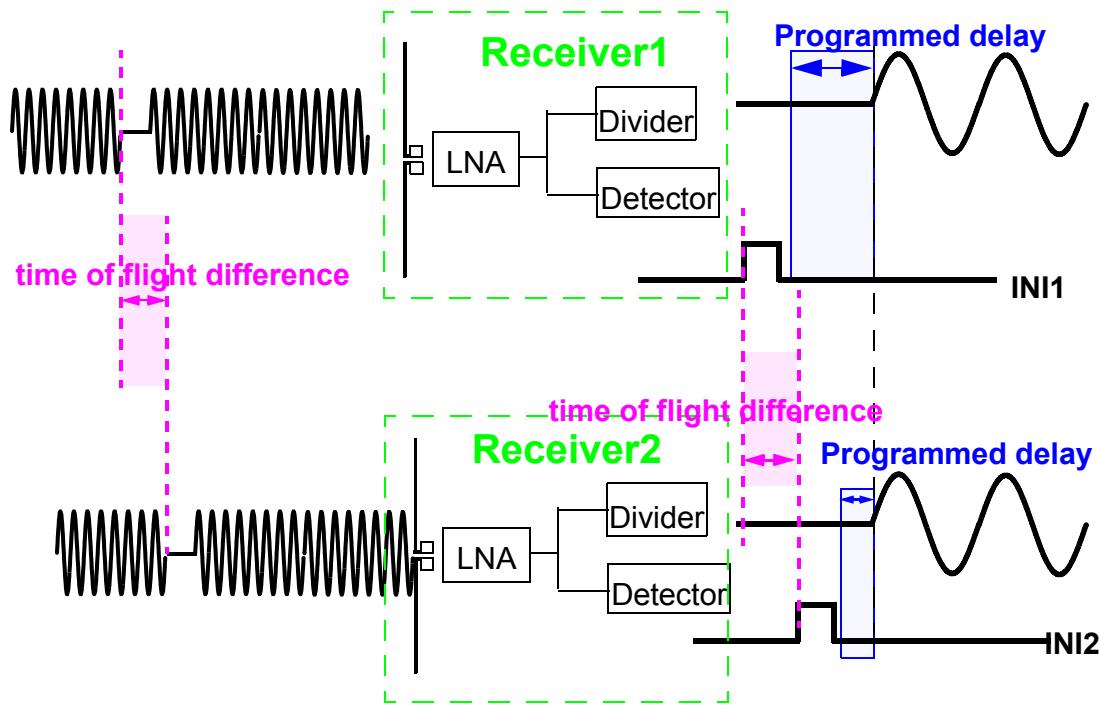


Figure 2-2 The synchronization scheme for two receivers.

The programmable divider [Yan04] is shown in Figure 2-3(a). There are four control bits (P_1, P_2, P_3, P_4) controlling the programmed delay. By switching these four control bits to high (V_{dd}) or low (ground), the divider can have 16 programmed delay values to compensate the static skew from 1/16 to 15/16 of the local clock period. Referring back to the global clock, the maximum static skew this programmable divider can compensate is $\frac{15}{16} \times 8 = 7\frac{1}{2}$ periods of global clock signal. If the global clock signal is propagated in air and there are no metal structures between antenna pairs, the maximum distance difference this divider can compensate for 20-GHz global clock is ~ 110 mm. In silicon, this is ~ 38 mm. This programmable divider can compensate a large distance difference. Accord-

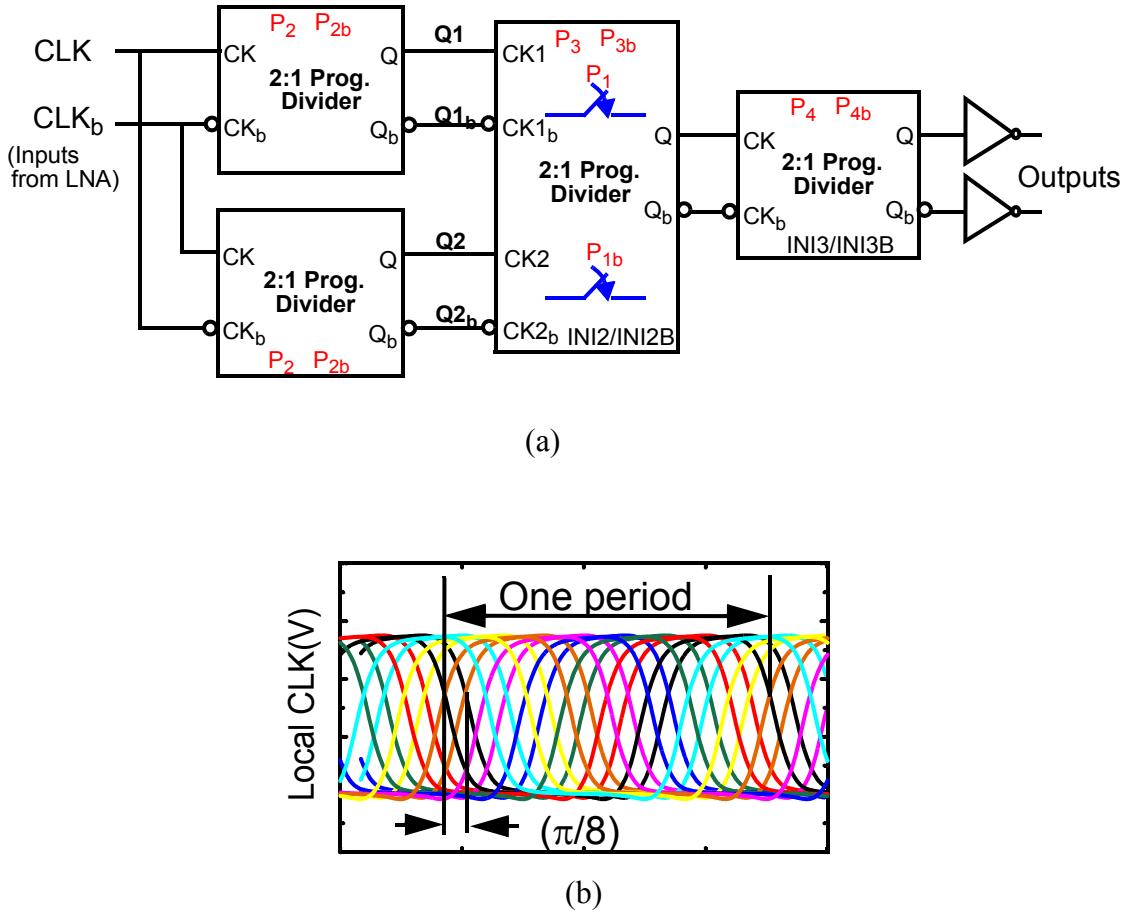


Figure 2-3 Programmable divide-by-8 divider. (a) The block diagram of the divider. (b) The 16 count programming in the divider.

ing to ITRS 2003, the microprocessor size is 17.6 mm by 17.6 mm. The distance from the center of the chip to a corner is \sim 12 mm. Counting in the phase change caused by the metal interference between antenna pairs, this divider should be good enough to compensate the static skew between all the receivers on the 17.6 mm by 17.6 mm chip.

Now, the problem is determining the static skew to different receivers and properly programming the delays. The simulation of the static skews from the transmitter to different receivers though possible in principle would be time consuming. This is particularly so because of the complex metal structures between the transmitter and receivers. To solve this difficulty, a practical correction scheme is proposed. First in the fabrication, all the dividers control bits (P1, P2, P3, P4) are connected to both ground and V_{dd} . By measuring the skews on sufficient samples of fabricated chips, the setting for control bits of the programmable dividers are determined and used to connect the control bits by a one metal mask revision.

2.3 The Bandwidth Consideration of the Wireless Clock Distribution System

The transmitted signal with 2-ns no transmission period has a finite bandwidth. In this system, this signal will pass through the antenna pair and the LNA before it reaches the divider and detector. Will these blocks (antenna pair and LNA) be sufficiently broadband that the 2-ns no transmission period of the signal at the input of detector is properly recognized by the detector to generate the INI signal? This is the issue this section discusses.

2.3.1 The Spectrum of the Transmitted Signal

The signal with a 2-ns no transmission period in time domain is

$$Y(t) = \sin(2\pi ft) \times [1 - u(t - 1 \times 10^{-9}) + u(t + 1 \times 10^{-9})] \quad (2.1)$$

where $u(t)$ is the step function. Figure 2-4(a) shows this signal in time domain. This sharp change from 0 to a sine wave indicates that the signal has a finite bandwidth. In frequency domain, its spectrum is shown in Figure 2-4(b). On the frequency representation, besides the main lobe due to the 20-GHz sine wave, there are also side lobes from 15 GHz to 25

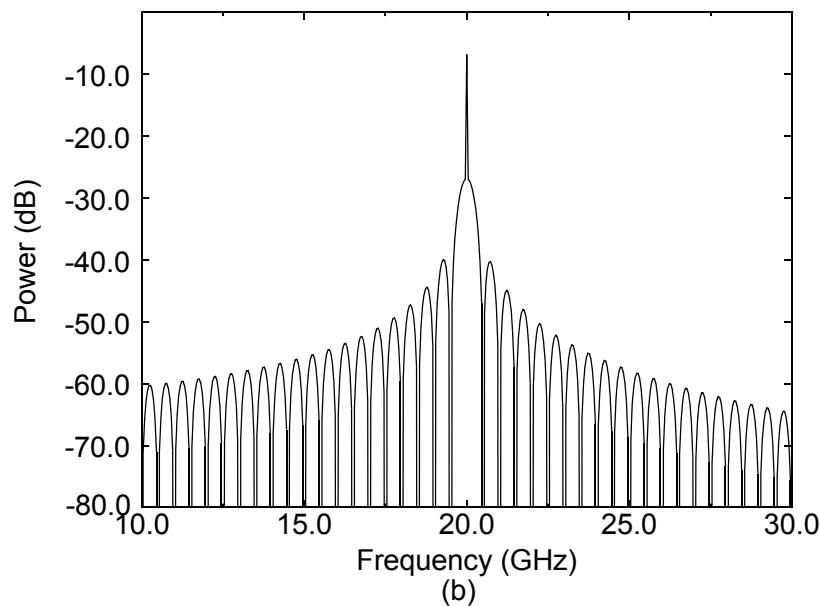
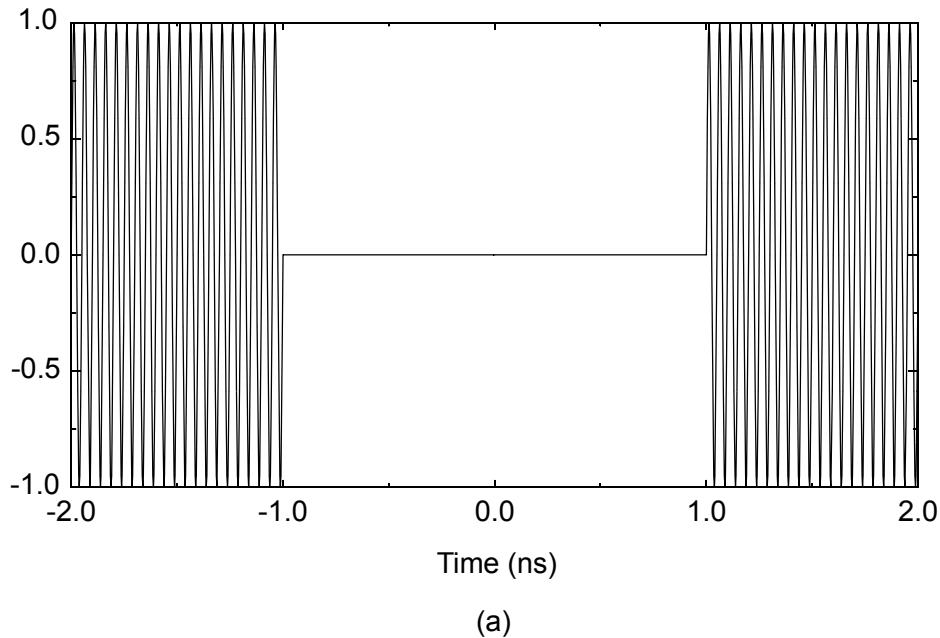


Figure 2-4 The ideal transmitted signal with 2-ns no transmission period. (a) Signal in time domain. (b) Signal in frequency domain.

GHz due to the 2-ns no transmission period. Feeding this broadband signal through a bandpass filter, the output waveforms shown in Figure 2-5 indicate that for 10-GHz bandwidth, the signal shape can be kept. However when the bandwidth of the filter is lowered to 2 GHz, the sharp edge of the transmitted signal can no longer be kept, and it takes several periods of the sine wave to reach the full swing. This time can be defined as the settling time.

Therefore, there is a bandwidth consideration for the system. Even if the transmitter can generate an almost ideal signal with sharp change from no transmission period to

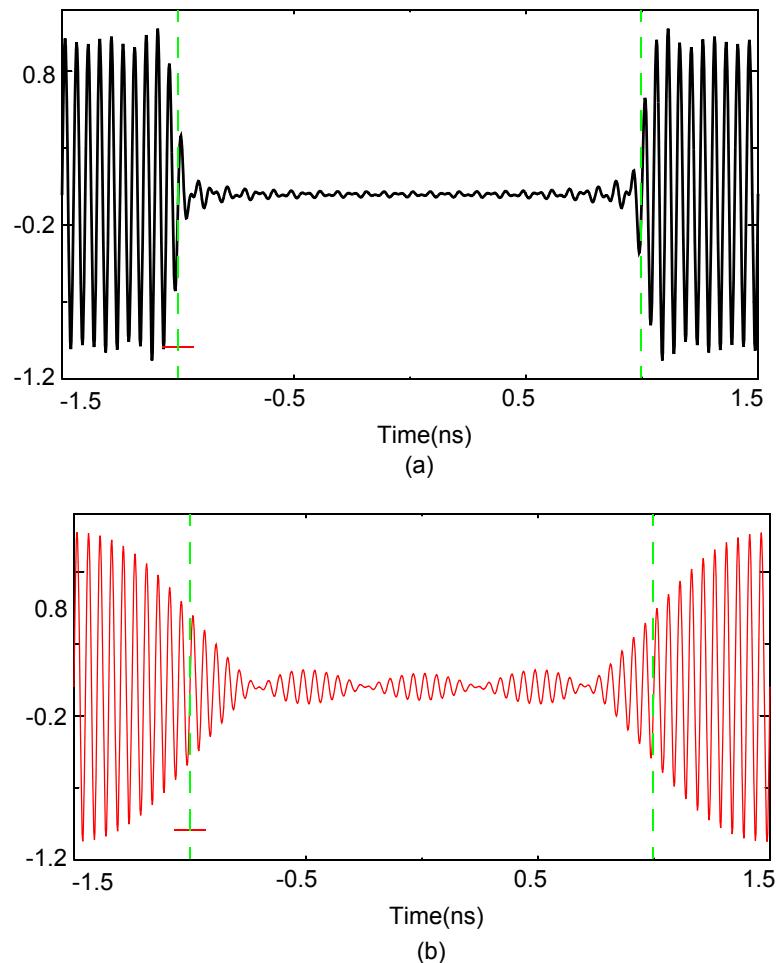


Figure 2-5 The output signal of the ideal transmitted signal from (a) a 10-GHz bandpass filter (15 GHz~25 GHz) and (b) a 2-GHz (19 GHz ~21GHz) bandpass filter.

20 GHz sine wave (reaching the full swing in one period), the signal at the detector input can be distorted by the frequency response of LNA and antenna pair.

2.3.2 The Transmitted Signal at the Output of On-chip Antenna Pair

First the signal through the on-chip antenna pair is considered. Figure 2-6 (a) shows the measured frequency response of a zigzag antenna pair (S_{21}). Figure 2-6 (b) is the simulation result of the ideal signal transmitted through the antenna. It shows that since the antenna pair is a broad band system (10-dB bandwidth around 20 GHz is ~ 11 GHz (from 15 GHz to 26 GHz)), it does not significantly affect the edge of signal. The output signal reaches the full swing after 1 or 2 periods, and the 2-ns no transmission period is preserved at the antenna pair output.

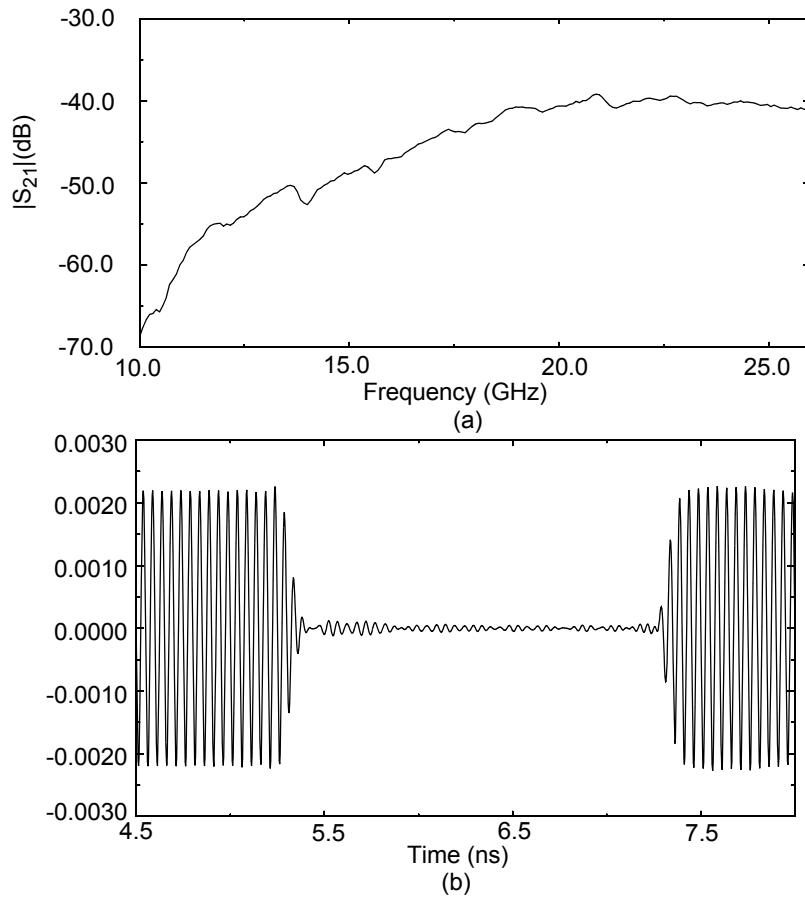


Figure 2-6 The antenna pair (a) $|S_{21}|$ of the antenna pair. (b) The simulated signal at the output of antenna pair.

2.3.3 The Effects of LNA to the Transmitted Signal

Figure 2-7 shows the schematic of a cascode LNA with its output tuned to the C_{load} for the maximum voltage gain. The effects of the LNA on the transmitted signal depends on the 3-dB bandwidth of the LNA gain, which is set by both the Q's of input and output tuning networks. The input of LNA can be simplified as a serial RLC circuit while the output can be simplified as a parallel RLC circuit. The Q-factors of input and output networks are

$$Q = \frac{f_{center}}{3 - dB\ bandwidth} = \begin{cases} \omega L / R & \text{serial RLC} \\ \omega CR & \text{parallel RLC} \end{cases} \quad (2.2)$$

Since the input Q of LNA is always set low (~1.5 or 2) for noise performance, the 3-dB bandwidth is mainly set by the output Q. The gain of this LNA is proportional to the output Q, which is usually high (~10), as well as input Q. Because of high output Q, LNA is narrow band, and it can affect the output signal settling time. From the derivative in

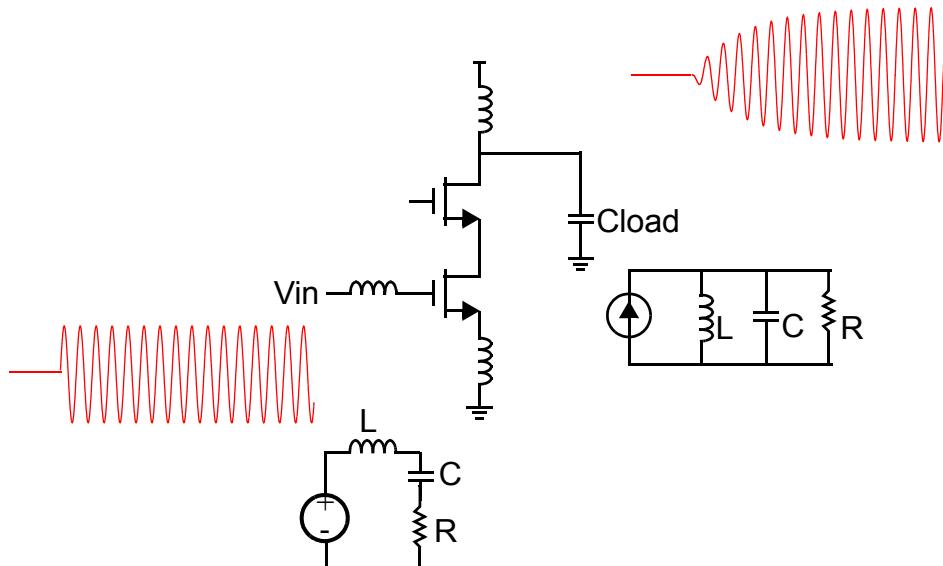


Figure 2-7 The schematic of a cascode low noise amplifier with source degeneration and the simplified input and output.

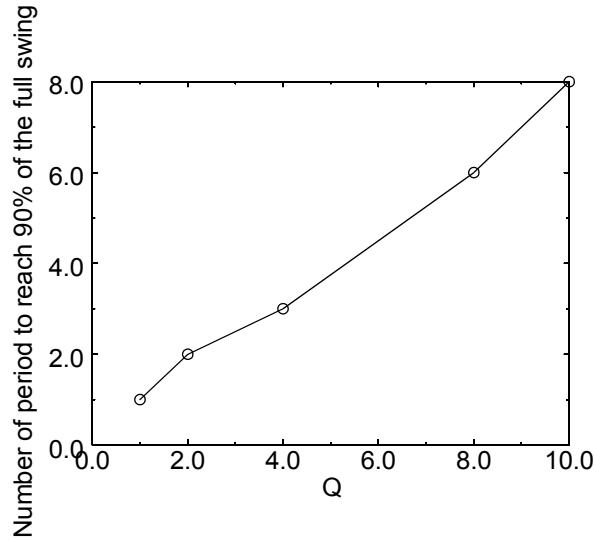


Figure 2-8 The relation between the settling time and Q of a RLC tuned circuit.

Appendix A, the settling time is $\sim 0.8QT$ (T is the period of resonant frequency). Figure 2-8 shows the relationship between the Q and output settling time of a RLC tuned circuit when the input is almost an ideal step. To reduce the settling time, the output Q of the LNA must be low or the LNA must be made broadband. The detailed design of this broadband LNA is discussed in Chapter 4. However, the Q of this LNA is still only ~ 3 , which means that the received signal at the output of LNA still needs two or three periods of settling time to reach the full swing.

2.3.4 Envelop Detector

The two or three periods of settling time for the signal at the input of divider will not affect the divider as long as the detector starts the divider working after the signal has reached the full swing. The problem lies on how to make the detector generate a sharp INI pulse from the input signal with gradual transition.

Figure 2-9 shows the block diagram of detector [Yan04]. Although the input of detector does not have an abrupt edge, the envelop detector can still detect the envelopes.

There are two outputs from the envelop detector (OUT1/OUT2). OUT1 is the low envelop signal generated by the pull-down PMOS transistor (M1, M2), while OUT2 is the high envelop signal generated by the pull-up NMOS transistor (M3, M4). The crossing point is generated by deleting the DC component of these two envelop detector outputs. The signal with crossing point is then amplified by the buffer and goes through the pulse generation circuit to generate the INI signal.

In the correction scheme proposed above, the static skew distribution for a set of samples with sufficient number is generated and this is used to correct skew. Since the detector is detecting the envelop of input signal instead of a particular point on which the signal changes from DC to sine wave, the INI edges can be more susceptible to the process variation. The reason is that the variations of the inductors, transistor and capacitors in LNA and envelop detector will change the envelop of detector input and envelop detector

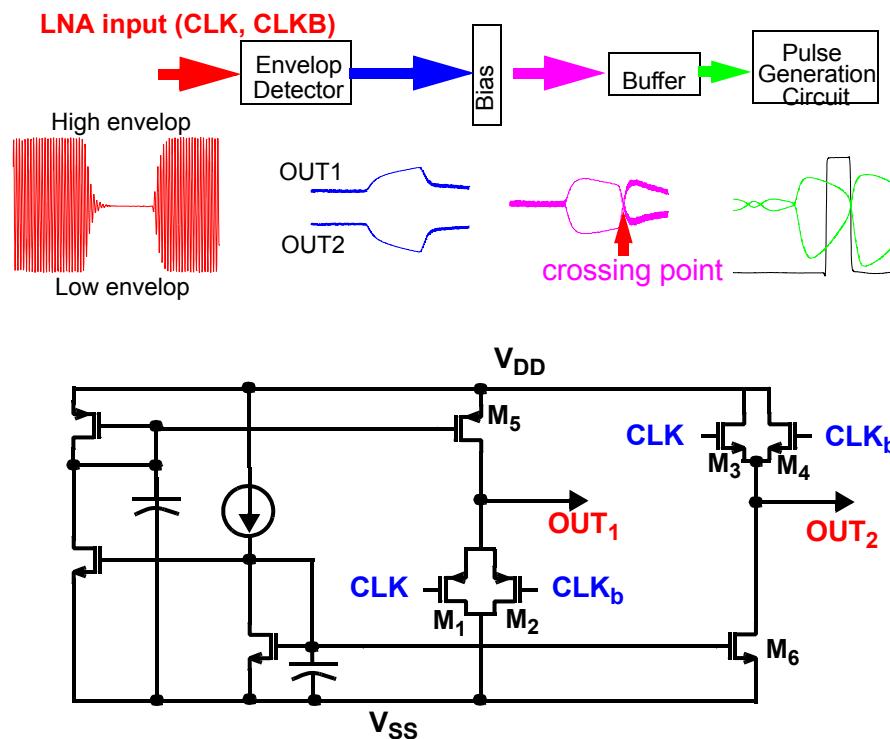


Figure 2-9 The block diagram of a envelope detector.

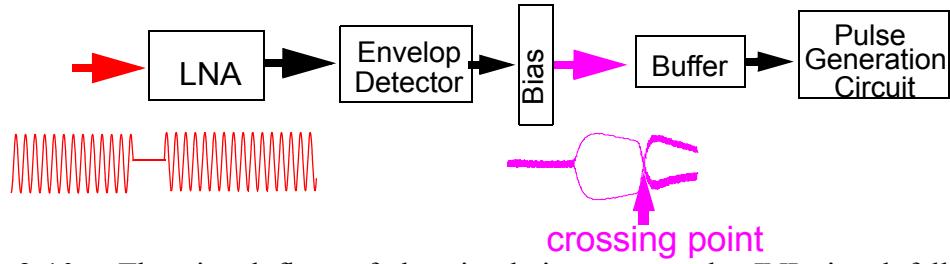


Figure 2-10 The signal flow of the simulation to test the INI signal falling edge variation due to process variation.

output, thus change the crossing point and cause the INI edges of each receiver to vary within a chip as well as chip to chip. As shown in Figure 2-1, if for the receiver at one particular position, the INI falling edge varies by more than one period of the transmitted signal ($\sim 20\text{GHz}$), then the divider may start at different times, losing at least one period of the global clock signal. If the receiver is still corrected by the same programmed value, there still exists an uncorrected static skew [Yan04]. Therefore, the INI signal falling edge variation due to process variation should be characterized to determine whether one set of static skew measurements is sufficient or each chip needs separate static skew measurement for correction. Figure 2-10 shows the signal flow to characterize the INI signal variation under the assumed process variation shown in Table 2-1. From the simulation results, the crossing point variation at the input of buffer is less than 40ps, which is within one period of the global clock signal. Therefore one set of static skew measurements should be adequate.

Table 2-1 The assumed process variation of the simulation

Variation	Crossing point of Buffer Input
Inductor: $\pm 5\%$	40ps (within one period of global clock signal)
Capacitors: $\pm 10\%$	
Transistor: tt, ff, ss	
Temperature: $70^\circ\text{~}90^\circ$	

2.4 Measurement Scheme for the System

2.4.1 Signal Generation to Demonstrate the System

As shown in Figure 2-11, the purpose of this system demonstration is to measure the difference between the starting points of two receivers at different distances to the transmitter (static skew). Also required is to program the two receivers to compensate the static skew and to demonstrate the working of the synchronization scheme.

The first problem addressed is checking the starting point of the receiver on an oscilloscope. The 2-ns no transmission period is a very short time and it only shows up once during synchronization. Therefore, one cannot observe the 2-ns no transmission period and the starting points of the two receivers on an oscilloscope. As a result, the measurement of the static skew of the two receivers is also impossible. The 2-ns no transmission period has to be shown statically on an oscilloscope screen so that the starting points can be observed.

Figure 2-12 shows the method to make the 2-ns no transmission period shown statically on an oscilloscope screen. First, the transmitter is made to repeatedly generate 2-ns

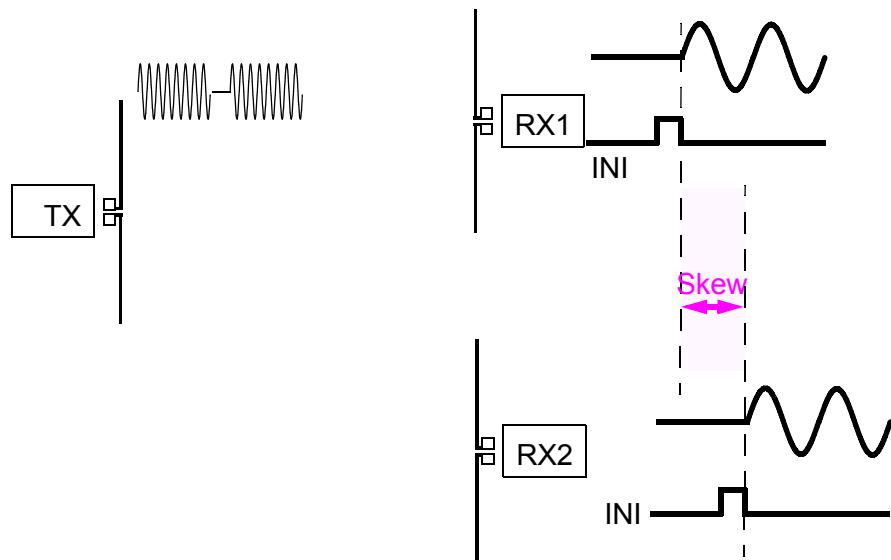


Figure 2-11 The system demonstration scheme.

no clock transmission periods. Then, the divider of receiver starts programming, dividing and stopping periodically as shown in Figure 2-12. Using the control signal generated by the transmitter as the triggering signal to an oscilloscope, the repetitive waveform in the window will appear statically on the oscilloscope. By putting the outputs of two receivers to the oscilloscope channel one and channel two, the static skew can be easily observed on the oscilloscope. Thus, the synchronization by using the divider with programmable delay can be evaluated.

2.4.2 Signal Input and Output Scheme of the Demonstration

To demonstrate the system, one transmitter and two receivers are needed to work concurrently, and the outputs of the two receivers are also needed to be connected to the oscilloscope at the same time. To connect a large number of DC power supplies and to provide the two matched paths for two receiver outputs, a measurement board was designed.

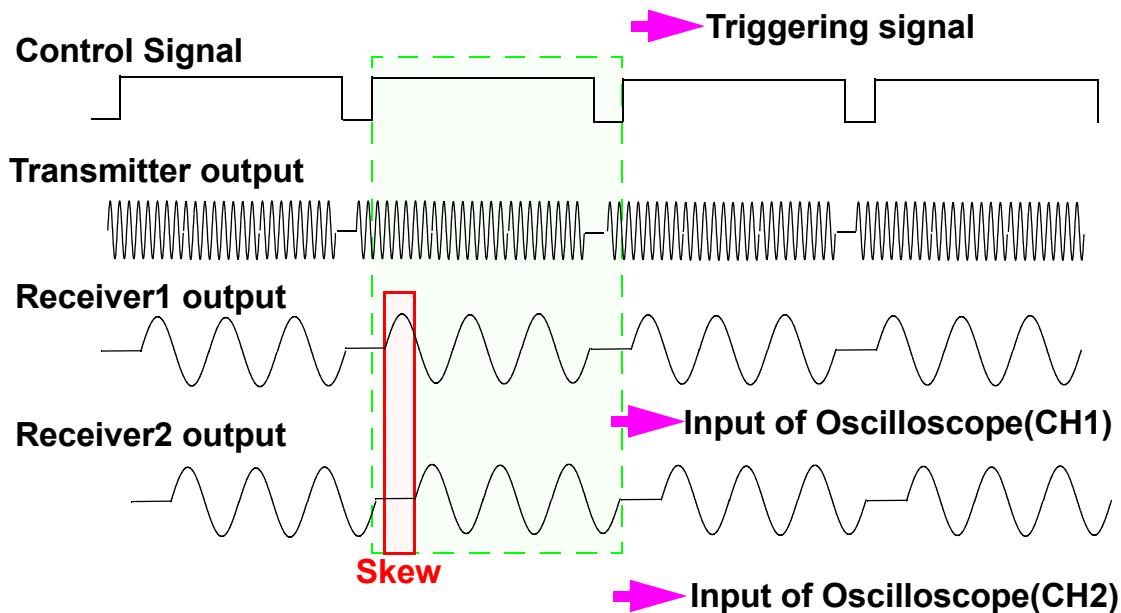


Figure 2-12 The generated signal in the demonstration system.

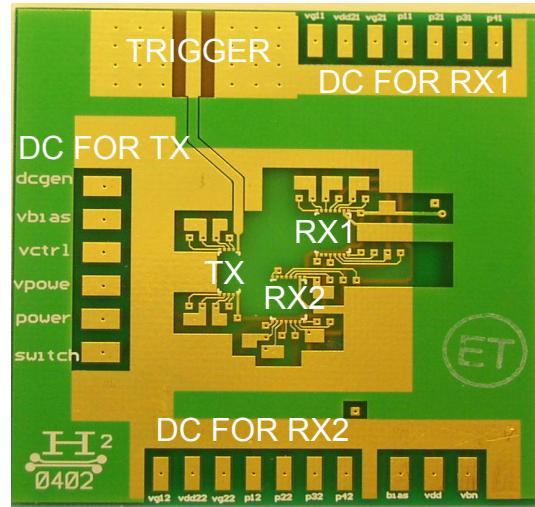


Figure 2-13 The measurement board.

Figure 2-13 shows the photo of a measurement board (the detailed board design process is discussed in Appendix B). Transmitter and two receivers chips are mounted on a board, and the pads on chips are connected to the traces on board using bondwires to provide the DC power supply to the transmitter and two receivers. One method to connect the two outputs of receivers to the oscilloscope (Figure 2-14) is to connect the bondwires to the transmission lines on board and then to SMA connectors, to cables and finally to the oscilloscope. However, the variation of these two paths will add additional delays, which will affect the accuracy of the skew measurements.

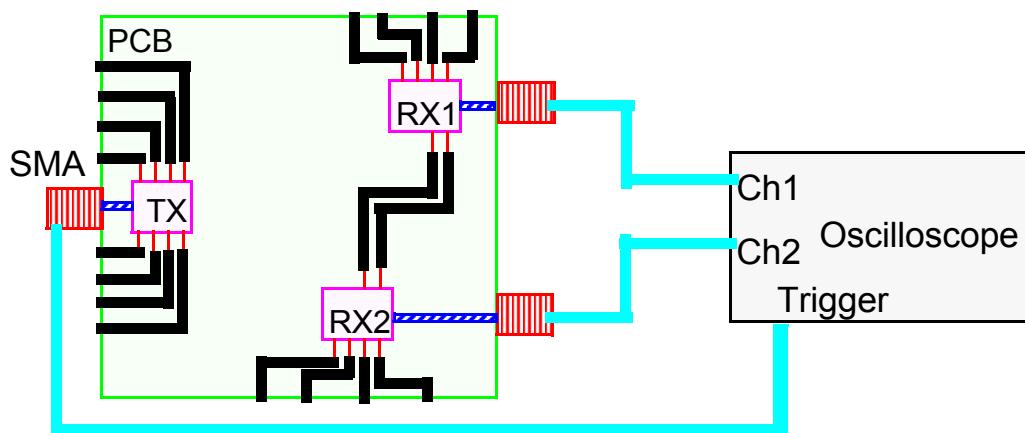


Figure 2-14 One method for connecting the two receivers' outputs to oscilloscope.

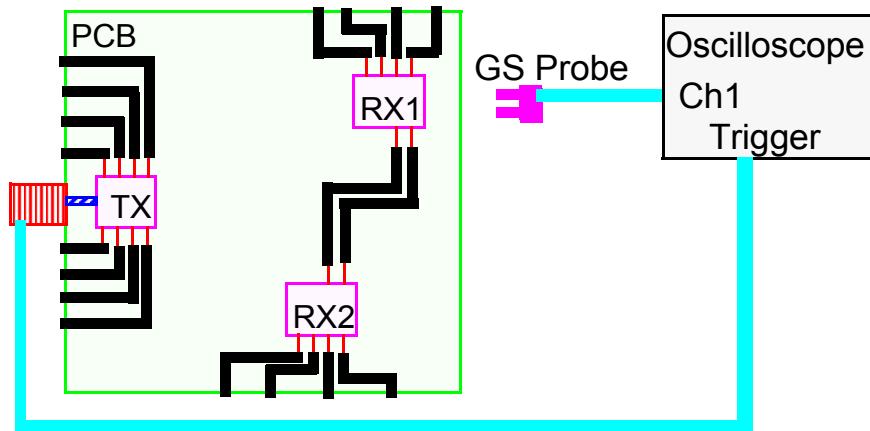


Figure 2-15 The output path for the two receivers with minimum phase difference.

An alternative would be instead of using two paths, only one path (Ground-Signal probe, cable) is used to connect the outputs of receivers to the oscilloscope. First, measure the output of the first receiver and save the waveform in the memory. Then, landing on the other receiver and measuring the other output waveform (Figure 2-15). Comparing the waveform stored in the memory and the waveform shown on the oscilloscope from the second receiver, the skew between two receivers can be estimated.

An obvious question for this technique is how much variations will be introduced in the skew measurement with different probe landing and cable bending? A simple experiment shown in Figure 2-16 is used to estimate this variation. One Ground-Signal (GS)

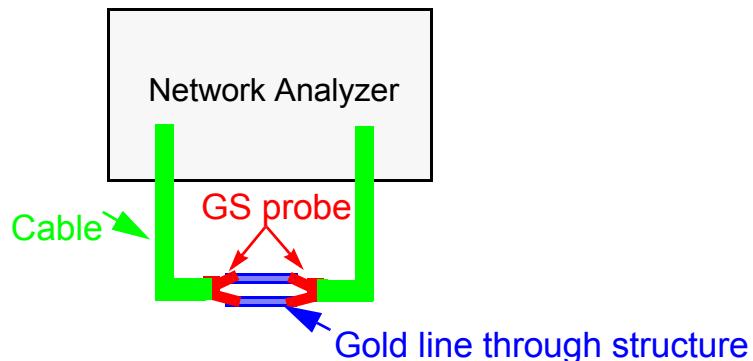


Figure 2-16 The measurement setup to test the added skew by different land of the GS probe and cable bending.

probe connected to port 1 of network analyzer is landed on one end of a through structure on a calibration substrate. The other GS probe is connected to the port 2 of network analyzer and landed on the other end of the through structure. The GS probe on port 2 is landed on the same position of the through structure several times and the bending of the cable was changed. The phases of S_{21} for different probe landing and cable bending vary only 3 degree at 24 GHz, which is <1% of a period at 24 GHz. The phase difference will of course be even less when the signal is divided down by 8. These indicate that the proposed skew measurement method should be acceptable.

2.5 Summary

In this chapter, a synchronization scheme for the wireless clock distribution system is proposed. Its feasibility and the requirements for different blocks of the system to implement this scheme are also discussed. Finally, a measurement scheme for the evaluation of the system is developed.

CHAPTER 3

ANTENNA PERFORMANCE IN THE PRESENCE OF INTERFERING STRUCTURES

3.1 Introduction

In the intra-chip wireless clock distribution system, the power transmission gain of the antenna pair between a transmitting antenna and a receiving antenna is a key factor determining the feasibility and performance of the system. Since the on-chip antennas are fabricated on lossy silicon substrates, the on-chip antenna efficiency is much lower compared to that of the off-chip antennas. In addition, as shown in Figure 3-1, the on-chip antenna will be affected by the metal structures around it, such as solder balls for packaging, a heatsink, and data lines and power grid across the chip. Research on how these metal structures affect the on-chip antenna characteristics and how to reduce their impact are discussed in this chapter.

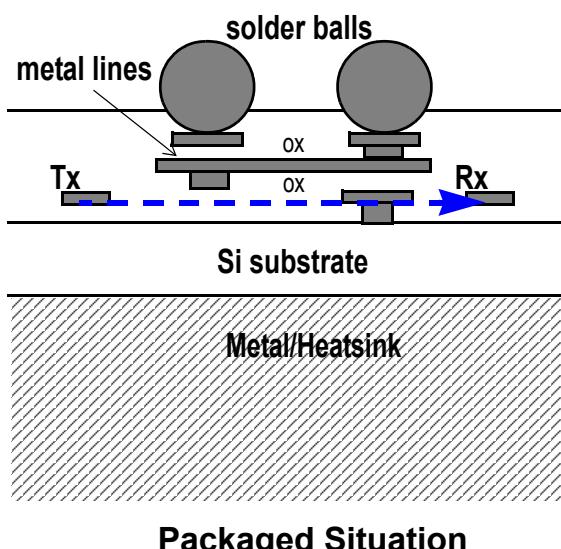


Figure 3-1 Wireless interconnection inside a ball-grid array package.

3.2 Antenna and Heatsink in Package

3.2.1 Introduction

For modern microprocessors, the power dissipation can be as high as 150W. A heatsink is essential to remove the heat from a chip. Without it, the performance and life time of chips will be severely degraded. For the typical ball-grid array package used in microprocessor (Figure 3-1), the heatsink is just below the chip. Therefore a large conductive metal plane is placed close to the on-chip antenna and this metal plane can severely degrade the on-chip antenna characteristics. In the previous works, an 1.0-cm thick wood block or a 1-mm glass layer is inserted between the wafer containing the integrated antennas and the metal chuck of a probe station to improve the antenna gain [Kim98], [Kim99]. However, this measurement condition is incompatible with the packaging technology for microprocessors. Therefore, providing an efficient means for heat removal while not degrading on-chip antenna power transmission gain is one of the key requirements for this system.

This section describes the impact of inserting an Aluminum Nitride (AlN) substrate, a dielectric with high thermal conductivity (150W/m-K, the same as Si and 100 times that of glass) between the wafer and metal chuck. This increases the antenna pair gain, while efficiently removing heat.

3.2.2 Measurement Setup and Propagation Model

To evaluate the impact of a propagating layer underneath a silicon wafer on the performance of integrated antennas, linear dipole antennas (Figure 3-2) were fabricated using a single metal (Al) level process on top of a 2- μm silicon dioxide layer on 20- $\Omega\text{-cm}$

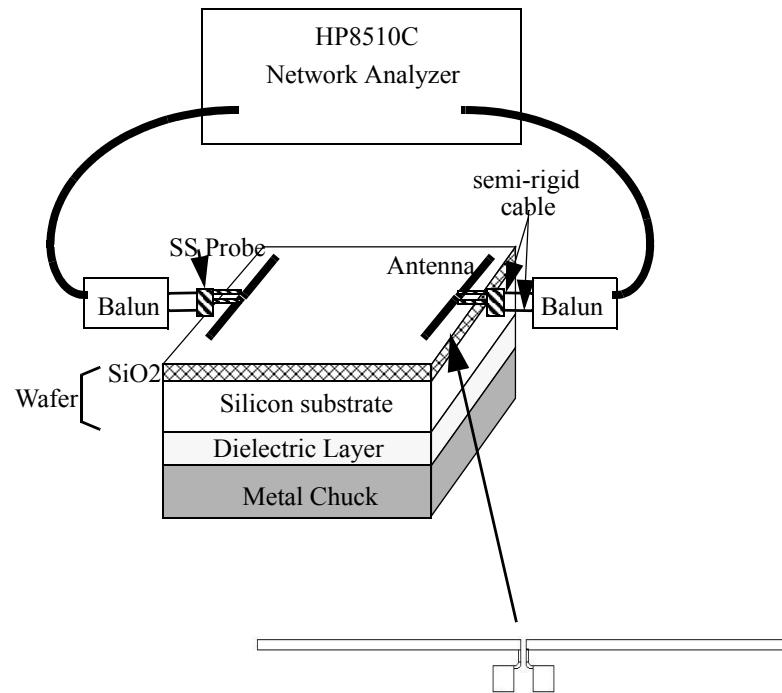


Figure 3-2 The measurement setup for the on-chip antenna pair measurement and the layout of an on-chip antenna.

or 5- Ω -cm silicon substrates. The antennas are 2 mm long, and the thickness and width of the metal lines are 2 μm and 10 μm , respectively.

The measurement setup is shown in Figure 3-2. This setup includes an HP network analyzer, baluns, semi-rigid cables and signal-signal probes [Kim98, Kim99]. Baluns are

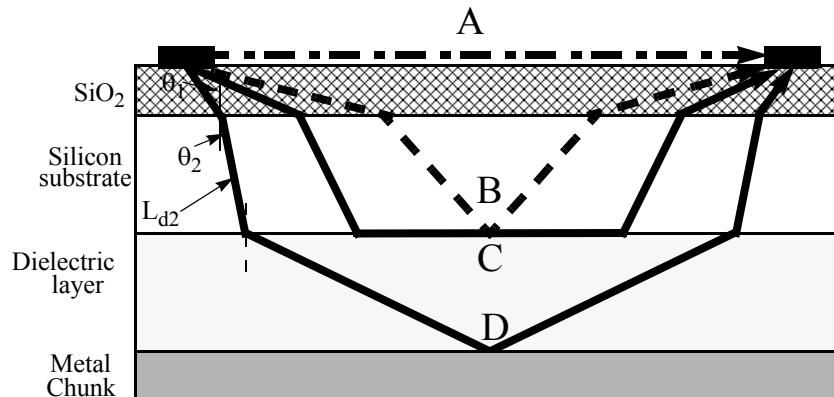


Figure 3-3 A plane wave model.

used to convert the singled-ended signal to differential signal and vice versa. The wafer is separated from the metal chuck of probe station using a dielectric propagation medium. In an actual packaged IC, the metal chuck represents the metal base of a lead frame or heat-sink. The power transmission relation between a receiving and a transmitting antenna is represented by Friis' transmission formula [Bal82].

$$\frac{P_R}{P_T} = |S_{21}|^2 = \left(1 - |\Gamma_t|^2\right) \left(1 - |\Gamma_r|^2\right) \left[\frac{G_t G_r \lambda^2}{(4\pi R)^2} \right] \quad (3.1)$$

In this equation, the first two terms represent the mismatch loss at the receiving and transmitting antennas, and the last term represents the actual transmission gain (G_a), which can be extracted from measurements using [Kim98]

$$G_a = \frac{|S_{21}|^2}{\left(1 - |S_{11}|^2\right)\left(1 - |S_{22}|^2\right)} \quad (3.2)$$

To further understand the characteristics of integrated antenna pair in a silicon substrate with a dielectric propagation layer between the wafer and metal chuck, a plane wave propagating model [Kim01] [Li02] has been developed and shown in Figure 3-3. In this simplified model, there are four propagation paths. Path A represents the direct path. Path B is the wave that goes through the lossy silicon substrate and is reflected back at the Si/dielectric layer boundary. Path C is the lateral wave propagating on the dielectric layer side of the silicon/dielectric layer boundary. Path D is the wave going through the dielectric layer and reflected back by the metal chuck. Among all these four paths, path B is negligible because of the lossy substrate. Since there is a 2-μm thick silicon dioxide layer between the antenna and silicon wafer, if the permittivity of the propagation layer is equal

to or larger than silicon dioxide, there is no total reflection at the silicon/dielectric layer boundary, and thus there is no lateral wave on the dielectric layer (Path C) [Li02]. In this case, only path A and path D dominate.

3.2.3 Measurement Results for Antenna Pair on Dielectric Layer

To verify the possibility of using AlN to increase the antenna pair gain, the power transmission gain (G_a) was compared for the case when the metal chuck is in direct contact with a wafer to when a dielectric layer is inserted between the chuck and wafer. The dielectric layers were a 0.76-mm AlN layer, an 1-mm glass layer and an 1-cm thick wood block (Figure 3-4). The G_a 's were measured using linear dipole pairs separated by 5 mm on a 20- Ω -cm substrate. The results show that G_a 's for the AlN and glass cases are almost the same, and they are ~ 8 dB higher than the case without a dielectric propagating layer. This gain increase can be explained by the propagation model mentioned above. When the wafer is in direct contact with metal, paths A and B exist. The signal in path B is so small

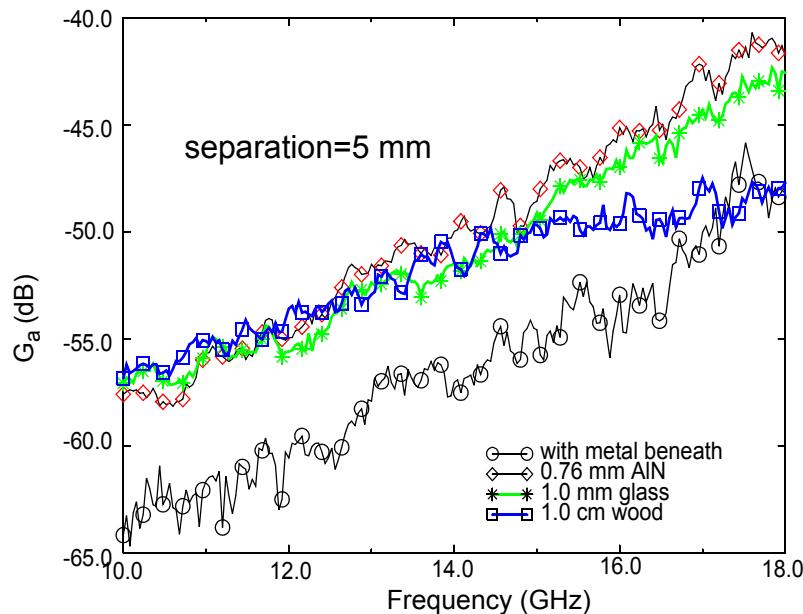


Figure 3-4 G_a vs. frequency when the propagating medium is a 0.76-mm AlN layer, a 1.0 mm glass layer, or a 1.0 cm wood.

that it can be neglected. By inserting the dielectric propagation layer between the wafer and metal, paths C and D are included. Since the permittivities of glass and AlN are equal or larger than that of the silicon dioxide (AlN: 8.8, glass and SiO₂: 3.9), path C, the lateral wave path, cannot exist. So only path D is added when a glass or an AlN layer is inserted. This result indicates that it is possible to replace the glass layer using an AlN layer to achieve a gain increase and to improve heat removal.

Figure 3-5 shows that when the layer thickness of AlN increases, the gain no longer increases monotonically. When the thickness is increased, dips are seen and the frequency at which the dips occur decrease as the AlN layer thickness increases. These dips significantly degrade the antenna gain at certain frequencies. For instance, the gain drops by 10 dB at 14 GHz for the 3.8-mm AlN case and drops by 20 dB at 11 GHz for the 5.32-mm AlN case. The dips are due to the destructive interference between waves traveling through different paths, path A and D. When the phase difference between signals traveling on Paths A and D is $n\pi$ ($n=\pm 1, \pm 3, \dots$), the waves will cancel and result in the

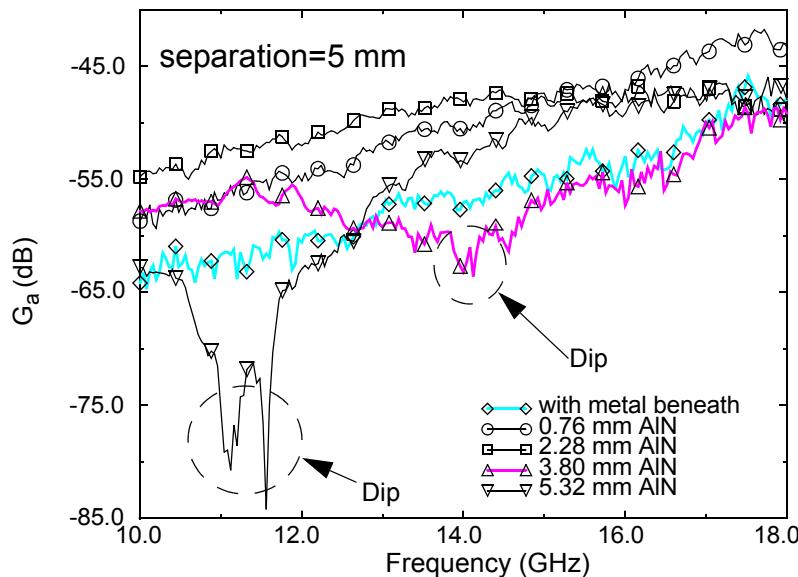


Figure 3-5 G_a vs. frequency when the AlN layer thickness is varied.

gain drop. As the thickness of AlN increases, θ_2 in Figure 3-3 becomes smaller, and the wave traveling length in lossy silicon substrate L_{d2} is also shorter. Then the power transmission through path D increases which results in an increase in the gain far away from the dip frequency.

The phase delay between the receiving and transmitting antennas extracted from S_{21} are shown in Figure 3-6. The slopes of phase plots are proportional to $l_{\text{eff}}/C_{\text{eff}}$, where l_{eff} and C_{eff} are the effective path length and speed of light. As the thickness of the AlN layer is increased, the length of path D is increased. In addition, because there are more signal transmission through the higher permittivity medium, the effective speed of light is decreased. These two changes in turn increase the slope of the phase plots in Figure 3-5. The sharp changes in the phase plots are due to the dip in the gain plots. At these dip frequencies, the waves from two paths are canceling each other, so the phases near the dip frequencies are noisier and dramatically change. With the increase of the slope, the phase

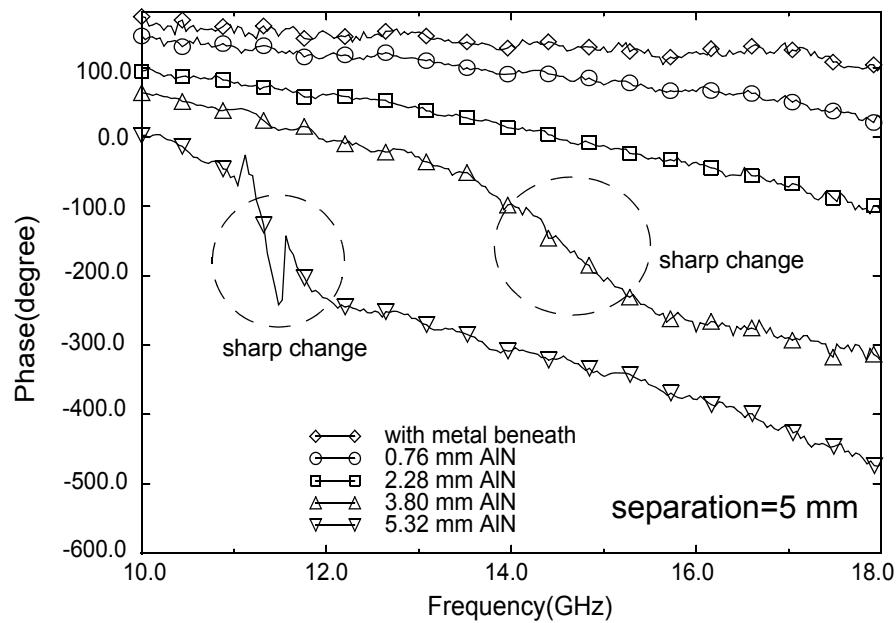


Figure 3-6 Phase of S_{21} vs. frequency when the AlN layer thickness is varied.

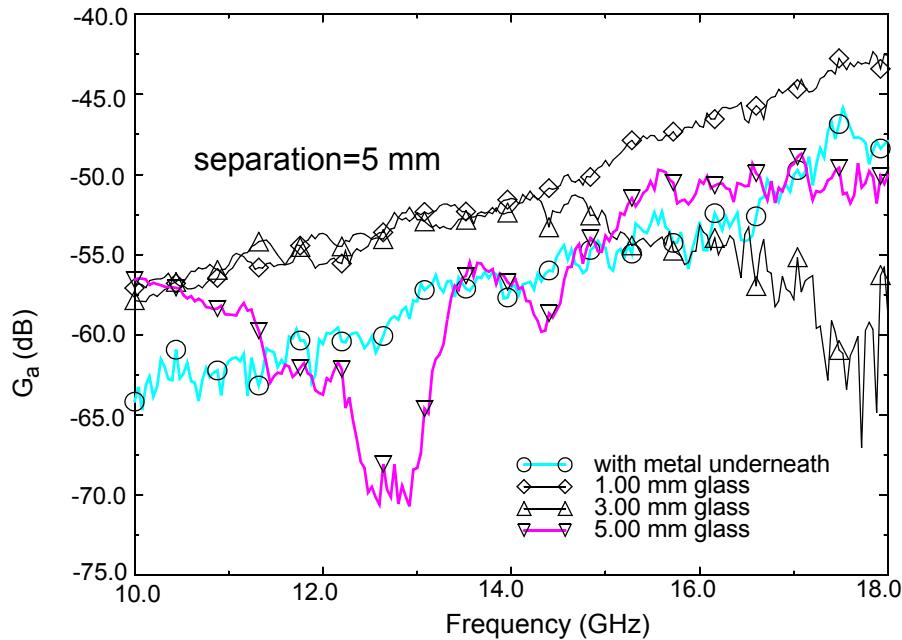


Figure 3-7 G_a vs. frequency when the glass layer thickness is varied.

changes faster with frequency, and the gap between dip frequency becomes smaller [Li02]. As can be seen from the gain plots in Figure 3-4, between 10 and 18 GHz, there is no dip for the 0.76-mm and 2.28-mm thick AlN cases. However, there is a dip frequency for the 3.8-mm and 5.32-mm AlN cases. These show that the thicker the AlN layer, it is more likely that a dip will exist in the frequency band of interest.

Therefore, there exists a trade off. With a thicker AlN layer, the loss of path D in lossy silicon substrate will be reduced and increase gain when the phases of signals traveling in paths A and D are almost the same. However the dip frequencies will occur more frequently and the gain at the dip frequencies will be low. With a thinner AlN layer, the loss in substrate will be higher, the gain increase will be moderate, but the dip frequencies do not occur so frequently and even at the dip frequencies, the gain may still be acceptable. So from the view of system robustness, thinner AlN is preferred. Also, thinner AlN means less thermal resistance, which is better for heat removal.

Shown in Figure 3-7 is the G_a of the antenna when the propagating medium is glass. When the glass layer thickness varies from 0 to 5 mm, G_a almost has the same characteristic as with the AlN. Only the frequencies at which the dips occur are different. This is due to the fact that the permittivity and thickness of the dielectric layers are different. This result proves that for a dielectric layer with permittivity larger than silicon dioxide, the dips in gain at certain frequencies is a common problem. This measurement result also provides the experimental support for the propagation model.

Figure 3-8 shows the gain of an antenna pair on a 0.76-mm thick AlN propagation layer separated by 5, 7.5, 10 and 20 mm. In the plots, for the 5, 7.5, and 10-mm separations, no dips associated with the interference effects are seen. For the 20-mm separation, the gain is too low and the plot is too noisy to determine whether the dips are present. This shows that an AlN layer with thickness less than or equal to 0.76 mm is preferred for the system. It can increase the gain around 8 dB compared to the case without a propagating

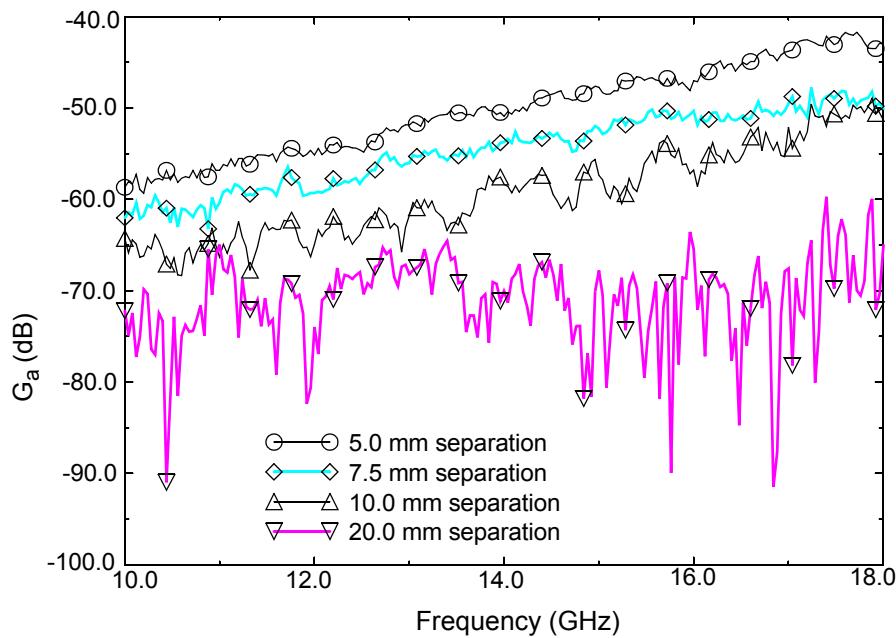


Figure 3-8 G_a vs frequency with different antenna separation on 0.76 mm AlN.

layer, and there is no destructive dip frequency in the measurement frequency range for 5 to 10 mm separations.

The measurements discussed above are for the antennas fabricated on a 20- Ω -cm silicon substrate. Figure 3-9 compares G_a 's measured on a 5- Ω -cm substrate to that on a 20- Ω -cm substrate when the AlN layer thickness is 0.76 mm. The gain of antennas fabricated on a 20- Ω -cm substrate is \sim 8 dB higher at 15 GHz, while that for the antennas on a 5- Ω -cm substrate is only around 2 dB. A plausible explanation for this is that the signal transmission in Path D has been attenuated by the lower resistivity. For the propagating layer to be effective for increasing the antenna pair gain, the substrate resistivity should be greater than 5- Ω -cm.

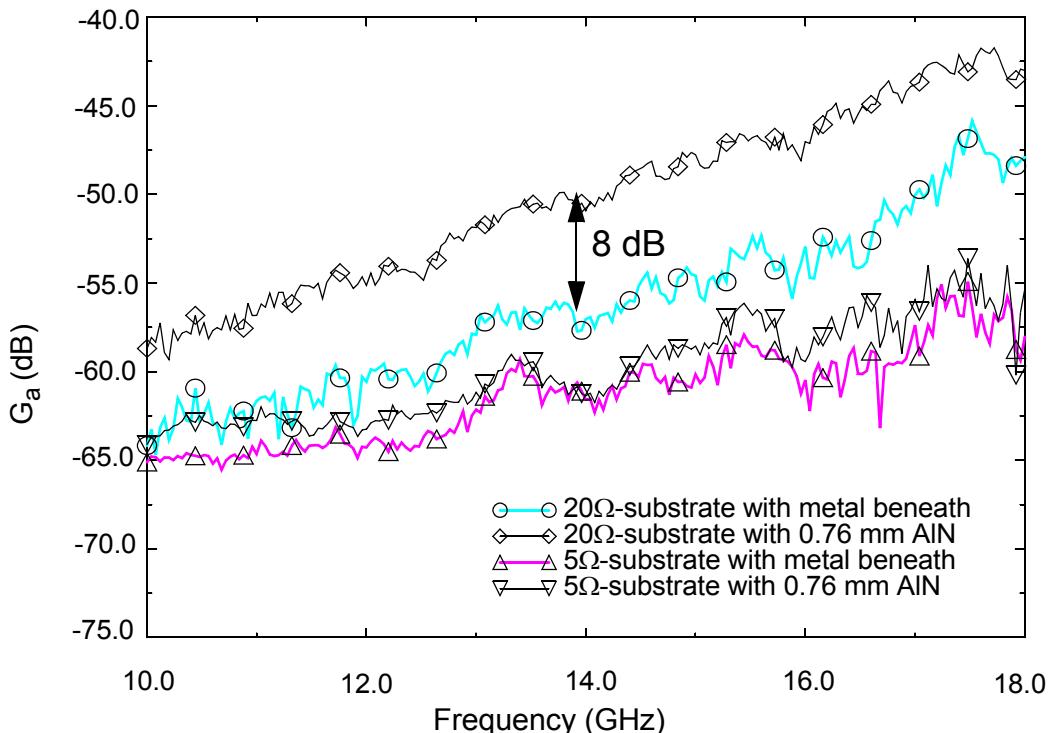


Figure 3-9 G_a vs. frequency for antenna pairs fabricated on 5- Ω -cm and 20- Ω -cm substrates when the AlN layer is 0.76 mm thick.

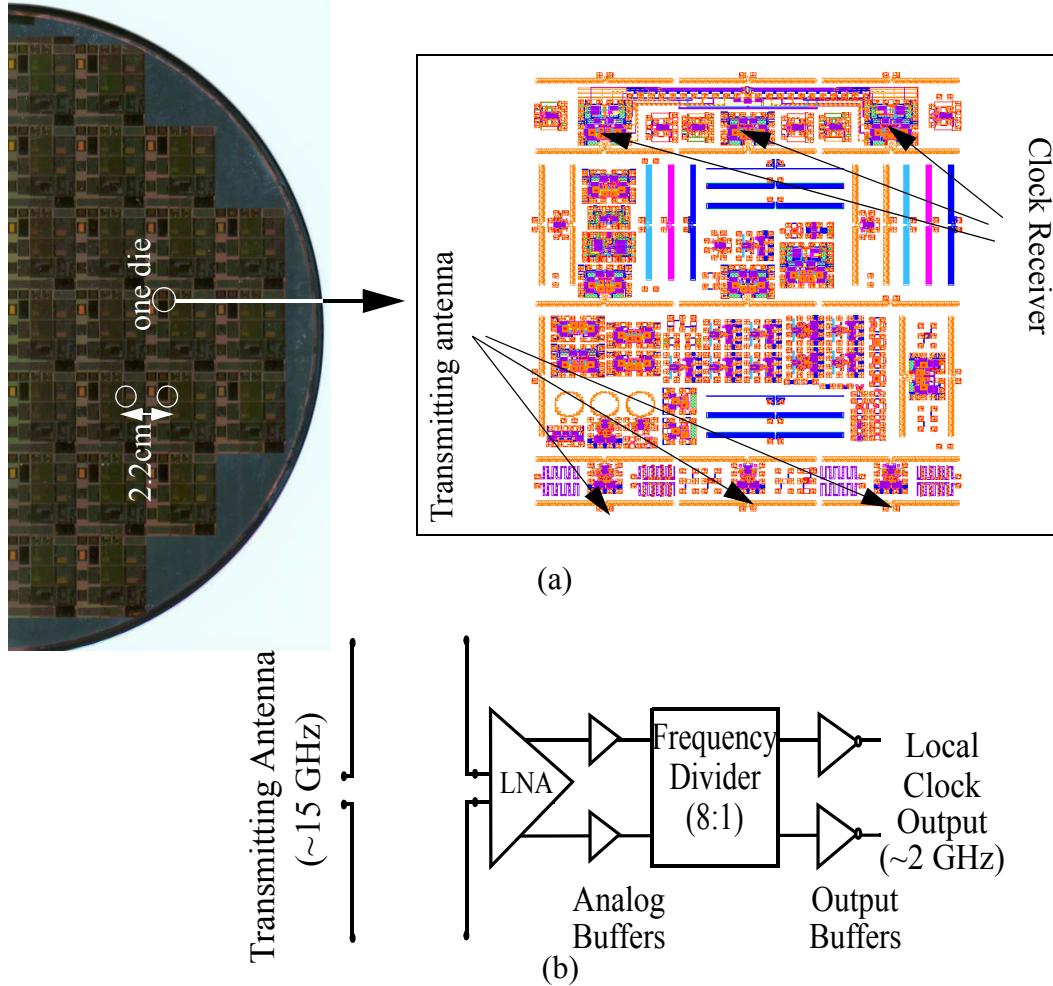


Figure 3-10 Clock distribution system. (a) Half wafer with multiple dies, and the 2.2cm measuring condition with transmitting antenna on one die and the receiver on the other die; also the layout of $7 \times 6\text{mm}^2$ test chip containing zigzag dipole antennas and clock receivers (b) Block diagram of the clock distribution system.

3.2.4 Measurement Results of the Receiver

To further demonstrate the benefits of including an AlN layer in a wireless interconnection system, signal transmission between an on-chip transmitting antenna and a clock receiver [Flo01] was characterized on top of the different propagating layers. The receiver shown in Figure 3-10 is implemented in a 0.18- μm process with 1- μm thick copper for the top two metal layers. The resistivity of the substrate is 20- $\Omega\text{-cm}$. The receiver is designed to pick up a 14~16 GHz signal from the transmitting antenna and divide this fre-

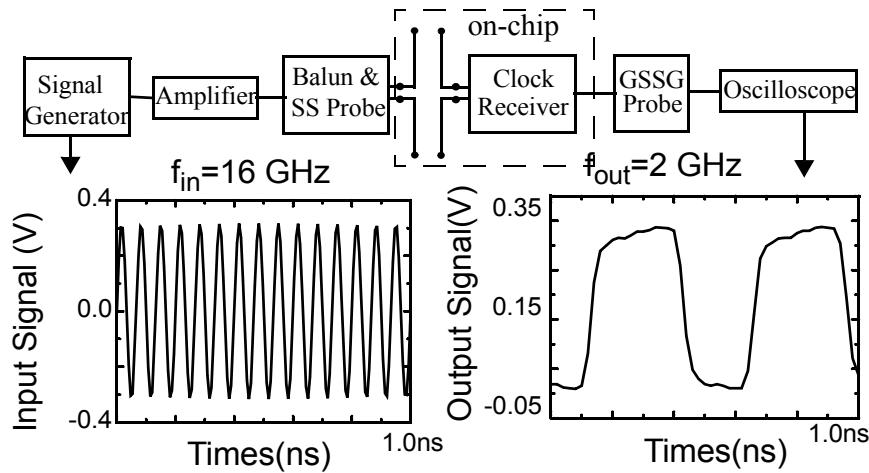


Figure 3-11 Measurement setup and input/output wave-form for clock receiver across 5.6 mm distance.

frequency to provide a local clock signal (Figure 3-11). The sensitivity is defined as the minimum power feeding into the transmitting antenna that can sustain the operation of local clock. The sensitivity depends on both the antenna pair gain and receiver gain, both of which are frequency dependent. Keeping the receiver gain the same, Figure 3-12 shows

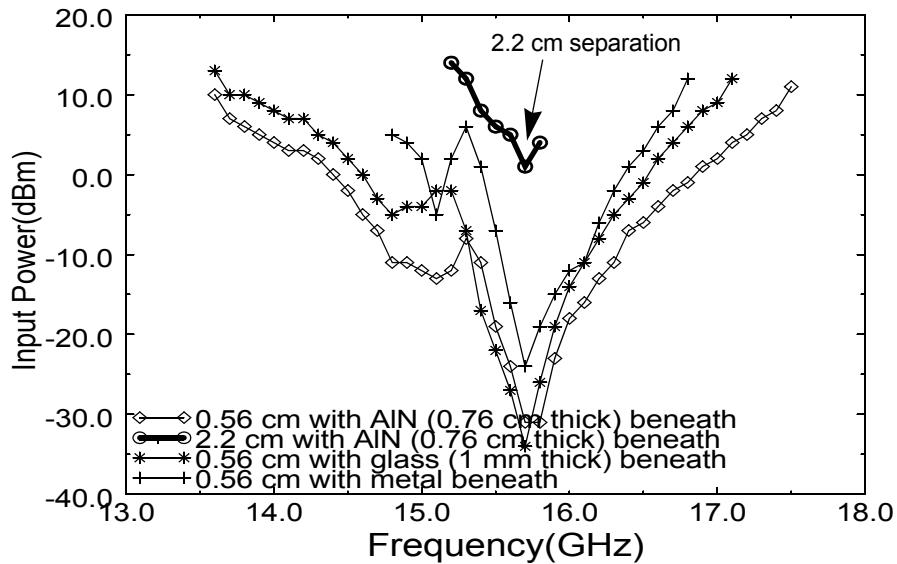


Figure 3-12 Measurement of sensitivity vs. frequency with different propagating media and different separations between antennas

the sensitivity when the receiver is placed on different propagation layers with varying separations between the antenna and receiver. The measurements show that the receiver on AlN has comparable performance to when it is on glass. Having an AlN layer above the metal chuck widens the operating frequency range and increases the sensitivity. A wider range makes the system more robust to process variations.

Also shown in Figure 3-12 for the first time is the wireless connection that works at a distance of 2.2 cm. This 2.2-cm separation is achieved by using a transmitting antenna on one die and the receiver of another die on the same wafer shown in Figure 3-10 (a). This distance is 3 times the previously reported separation and larger than that needed for clock distribution in a chip with the maximum die size projected by ITRS.

3.2.5 Conclusion

Based on the plane wave propagation model and measurement results, an AlN layer inserted between a wafer containing integrated antennas and metal chuck simultaneously improves gain and heat removal in the wireless clock distribution system. In order to alleviate the gain degradation near the dip frequencies, the optimum thickness of the dielectric propagating layer to satisfy both the gain improvement and system robustness requirement is explored. A wireless interconnect including a transmitting antenna and a receiver is used to demonstrate the feasibility of using 0.76-mm AlN layer. The 2.2-cm working distance between the transmitting antenna and receiver with the AlN layer beneath shows the possibility of the wireless system working in a chip with the maximum die size projected by ITRS.

3.3 On-chip Metal Interference Structures

3.3.1 Introduction

A serious concern for the on-chip antennas is that the on-chip metal structures, such as bus lines or power lines near an antenna, can act as interference structures and significantly affect the on-chip antenna characteristics, such as the gain, phase, and input matching (S_{11}). Understanding the effects of metal structures on antennas and developing design guidelines to reduce the impact of the structures to antenna gain and S_{11} are essential for demonstrating the wireless clock distribution system. A test chip with various metal interference structures is fabricated using a three metal layer process and based on evaluation of the structures, a set of design guidelines has been developed, and presented

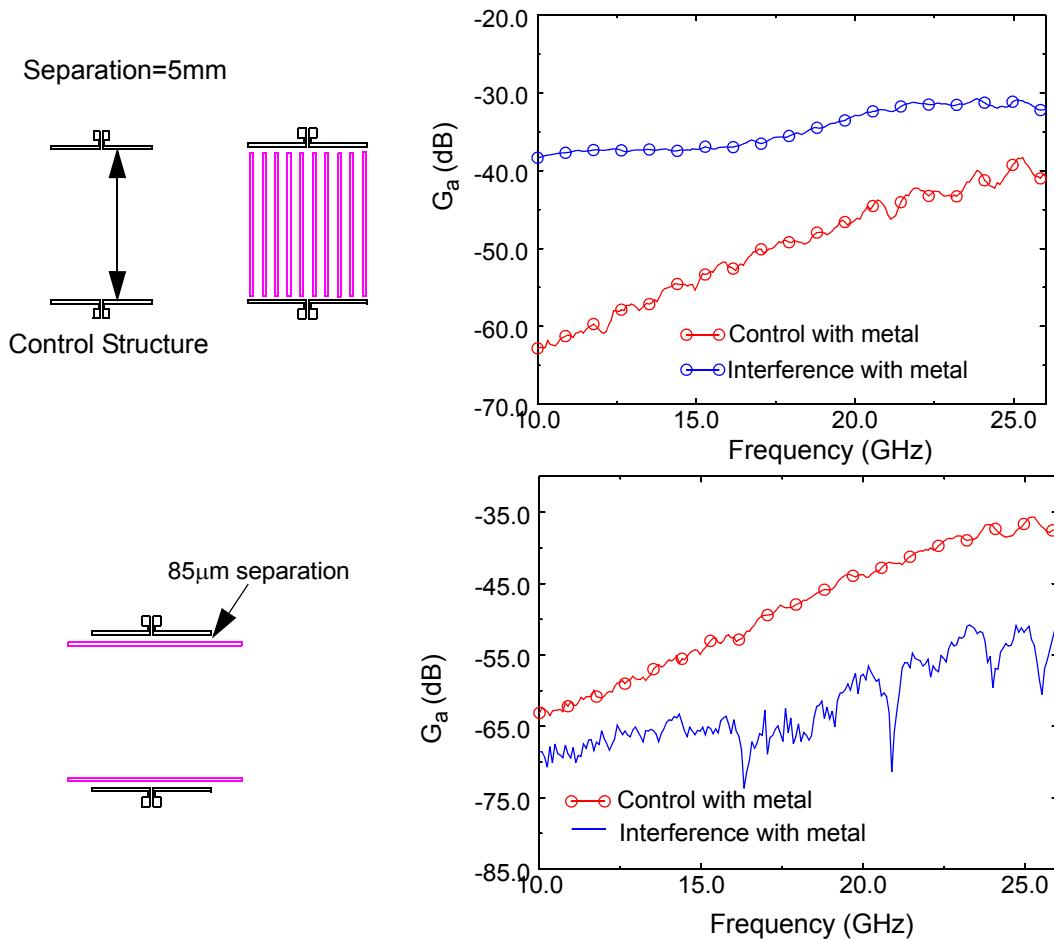


Figure 3-13 Layout of the two former interference structures.

in this section. Additionally, the impact of interference structures in the presence of AlN propagation layer is investigated and described in this section.

3.3.2 Interference Test Structures

An initial study using a single metal layer process [Har02] has shown that having parallel metal lines between an antenna pair dramatically decreases antenna power transmission gain (G_a) defined in Equation 3-2. On the other hand, perpendicular metal lines increase the antenna gain (Figure 3-13). In this section, a more comprehensive set of metal interference structures near antennas is studied. The structures were fabricated on 20- Ω -cm silicon substrates. The thickness of metal layers is 1.5 μm , and the thickness of

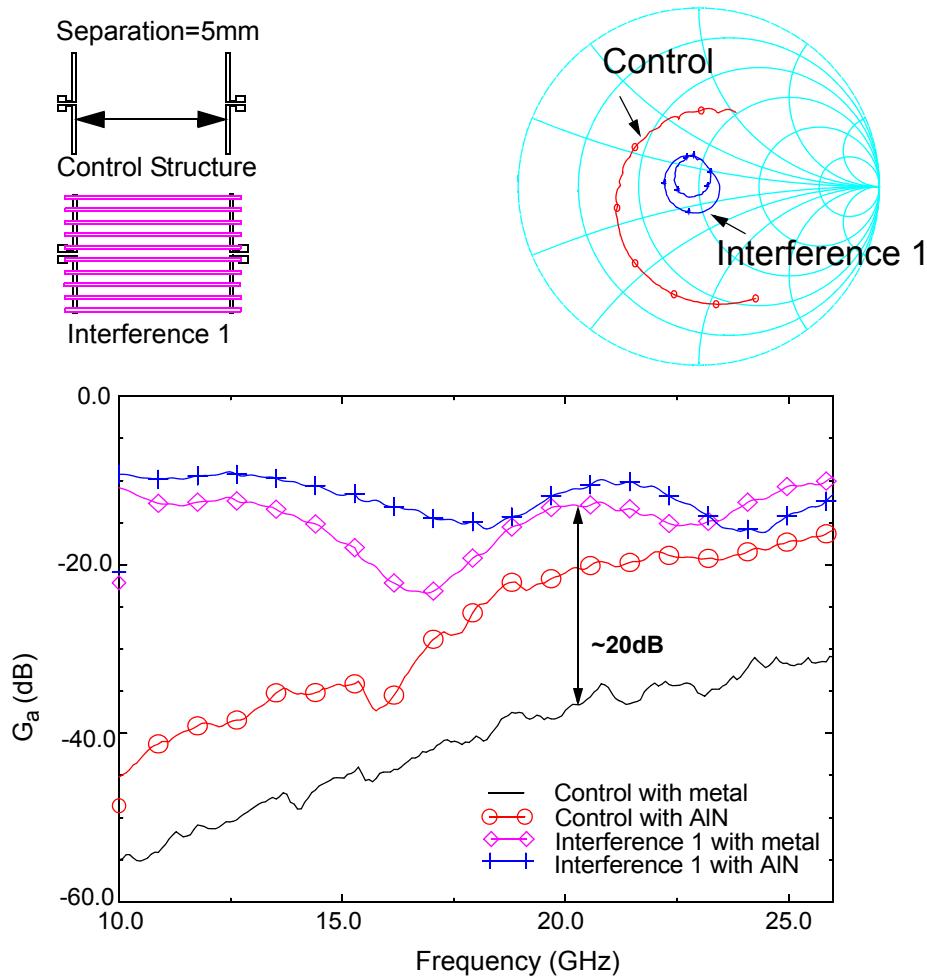


Figure 3-14 The S_{11} and antenna transmission gain of interference structure 1.

SiO_2 layers separating two adjacent metal layers is 1 μm . For consistency, all the antenna pairs are formed with 2-mm zigzag antennas formed with metal-1 layer separated by 5 mm. The antenna pair with no metal interference structures in between is used as the control structure, and adding a \sim 0.7-mm AlN layer increases the antenna pair gain by \sim 8 dB. Metal interference structures are fabricated using metal 1, 2, or 3 layers, and are placed on top or between antenna pairs. The structures were characterized from 10 to 26 GHz.

A set of perpendicular metal lines running over an antenna pair is shown in Figure 3-14. S_{11} dramatically changes. S_{11} spins around in the smith chart like that for a transmission line. The gain (G_a) increases \sim 20 dB at 20 GHz, and the gain no longer increases monotonically like that for the control structure. The gain and S_{11} behaviors suggest that

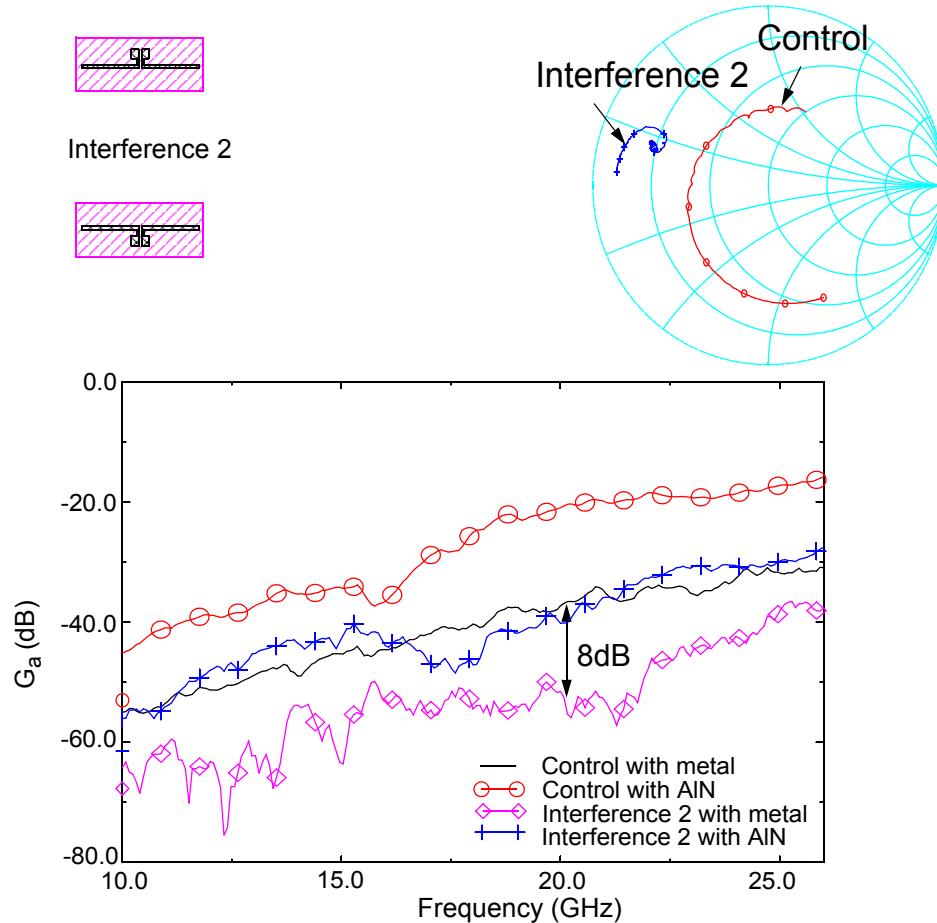


Figure 3-15 The S_{11} and antenna transmission gain of interference structure 2.

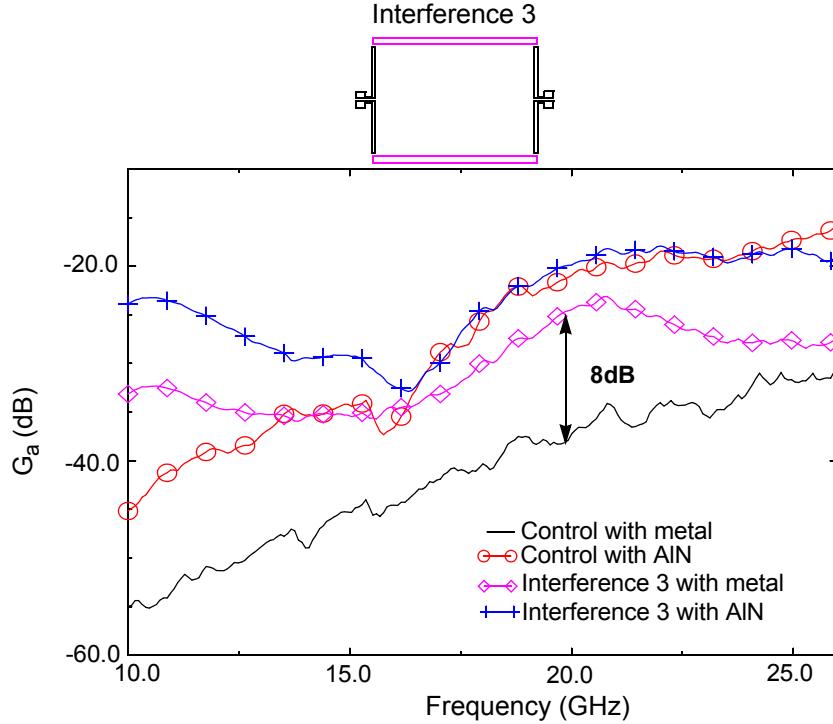


Figure 3-16 The antenna transmission gain of interference structure 3.

the metal lines running over the antenna pair are acting like a transmission line. When an AlN layer is added, the gain only slightly increases. This slight increase in gain is most likely due to the fact that the power transmission through Path A shown in Figure 3-3 dominates. When a block of metal is put on top of antenna (Figure 3-15), S_{11} once again significantly changes, and the gain drops ~ 8 dB at 20 GHz. Like for the control structure, adding an AlN layer increases this antenna pair gain by ~ 8 dB. The dramatic changes of S_{11} for these two interference structures will de-tune the input matching network for a clock receiver, therefore structures like these should be avoided.

The metal lines perpendicular to an antenna pair at the top and bottom of the antennas increase gain by ~ 8 dB at 20 GHz (Figure 3-16). The gain does not increase monotonically with frequency, which is similar to that with Interference structure 1 shown in Figure 3-14 and suggests that the two metal lines are acting like a transmission line. AlN

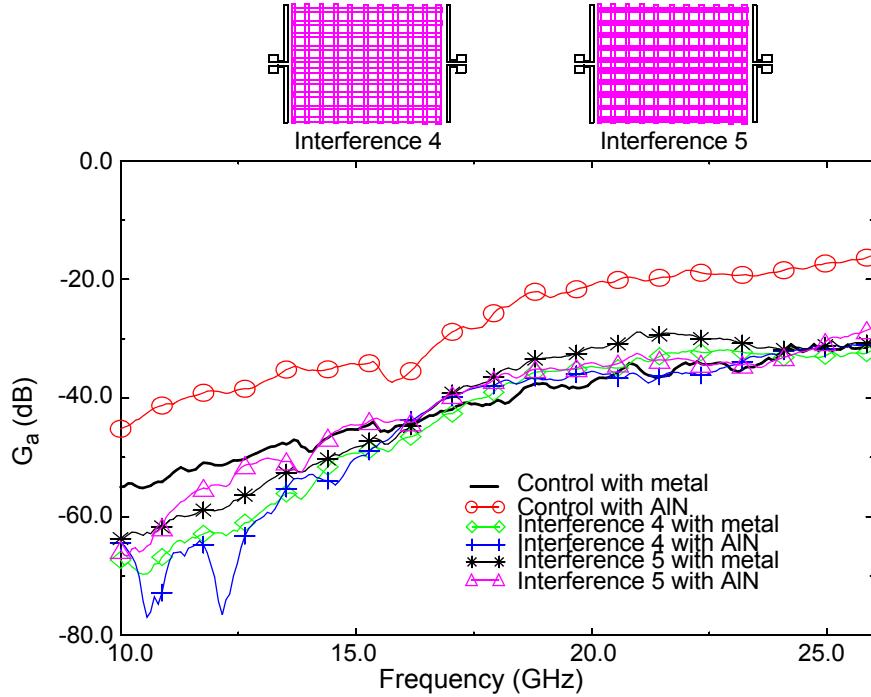


Figure 3-17 The antenna transmission gain of interference structures 4 and 5.

improves antenna gain ~ 5 dB. When a grid of metal lines representing power or ground lines in an integrated circuit is inserted between an antenna pair (all in metal 2 (Interference 4) or parallel lines in metal 2 and perpendicular lines in metal 3 (Interference 5) shown in Figure 3-17), the gains do not change significantly from that of the control structure. However, inserting an AlN layer does not increase the antenna gain. For all these structures, S_{11} measurements are not changed, which maybe due to the fact that the metal lines are $100 \mu\text{m}$ away from the antennas.

When short metal lines ($350\mu\text{m}$) run above an antenna (Figure 3-18), the gain and S_{11} of the antenna change minimally. Inserting a dummy pattern used in advanced metallization processes [Liu99] in between an antenna pair (Figure 3-19) also does not significantly affect the gain and S_{11} . These small changes indicate that discontinuous metal structures are preferable near antennas. Adding an AlN layer increases the antenna gain ~ 8 dB, like that for the control structure.

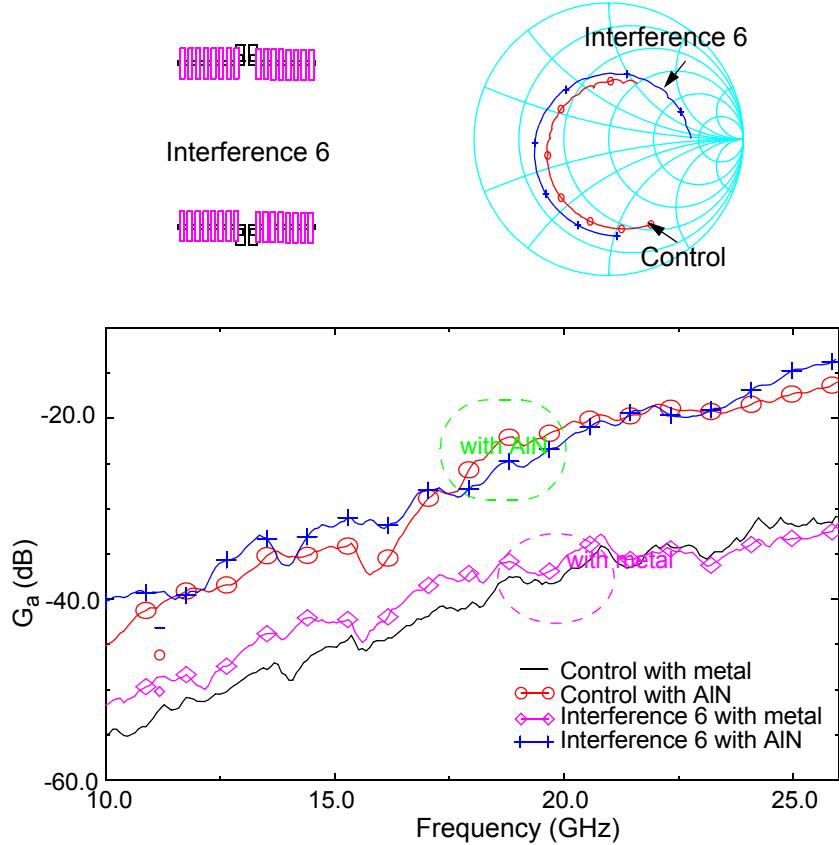


Figure 3-18 The S_{11} and antenna transmission gain of interference structure 6

Except Interference structures 6 (short metal lines) and 7 (dummy pattern), all other interference structures significantly change the phase delay between the receiving and transmitting antennas extracted from S_{21} compared to that for the control structure (Figure 3-20). Particularly, Interference structure 2 has a large impact. As will be discussed, presence of this interference structure and others with large impacts should be excluded by design guidelines. Because of these changes of the phase delay, even though the distances of the receiving antennas and the transmitting antenna are the same, the phases of the received clock signal will vary. This variation of the received signal phase will introduce clock static skews in the system. To avoid the phase changes by excluding all these structures is area consuming and impractical. To use simulation tools in predict-

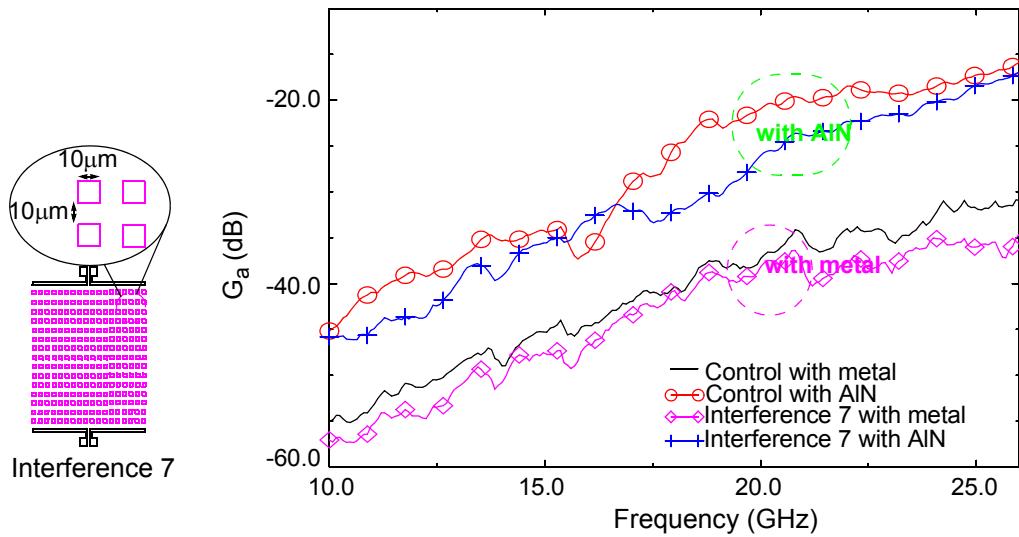


Figure 3-19 The layout and antenna transmission gain of interference structure 7.

ing the phase changes in the real layouts would be desirable but difficult. As mentioned in Chapter 2, a more practical way to correct these static skews is to measure the skew and correct using the programmable divider in combination with one metal mask revision.

3.3.3 Design Guidelines

Based on the above measurement results, inserting an AlN layer generally improves antenna gain even with interference structures. Assuming that the phase change

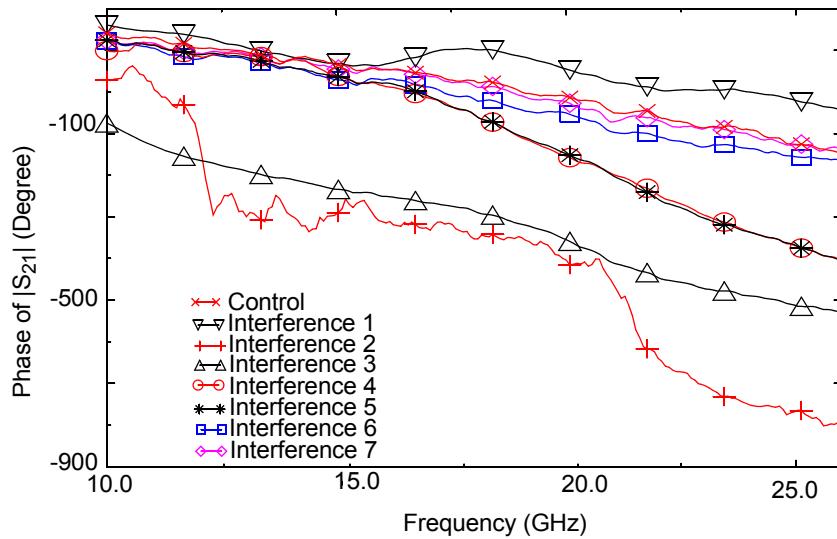


Figure 3-20 Phase of the received signal of all interference structures.

problem will be solved, a set of design guidelines is established to reduce the impact of the interference structures on antenna pair gain and S_{11} .

1) Metal structures directly on top of antennas should be avoided since they will change S_{11} , and thus de-tune the input matching network. However, short perpendicular metal lines are acceptable.

2) Long perpendicular lines between or beside an antenna pair not running over antennas are acceptable.

3) Long parallel lines and big metal blocks close to antenna should be avoided.

However short discontinuous metal lines are tolerable.

4) Metal grids, one metal layer parallel lines and the other layer perpendicular lines, or all at the same layer, are acceptable assuming the separation to the antennas are greater than $100\mu\text{m}$.

5) Discontinuous metal blocks ($10 \mu\text{m} \times 10 \mu\text{m}$) between antenna pairs are acceptable.

These design guidelines are qualitative in nature and more experiments and simulations are needed to develop more specific and quantitative rules.

3.4 Substrate Backlapping for On-chip Antenna

3.4.1 Introduction

Compared to off-chip antennas, the low G_a 's of integrated antennas on commonly utilized silicon substrates are due to the loss caused by the conductive substrate, which degrades the efficiency of on-chip antenna and adds path loss [Kim00]. Increasing silicon resistivity has been shown to be effective for improving antenna characteristics [Cha01], [Ras02]. These methods however involve use of more costly substrates or non-standard

processing steps. In this section, another possibility, thinning the lossy substrate to lower the substrate loss and thus, increasing the gain between antenna pairs, is discussed.

3.4.2 Measurement Results

The antennas used for this work are 2-mm zigzag dipoles with 60° bend angle fabricated on 20- Ω -cm silicon substrates with a 3 μm oxide layer. The metal thickness and width are 1.5 μm and 10 μm . The separations between antenna pairs are 0.5 cm, 1 cm and 2 cm.

Figure 3-21 shows G_a for antenna pairs with a 5-mm separation, when the wafers are on varying propagation media [Guo02] (Figure 3-2). When the wafer is in direct contact with the metal chuck, the antenna pair on the thin substrate has \sim 15-dB lower gain than that on the thick substrate. The thicknesses of thin and thick substrates are 100 and 600 μm , respectively. This gain decreases because the closer ground plane to the antenna for the thinner substrate case more severely degrades the efficiency of antenna. For the thick wafer case, G_a is the maximum, when one layer of AlN (0.76 mm) is placed between

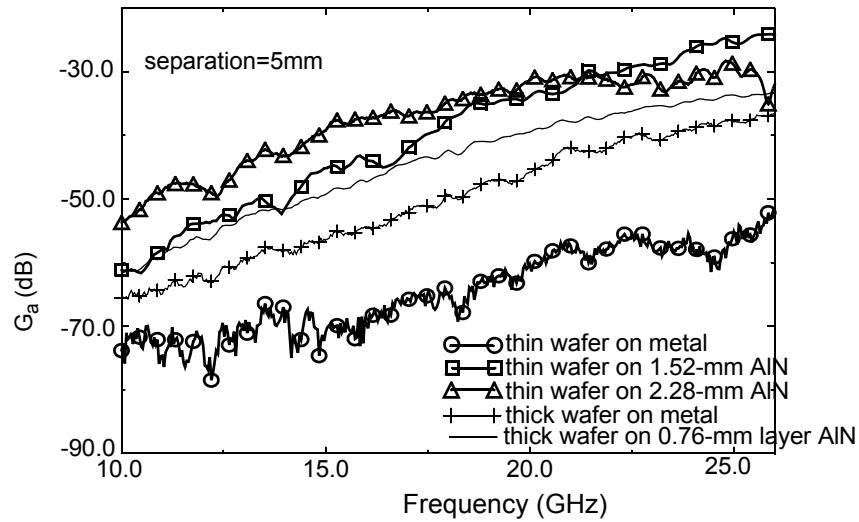


Figure 3-21 Antenna pair transmission gain for thin and thick wafers with different dielectric propagation layers underneath.

wafer and the metal chuck [Guo02]. As the AlN layer thickness is increased, due to the interference dips [Guo02], the gains are often lower. For the thin wafer case, G_a is the maximum, when a 1.52-mm thick AlN layer is placed underneath. The best thin wafer case has ~ 10 dB higher gain than the best thick wafer case at 24 GHz which is being targeted for demonstration of a clock distribution system. A plausible reason for this gain difference is that the propagation length through lossy silicon wafer (part of path D in Figure 3-3 [Kim01]) is shorter for the thin wafer.

G_a 's at different antenna separations when the thin wafer has the 1.52-mm thick AlN and the thick wafer has a 0.76-mm thick AlN layer beneath are shown in Figure 3-22. For 0.5-cm and 1-cm separations, the gain improvement at 24 GHz is ~ 10 and ~ 15 dB due to the wafer thinning. The larger the separation, the higher the gain improvement. For the case of thin substrate and 2-cm separation, at low frequency, the gain is ~ 8 dB lower than that at 1-cm separation. This gain difference is normal. However, at higher frequencies the gain increases so much that it is even higher than that at the 1 cm separation, which is

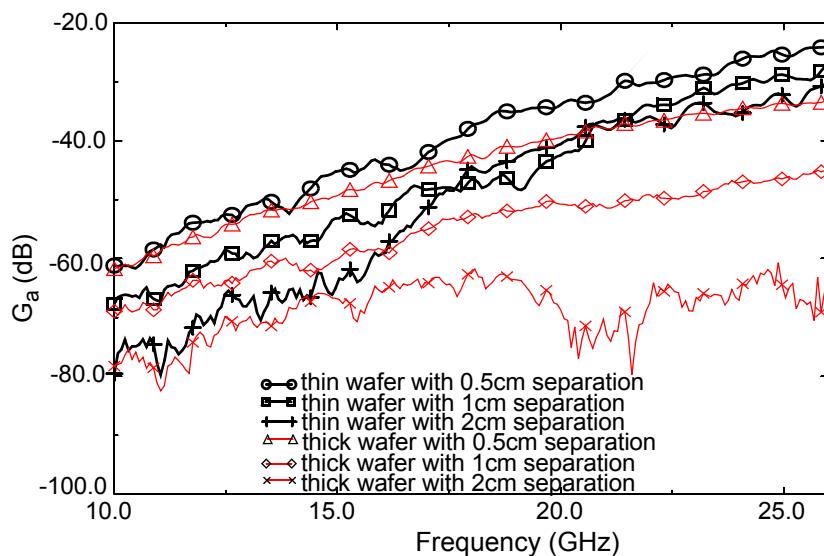


Figure 3-22 Antenna pair transmission gain with different antenna separations for thin and thick wafers.

interesting. One possible reason is that when the substrate is very thin, it may not be in good contact with the AlN and air gaps may exist between the wafer and AlN layer. These air gaps may affect the antenna gain measurements at high frequencies, especially with larger distance separations. Therefore, the 2-cm data on a thin substrate may not be accurate. However, from the 0.5-cm and 1-cm data, the substrate thinning does help to increase the antenna gain.

3.5 Conclusion

In this chapter, the efforts to characterize the interference effects of the package (mainly the heatsink) and the on-chip metal structures surrounding on-chip antennas are described. AlN, with its high thermal conductivity and excellent dielectric properties, is used as the propagation layer. The propagation layer is to reduce the negative effects of the heatsink and to maintain good heat removal. In addition, general design guidelines are proposed to avoid some metal structures with deleterious effects on the antenna pair gain and input impedance. Finally, the antenna gain on thinner lossy substrate (100 μm) is tested and increases \sim 10 dB for 0.5-cm separation and \sim 15 dB for 1-cm separation compared to that for the thick substrate case (600 μm).

CHAPTER 4

BROADBAND LOW NOISE AMPLIFIER

4.1 Introduction

As mentioned in Chapter 2, in this wireless clock distribution system, a wideband low noise amplifier (LNA) is needed at the receiver side to reduce its output signal settling time (Figure 4-1). For a broadband LNA, several topologies are proposed in the literature [Lim03, Lu04, Bev04, Ism04]. One method is to cascade two or three stages of narrow band LNAs resonant at frequencies close to each other [Lim03, Lu04]. This method does not significantly improve the bandwidth and may need two to three stages. The bandwidth of input matching network can be widened using a doubly-terminated LC ladder or a three-section Chebychev band-pass filter instead of a single second order resonator [Bev04, Ism04]. The input matching is wide in these designs (from 3 to 10 GHz), and for output, low Q inductance (Q_{ind} is ~ 1.1) is used to lower the output Q for broadband matching. Because of this low output Q, the gain of broadband LNA's using CMOS technology is low, ~ 10 dB. The drawback of these complex input matching is that one or two

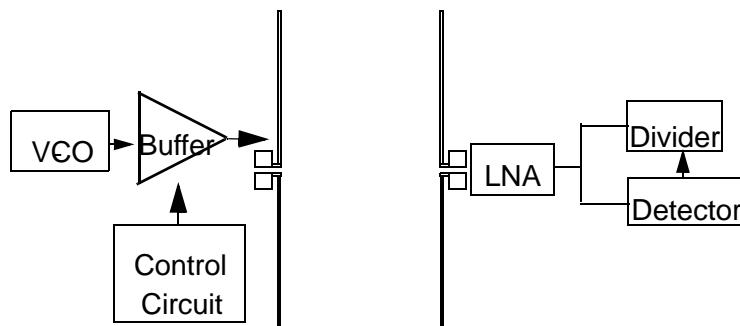


Figure 4-1 The block diagram of a transmitter and a receiver in the wireless clock distribution system.

more inductors are added at input. These inductors may occupy more area, and the parasitic resistances associated with these input inductors will degrade the LNA noise figure.

In this broadband LNA design, a simple series low Q (1.4) RLC tuning network is used for input matching to achieve acceptable broadband input matching (~ 8 GHz), and good noise performance, and to reduce the area occupied by this circuit. The challenge in this broadband LNA design is to design a broadband output matching network with higher gain.

4.2 LNA Topology and Measurement Results

4.2.1 LNA Topology

In this design, a differential two-stage cascode amplifier topology with inductive degeneration at the source is used [Sha97, Ho96]. The amplifier is fully integrated including the input and output matching networks. Instead of using current sources for biasing, inductors (L_{c1} and L_{c2}) are used to increase headroom thereby improving the linearity (Figure 4-2). The output of first stage is AC coupled to the input of second stage through a coupling capacitor to enable independent biasing of the two gain stages. The gates of M_3

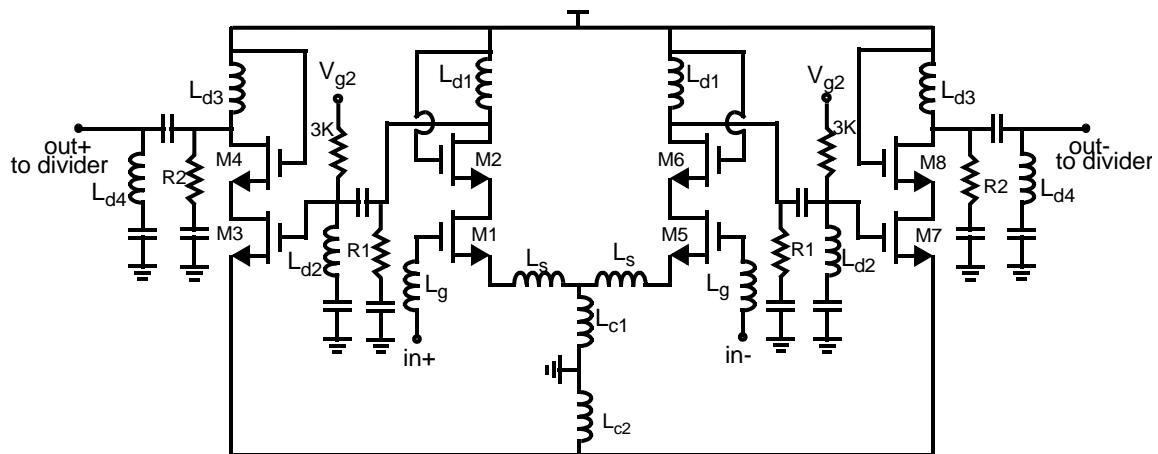


Figure 4-2 The schematic of 2-stage differential LNA.

and M₇ are biased through 3-kΩ on-chip resistors using an off-chip voltage source. The outputs of LNA are intended to be AC coupled to the divider and detector inputs like the coupling between the two stages of LNA.

To design an amplifier with a large 3-dB bandwidth, the quality factor (Q) of the input network ($L_g\omega_o/2Z_s = (2C_{g1}\omega_o Z_s)^{-1}$) including the source impedance is set to 1.4. This results a bandwidth around 8 GHz. The real challenge to attain the large bandwidth is lowering the Q of the output matching network while achieving acceptable gain. Typically, an inductor L_d is used to resonate with the output capacitance which includes the capacitance of cascode amplifier output (C_{out}), and coupling capacitor (C_{coupling}) in series with the input capacitance of the divider and detector (C_{load}), and parasitic capacitance from C_{coupling} to ground (C_{para}) (Figure 4-3). In theory, C_{para} of a MOS capacitor is ~20% of the total capacitance, and for a metal insulator (inter-level dielectric) metal capacitor (MIM), C_{para} is ~10%. Because of this non-negligible C_{para}, a difficulty is to simultaneously achieve high gain and large bandwidth. Making C_{coupling} larger increases the C_{para} and

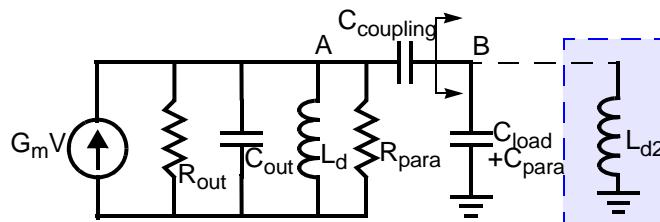


Figure 4-3 A simplified circuit schematic for the LNA output.

decreases the required L_d. Assuming the inductor Q_{ind} is approximately constant with inductance at resonant frequency, decreasing L_d also decreases the parasitic resistance of L_d and $R_{para} = \omega L_d Q_{ind}$ (the equivalent parallel representation of the inductor series resistance). Because the output resistance of cascode amplifier (R_{out}) and R_{para} are compa-

rable, the reduction of parallel combination of R_{out} and R_{para} (R_{output}) is not as rapid as the reduction of L_d , therefore $Q_{output} = R_{output}/(\omega L_d)$ increases with decreasing L_d . However, this will still not only lower the LNA bandwidth, but also the voltage gain because the output resistance (R_{output}) is lower. On the other hand, the capacitance of $C_{coupling}$ cannot be too small compared to $C_{load}+C_{para}$ because of the voltage drop across $C_{coupling}$. The same issue is present for the coupling between the first and second cascode stages.

In order to alleviate this problem, a new output tuning network is used between the two amplifying stages, and between the output of LNA and the divider and detector input. As also shown in Figure 4-3, L_d is used to resonate with the C_{out} , and an additional L_{d2} is used to resonate with the divider and detector input capacitance and the parasitic capacitance of the coupling capacitor ($C_{load}+C_{para}$). Therefore, at the resonant frequency, the impedance looking into B is large. There is a smaller voltage drop across $C_{coupling}$, and the voltage gain at the resonant frequency is increased. The output network behaves like a capacitively coupled 2 L-C-section filter. By proper selection of the values of $C_{coupling}$ and L_{d2} , the frequency response around the resonant frequency can be made flatter. To further decrease the output Q to around 3, a parallel resistor R_1 (500- Ω polysilicon resistor) is added. Since R_1 is located at the output of a cascode stage, its impact on noise performance is small. In this topology, the voltage gain is sacrificed to achieve a wider bandwidth. To achieve acceptable gain, another amplifying stage is added.

4.2.1 Measurement Setup and Results

To characterize the LNA by itself, an LNA test circuit was fabricated. In this circuit, a shunt-C and series-L on-chip matching network is used to match the output to 50 Ω

(Figure 4-4). This reduces the uncertainties in 50- Ω noise figure measurements [Agi05].

Directly connecting the LNA to a 50- Ω load would dramatically change the loading at point A in Figure 4-4 and could change the noise figure and linearity. The addition of the L matching network reduces the change of voltage gain at point A due to the 50- Ω load for the measurements. This should provide the measurements of noise figure and linearity of the LNA nearer to the actual operating situation in the receiver (Figure 4-1). The impact of

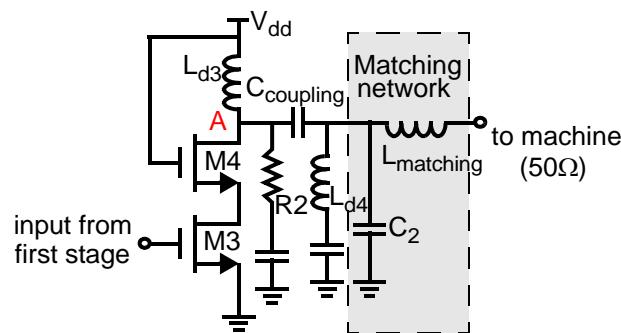


Figure 4-4 The output matching network for the LNA test structure.

the added output matching network on noise figure measurements should be negligible, because the noise performance is dominated by that for the first gain stage. The S-parameters of the additional matching network can be separately measured and can be de-embedded. Using the de-embedded LNA S-parameters along with the input impedance of the divider and detector, the voltage gain versus the frequency plot of the LNA in Figure 4-1 can be computed.

This LNA is fabricated in an 8-level-metal 130-nm CMOS process. A die photo of the LNA is shown in Figure 4-5. The die area is $800 \times 1000 \mu\text{m}^2$. Excluding the extra matching network for measurements and bond pads, the die area is $600 \times 600 \mu\text{m}^2$. The symmetry of the two branches is maintained to reduce the offsets and to keep common mode rejection high. C_{coupling} is realized using the metal insulator metal capacitor (MIM)

structure. The top plate is formed using metal 6 and 8 layers, and the bottom plate is formed with metal 5 and 7 layers. The capacitor value is 100fF and the area is $600 \mu\text{m}^2$. The parasitic capacitance value is $\sim 10\text{fF}$. For better substrate noise isolation, all pads and metal capacitors are ground-shielded using a polysilicon block.

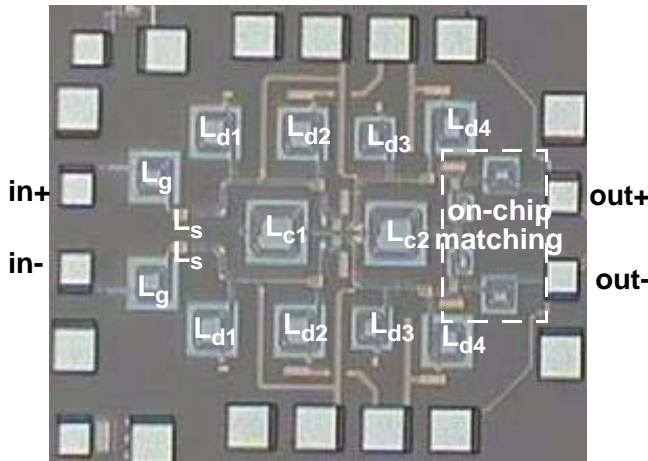


Figure 4-5 The die photo of the two-stage differential LNA.

The set up for measuring S-parameters is shown in Figure 4-6. At the input side, a balun transforms a single-ended signal into balanced or differential signals, which are fed into the LNA using a GSSG probe. At the output, the balanced signals are turned into a single ended signal and fed into a network analyzer. The set-up is calibrated to the interfaces between the probes and LNA. The measurement results are shown in Figure 4-7. This figure shows that at $V_{DD}=1.2\text{V}$ and 20 mA bias current, the LNA has 9 dB transducer

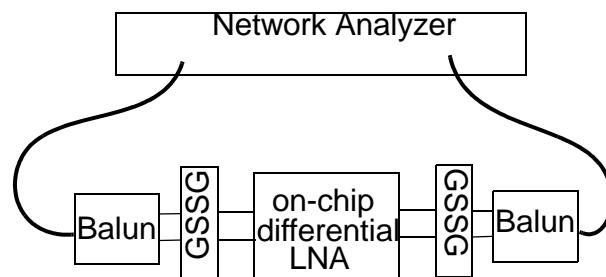


Figure 4-6 Measurement setup for on-chip differential LNA's.

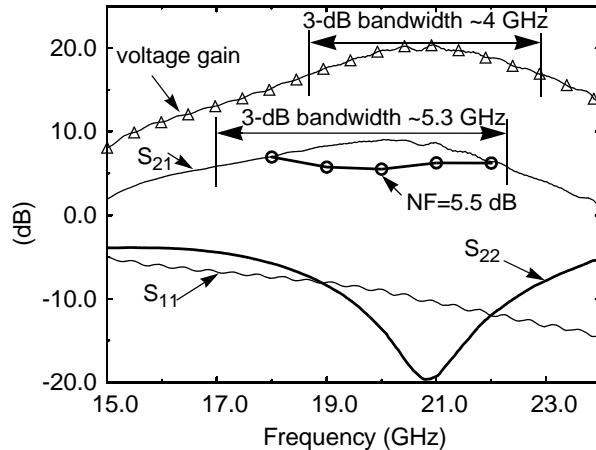


Figure 4-7 The measured noise figure, voltage gain, transducer gain ($|S_{21}|^2$), and input and output reflection coefficients of the differential LNA. The LNA achieves ~ 5.5 dB NF, and 20-dB voltage gain at 20 GHz with power consumption of 24 mW.

gain ($|S_{21}|^2$) peaked at 20 GHz. The gain curve is quite flat with a 3-dB bandwidth of 5.3 GHz. For matching, $|S_{11}|$ is -9 dB and matching is broadband. $|S_{22}|$ is -14 dB at 20 GHz and has ~ 1.5 -GHz span below -10 dB. This narrow band response is due to the L-C matching network added at the output for measurements. The extracted voltage gain of the LNA expected when it operates as part of the receiver is also shown in Figure 4-7. This plot is extracted from the measured data using the technique outlined in the beginning of this sec-

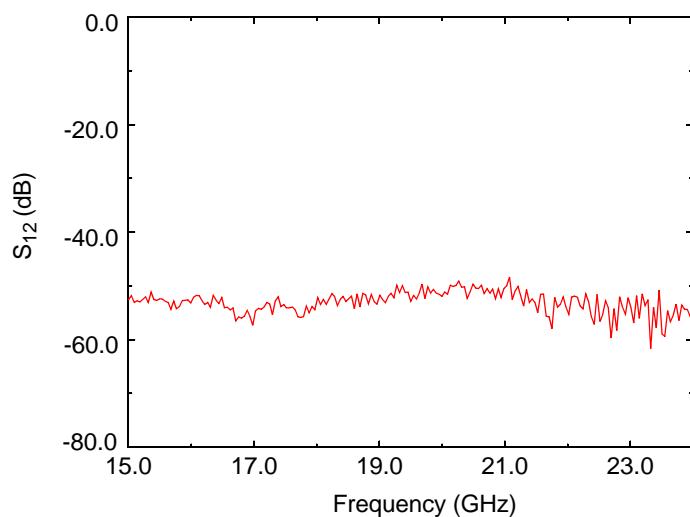


Figure 4-8 Reverse isolation (S_{12}) of the differential LNA.

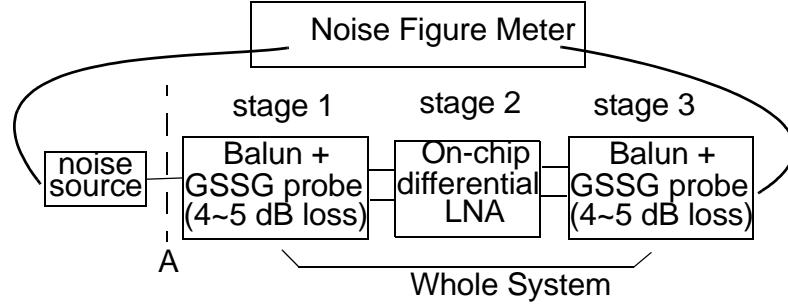


Figure 4-9 Noise figure setup for on-chip differential LNA's.

tion. The peak voltage gain is 20 dB with 4-GHz wide 3-dB bandwidth. The reverse isolation $|S_{12}|$ (Figure 4-8) is approximately -43 dB at 20.67 GHz. This excellent isolation is due to the use of a 2-stage topology.

Near 20 GHz, the baluns and the probes have significant loss (around $4 \sim 5$ dB combined loss). This in combination with the fact that the noise figure meter can only calibrate up to the output of the noise source (interface A in Figure 4-9) [Agi05] makes the direct measurement of the 50Ω noise figure of the LNA impossible. Therefore, the noise figure of the entire system is measured. Using the Friis's equation [Fri44] (4.1),

$$F_{total} = F_1(R_s) + \frac{F_2(Z_{out1}) - 1}{G_{A1}} + \frac{F_3(Z_{out2}) - 1}{G_{A1}G_{A2}} \quad (4.1)$$

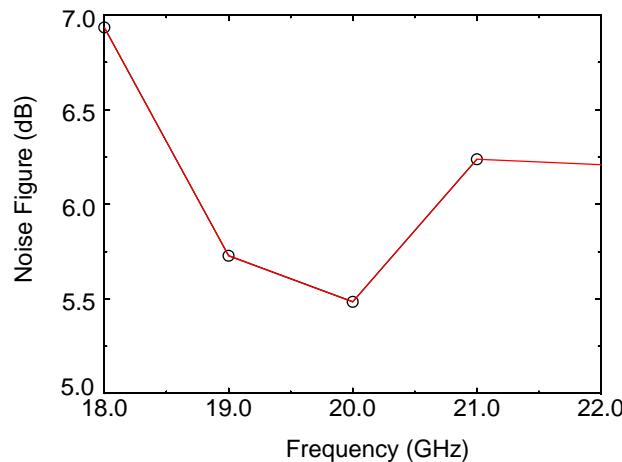


Figure 4-10 Noise figure of the LNA.

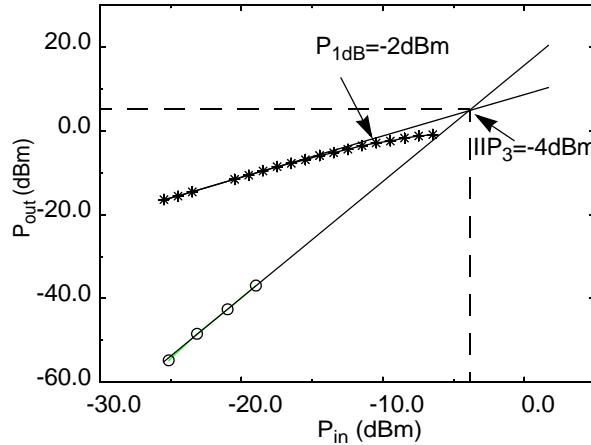


Figure 4-11 Measured P_{1dB} and IIP_3 .

the noise factor of LNA is extracted from the measurements of noise factors/insertion losses of the baluns and probes. G_A 's are the available power gains. The detailed noise measurement process is discussed in Appendix D. The extracted noise figure of the LNA is shown in Figure 4-10. The noise figure is ~ 5.5 dB with measurement uncertainty of $+/ -0.5$ dB. The output power versus input power plots are shown in Figure 4-11. The measured P_{1dB} is -2 dBm and IIP_3 is -4 dBm at power consumption of 24 mW, which are excellent.

4.3 LNA Simulation and Measurement Discrepancy Analysis

4.3.1 Reasons for the Frequency Shift and Lower Gain of LNA

Comparing the measurements to the simulations in Cadence, there are significant differences in gain and the peak frequency. In simulation, the peak gain is ~ 22 dB and the peak gain frequency is at 24GHz instead of 20GHz (Figure 4-12). The cause for this gain and frequency mismatch between simulation and measurements must be found to avoid this mismatch in the future.

One possible reason is that the values of the passive components in the circuits, the metal capacitors or the inductors, are off at high frequencies, causing the mismatch in gain

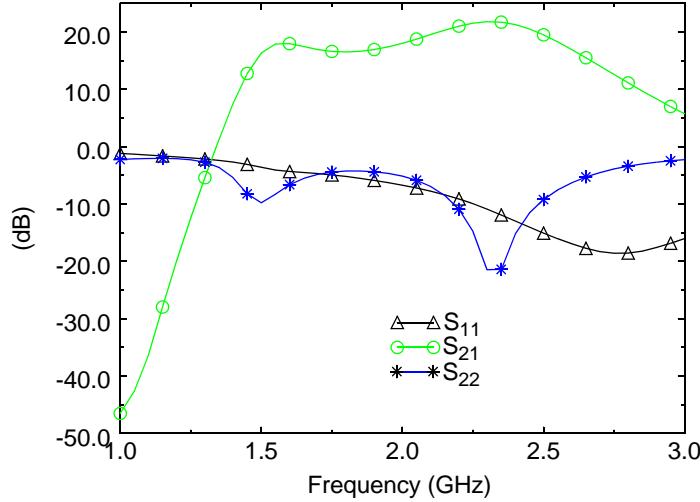


Figure 4-12 The simulation results of the LNA S-parameters.

and frequency. To verify this, the test structures of these passive components are measured. The first one is the C_{coupling} . As mentioned before, C_{coupling} is realized using the metal insulator metal capacitor (MIM) structure. The top plate is formed using metal 6 and 8 layers, and the bottom plate is formed with metal 5 and 7 layers. In simulation, the capacitor value was 100 fF and the area was $600 \mu\text{m}^2$. The parasitic capacitance value was ~ 10 fF. The measurements have shown that the capacitance is ~ 120 fF, and the parasitic capacitance is increased to 18 fF. For the on-chip inductors, the measurements show that the inductance values are quite accurate, and the Q at 20 GHz is ~ 15 , close to the simulation value. Putting these measurement results into the simulation in Cadence, the gain only

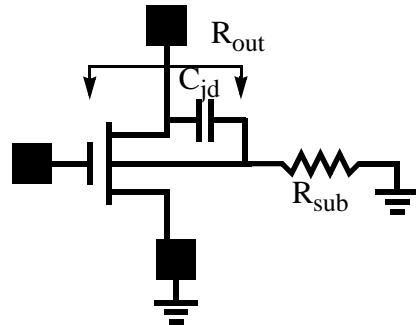


Figure 4-13 The schematic of transistor test structure.

drops 1 dB and the frequency shifts from 24 GHz to 23 GHz. Therefore the modeling and design limitations of the passive components are not the main reason for the big gain drop and frequency shift.

Another component that has to be considered is the transistor itself. Presented in Table 4-1 are the main differences between the measurement results and the simulation results for the test structures shown in Figure 4-13 [Su]. The two main differences come

Table 4-1 Transistor test structure simulation value and measurement results

Transistor test structure ($14\mu/0.13\mu$)	simulation value	measurement result
C_{jd}	10fF	19fF
R_{sub}	10Ω	45Ω
R_{out}	$1.2K\Omega$	600Ω

from the C_{jd} and the series resistance R_{sub} connecting the body of the transistor to the substrate. The value for C_{jd} increased by about 100% from simulation. And in Cadence simulations, the series resistor connecting the body to the ground was set to be 10Ω . However the measured R_{sub} was 45Ω . At low frequencies, this resistance will not significantly affect the transistor output resistance R_{out} because the Q of C_{jd} ($Q = 1/(\omega C_{jd} R_{sub})$) is high and thus the equivalent parallel representation of R_{sub} ($R_{para} = R_{sub} \times (1 + Q^2)$) is high. At 24 GHz, however, the Q of C_{jd} is 7.8 and the equivalent parallel representation of R_{sub} is lower. This change lowers the output resistance looking at the drain of the transistor (R_{out}) and lowers the voltage gain.

Based on the measurement results, the transistor model was augmented as shown in Figure 4-14. The LNA simulation using this model shows that the parasitic resistor lowers the LNA gain approximately 4dB. The 100% increase in C_{jd} and C_{js} caused the resonant frequency shifting to 21 GHz. Also the increased parasitic capacitance at the middle

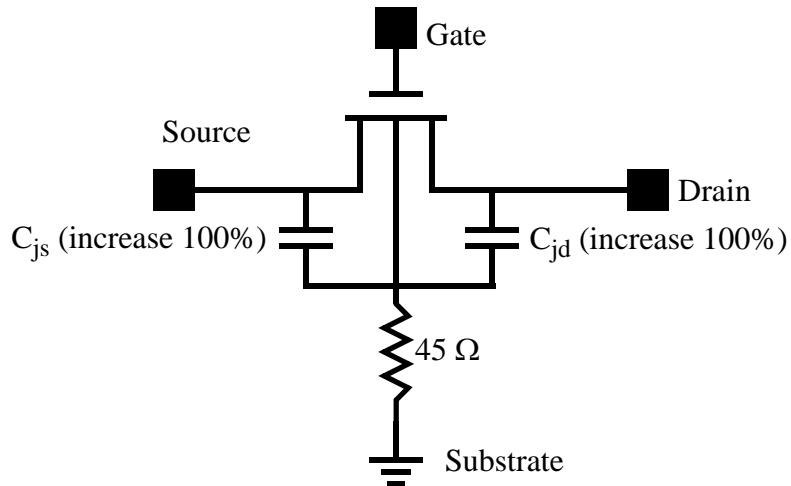


Figure 4-14 The modified model for simulation in Cadence.

point of the cascode structure (the source point of M2, M4, M6, M8 in Figure 4-2) lowers the LNA gain by another 8 dB.

4.3.2 Redesigned LNA Using the Modified Transistor Model

To verify the accuracy of the modified transistor model, the LNA is redesigned using the modified model. In this design simulation, the LNA is retuned to 19GHz. Also,

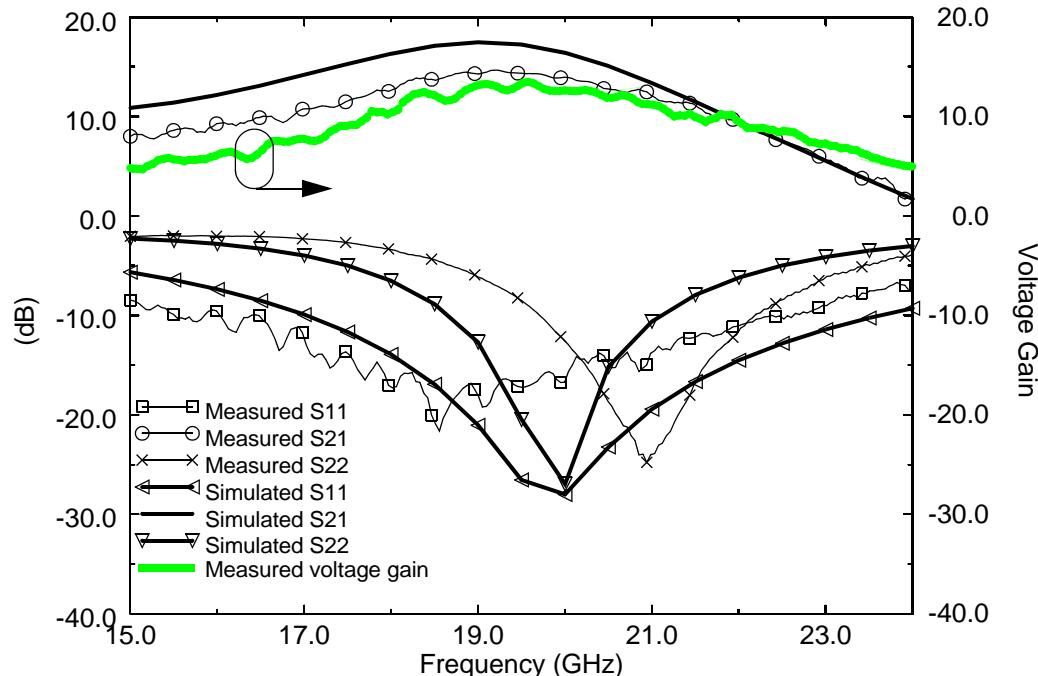


Figure 4-15 The comparison between the simulation and the measurement results of redesigned LNA using modified transistor model.

the resistors for reducing the output Q (R1, R2 in Figure 4-2) are removed. Figure 4-15 shows the simulation and measured results of the redesigned LNA. The measured gain is 14dB, which is around 3 dB lower than the simulated gain, but they are all peaking around 19GHz. The 3-dB bandwidth of this redesigned LNA is 4 GHz, ~1.3 GHz lower than the former LNA because of the removal of R1 and R2. And for input and output matching, the measured results are just 1 GHz off from the simulation. These results verify the improved accuracy of the modified transistor model. The LNA voltage gain is 13 at 19 GHz, and is 7 at 17 GHz and 9 at 18 GHz. For the system demonstration discussed in Chapter 5, the LNA in the receiver is this redesigned LNA.

4.3.3 Suggestions about the Future LNA Design

Having determined of the causes for the reduced measured gain of the LNA, methods to increase the LNA gain can be formulated. From the discussion above, there are three causes for the reduction of the first LNA gain. One is the tuning frequency mismatch between the first and second stage because of the parasitic capacitance mismatch. The second reason is the lowered output impedance caused by the parasitic capacitance between the transistor drain and body, and the series body resistance. The third reason is the parasitic capacitance at the middle point of the cascode structure [Sam00].

From the results of the redesigned LNA, re-tuning the matching network to address the first cause can help to increase the LNA gain. Regarding the second cause, since the output resistance is lowered, the added resistors (R1, R2 in Figure 4-2) is not needed to lower the output Q. By removing these resistors in the resigned LNA, the output Q is increased from 3 to 4, and the gain is also increased. These two modifications increase the LNA gain ~5dB.

The most gain reduction comes from the parasitic capacitance at the middle point of the cascode structure (point X in Figure 4-16). This parasitic capacitance lowers the impedance at point X and lowers the gain of the cascode structure. To address this problem, the effect of this capacitance must be nullified. Placing an inductor in parallel with the capacitor can be a remedy for this problem [Sam00]. This tuned circuit can increase the LNA gain by another 5 dB in simulation. This added tuned structure does not significantly affect the over all Q of this circuit because there is a small resistor ($1/gm_2$, $\sim 30 \Omega$) in parallel with the L-C circuit, which keeps the Q of this tuned network small. However, adding 2 more inductors complicates the design layout. In the redesigned LNA, this method is not incorporated because of the limited time.

4.4 Conclusion

The performance of published MOS LNA's operating above 20 GHz is summarized in Table 4-2. The first designed LNA in this work has the lowest noise figure and the lowest power consumption among all the LNAs that are working above 20 GHz except for the one fabricated using 90-nm SOI technology measured at the high V_{DD} of 2.4 V. The LNA presented here also has a 3-dB bandwidth for voltage gain of 4 GHz. Considering the

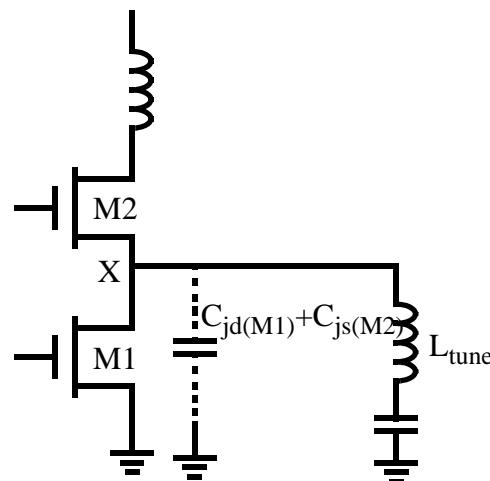


Figure 4-16 Adding a tuning inductor at the middle point of the cascode structure.

fact that this LNA uses a differential topology, the power consumption is especially low compared to those for the previously published MOS LNA's. The results show that it is possible to implement LNA's with moderate NF and power consumption and an acceptable 3-dB bandwidth above 20 GHz using bulk CMOS technologies.

Also, comparing the simulation and measurement results of the redesigned LNA using the modified transistor model, the close resemblance between these two results suggest that the modified transistor model is quite accurate.

Table 4-2 MOS LNA's operating above 20GHz

Technology Amplifier type	f_{center} GHz	S_{21} dB	NF dB	IIP3 dBm	V_{dd} $/I_{dd}$ /Power	3dB BW $ S_{21} $
180-nm CMOS [Gua04] Single Ended, not matched to 50Ω (output)	21.8	15	6	N.A.	1.5V 16mA 24 mW	N.A.
180-nm CMOS [Yu03a] Single Ended	23.5	12.8	5.6	N.A.	1.8V 30mA 54 mW	N.A.
180-nm CMOS [Yu03b] Single Ended	25.7	8.9	6.9	N.A.	1.8V 30mA 54 mW	4.5G
180-nm CMOS [Fra03] Single Ended	24	10	6	N.A.	1.8V 188mA 338 mW	N.A.
100-nm SOI [Flo02b] Differential	23.8	7.3	10	-7.8	1.5V 52mA 78 mW	4.5G
90-nm SOI [Eli04] Single Ended	35	11.9	3.6	N.A.	2.4V 17mA 40.8 mW	16G
130-nm CMOS Differential (this work)	20.6	9	5.5	-4	1.2V 20mA 24 mW	5.3G

CHAPTER 5

INTRA-CHIP WIRELESS CLOCK DISTRIBUTION DEMONSTRATION

An intra-chip wireless clock distribution system is implemented using the UMC 130-nm CMOS technologies. As mentioned in Chapter 2, in this system (Figure 5-1), there are three major sub-components: transmitter, receiver, transmitting and receiving antenna pair. In the transmitter, a voltage control oscillator (VCO) generates a continuous 20-GHz sine wave and the output buffer amplifies this signal. The control circuit generates periodic 2-ns long no clock transmission [Li05]. On the receiver side, the LNA amplifies this received signal, and feeds it into both the divider with programmable delays and the detector. As described in Yang's thesis [Yan04], the detector generates a pulse signal (INI) from this 2-ns no clock transmission period to control the programmable divider. At the rising edge of the INI, the divider loads the programmed delay. After the INI falling edge, the divider starts counting down the programmed delay at the first crossing point of the clock signal. The programmed delay is used to compensate the static skew to different receivers.

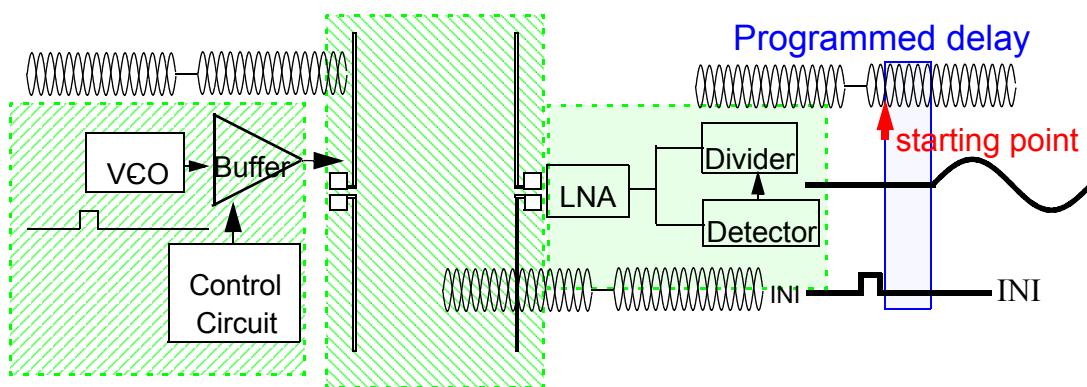


Figure 5-1 The block diagram of intra-chip wireless clock distribution system including a transmitter, on-chip antenna pair and a receiver.

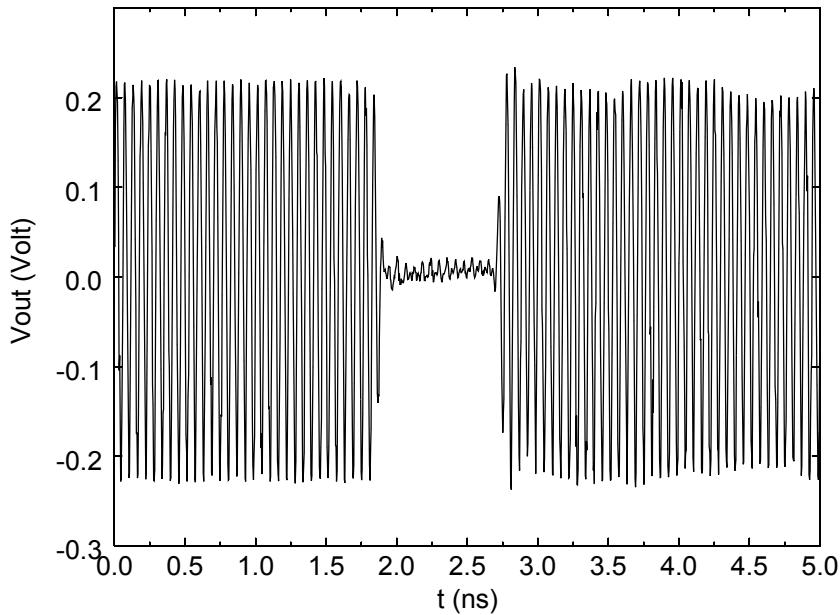


Figure 5-2 (a) The output signal of transmitter with 1 ns no transmission period.

In the system demonstration, two factors are critical. One is the divider start-up scheme, that is the divider starts to divide at a proper moment after receiving the INI signal falling edge. The other is the programmability of divider to control the output delay of receiver. Before the system demonstration, the individual blocks are first characterized.

5.1 Individual Blocks

5.1.1 Transmitter Characteristic

As mentioned in Chapter 2, the transmitter generates the high frequency clock signal with 2-ns no transmission period to control the receiver. The transmitter output signal with no transmission period is shown in Figure 5-2. Here this period is 1 ns instead of the simulated 2 ns in Chapter 2. Figure 5-3 shows the output power of transmitter versus frequency. The maximum output power is $\sim 5 \text{ dBm}$ at 17 GHz. At 18GHz, the transmitter output power is $\sim 4 \text{ dBm}$, and at 19GHz, $\sim 3 \text{ dBm}$. However, as shown in Figure 5-4, the VCO tuning range is from 20.1GHz to 23.3 GHz. Therefore, there exists a discrepancy between

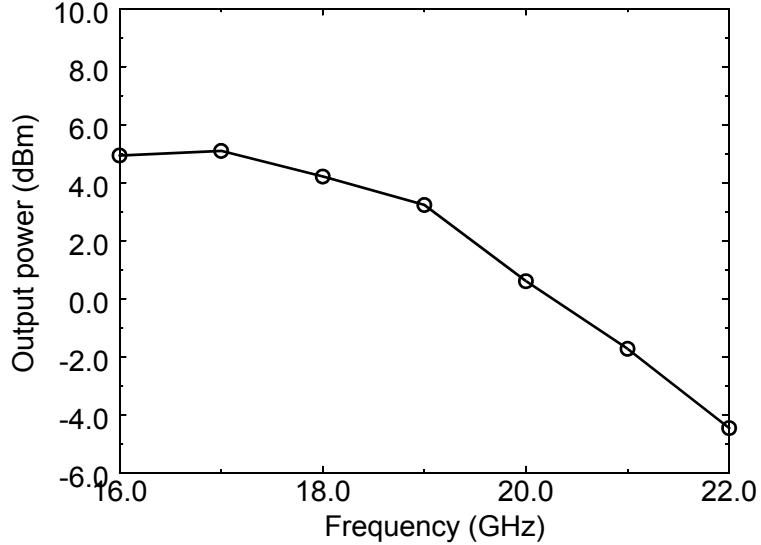


Figure 5-3 The output power of the transmitter at different frequencies.

the oscillator frequency range and the maximum transmitter output power frequency range.

5.1.2 Receiver Characteristic

The receiver is composed of two parts, the LNA and programmable divider. The performance of LNA is discussed in Chapter 4. It has the maximum voltage gain at 19 GHz, which is \sim 13 or 22 dB. This section discusses the measured performance of the programmable divider which was originally designed and characterized by Yang [Yan04]. In

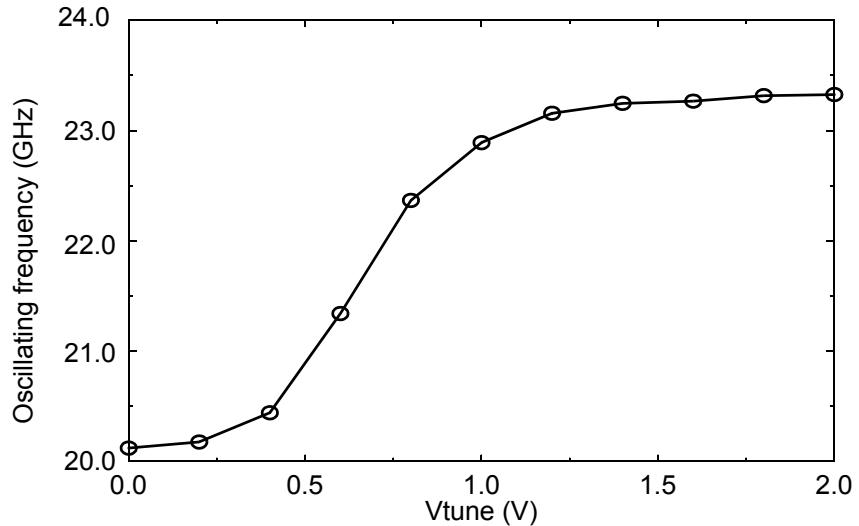


Figure 5-4 The tuning range of the VCO in transmitter.

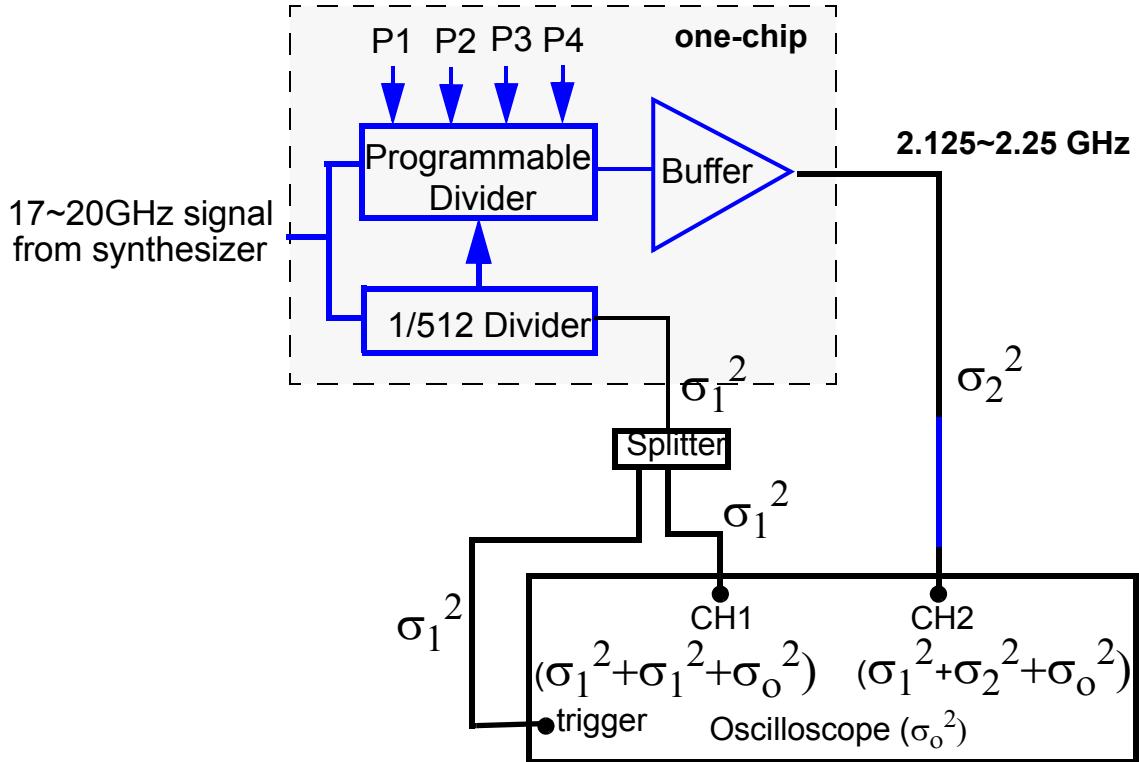


Figure 5-5 The measurement setup to characterize the programmable divider.

the redesign of the receiver in the second tapeout, an output buffer is added to the divider output to increase the receiver output swing when driving the 50Ω load of the oscilloscope. This greatly improves the jitter performance. Figure 5-5 shows the measurement

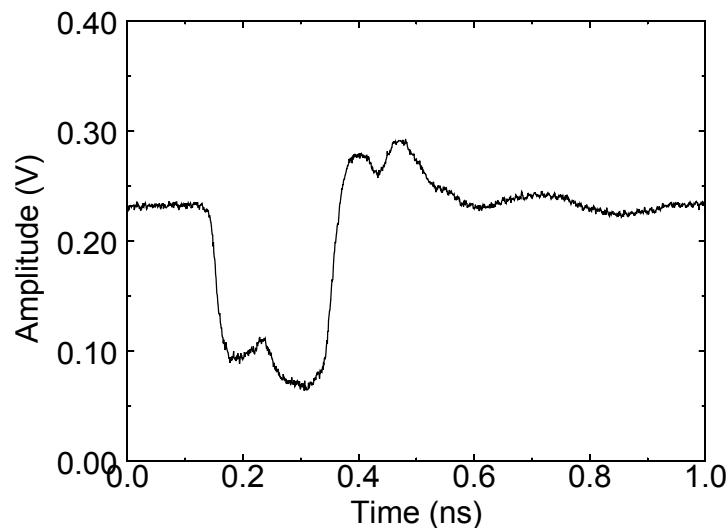


Figure 5-6 The output signal of the 1/512 divider as the oscilloscope triggering signal.

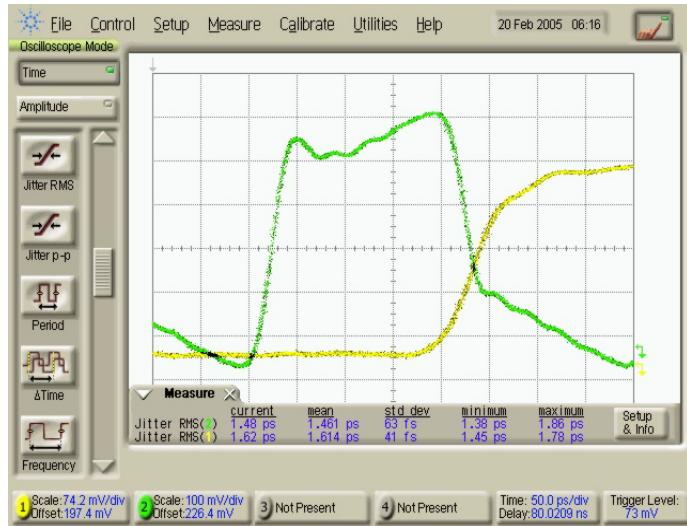


Figure 5-7 The measured RMS jitter of the two channels on oscilloscope. Channel 1 has 1.62ps RMS jitter and channel 2 has 1.48ps RMS jitter.

setup for characterizing the divider. The high frequency input signal is fed into the programmable divider and a 1/512 divider. The output signal of the 1/512 divider (Figure 5-6) is used as the INI signal to reset the programmable divider every 30ms. Also, it is used to trigger the oscilloscope. The programing bits (P_1, P_2, P_3, P_4) are connected to either ground or V_{dd} to program the delay of the divider. The working frequency range of the programmable divider is from 17 GHz to 20 GHz. The measurements show that the divider needs 0.13-V input signal amplitude for its operation. From the data shown in Chapter 4, the LNA voltage gain is ~ 9 , or 19 dB at 18GHz. Therefore, the input power of the receiver should be at least -24 dBm. The transmitter output power at 18GHz is around 4dBm, which leads to the conclusion that the antenna pair gain at 18GHz should be larger than -28 dB to make the system work.

Using the output signal of 1/512 divider as the triggering signal (Figure 5-6), the measured RMS jitter of the triggering signal is 1.62ps and the measured RMS jitter of the divider output signal is 1.48ps when the divider is operating at 17GHz (Figure 5-7). The

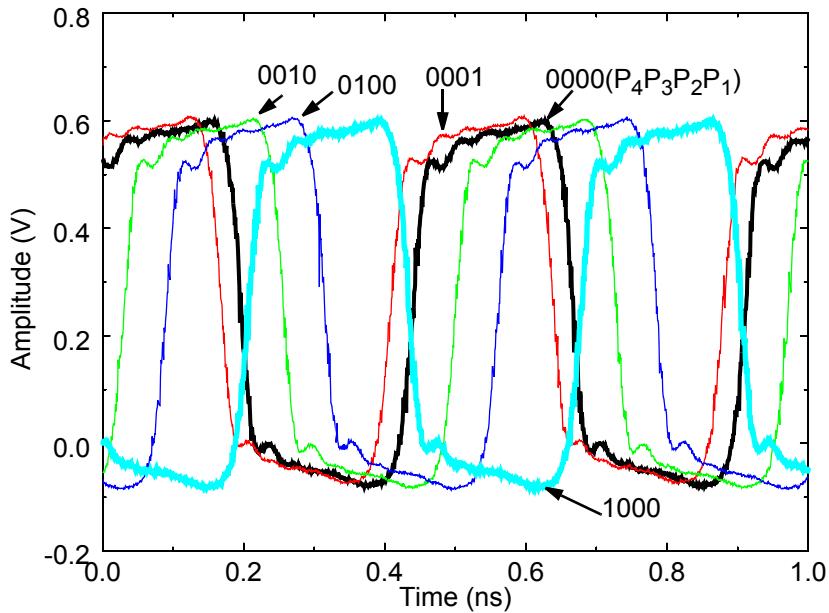


Figure 5-8 The output waveforms of the divider when the programming bits (P_4, P_3, P_2, P_1) are varied. The divider is working at 17GHz.

characteristic jitter of the oscilloscope, σ_0 is 1.2ps. Defining the RMS jitter of the 1/512 divider as σ_1 , and the RMS jitter of the divider as σ_2 (Figure 5-5), and assuming that the jitter of input signal from the synthesizer is quite small so that it can be ignored, the measured RMS jitter on the oscilloscope is $\sqrt{\sigma_1^2 + \sigma_1^2 + \sigma_0^2} = 1.62\text{ps}$ for the triggering signal, and the measured RMS jitter of the divider output is $\sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_0^2} = 1.48\text{ps}$ (Appendix E). The RMS jitter of the divider is $\sigma_2 = 0.43\text{ps}$, and the peak-to-peak jitter is 2.6ps, or $\sim 0.56\%$ of a divided clock period, which is small.

As mentioned in Chapter 2, the programming bits of divider (P_1, P_2, P_3, P_4) can set the delay of divider to $n \times \frac{1}{16}$ of a local clock period, where $n=1,2,\dots,15$ in order to compensate the static skew caused by different distances between a receiver and the transmitter, and the varying metal structures between the transmitting and receiving antennas. This is a critical feature of the divider that must be tested. The programmable divider output

waveforms for different programming bits are shown in Figure 5-8. Also, the differences between the expected and measured delays are compared in Table 5-1. The maximum deviation of measured delays from the expected is 3 ps. This difference mainly comes from the jitter of the divider output signal. It may also be caused by the DC power supply drift for the divider.

Table 5-1 The expected and measured delays of programmable divider when the divider is working at 17 GHz.

Programming (P ₄ P ₃ P ₂ P ₁)	0001	0010	0100	1000
Expected Delay (ps)	29.3	58.75	117.5	235
Measured Delay (ps)	32	60	120	238

In addition, the overlay of the divider output waveforms with different input power level is shown in Figure 5-9. Here the input power of the divider is varied from -1.5 dBm to 7 dBm (the input amplitude change from 0.18 to 0.5V). The skew caused by this input power variation is ~ 5 ps, which is 1.1% of the local clock period. Incidentally, the change of the divider output signal jitter with input power level is almost negligible.

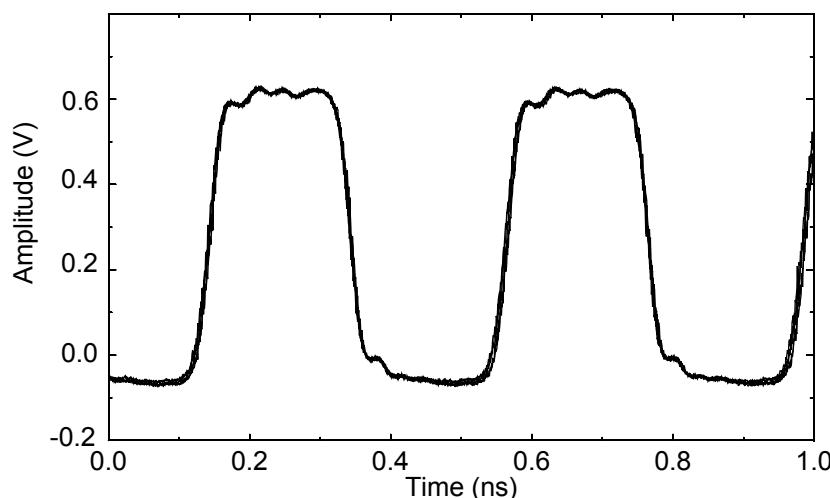


Figure 5-9 The output waveform of the programmable divider when the divider input power varies between -1.5 dBm to 7 dBm. The divider is working at 19GHz.

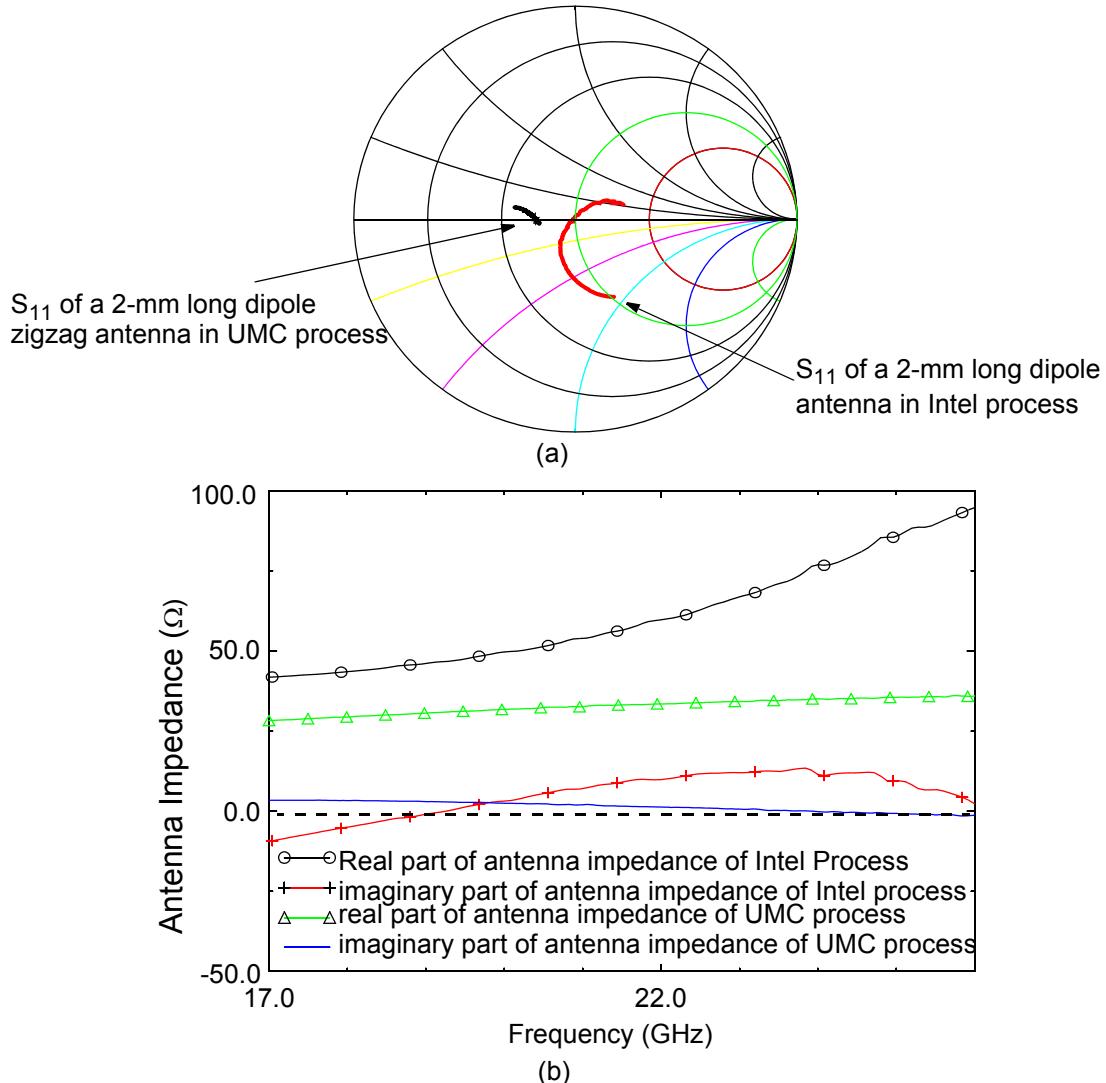


Figure 5-10 The characteristics of antennas using UMC and Intel processes. (a) The S_{11} of antenna fabricated using the UMC and the Intel processes. (b) The difference of antenna input impedance between antennas fabricated using UMC (first tapeout) and Intel processes.

5.1.3 Antenna Pair Characteristic

The transmitting and receiving antenna pair is another critical part in the system feasibility demonstration. From the above discussion, the antenna pair gain has to be greater than -28 dB to make the system work. Also, the antenna impedance has to be power matched to the transmitter output buffer and receiver input LNA. The antenna pair gain and impedance of antenna fabricated in the UMC process are characterized.

In the first design of the system, the characteristics of 2-mm zigzag antenna fabricated using an Intel process (gain and impedance) are used in the simulation. However, in the first UMC tapeout, the measured antenna characteristics were far off from that used in simulations. As shown in Figure 5-10, the antenna impedances are quite different. The antenna from the Intel process is tuned at 20 GHz, while the UMC antenna is tuned at 18 GHz. The real part of the antenna impedance of UMC antenna is $\sim 30\Omega$, while the Intel antenna is $\sim 45\Omega$ at 18GHz. This low antenna impedance of UMC antenna results in power mismatch at the transmitter output and receiver input. Also, the antenna pair gain (Figure 5-11) in UMC process is ~ -33 dB at 18GHz with 0.9-mm separation. While for the Intel antenna, it is ~ -42 dB at 4-mm separation. According to the former measurements, antenna pair gain drops ~ 8 dB when the separation is doubled. Then, the UMC antenna pair gain should be around -50 dB for 4-mm separation, which is ~ 8 dB lower than that for the Intel antennas. In addition, for the Intel antenna, the gain increases with frequency from 17 GHz to 21 GHz, and stay flat up to 26 GHz. On the other hand, the UMC antenna pair gain decreases monotonically from 17 to 26 GHz. This measurements of the gain show that the

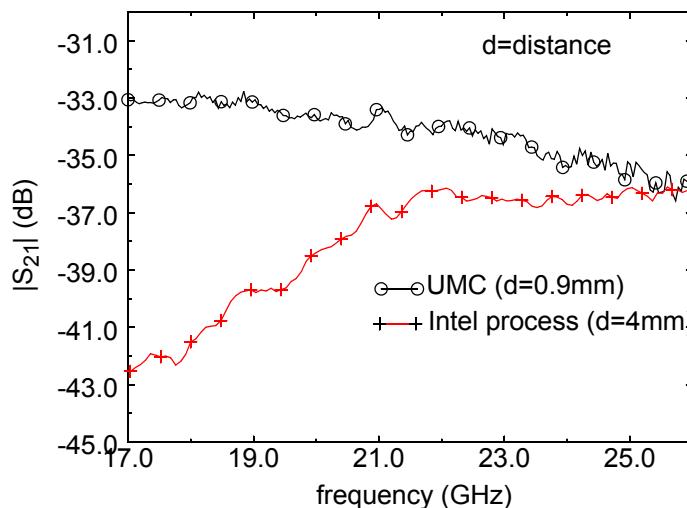


Figure 5-11 The comparison of the antenna pair gain for the first UMC tapeout and the Intel process at different frequencies.

antenna fabricated using Intel process is better suited to operate from 21 to 26 GHz, while the antenna fabricated using the UMC process is better suited for frequencies lower than 17 GHz.

There are two reasons for these gain and impedance differences between the antennas fabricated using the UMC and Intel processes. First, the layouts are different due to the different design rules. Figure 5-12 shows the layouts for the two different processes. In the Intel process, the zigzag antenna is realized using four 6- μm parallel lines with 0.6- μm separation in metal 1. In the UMC process, the antenna is implemented using three 8- μm parallel lines with 4- μm separation stacked from metal 1 to metal 4. This larger separations between parallel lines reduce the mutual inductance between the parallel lines, and change the antenna impedance and the antenna pair gain peak frequencies. The other reason is due to the different substrate doping. The previous measurements of antenna pairs on different substrates show that antennas on low-resistivity substrate have smaller impedance and lower antenna pair gain [Kim00]. UMC antenna are fabricated using a full CMOS process. Although its substrate resistivity is 20- $\Omega\text{-cm}$, the surface of substrate are more heavily doped (p-well or n-well) with significantly lower resistivities. Therefore, the

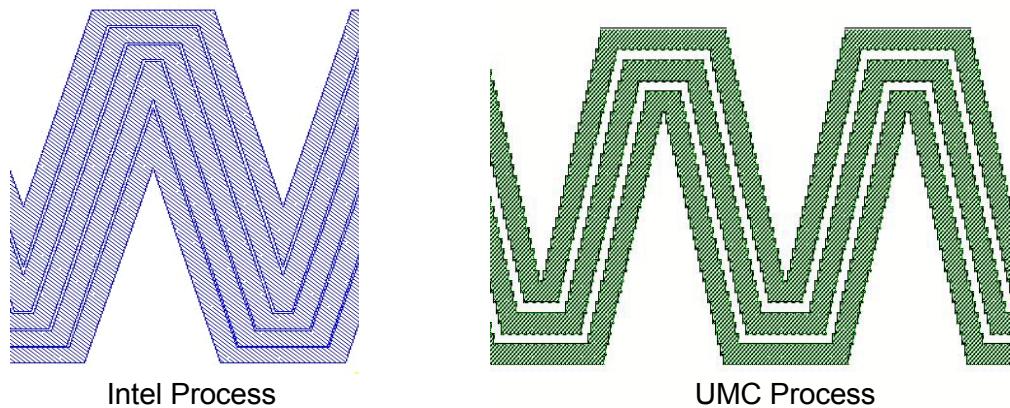


Figure 5-12 The comparison of antenna layout in different processes.

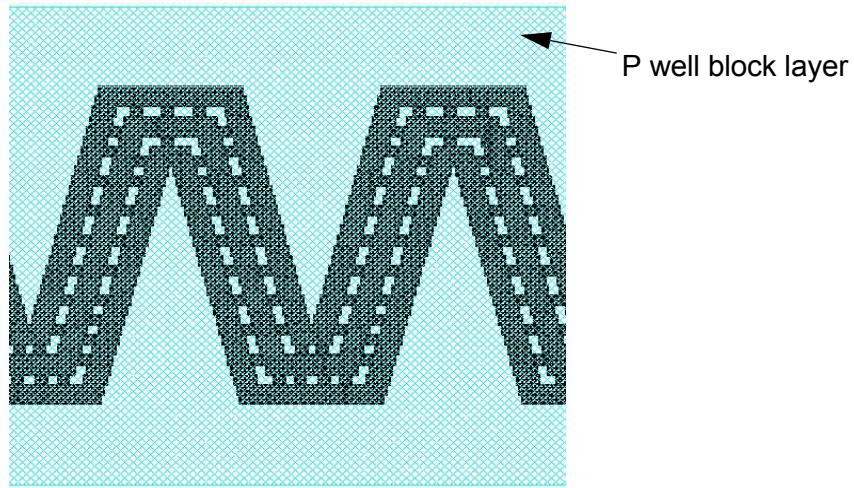


Figure 5-13 The layout of the new antenna.

substrate below the antenna, and between the antenna pair also has lower substrate resistivities than $20\Omega\text{-cm}$. However, for the Intel antennas, the substrates had uniform $20\Omega\text{-cm}$ resistivity. Therefore, the UMC antennas were on a more heavily doped substrate than the Intel antennas, which may have led to lower antenna gain and smaller antenna impedance.

In the second UMC tapeout, the antenna layout is modified to increase antenna gain and antenna impedance. Figure 5-13 shows the layout of the new antenna. Here the

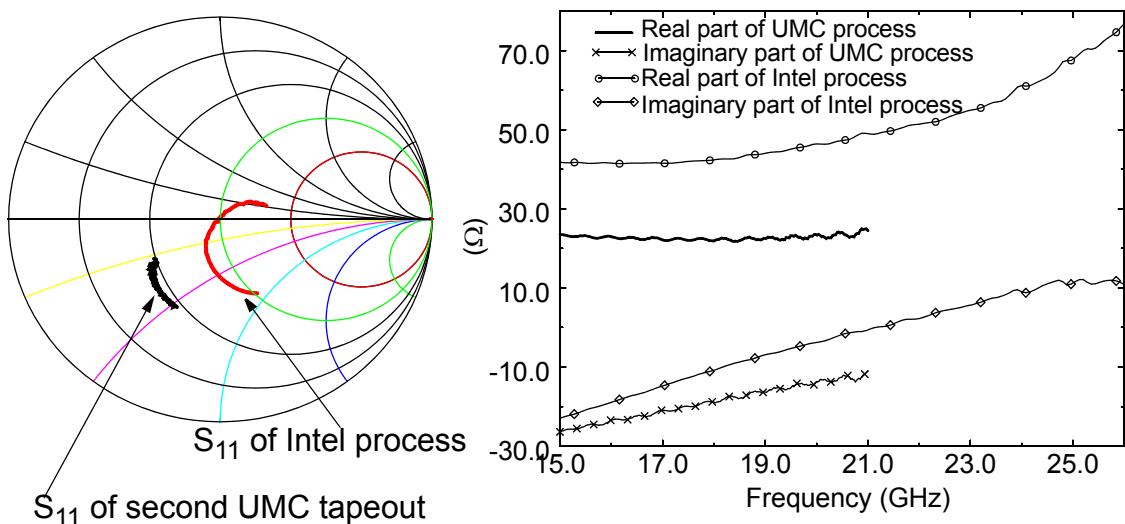


Figure 5-14 The characteristics of antennas using UMC (2nd version) and Intel processes. (a) The S_{11} of 2-mm antennas fabricated using UMC process and Intel process. (b) The impedances of the two antennas.

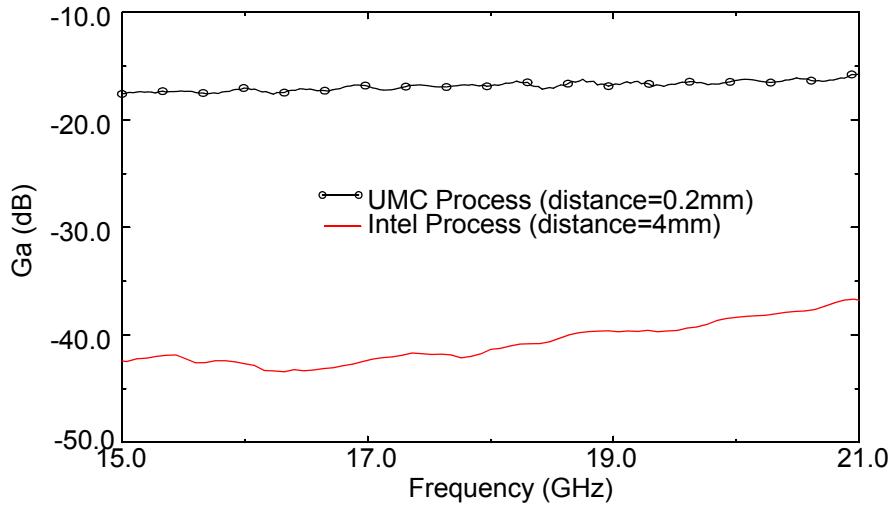


Figure 5-15 The antenna pair gain comparison between the modified UMC antenna with 0.2-mm separation and the Intel antenna with 4-mm separation.

antenna is implemented using three 8- μm parallel lines stacked from metal 1 to metal 8, with 4- μm separation. And these lines are also connected using 4- μm wide metal lines. Also, a p-well doping block layer was placed in order to leave the substrate resistivity below the antenna at $20\Omega\text{-cm}$. Comparing the antenna impedances, the new antenna characteristics are closer to that for the Intel antennas. As shown in Figure 5-14, the dependence of the new antenna impedance on frequency is similar to that of the Intel antennas. Its tuned frequency is ~ 22 GHz, although the real part is still less than that of the Intel antennas. Comparing the antenna pair gain shown in Figure 5-15, the modified antenna pair gain is around -17 dB with 0.2-mm separation at 18 GHz, translates to around -50 dB with 4-mm separation, which is still ~ 8 dB lower than the Intel antenna pair gain. However, the gain rises monotonically with frequency like the Intel antennas. A possible reason for the lower gain is that the substrate between the antenna pair still has lower resistivity regions.

The above measurement results show that comparing to the first UMC antenna, the new antenna is more suitable for the system operating at frequencies higher than 21 GHz.

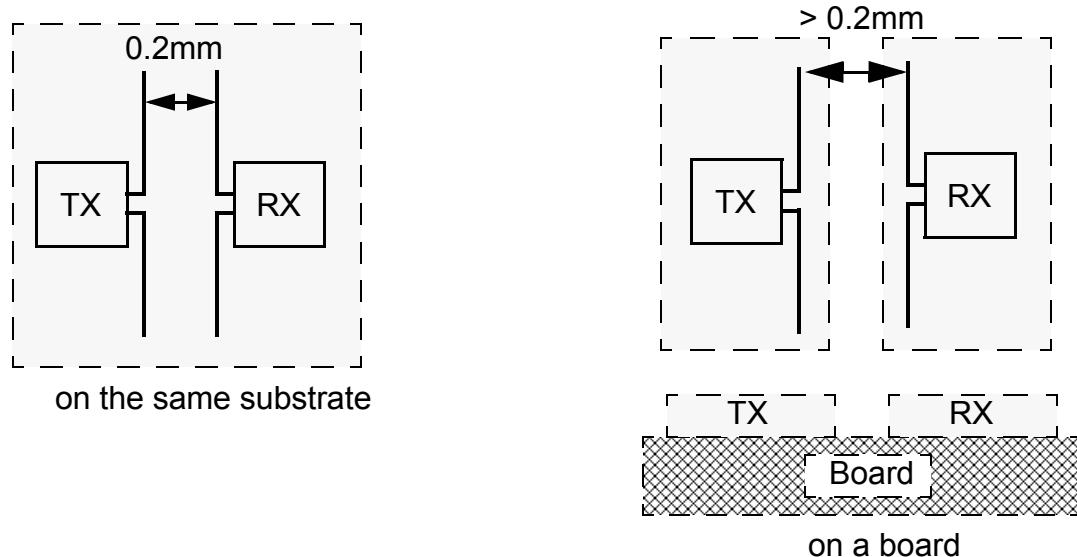


Figure 5-16 Measurements with two antennas on the same substrate, and with two antennas on a printed circuit board.

The above measurements are done when the transmitting antenna and the receiving antenna are on the same substrate and the propagating medium is silicon. For measurements of antenna pairs at separations greater than 0.2 mm (Figure 5-16), the transmitter and receiver are cut and glued on a printed circuit board made of FR4. Because of this, the propagating medium is a combination of silicon, air and FR4 on the printed circuit board.

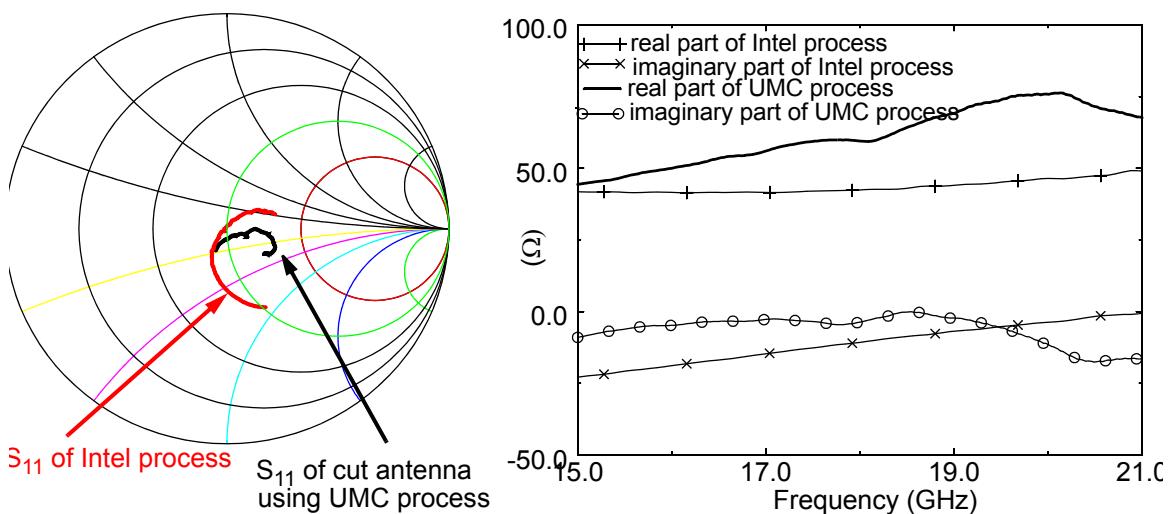


Figure 5-17 The comparison of S_{11} and antenna impedance between Intel antennas and the UMC antennas (2nd version) on a printed circuit board.

The change of propagating medium changes the antenna pair characteristics. Figure 5-17 shows that the antenna impedance changes from 23Ω to 60Ω at 18GHz, and the antenna is tuned at 18 GHz. The antenna pair gains at different separations are shown in Figure 5-18. For separations between 0.2 mm and 0.8 mm, the antenna pair gain drops by around 8 dB when the separation is doubled. The gain plots are quite smooth, and there are no dips. However, when the separation increases to 1.2 mm and 2.3 mm, the gain plots begin to fluctuate, and dips appear. Also, the gain drops for larger separation at higher frequency is smaller comparing to those at lower frequencies. At frequencies higher than 19 GHz, the antenna gain with 2.3mm separation is almost the same as that at 0.8-mm separation.

According to the earlier discussion, the antenna gain has to be greater than -28dB to make the system work. This means when the system is operating below 19 GHz, the maximum acceptable separation of the antenna pair is between 0.26mm to 0.52mm, which is far below the range expected in Chapter 2. However, if the system can be operated at 20 GHz, then the antenna pair can be separated with 2.3mm. Therefore, from the antenna per-

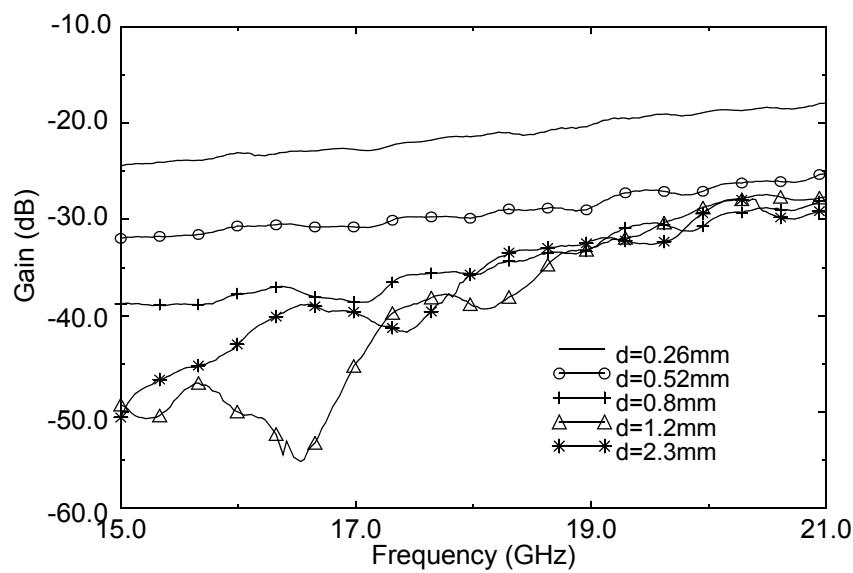


Figure 5-18 The gain of the cut antenna pair at varying separations.

formance point of view, it is beneficial to operate the system at frequencies higher than 20 GHz to reduce antenna loss and to increase the system working range.

5.2 System Demonstration

Following the characterization of different blocks, the system is demonstrated. Figure 5-19 shows the measurement board for the system demonstration (Appendix B). The transmitter and receiver are glued close to each other. The separation between the transmitting and receiving antenna are 0.26mm, and the antenna pair gain is -22 dB. The block diagram of measurement setup is shown in Figure 5-20. Instead of using the VCO (20~23GHz) on the transmitter to generate the global clock signal, a synthesizer is used to

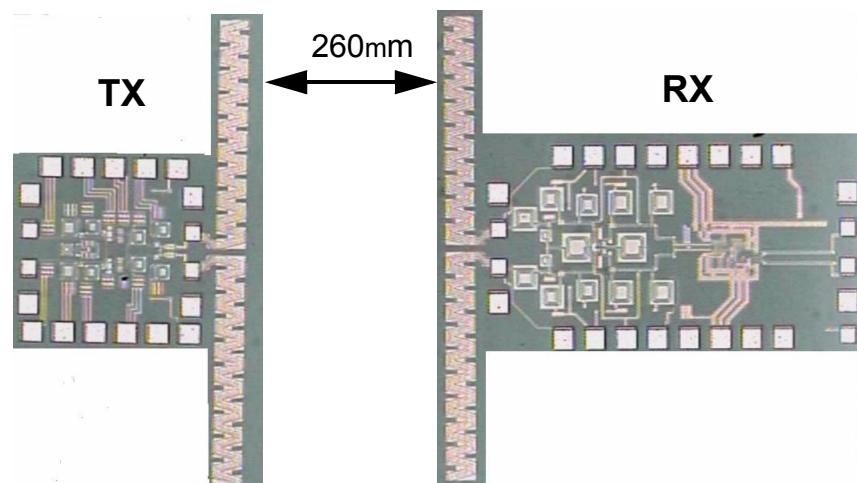
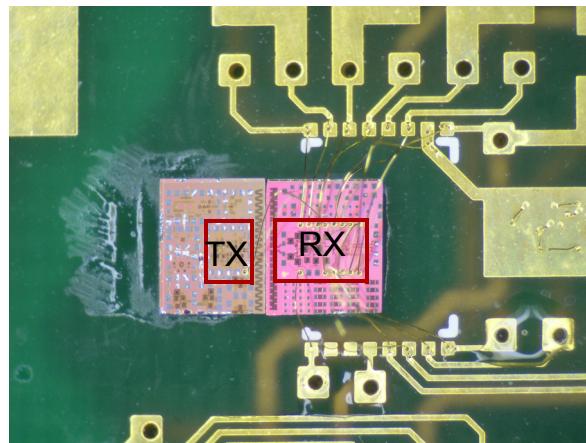


Figure 5-19 Photographs of the transmitter, receiver, and measurement board with a transmitter and a receiver.

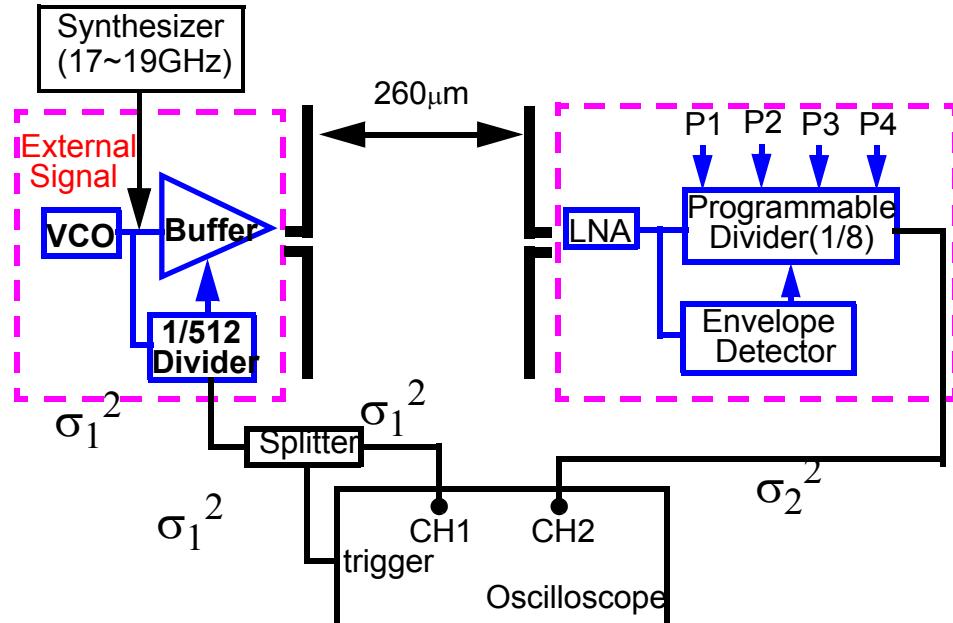


Figure 5-20 The block diagram of the system demonstration with one transmitter and one receiver.

provide the 17~19GHz clock signal. On the measurement board, the clock signal from the synthesizer and the DC power for the transmitter are fed using probes. The 1/512 divider in the transmitter generates the control signal to control the transmitter output buffer. The control signal is also used to trigger the Agilent 86100B wide-bandwidth oscilloscope, and is connected out using AC probes. On the receiver side, the DC power is fed through

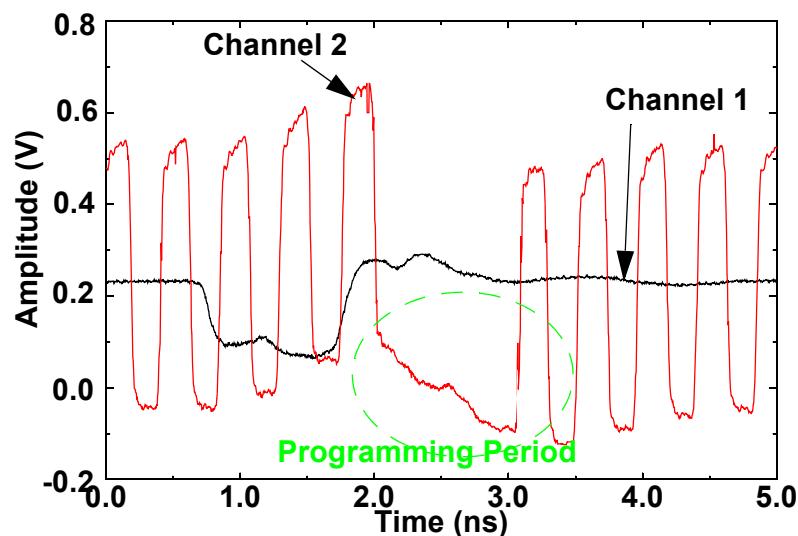


Figure 5-21 The output waveforms shown on an oscilloscope.

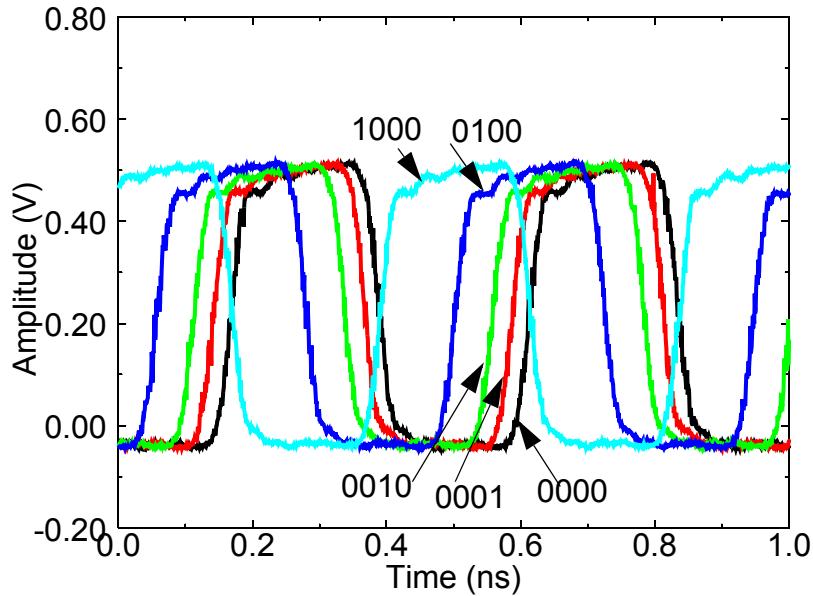


Figure 5-22 The output waveforms of the receiver for varying programming bit (P_4 , P_3 , P_2 , P_1) settings. The receiver is working at 18GHz.

bondwires on board, and the receiver output is connected out using a GSSG probe, and fed into the channel 2 of an oscilloscope. Figure 5-21 shows the signals on the oscilloscope channels 1 and 2. The channel 1 signal is the triggering signal generated by the transmitter. The signal on channel 2 is the receiver output signal. The input signal frequencies range is between 17 and 18.7 GHz. In Figure 5-21, the programming period when the receiver stops and then restarts after the falling edge of the INI signal is clearly shown. This result demonstrates that the antenna pair and receiver LNA bandwidths are broad enough that the no-transmission periods are preserved, and the detector successfully generates the INI signal from the no-transmission period to control the divider programming. During the programming period, the divider stops working and loads the programming bits ($P_1P_2P_3P_4$). After programming, the divider starts to count down the programmed value at the first crossing point of the clock signal, and then resumes the divide operation.

Figure 5-22 shows the transmitter output for varying programming bit ($P_1P_2P_3P_4$) settings. When the four programming bit settings change, the receiver output delay

changes. Table 5-2 shows the expected and measured delays of the receiver output when

Table 5-2 The expected and measured delays of programmable divider when the system is working at 18 GHz.

Programming (P ₄ P ₃ P ₂ P ₁)	0001	0010	0100	1000
Expected (ps)	222	111	55.5	27.5
Measured (ps)	220	109	55	24
Programming (P ₄ P ₃ P ₂ P ₁)	0001	0010	0100	1000

the receiver output V_{out}=0.3V. The system is working at 18 GHz. The differences between the expected and measured delays are less than 3.5ps. The cause of these differences is the same as the case for the divider characterization. It mainly comes from the jitter of the receiver output signal, and may also be caused by the receiver DC power supply drift.

Using the output of 1/512 divider (Figure 5-6) to trigger the oscilloscope, the measured RMS jitter of the channel 1 (triggering signal) is 1.91ps and the measured RMS jitter of the divider output signal is 1.83ps when the receiver is operating at 18GHz (Figure



Figure 5-23 The waveforms used to estimate jitter. Channel 1 (triggering signal) has 1.91ps RMS jitter and Channel 2 (receiver output) has 1.83ps.

5-23). Using the same method for estimating the RMS jitter of the programmable divider, the jitter for the receiver can be estimated. The jitter of the input signal from the synthesizer is quite small and once again can be ignored. Defining the RMS jitter of the triggering signal is σ_1 , and the RMS jitter of the receiver output is σ_2 (Figure 5-20), the measured RMS jitter of channel 1 (triggering signal) on the oscilloscope is $\sqrt{\sigma_1^2 + \sigma_1^2 + \sigma_0^2} = 1.91\text{ps}$, and the measured RMS jitter of receiver output is $\sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_0^2} = 1.83\text{ps}$ (Figure 5-20). Therefore, the The RMS jitter of the system, including the noise generated by the transmitter buffer, the receiver LNA and the programmable divider, can be obtained as $\sigma_2 = 0.9\text{ps}$. The peak-to-peak jitter is six times the RMS jitter, which is 5.4ps, or $\sim 1.21\%$ of a clock period. This is small.

Because of the limitation of the antenna pair separation, this system could not be used to measure skew among receivers. However, because of the programmable divider, the maximum skew of this system can be controlled within 1/16, or 6.25% of a period of the local clock signal.

Taking the intra-chip fabrication variation into consideration, the divider output signal in simulation is compared using typical, fast and slow transistor models. The skew caused by different transistor models is $\pm 30\text{ ps}$. However, this result over estimate the fabrication variation, because this transistor model variation is based on wafer to wafer and lot to lot variation. In a small chip with 310 mm^2 area, the transistor fabrication variation should be much smaller. Assume the fabrication variation within a small chip (310 mm^2) is 1/10th of the lot to lot variation, then the maximum skew caused by intra-chip fabrication variation is $\pm 3\text{ ps}$, or 1.35% of a local clock period. Changing the temperature by 10°C from 25°C to 35°C in simulation, the skew cause by this variation is 45 fs,

which is almost negligible. Therefore, the system total skew with intra-chip fabrication variation and temperature variation should be less than 8% of a local clock period.

Table 5-3 lists the comparison of jitter and skew performance between this wireless clock distribution system and other clock distribution systems. Although the

Table 5-3 The jitter and skew comparison between the wireless clock distribution system and other clock distribution systems.

Clock System	Working Frequency	Jitter (peak-to-peak jitter % in a clock period)	Skew
Low Power RF Clock Distribution [Ryu02]	5 GHz	peak-to-peak jitter=12ps (6%)	20ps (10%)
Coupled Standing-wave Oscillators [Mah03]	10 GHz	peak-to-peak jitter=4.8ps (4.8%)	4ps (4%)
Resonant Global Clock Distribution [Cha03]	1.1 GHz	cycle-to-cycle jitter=2ps (0.22%)	N.A.
Distributed PLL [Gut00]	1.1 GHz	cycle-to-cycle jitter=10ps (1.1%)	30ps (3.3%)
Wireless Clock Distribution (This Work)	2.25 GHz	peak-to-peak jitter=5.4ps (1.21%)	34ps (7.6%)

cycle-to-cycle jitter gives more optimistic estimation, it is assumed to be the same as the peak-to-peak jitter (Appendix E). The jitter performance is compared according to the percentage the jitter will occupy in a clock period. Among all the systems, the resonant global clock distribution system has the best jitter performance. The wireless clock distribution has similar jitter and skew performance as the system using distributed PLL, and better than the low power RF clock distribution system and the system using coupled standing-wave oscillators.

The power consumption of different blocks in the system is listed in Table 5-4. The power consumption of the receiver divider can be cut by half, because the power consumed by the buffer to drive the 50Ω load of the oscilloscope can be removed. Assuming that the antenna pair gain is sufficient to support operation at 1.0-cm separation, and using the configuration described in Chapter 1 (1 transmitter and 16 receivers to distribute the clock across 1.8cm x1.8cm chip area), then the total power consumption of the clock distribution system is 840mW.

Table 5-4 The power consumption of the different blocks in the system

	V_{dd} (V)	I (mA)	Power (mW)
Transmitter (without VCO)	1.2	34	40.8
Transmitter VCO	1.4	12	16.8
Receiver LNA	1.4	22	30.8
Receiver divider	1.472	27	39.7

Because of the larger than expected antenna pair loss and lower transmitter output power, the full system is demonstrated just for 0.26-mm separation between the transmitter and receiver. To demonstrate the system with a larger distance, an off-chip power amplifier (PA) is used to increase the transmitter output power to compensate the large antenna pair loss and low output power of transmitter. The setup is shown in Figure 5-24. In this setup, the transmitter board [Li05] output signal (16.59GHz) is fed into an off-chip PA. The PA output is used to drive a 3-mm zigzag on-chip antenna glued on the test board 2.5-mm away from the receiver. The P_{1dB} of the PA is 15dBm at 17 GHz. Subtracting the balun and the probe losses, the power fed into the 3-mm zigzag transmitting antenna is 11dBm, which is ~ 7 dB higher comparing to the case transmitter directly driving the on-chip antenna. Also, the use of a -mm zigzag transmitting antenna increases the antenna

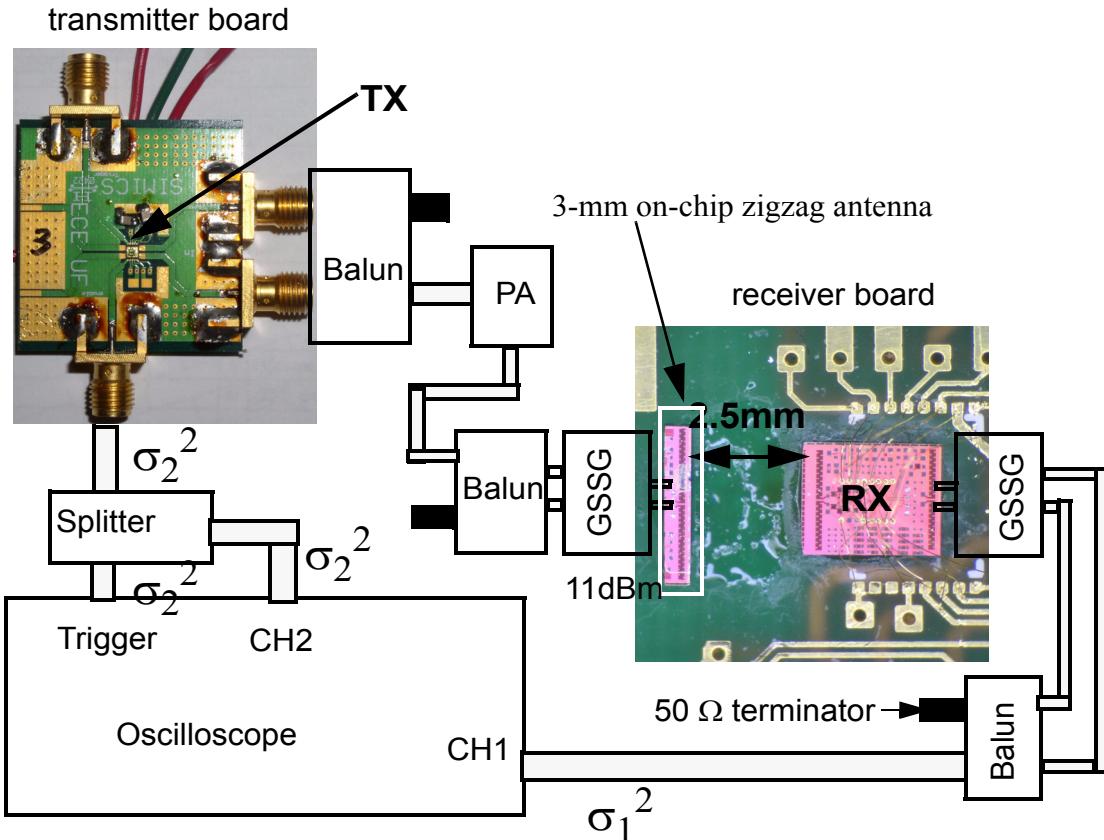


Figure 5-24 The measurement setup using an off-chip PA.

pair gain by another 2dB. Therefore, all together this system needs an antenna pair gain larger than -37 dB. This is ~9dB lower than the case transmitter directly driving the 2-mm on-chip antenna, and enables the system to work at a larger distance. The transmitter has an on-chip VCO working at 16.5 GHz with 200-MHz tuning range, which limits the frequency range of this system. The output signal of the receiver and the transmitter triggering signal are shown in Figure 5-25. Figure 5-26 shows the oscilloscope output used to estimate jitter. The RMS jitters of the channel 1 (receiver output) and channel 2 (triggering signal) are σ_1 and σ_2 , respectively (Figure 5-24). The measured RMS jitter of channel 2 (triggering signal) on the oscilloscope is $\sqrt{\sigma_2^2 + \sigma_2^2 + \sigma_o^2} = 3.23\text{ps}$, and the measured RMS jitter of the receiver output is $\sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_o^2} = 3.32\text{ps}$ (Figure

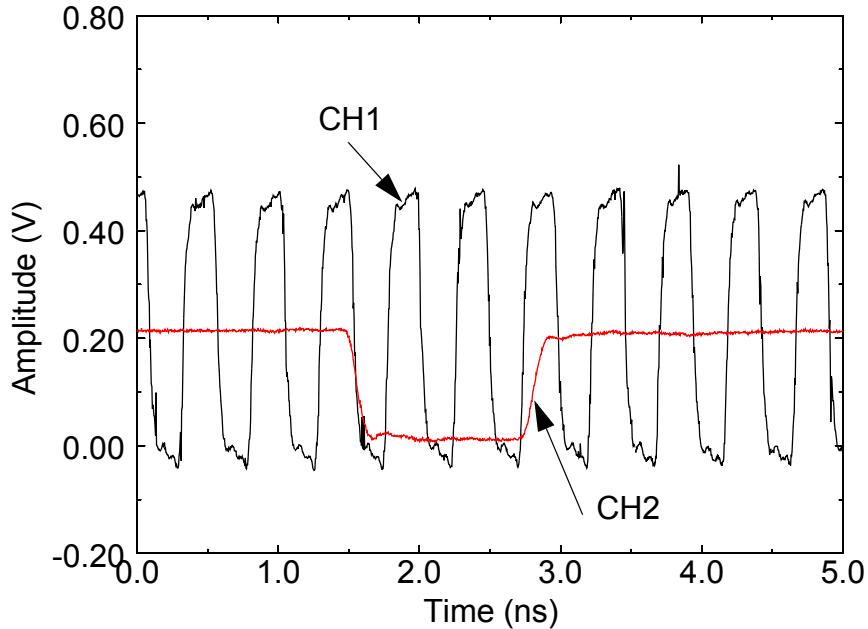


Figure 5-25 The receiver output and transmitter triggering signal waveforms when the system is operated with 2.5mm separation between the transmitting antenna and receiver and using an off-chip PA. The system is working at 16.59GHz.

5-24). Accordingly, the RMS jitter of the system, including the noise generated by the transmitter VCO, buffer, the off-chip PA, the receiver LNA and the programmable divider, is 2.25ps. And the peak-to-peak jitter is six times the RMS jitter, which is 13.5ps, or

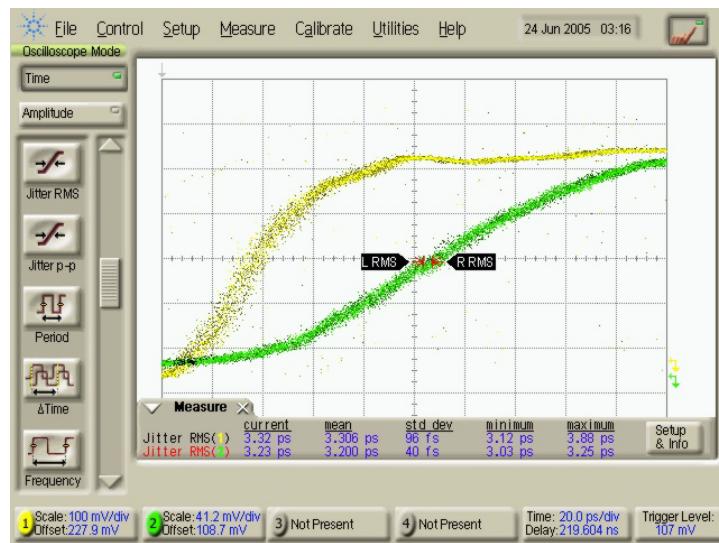


Figure 5-26 The waveforms used to estimate jitters. The RMS jitter of the channel 1 (receiver output) is 3.32ps and channel 2 (triggering signal) is 3.23ps.

~2.8% of a local clock period. Comparing to the system without the off-chip PA, the jitter is a little bit larger. This jitter difference is mainly caused by the jitter added by the off-chip PA which requires a large current (~800mA).

5.3 Methods to Increase System Working Range

As proposed in Chapter 1, for the intra-chip wireless clock distribution system to provide synchronized clock signal across a 18 mm by 18 mm microprocessor, the largest working distance between the transmitting antenna and receiver should be 9 mm. By using an off-chip PA to increase the transmitter output power from 4 dBm to 11 dBm, the largest working distance demonstrated is 2.5 mm, around 4 times smaller than the required distance.

From the discussion in Chapter 3, with the distance doubled, the antenna pair gain will decrease around 8 dB. Therefore, ~16-dB more power are needed in the system to work at 9-mm separation with 11 dBm transmitter output power. It is possible to increase the transmitter output power to 10 dBm [Cao05]. However, the system still needs ~17 dB more power to work at the 9-mm separation.

There are several approaches which can be used to increase the system power. First, two more stages can be added to the receiver LNA, increasing the LNA gain by another 14dB. However, this will increase the receiver power consumption by ~40%. The second method is to increase the system working frequency from 18 GHz to 20 GHz. The antenna pair gain can increase ~ 6 dB. In this system, the frequency limitation is mainly set by the programmable divider. However, divider frequency can be increased by using a more advanced CMOS technology, such as 90-nm technology. Third, backlapping the wafer can be used to achieve higher antenna pair gain. As discussed in Chapter 3, the

antenna pair gain improves \sim 10 dB at 20 GHz with 1-cm separation due to the wafer thinning from 650 μ m to 100 μ m. Although the chip we measured is already thinned to 250 μ m, the antenna pair gain can still be improved by thinning the chip to 100 μ m. Using the above three methods, more than 20 dB power increase can be achieved so that the system can work with 10-mm separation.

5.4 Summary

In this chapter, the intra-chip wireless clock distribution system implemented using the UMC 130nm CMOS technology is described. First, individual blocks in the system are characterized, and their operation is demonstrated. The programmability of divider in the receiver is successfully demonstrated, and the estimated peak-to-peak jitter of the divider is 2.6ps, or \sim 0.56% of a local clock period when the divider is working at 17 GHz. However, there exists a frequency mismatch between the transmitter maximum output power and the receiver LNA maximum gain frequencies. Also, the on-chip antenna pair gain is lower than expected by 8dB. Therefore, the largest working distance between the transmitter and the receiver is only 0.26mm.

With this 0.26-mm separation between the transmitter and receiver, the system is demonstrated on a printed circuit board. The working frequency range of the system is from 17 to 18.7 GHz. The system programmability to compensate the skew caused by the different distance from the receivers to the transmitter is demonstrated in this frequency range. The differences between the expected and measured delays are less than 3ps, which are mainly caused by the jitter of the receiver output signal, and the receiver DC power supply drift. The successful working of programmable divider limits the maximum skew of this system to within 1/16 (6.25%) of a local clock signal period. Adding skew caused

by the intra-chip fabrication variation and temperature variation (10°C), the total skew is 7.6% of a local clock period. Also the estimated peak-to-peak jitter of the system is 5.4ps, or $\sim 1.21\%$ of a local clock period when the divider is working at 18 GHz. Assuming that the antenna pair gain is big enough to support 1.0-cm separation, for the clock network described in Chapter 1 (1 transmitter and 16 receivers in an 1.8cm x1.8cm chip area), then the total power consumption of this clock distribution system is on the order of 1W, which is significantly lower than $\sim 180\text{W}$ power consumption of a microprocessor.

By using an off-chip PA which increases the transmitter output power to 11dBm, the system is demonstrated at 2.5-mm separation between the transmitting antenna and the receiver. The system works at 16.59GHz.

There are several methods can be used to increase the system working distance to 10mm, such as increasing the system working frequency, increasing the transmitter output power and LNA gain, and backlapping the wafer to 100 μm . The intra-chip wireless clock distribution is a practical clock distribution option for future microprocessors.

CHAPTER 6

SUMMARY AND SUGGESTIONS FOR FUTURE WORK

6.1 Summary

With increasing global clock frequency and chip size, clocking large digital chips with a single high-frequency global clock is becoming a more and more difficult task using the conventional clock distribution network. An intra-chip wireless clock distribution system has been demonstrated using the UMC 130-nm CMOS technology as an alternative approach for future clock distribution. In this clock distribution system, high frequency clock signal is transmitted through antenna pairs. To evaluate its feasibility, the techniques to synchronize this clock signals across the chip and to maintain the antenna pair gain in complex environments surrounded by metal structures are investigated.

In chapter 2, a synchronization scheme has been proposed to synchronize all the receivers in the chip. The transmitter generates the global clock signal (18 GHz) with a 2-ns no transmission period. The receiver detects this no transmission period, generates the INI signal to control a programmable divider. The falling edge of INI signal starts the divide by eight circuit to count down the pre-programmed delay at the first crossing point of the received clock signal. The divider programmable delay is used to compensate the static skew caused by the different distances to the receivers from the transmitter, and limits the skew within 1/16 of a local clock period.

In the intra-chip wireless clock distribution system, the antenna pair gain is one of the determining factors for the feasibility of the whole system. The on-chip antenna pairs

are in complex environments surrounded by various metal structures, which can significantly affect the antenna pair gain. Among these metal structures, the most typical and significant metal structures are the heatsink and the metal lines near the on-chip antenna. Most of them can severely reduce the antenna gain, and making the system realization more difficult. Therefore, in Chapter 3, methods to reduce these effects are discussed. To reduce the heatsink effects on antenna pair gain, AlN, an insulator with high thermal conductivity, is inserted between the heatsink and the wafer containing the antenna pair. Measurements show that AlN can help to increase the antenna pair gain by $\sim 8\text{dB}$, while maintaining the good thermal conductivity between the heatsink and backside of the wafer. To characterize the antenna pair gain with metal lines between the antenna pair or above the on-chip antenna, test structures are fabricated. Based on the characterization of antenna gains of the structures with those metal interfering structures, a set of design guidelines are proposed to reduce the effects of metal interference structures on antenna pair performance.

In this intra-chip wireless clock distribution system, both the antenna pair and LNA of the receiver should be broadband to preserve the 2-ns no transmission period of transmitted signal. The antenna pair is broadband due to the loss associated with substrate, and should not significantly distort the no transmission period of transmitted signal. Therefore, the LNA between the receiving antenna and detector should be broadband to preserve the no transmission period. The design and measurement results of a 20-GHz broadband LNA are presented in Chapter 4. This LNA is a differential two-stage cascode amplifier with inductive degeneration at the source. The amplifier is fully integrated including the input and output matching networks. At $V_{dd}=1.2\text{ V}$ and 20 mA bias current,

the LNA has 9 dB transducer gain peaking at 20 GHz, and the amplifier has 5.3-GHz 3-dB bandwidth. The noise figure at 20 GHz is 5.5dB, with -2dBm P_{1dB} and -4dBm IIP₃.

In Chapter 5, the individual working blocks in the system (transmitter, antenna pair, receiver), and the entire system are demonstrated. Because of the low antenna pair gain, the system is first demonstrated with 0.26-mm separation between the antenna pair without using an off-chip power amplifier. The system works from 17 GHz to 18.7 GHz. The RMS jitter of the system, including the noise generated by the transmitter buffer, the receiver LNA and programmable divider, is 0.9ps. And the peak-to-peak jitter is six times the RMS jitter, which is 5.4ps, or ~1.21% of a local clock period. The programming bits of the divider (P₁, P₂, P₃, P₄) set the delay of the divider to $n \times \frac{1}{16}$ of a local clock period, where n=1,2,...,15. This enables compensation of the static skew in the wireless clock distribution system caused by different distances to the transmitter and the different metal structures between the transmitting and receiving antenna. This programmability of the divider delay is successfully demonstrated when the system is working at 18 GHz. The differences between the expected and the measured delays due to the accuracy limitation of the oscilloscope are less than 3.5ps. The power consumption of transmitter and receiver are 41mW and 70mW, respectively. Due to the gain limitation of the antenna pair, the largest working distance of this system is only 0.26mm now. Because of this limitation, the skew among multiple receivers could not be measured. However, the programmability of the divider delay is successfully demonstrated. This means that if the antenna gain limitation is removed, then the maximum skew of this system should be less than 1/16 (6.25%) of a local clock period. Adding skew caused by the intra-chip fabrication variation and temperature variation (10°C), the total skew is 7.6% of a lock clock period. To increase the

system working distance, an off-chip power amplifier is used to increase the transmitted output power from 4 to 11 dBm. The largest distance over which the system can work is 2.5mm at 16.59 GHz. The peak-to-peak jitter is 2.8% of a local clock period. The total timing uncertainty is 10.4% when the skew is added.

These measurements demonstrate the synchronization scheme of the intra-chip wireless clock distribution system, and indicate that after increasing the system working frequency to 20 GHz, the transmitter output power to 10 dBm, LNA gain by another 14dB, and backlapping the wafer to 100 μ m, it should be possible to increase the working distance between the transmitter and receiver to more than 10mm. This clock distribution system is a realistic option for the future microprocessors.

6.2 Suggestions for Future Work

Presently, the main problem is the short working distance between the transmitter and receiver. Because of the power limitation, the largest distance the system can work now is only 0.26mm, while the system need to work at least up to 9mm. Therefore, future work should focus on increasing the working distance between the transmitter and receiver.

Optimize on-chip antenna performance. A major reason for the short working distance is the low gain of the on-chip antenna pair. In our previous studies of the on-chip antenna, they were all fabricated on uniformly doped substrates. There were no p-wells n-wells, and the fabrication process allow either wider metal lines or smaller separation between the wide metal lines. However, in the 130-nm CMOS standard process, the surface of substrate contains p and n-wells with lower resistivity. Also, the wide metal lines must be broken into multiple stripes with bigger spacing (4 μ m). Because of these two

limitations, the antenna pair gain is much less than the ones formed on uniformly doped substrates and the characteristics of the antenna performance are changed. Therefore, on-chip antenna design should be optimized in the presence of n and p-wells to increase the antenna pair gain. Also, thinning the wafer to 100 μm could be considered in the process to increase the antenna pair gain.

Increase system working frequency. The main benefit of increasing the working frequency is that the antenna gain increases with the increase of the frequency. Now the system is working at 18GHz. The transmitter VCO and output buffer, and the receiver LNA can be tuned to a higher frequency. The frequency limitation is mainly set by the programmable divider. To increase the working frequency, the divider design should be improved.

Match the working frequencies of the transmitter and receiver. The mismatch among the transmitter VCO tuning frequency (20GHz), the frequency of the transmitter output buffer maximum output power (17GHz), the frequency of LNA maximum gain (19GHz), and the divider working frequency range (17GHz ~ 18.7 GHz) is another reason for the short working distance. If the operating frequencies of these blocks can be made the same, the power limitation can be alleviated.

Increase receiver LNA gain. On the receiver side, the LNA gain is still low. Even after modification, the maximum LNA gain is only \sim 14dB at 19 GHz. If this gain can be increased by another 6 to 10 dB, the system will work at larger distance (\sim 6mm). The easy way is to cascade another one or two amplifying stages. However, this will increase the receiver power consumption around 40% and potentially reduce the bandwidth. There-

fore, methods to increase the LNA gain without significantly increasing the receiver power consumption are needed.

Increase the transmitter output power. The transmitter output power is still low (4dBm). It should be possible to increase the transmitter output power to \sim 10dBm [Cao05].

Fine adjustment of the divider programmable delay. Comparing to the other newly proposed clock distribution systems, the jitter is small, but the skew is still too high (7.6% of a clock period) due to the limitation of divider programmable delay (1/16th of a clock period). New methods for more finely adjusting the programmable delay to decrease the system skew are needed to make the total time uncertainty smaller.

APPENDIX A
THE RELATION BETWEEN THE QUALITY FACTOR OF SERIES RLC CIR-
CUIT AND THE CURRENT RESPONSE SETTLING TIME

This section analyzes the current response of a series RLC circuit (Figure A-1) with a voltage source $V(t) = \sin\omega t \times u(t)$, where $u(t)=1$ when $t>0$. In particular, the relation between the quality factor (Q) and the current response settling time of this RLC circuit is derived.

The current in this circuit satisfies equation A.1

$$L \times \frac{di(t)}{dt} + R \times i(t) + \frac{1}{C} \times \int_{-\infty}^t i(\lambda) d\lambda = \sin\omega t \quad t>0 \quad (\text{A.1})$$

The steady-state response is $i_p(t) = a_1 \times e^{j\omega t} + a_2 \times e^{-j\omega t}$. By substituting this into Equation (A.1),

$$a_1 = \frac{1}{2 \times (j\omega R - \omega^2 L + \frac{1}{C})} \text{ and } a_2 = \frac{1}{2 \times (-j\omega R - \omega^2 L + \frac{1}{C})}$$

When ω is the resonant frequency of this RLC circuit, $\omega_0 = \sqrt{\frac{1}{LC}}$,
 $i_p(t) = \frac{\sin\omega t}{R}$.

The characteristic equation of (A.1) is

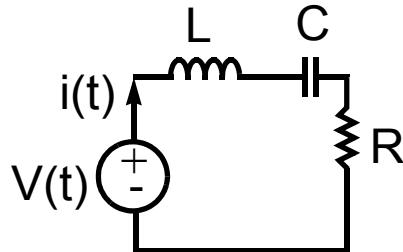


Figure A-1 A series RLC circuit with a voltage source.

$$L \times s^2 + R \times s + \frac{1}{C} = 0$$

and the roots are

$$s_{1,2} = \frac{-R \pm \sqrt{R^2 - \frac{4L}{C}}}{2L}$$

so the complete response is

$$i(t) = \frac{\sin \omega t}{R} + A_1 e^{s_1 t} + A_2 e^{s_2 t}$$

Because the voltage source $V(t)$ is zero for $t < 0$, therefore, $i(0^+) = 0$, and $\frac{d}{dt}i(t)|_{t=0} = 0$. After evaluating $i(t)$ for these two conditions,

$$A_1 + A_2 = 0 \quad \text{and} \quad \frac{1}{R} + A_1 s_1 + A_2 s_2 = 0$$

Therefore we get $A_1 = -\frac{L}{R^2 \sqrt{1-4Q^2}}$ and $A_2 = \frac{L}{R^2 \sqrt{1-4Q^2}}$, where $Q = \frac{j\omega_0 L}{R} = \frac{1}{j\omega_0 CR}$.

The complete response of this series RLC circuit is

$$i(t) = \frac{\sin \omega t}{R} - \frac{L}{R^2 \sqrt{4Q^2 - 1}} e^{-\frac{\omega t}{2Q}} \sin\left(\frac{\sqrt{4Q^2 - 1}}{2Q} \omega t\right) \quad \text{when } Q > 1/2$$

Analyzing this equation, the last part is a sine wave with a damping factor $e^{-\frac{\omega t}{2Q}}$. The larger the Q , the slower this sine wave amplitude goes down, and the slower $i(t)$ reaches the steady-state response $\frac{\sin \omega t}{R}$.

The settling time of this RLC circuit is defined as the time before the system operates in the steady state, when $i(t)$ reaches the 90% of the full swing of the sinusoidal steady-state response $\frac{\sin \omega t}{R}$. At settling time, $e^{-\frac{\omega t}{2Q}} = 0.1$ is approximately equal to 0.1, or $t_s = \frac{\ln(0.1)Q}{\pi f} = 0.74QT$, where T is the period of the resonant frequency.

APPENDIX B BOARD DESIGN FOR SYSTEM DEMONSTRATION

This section discusses the design of a receiver board for system demonstration. A photograph of the receiver board is shown in Figure B-1. This board is mainly used to provide the DC power supply to one transmitter and two receivers glued on the board. This board is 1.5 inch by 1.5 inch, with three layers of metal. The metal layers are 1 oz. copper, which translate to 1.4-mil or 36- μ m thickness. Between the metal layers are 10mil FR4 (Figure B-2). Because on this board, there is no high frequency transmission lines, FR4 is

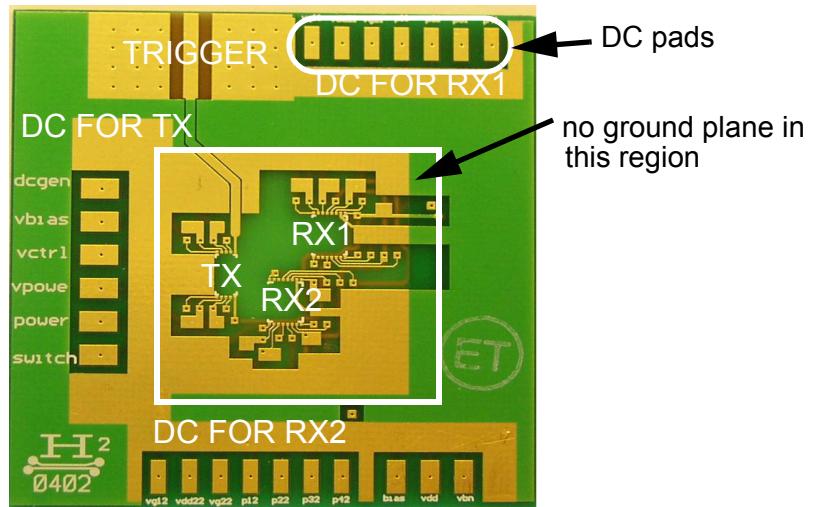


Figure B-1 A photography of the measurement board.

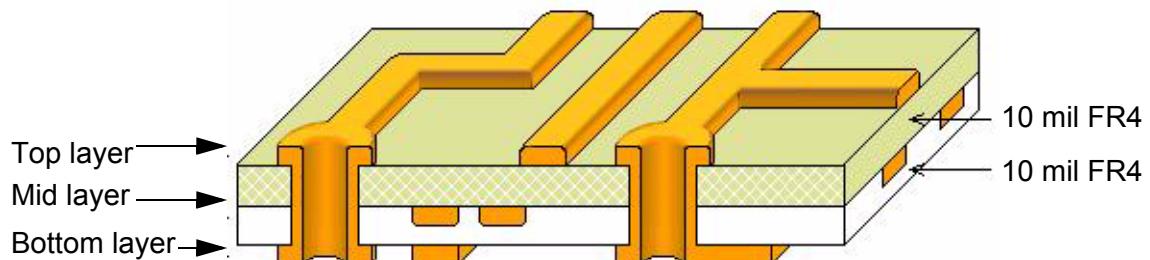


Figure B-2 The stack structure of the measurement board.

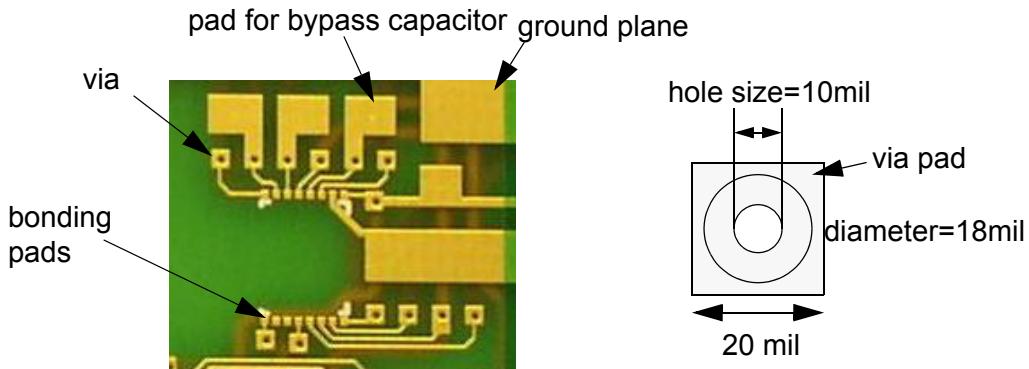


Figure B-3 The bonding pads layout for a receiver and the parameters of a top layer to bottom layer via.

acceptable. The top layer metal is used to place the bonding pads and DC pads, the middle layer is used to provide a ground plane, and the bottom layer is used to provide routing from bonding pads to DC pads (Figure B-1). Because metal structures close to the antenna pair will degrade the antenna pair gain, there is no ground plane between and below the transmitter and two receivers. There is a hole on the ground plane (mid layer) below and between the transmitter and two receivers (Figure B-1).

1. Bonding pads, vias and DC pads

The bonding pads shown in Figure B-3 are used for wire bonding. The size of the bonding pads are 8 mil by 8 mil with 4 mil separation. 4 mil wide metal lines connect these bonding pads out to a top-to-bottom via. Through these vias, the lines are connected to the metal lines on the bottom layer. These lines are routed out, and connected to the top layer DC pads using another set of vias. The hole size of vias are 10 mil, with an 18-mil diameter (Figure B-3). The size of the hole depends on the board thickness. The thicker the board, the larger the hole size. Also, some bonding pads are connected to large metal blocks close to a ground plane on the top layer. These large metal blocks are used to solder down the bypass capacitors between the bonding pads and ground plane (Figure B-3).

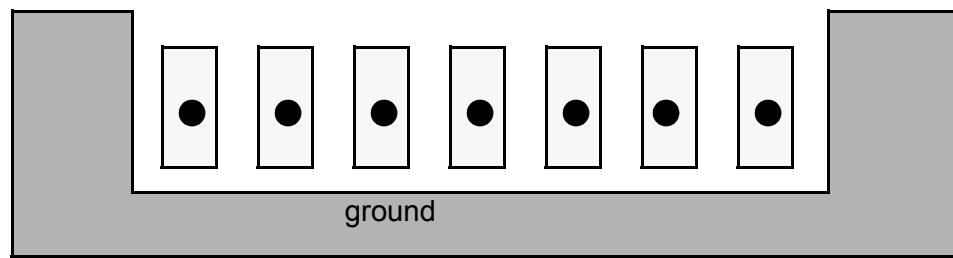


Figure B-4 The layout of DC pads surrounded by ground.

The layout of the top layer DC pads are shown in Figure B-4. These DC pads are used to solder the wires on the board. Surrounding these DC pads are ground planes. Bypass capacitors could be soldered between the DC pads and ground.

2. Transmission line and SMA pad

There is one transmission line connecting the triggering signal generated by the transmitter to an SMA connector mounted on a board. The frequency of this signal is ~ 30 MHz. The cross section of the transmission line is shown in Figure B-5. This transmission design is based on the simulation result of Advanced Design System (ADS) from Agilent. The layout of the pad for SMA connector is shown in Figure B-6. The pad dimensions are decided based on the size of an end-launch SMA plug receptacle 142-0701-881 from Johnson Components (Figure B-6(c)).

3. Bonding pads and their corresponding DC and SMA pads

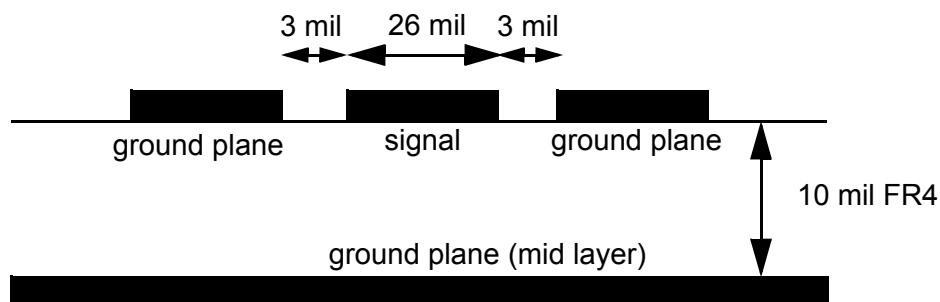


Figure B-5 Cross section of the transmission line on the board.

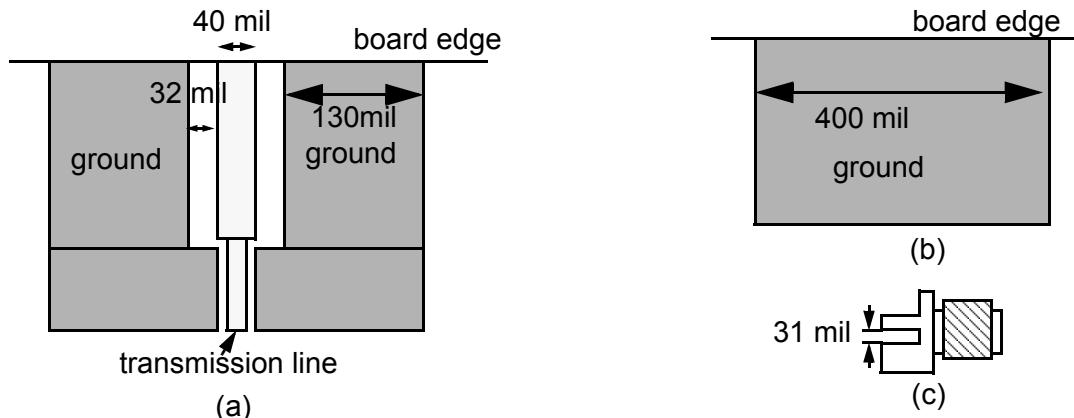


Figure B-6 The SMA pad and connector. (a) The SMA pad layout on top layer. (b) The SMA pad layout on bottom layer. (c) An end launch SMA plug receptacle for board mounting.

The bonding pads for the transmitter and receivers are shown in Figure B-7. Their corresponding DC and SMA pads are also shown in Figure B-8. When bonding pads have the same name, they are actually connected through metal lines on board, such as EN signal.

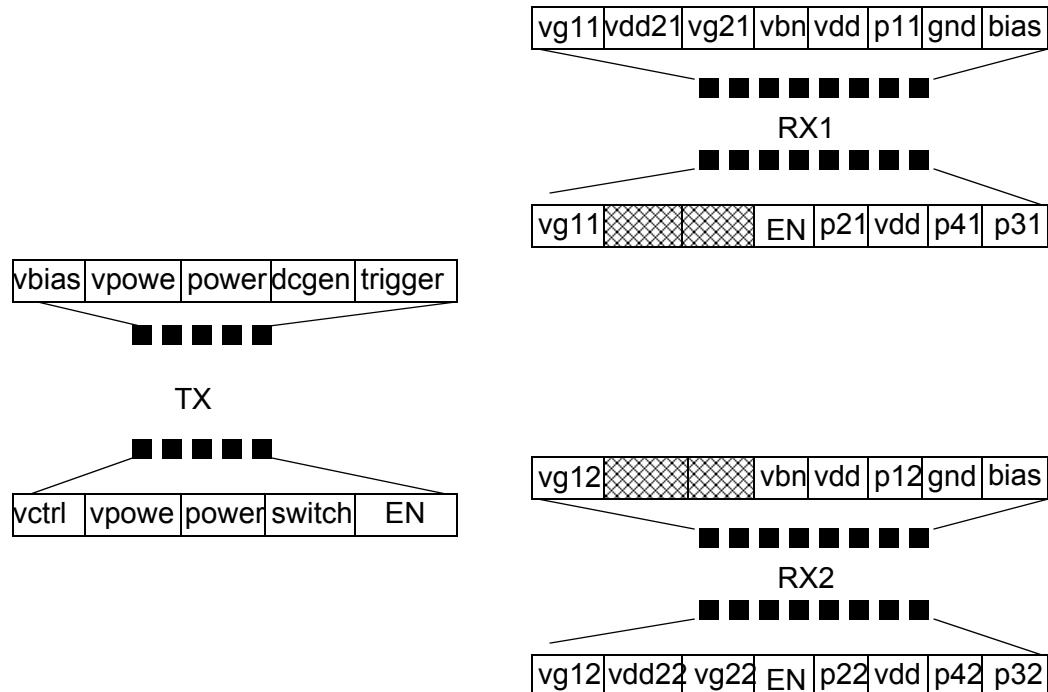


Figure B-7 The bonding pad layout for one transmitter and two receivers.

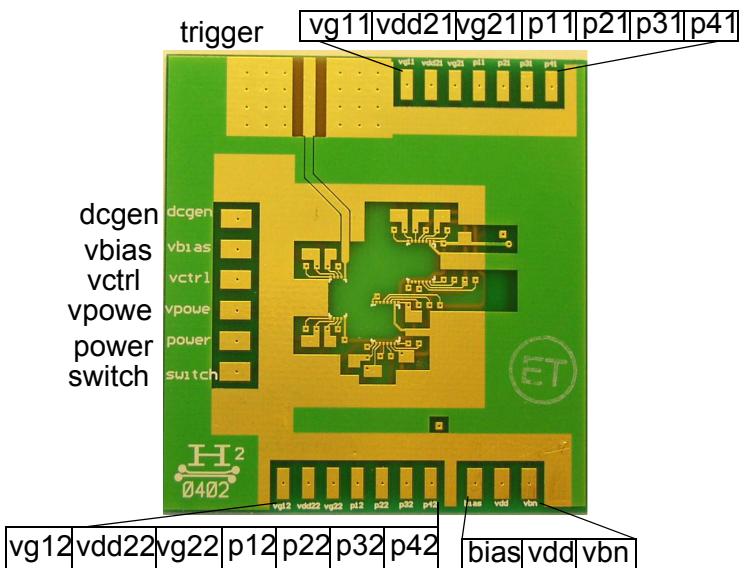


Figure B-8 The DC pads for transmitter and receivers on the measurement board.

APPENDIX C

THREE-METAL-LAYER ANTENNA FABRICATION PROCEDURE

This section describes the fabrication process for the three-metal-layer on-chip antenna in the Microelectronics Lab at the University of Florida. To stack three metal layers, align masks shown in Figure B-1 are used to align different layers.

1. Deposit $1.0\mu\text{m}$ SiO_2 using Chemical Vapor Deposition (CVD) machine on silicon wafer.
2. Photolithography
 - (1) Place a wafer on the spinner, apply photo resist AZ1529, and spin the wafer at 4000 RPM for 50 seconds. The wafer is then covered with a $2\text{-}\mu\text{m}$ thick photo resist layer.
 - (2) Place a wafer into the oven for soft bake: 80°C for 30 minutes.

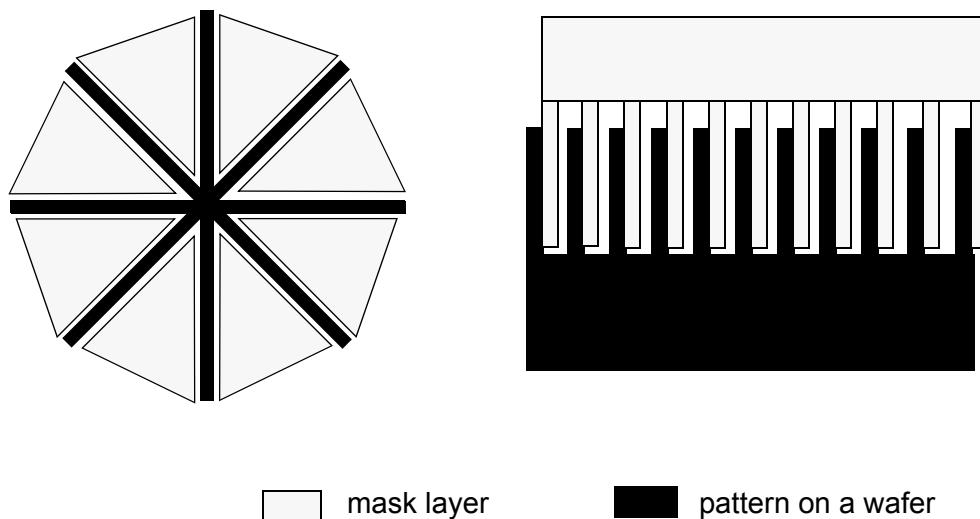


Figure C-1 The layout of alignment marks on a mask and a pattern on a wafer.

- (3) Align the mask for contact layer with the wafer. Then expose the wafer using the mask aligner: expose for 17 seconds.
- (4) Develop the wafer using developer (MR312 1:1.2) for 40 seconds. Make sure that all the photo resist on the exposed area are removed. After development, wash the wafer in DI water, and dry it using nitrogen.
- (5) Inspect the wafer using a microscope. If the photo resist lines are broken, or not properly aligned, the photo resist has to be removed using Acetone and repeat from the photolithography step (1).
- (5) Put wafer into oven for hard bake: 110°C, 20 minutes.
3. Remove the SiO₂ using SiO₂ etchant. Wear all the protection gear, including the helmet. This etchant is very dangerous. Put a small silicon wafer with the same thickness of SiO₂ layer in the etchant at the same time. When the water does not stick on the wafer, the SiO₂ is completely removed.
4. Deposition Aluminum using an e-beam machine. The instructions are on the machine. Every time, one crucible containing a small piece of Aluminum is used. The typical deposition thickness of Aluminum with one crucible is ranging from 0.5μm to 0.8μm. Using two crucibles, the deposition thickness of the aluminum layer is from 1.0μm to 1.6μm.
5. Repeat the photolithography step. The mask used is the metal 1 layer mask. Make sure that the alignment marks on the mask is aligned with the contact pattern on the wafer (Figure B-1).
6. Aluminum etching

(1) Put the wafer into the aluminum etchant for about 30 minutes (for $1.6\mu\text{m}$ thick aluminum). When the area not covered by photo resist is turning black, that means the aluminum is removed and the SiO_2 is exposed.

(2) Rinse the wafer using DI water and inspect the wafer using a microscope. If Aluminum is not removed completely, put the wafer back into the etchant for another 10 to 20 seconds, then rinse and inspect until the aluminum is removed completely.

(3) Remove photo resist using acetone. Rinse in DI water, and dry the wafer using N_2 .

7. Deposit $1.0\text{-}\mu\text{m}$ SiO_2 using Chemical Vapor Deposition (CVD) machine.

8. Repeat the photolithography step. The mask used is the mask for Via12. Make sure that the alignment marks on the mask is aligned with the metal 1 pattern on the wafer.

9. Remove the SiO_2 using SiO_2 etchant. Wear all the protection gear, including the helmet. This etchant is very dangerous. As before, put a small silicon wafer with the same thickness of SiO_2 layer in the etchant at the same time. When the water does not stick on the wafer, the SiO_2 is completely removed. Land the probes on the two pads at the ends of a metal lines to check the resistivity to make sure that the SiO_2 layer on pads are removed (Figure B-2).

10. Deposit Aluminum for metal 2 using an e-beam machine.



Figure C-2 The metal structure for checking the via opening.

11. Repeat the photolithography step. The mask used is the mask for metal 2 layer. Make sure that the alignment marks on the mask is aligned with the pattern on the wafer (Figure B-1).
12. Aluminum etching using the aluminum etchant.
13. Deposit $1.0\mu\text{m}$ SiO_2 using Chemical Vapor Deposition (CVD) machine.
14. Repeat the photolithography step. The mask used is the mask for Via23. Make sure that the alignment marks on the mask is aligned with the pattern on the wafer.
15. Remove the SiO_2 using SiO_2 etchant. Wear all the protection gear, including the helmet. This etchant is very dangerous. Put a small silicon wafer with the same thickness of SiO_2 layer in the etchant at the same time. When the water does not stick on the wafer, the SiO_2 is completely removed. Land the probes on the two pads at the ends of a metal lines to check the resistivity to make sure that the SiO_2 layer on pads are removed (Figure B-2).
16. Deposit Aluminum for metal 3 using an e-beam machine.
17. Repeat the photolithography step. The mask used is the mask for metal 3 layer. Make sure that the alignment marks on the mask is aligned with the pattern on the wafer (Figure B-1).
18. Aluminum etching using the aluminum etchant.

APPENDIX D

MEASUREMENT PROCESS OF DIFFERENTIAL LNA ABOVE 20 GHZ

This section discusses the measurement procedure of the differential LNA above 20 GHz. Figure D-1 shows the LNA noise measurement setup. In this setup, a balun is used to provide the differential signal to the LNA input and transform the LNA differential output signal into single-ended signal. The noise source is connected to the LNA input pads through a balun and a GSSG probe, and LNA output is connected to the noise figure meter measuring port through another set of GSSG probe and balun. Here the balun and GSSG probe have significant loss (3~4dB) around 20 GHz.

First, the noise source is directly connected to the noise figure meter measuring port for calibration. After completing this, the meter is calibrated to the noise source output port (interface A in Figure D-1). Therefore, the noise figure measured in the setup in Figure D-1 is the noise figure of the whole system, including the input balun and GSSG probe, the LNA, and the output balun plus GSSG probe. To obtain the LNA noise figure,

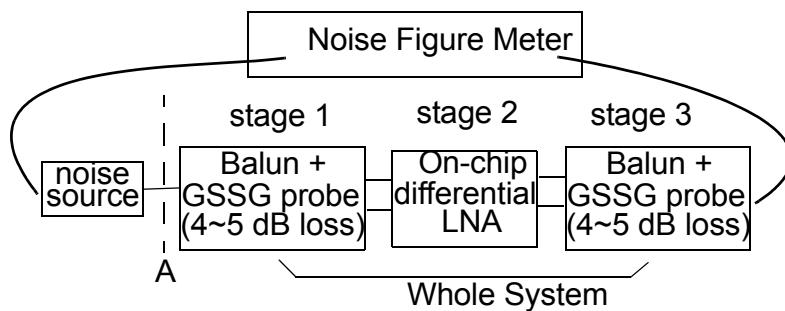


Figure D-1 Noise figure setup for on-chip differential LNA's.

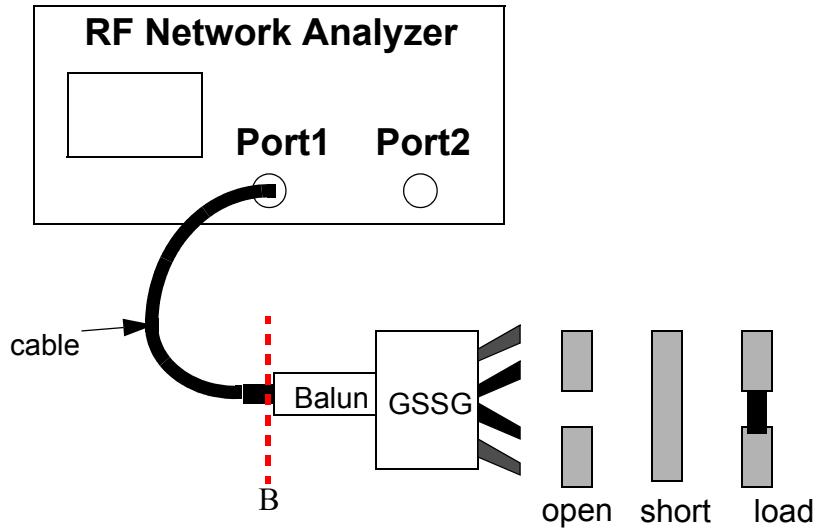


Figure D-2 The characterization setup for balun plus GSSG probe using network analyzer.

the noise added by input balun plus GSSG probe (stage 1 in Figure D-1), and the output balun plus GSSG probe (stage 3 in Figure D-1) must be de-embedded.

A network analyzer is used for the characterization of the two stages. Figure D-2 shows the characterization setup. The purpose of this setup is to separately measure the S-parameters of the two stages. First, the network analyzer is calibrated to the cable output (Interface B in Figure D-2) using the 3.5-mm calibration. After that, the cable output is connected to the balun plus the GSSG probe. The GSSG probe was connected to the short, open and load structures of the GGB calibration substrate to obtain three input reflection coefficients:

$$\Gamma_{in(open)} = S_{11} + \frac{S_{12}S_{21}}{1 - S_{22}} \quad (D.1)$$

$$\Gamma_{in(short)} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \quad (D.2)$$

$$\Gamma_{in(load)} = S_{11} \quad (D.3)$$

From the above three equations, the S-parameters of the balun plus GSSG probe can be obtained.

$$S_{22} = \frac{\Gamma_{in(open)} + \Gamma_{in(short)} - 2S_{11}}{\Gamma_{in(open)} - \Gamma_{in(short)}} \quad (D.4)$$

$$S_{12}S_{21} = (\Gamma_{in(open)} - S_{11}) \frac{2[S_{11} - \Gamma_{in(short)}]}{\Gamma_{in(open)} - \Gamma_{in(short)}} \quad (D.5)$$

Because S_{12} is equal to S_{21} for passive networks [Poz98], the four S-parameter are obtained for stage 1. The same process is used to obtain the S-parameters of stage 3.

After obtaining the S-parameter of 2 stages, the available power gain G_a of the two stages can be calculated.

$$G_a = \frac{1 - |\Gamma_s|^2}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{out}|^2} \quad (D.6)$$

where

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0}, \quad (D.7)$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (D.8)$$

and

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (D.9)$$

Here, $Z_s = Z_L = Z_0 = 50\Omega$. At the same time, since the stage 1 and stage 3 are lossy network, their noise factor F are equal to $\frac{1}{G_a}$. Also, the S-parameters of LNA can be obtained using the network analyzer. Using the equation

$$F_{total} = F_1(Z_s = Z_0) + \frac{F_2(Z_s = Z_{out1}) - 1}{G_{a1}} + \frac{F_3(Z_s = Z_{out2}) - 1}{G_{a1}G_{a2}} \quad (D.10)$$

the noise factor of the LNA (F_2) can be obtained. Here F_{total} is the total noise factor measured by the noise figure meter. F_1 is the noise factor of stage 1, G_{a1} is the available power gain of stage 1, G_{a2} is the available power gain of LNA, F_3 is the noise factor of stage 3. Z_{out1} is the output impedance of the first stage, and Z_{out2} is the output impedance of the second stage (LNA). Shown in Figure D-3 is the S_{11} and S_{22} of the GSSG probe and balun. Since they are all below -10dB in the measurement frequency range, the GSSG probe and balun are almost matched to 50Ω , and Z_{out1} can be assumed to be the same as $Z_0=50\Omega$. Also in the frequency range, the output impedance of LNA is also matched to 50Ω , therefore, $Z_{out2}=50\Omega$.

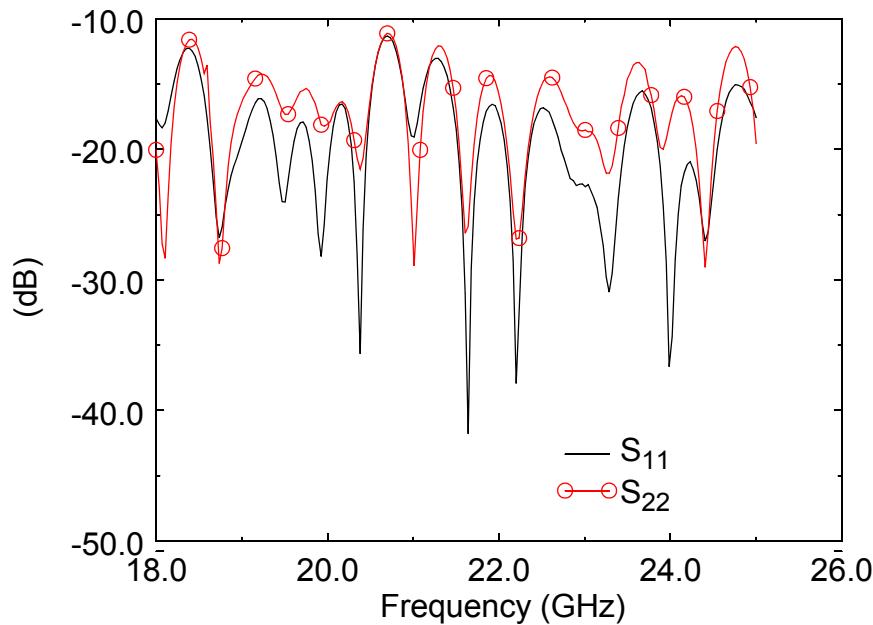


Figure D-3 S_{11} and S_{22} of the GSSG probe and balun.

APPENDIX E

JITTER DEFINITION AND MEASUREMENTS

1. Jitter Definition

Jitter is short-term variation of the significant instance of a digital signal from their ideal positions in time. It is expressed in units of time describes the magnitude of the jitter in appropriate orders of magnitude, usually picoseconds. Period jitter and cycle-to-cycle jitter are the most widely used and understood.

a) Period jitter is a standard measurement for divider. The period jitter consists of peak-to-peak jitter and RMS (Root Mean Squared) period jitter. The peak-to-peak period jitter is the difference between the maximum and minimum periods of a signal. The RMS period jitter is the standard deviation of the peak-to-peak period jitter. The peak-to-peak jitter is approximately 6~7 times the RMS value.

(b) Cycle-to-cycle jitter is the difference between two adjacent cycles of the signal. The peak-to-peak jitter is the worst case of cycle-to-cycle jitter.

2. Jitter Measurement

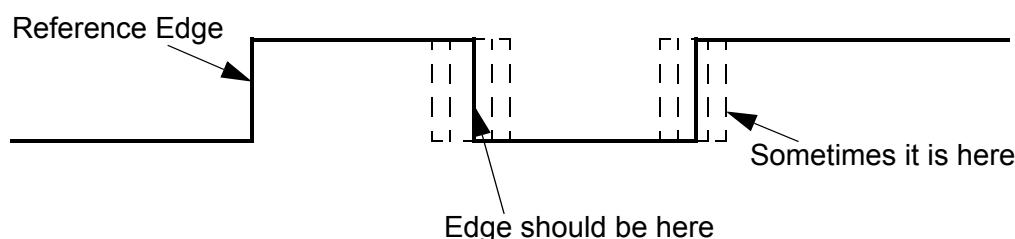


Figure E-1 Digital waveform with jitter.

A true measure of clock jitter is the measurement of accurate positions of clock edges over time. The most direct method of examining the placement of edges would be to look at the edges using an oscilloscope. Unfortunately, using standard oscilloscopes, it is impossible to determine the location of edges in absolute time. Any jitter measured with a standard oscilloscope is affected by the trigger instability. Therefore, the jitter however can be estimated using the method below. The total jitter measured using an oscilloscope is a sum of device jitter, trigger jitter and the oscilloscope jitter.

$$(Device\ Jitter)^2 = (Total\ Jitter)^2 - (Oscillator\ Jitter)^2 - (Trigger\ Jitter)^2 \quad (C.1)$$

Oscillator Jitter = Oscillator characteristic jitter

Device Jitter = Jitter of the device under test

Total Jitter = Total measured jitter

Trigger Jitter = Jitter of the test equipment

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BIOGRAPHICAL SKETCH

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