AXI4-ST-Duplex User Guide

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Glossary

Abbreviation	Description
M2S	Master-to-Slave / Leader-to-Follower
S2M	Slave-to-Master / Follower-to-Leader

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1 Introduction

1.1 Purpose

This document explains how AXI4-ST Duplex functions and serves as an addendum user guide for AXI4-ST Logic Link located in axi4-st/doc.

1.2 Notational Conventions

The following notational conventions are used in this document.

Notation	Description

2 AXI4-ST Duplex

2.1 Theory

AXI-ST Duplex consists of two AXI-ST Logic Links called “ST_M2S” (Leader-to-Follower llink) and “ST_S2M” (Follower-to-Leader llink) which are complementary to each other only in terms of direction of flow of data and flow-control between Leader and Follower: The ST_M2S Logic Link, like the existing “ST” Logic Link, enables data flow from Leader DUT to Follower DUT, whereas the ST_S2M Logic Link enables data flow from Follower DUT to Leader DUT. All the features that apply to AXI-ST Logic Link applies to AXI-ST-Duplex Logic Links as well [1]

```
llink ST_M2S
{
TX_FIFO_DEPTH            1
RX_FIFO_DEPTH            40
output user_m2s_tkeep    8
output user_m2s_tdata    64
output user_m2s_tvalid   valid
input user_m2s_tready    ready
}

llink ST_S2M
{
TX_FIFO_DEPTH            1
RX_FIFO_DEPTH            40
input user_s2m_tkeep     8
input user_s2m_tdata     64
input user_s2m_tvalid    valid
output user_s2m_tready   ready
}
```

As can be seen, direction of interface signals of ST_M2S and ST_S2M Logic Links are complementary to each other:

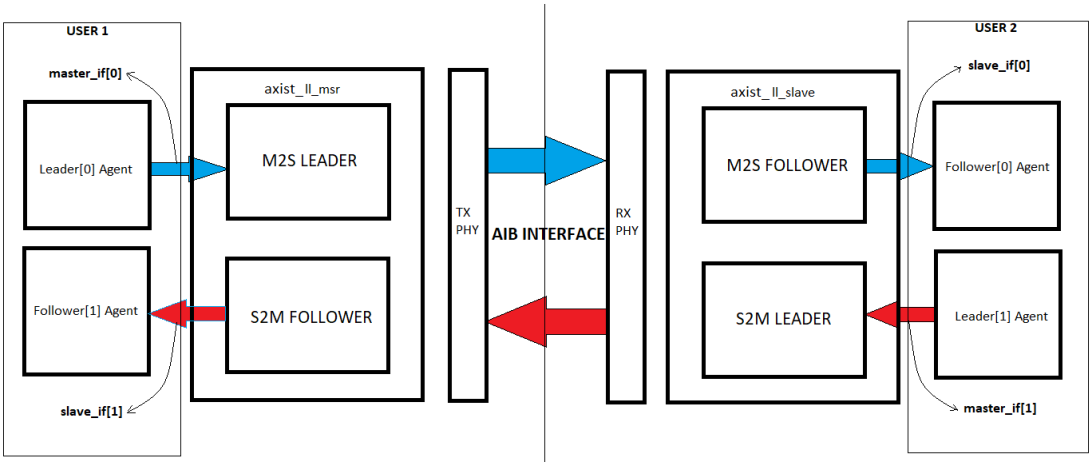

Figure 1: AXI-ST-Duplex data flow diagram

2.2 Example

The configuration for this file located in $(PROJ_DIR)/axi4-st-duplex/cfg/axi_dual_st_d64.cfg This implements a simple, no frills AXI-ST Duplex over two Full Rate Gen2 channels for each AXI-ST Logic Links respectively. This has a simple, Verilog, Logic Link only testbench here: ${PROJ_DIR}/axi4-st-duplex/dv/axi_dual_st_d64

The leader side is designated by user1_* signals and the follower side is designated by user2_* signals.

2.3 Asymmetric Gearboxing

The Asymmetric Gearboxing feature [2], as supported by AXI-ST logic Links, applies to AXI-ST Duplex Logic Links as well. The replicated struct for full case for AXI-ST Duplex can be defined as follows:

```
llink ST_M2S
{
M2S_TKEEP 8
M2S_TDATA 64
M2S_TVALID
M2S_TREADY
}

llink ST_S2M
{
S2M_TKEEP 8
S2M_TDATA 64
S2M_TVALID
S2M_TREADY
}
```

The generated Leader and Follower RTLs for FULL, HALF and QUARTER configurations will have user interfaces that look like the modules below.

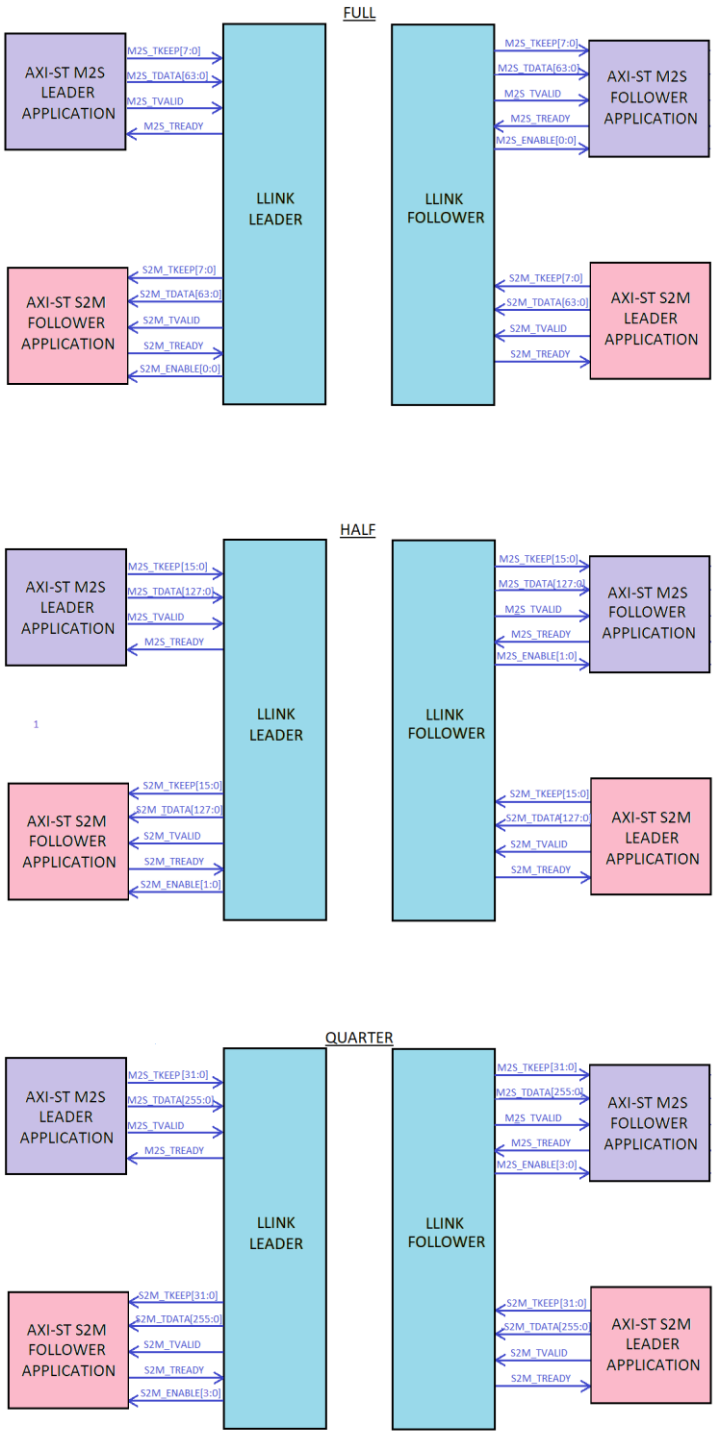

Figure 2: Asymmetric Leader and Follower Example

As can be seen, Follower Logic Links generally have a mirror version of the Leader but note that the Followers have an extra signal called “ENABLE”. This is an artifact of the asymmetric interface, and it acts as a kind of VALID for the entire replicated struct [3].

Reference:

[1] For details on AXI-ST features, implementations and examples, please refer to section 5 (AXI-ST) of llink_ug.pdf document

[2] For details on Asymmetric Gearboxing, please refer to section 5.4 (Asymmetric Gearboxing) of llink_ug.pdf document

[3] For details on ENABLE signal, please refer to section 5.4.1.3 (Replicated Struct Example) of llink_ug.pdf document