

AXI4 Protocol over AIB Latency Reference Guide Revision 1.0

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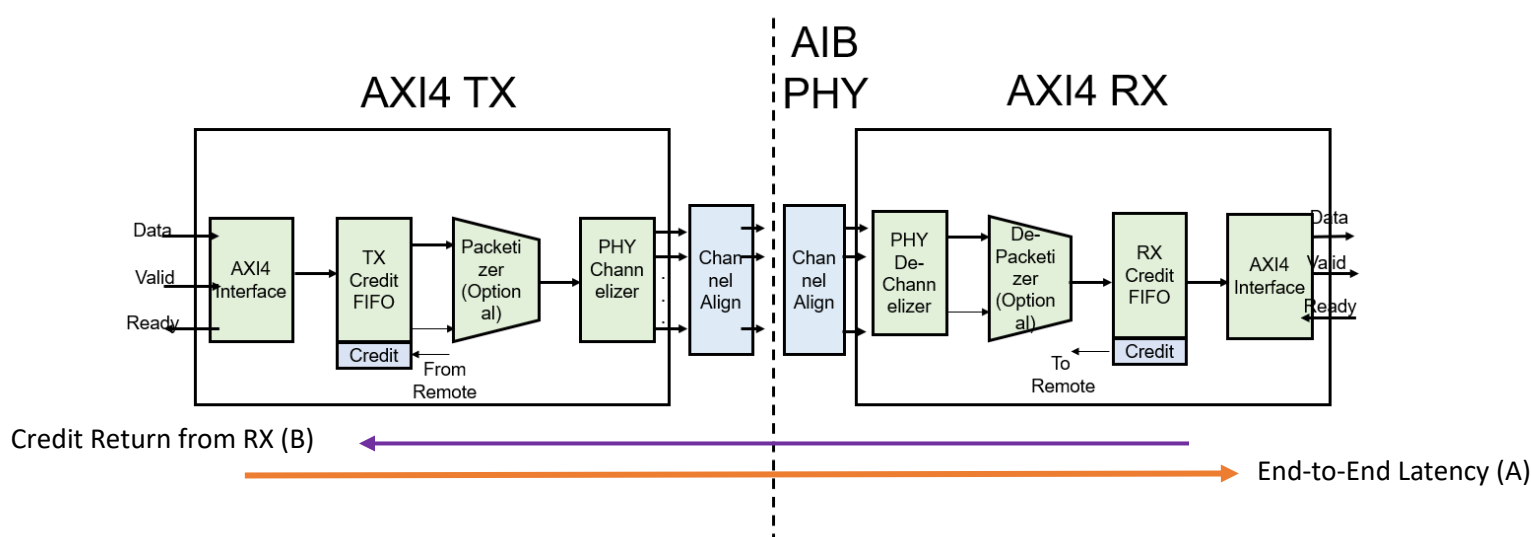
1. Background

There are 2 critical latency paths in AXI4 protocol:

- A) End-to-End latency – from TX to RX
- B) Credit return latency – from RX to TX

For AXI4 without flow control (AXI4-Stream without ready) B is not relevant for other AXI4 protocols with flow control both A and B play an important role as discussed below.

AXI4 protocol over AIB uses credit mechanism to manage flow control between follower and leader chiplet. This credit mechanism also allows to manage the multiple clock cycle handshake between chiplets.



To avoid stalling in the traffic (bubbles) the recommendation is to size the RX credit FIFO to match $A+B+k$ where k is an additional buffer. RX FIFO size is parameter for IP generation.

2. Simulation Parameters

Below is a table of measured latency in simulation and RX FIFO buffer size recommendation for AXI4-Stream and AXI4 based on the following parameters.

AXI4 Mode	Freq (Ghz)
Half (Gen1)	0.5
Full (Gen1)	1
Quarter (Gen2)	0.5
Half (Gen2)	1
Full (Gen2)	2

3. AXI4-Stream Latency and FIFO Buffer

Config No	Leader AIB Mode	Followe r AIB Mode	FIFO Mode (TX→RX)	A (normalized to AIB Fwd clk)	B (normalized to AIB Fwd clk)	k	Freq Factor between n AXI and AIB (F)	RX FIFO Size = Ceiling $((A+B+k)/F)$
1	AIB2.0 (Gen1)	AIB 1.0	Half→Half	44	40	2	2	43
2	AIB2.0 (Gen1)	AIB1.0	Full→Half	40	26	2	1	68
3	AIB2.0 (Gen1)	AIB1.0	Half→Full	30	40	2	1	72
4	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Half→Half	50	38	2	2	45
5	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Full→Full	31	28	2	1	61
6	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Quarter→Quarter	88	66	2	4	39
7	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Full→Half	48	29	2	1	79
8	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Full→Quarter	84	31	2	1	117
9	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Half→Full	34	38	2	1	74
10	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Half→Quarter	84	40	2	1	126
11	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Quarter→Full	39	65	2	1	106
12	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Quarter→Half	58	66	2	1	126

4. AXI4 Latency and FIFO Buffer

Config No	Leader AIB Mode	Followe r AIB Mode	FIFO Mode (TX→RX)	A (normalized to AIB Fwd clk)	B (normalized to AIB Fwd clk)	k	Freq Factor between n AXI and AIB (F)	RX FIFO Size = Ceiling $((A+B+k)/F)$
1	AIB2.0 (Gen1)	AIB 1.0	Half→Half	50	32	2	2	42
2	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Half→Half	50	40	2	2	46
3	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Full→Full	31	24	2	1	57
4	AIB2.0 (Gen2)	AIB2.0 (Gen2)	Quarter→Quarter	88	68	2	4	40

5. How to Specify RX FIFO Buffer Size

Can be specified as a configuration parameter in IP configuration file. Here are examples for AXI4-Stream and AXI4-MM

5.1. AXI4-Stream

MODULE axi_st		
// PHY and AIB Configuration		
NUM_CHAN		7
CHAN_TYPE		Gen1Only //Gen1Only, Gen2Only, Gen2, AIBO
// Channel Alignment Strobe Configuration		
TX_ENABLE_STROBE	True	// If False, all strobe functionality is removed.
RX_ENABLE_STROBE	True	// If False, all strobe functionality is removed.
TX_PERSISTENT_STROBE	True	// If True strobes are persistent (always there). If false, they are recoverable and can be reused for data
RX_PERSISTENT_STROBE	True	// If True strobes are persistent (always there). If false, they are recoverable and can be reused for data
TX_USER_STROBE	True	// If True, then we input user generated signal
RX_USER_STROBE	True	// If True, then we input user generated signal

TX_STROBE_GEN1_LOC	8	// Location of Strobe when in Gen1 Mode
RX_STROBE_GEN1_LOC	8	// Location of Strobe when in Gen1 Mode
// Word Marker Configuration		
TX_ENABLE_MARKER	True	// If False, all Marker functionality is removed.
RX_ENABLE_MARKER	True	// If False, all Marker functionality is removed.
TX_PERSISTENT_MARKER	True	// If True Markers are persistent (always there). If false, they are recoverable and can be reused for data
RX_PERSISTENT_MARKER	True	// If True Markers are persistent (always there). If false, they are recoverable and can be reused for data//
TX_USER_MARKER	True	
RX_USER_MARKER	True	
TX_MARKER_GEN1_LOC	39	// Location of Marker when in Gen1 Mode
RX_MARKER_GEN1_LOC	39	// Location of Marker when in Gen1 Mode
TX_REG_PHY	False	
RX_REG_PHY	False	
SUPPORT_ASYMMETRIC	True	// Support Asymmetric Gearboxing (e.g. Full to Half)
llink ST		
{		
TX_FIFO_DEPTH	1	
RX_FIFO_DEPTH	68 # for Full→Half	
output user_tdata 256		
input user_tready ready		
output user_tvalid valid		
}		

5.2. AXI4-MM

MODULE axi_mm		
// PHY and AIB Configuration		
NUM_CHAN	2	
CHAN_TYPE	Gen1Only	//Gen1Only, Gen2Only, Gen2, AIBO
TX_RATE	Half	// Full, Half, Quarter
RX_RATE	Half	// Full, Half, Quarter
// Channel Alignment Strobe Configuration		
TX_ENABLE_STROBE	True	// If False, all strobe functionality is removed.
RX_ENABLE_STROBE	True	// If False, all strobe functionality is removed.
TX_PERSISTENT_STROBE	True	// If True strobes are persistent (always there). If false, they are recoverable and can be reused for data
RX_PERSISTENT_STROBE	True	// If True strobes are persistent (always there). If false, they are recoverable and can be reused for data
TX_USER_STROBE	False	// If True, then we input user generated signal
RX_USER_STROBE	False	// If True, then we input user generated signal
TX_STROBE_GEN1_LOC	7	// Location of Strobe when in Gen1 Mode
RX_STROBE_GEN1_LOC	7	// Location of Strobe when in Gen1 Mode
// Word Marker Configuration		
TX_ENABLE_MARKER	True	// If False, all Marker functionality is removed.
RX_ENABLE_MARKER	True	// If False, all Marker functionality is removed.
TX_PERSISTENT_MARKER	True	// If True Markers are persistent (always there). If false, they are recoverable and can be reused for data
RX_PERSISTENT_MARKER	True	// If True Markers are persistent (always there). If false, they are recoverable and can be reused for data//
TX_USER_MARKER	False	
RX_USER_MARKER	False	
TX_MARKER_GEN1_LOC	39	// Location of Marker when in Gen1 Mode
RX_MARKER_GEN1_LOC	39	// Location of Marker when in Gen1 Mode
TX_REG_PHY	False	

```

RX_REG_PHY      False

// Packetization
TX_ENABLE_PACKETIZATION      True
RX_ENABLE_PACKETIZATION      True
TX_PACKET_MAX_SIZE           0      // Number of bits to packetize to. 0 means all available data.
RX_PACKET_MAX_SIZE           0      // Number of bits to packetize to. 0 means all available data.
PACKETIZATION_PACKING_EN     False  // If True, enable packing which makes better use of the BW

llink AR
{
    TX_FIFO_DEPTH    1
    RX_FIFO_DEPTH    42

    output user_arid    4
    output user_arsize  3
    output user_arlen   8
    output user_arburst 2
    output user_araddr  32
    output user_arvalid valid
    input  user_arready ready
}

llink AW
{
    TX_FIFO_DEPTH    1
    RX_FIFO_DEPTH    42

    output user_awid    4
    output user_awsize  3
    output user_awlen   8
    output user_awburst 2
    output user_awaddr  32
    output user_awvalid valid
    input  user_awready ready
}

llink W
{
    TX_FIFO_DEPTH    1
    RX_FIFO_DEPTH    42

    output user_wid    4
    output user_wdata  128
    output user_wstrb   16
    output user_wlast
    output user_wvalid valid
    input  user_wready ready
}

llink R
{
    TX_FIFO_DEPTH    1
    RX_FIFO_DEPTH    42

    input  user_rid    4
    input  user_rdata  128
    input  user_rlast
    input  user_rresp   2
    input  user_rvalid valid
    output user_rready ready
}

llink B
{
    TX_FIFO_DEPTH    1
    RX_FIFO_DEPTH    42

```

```
input user_bid    4
input user_bresp  2
input user_bvalid valid
output user_bready ready
}
```

6. Latency Optimization

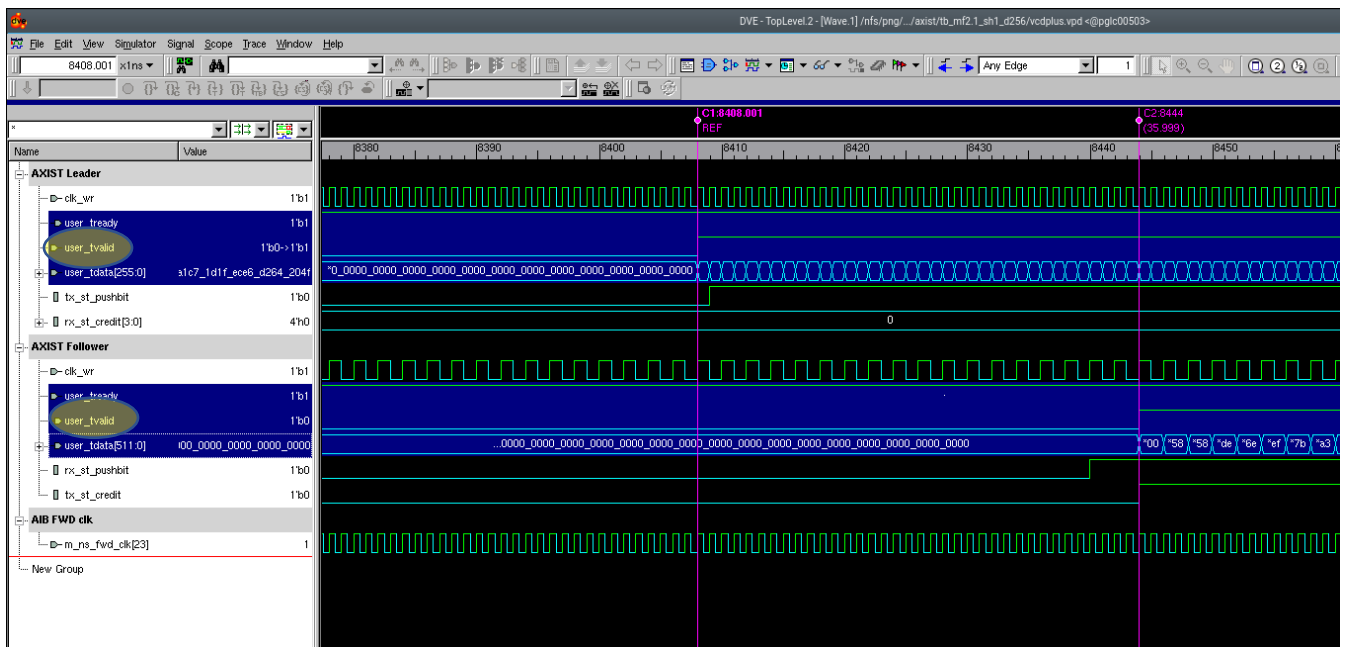
These latencies reported here are out of the box. Here are some tips to improve latency with system knowledge:

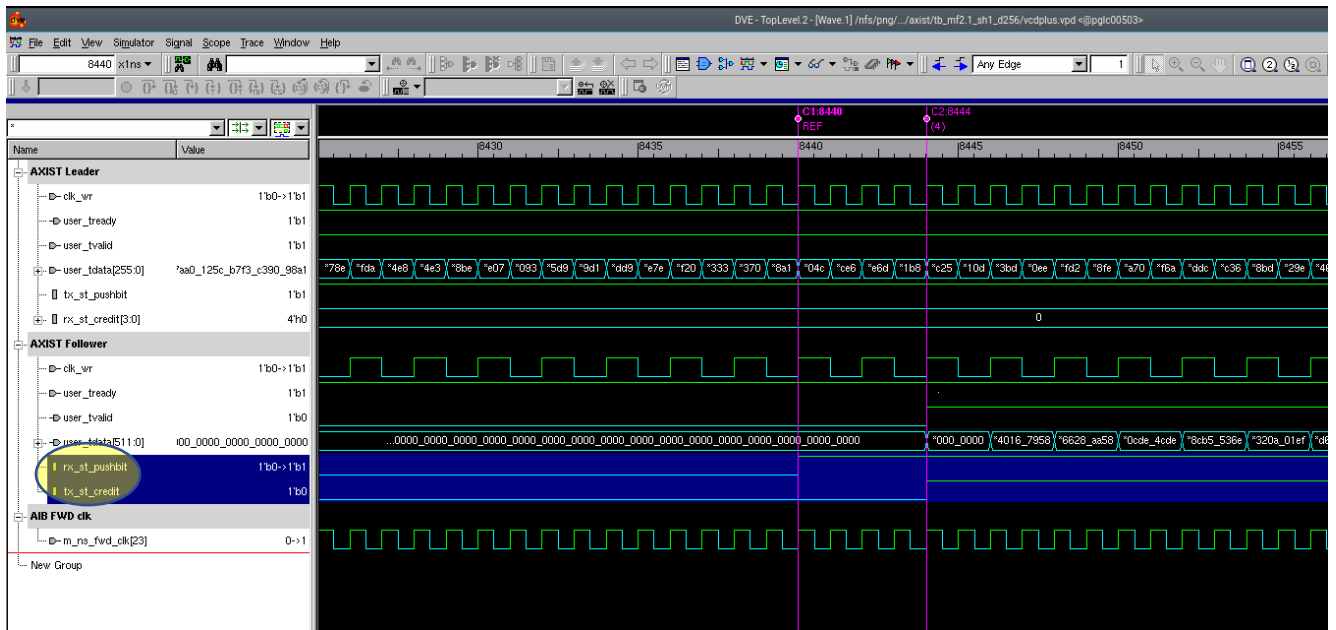
- a) Lane to lane to skew modeled in testbench as delay between AIB and CA. This delay is worst cased at 5 clock cycle this can be optimized for your interface and system once you have the system parameters extracted.
- b) Improve RX/TX phasecomp RD delay with the knowledge of AIB write vs read clock wander margin. These values can be programmed to AIB CSR 0x208/0x218.

7. Addendum: Example waveform capture for Parameters A and B (Config 2 for AXI4-ST)

7.1. Latency A

Sum of valid to valid + push to pop on RX FIFO Buffer





7.2. Latency B

Credit return from follower to leader

