Cole Maxwell (25017014): ECE 658

Lab 2: Design of a Bitslice Accumulator

November 2020

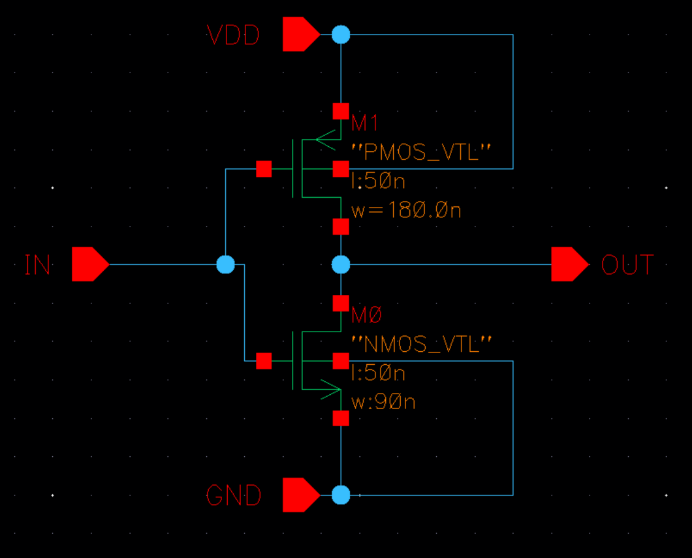
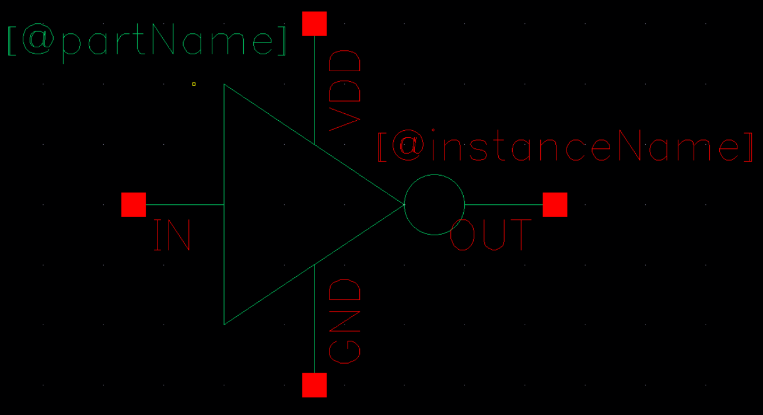
**Step 1: Truth Table**

Full Adder

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input** | | | | **Output** | |
| **A** | **SOUT** | **CIN** | **RST** | **COUT** | **D** |
| 0 | 0 | 0 | 0 | **0** | **1** |
| 0 | 0 | 0 | 1 | **0** | **1** |
| 0 | 0 | 1 | 0 | **0** | **1** |
| 0 | 0 | 1 | 1 | **0** | **0** |
| 0 | 1 | 0 | 0 | **0** | **1** |
| 0 | 1 | 0 | 1 | **0** | **0** |
| 0 | 1 | 1 | 0 | **1** | **1** |
| 0 | 1 | 1 | 1 | **1** | **1** |
| 1 | 0 | 0 | 0 | **0** | **1** |
| 1 | 0 | 0 | 1 | **0** | **0** |
| 1 | 0 | 1 | 0 | **1** | **1** |
| 1 | 0 | 1 | 1 | **1** | **1** |
| 1 | 1 | 0 | 0 | **1** | **1** |
| 1 | 1 | 0 | 1 | **1** | **1** |
| 1 | 1 | 1 | 0 | **1** | **1** |
| 1 | 1 | 1 | 1 | **1** | **0** |

**Step 2: Create Schematic**

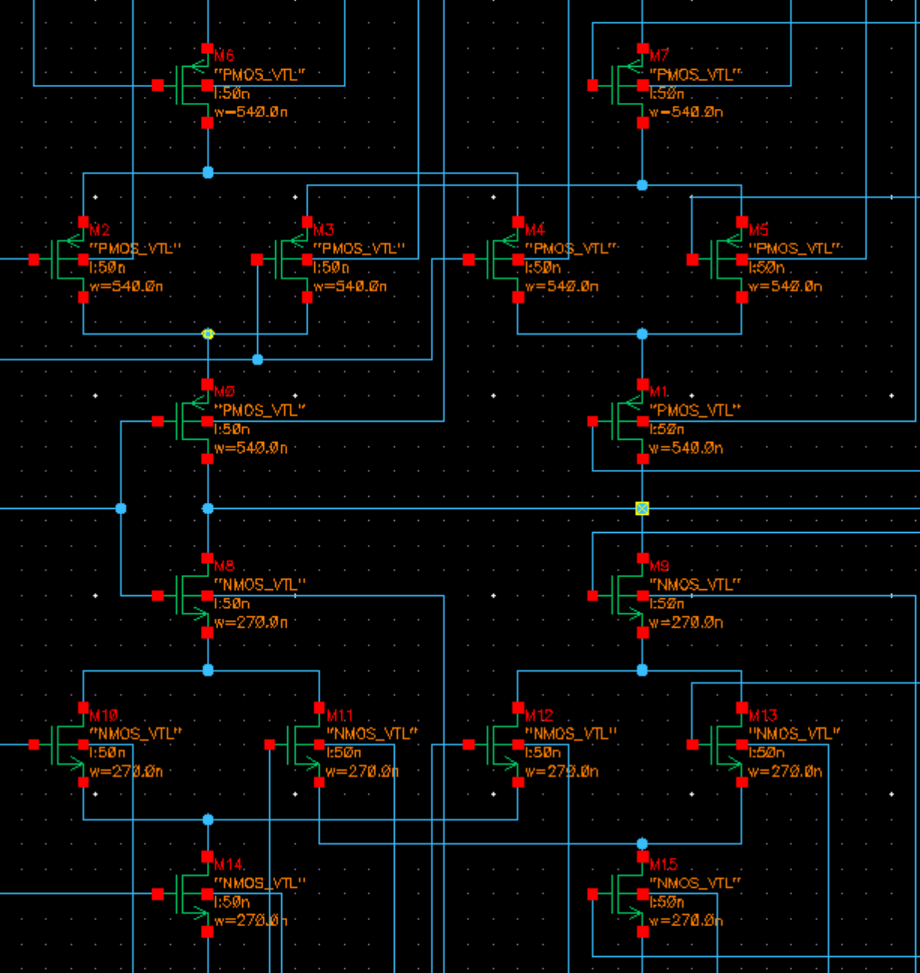
Inverter schematic & symbol:

XOR gate schematic (full view):

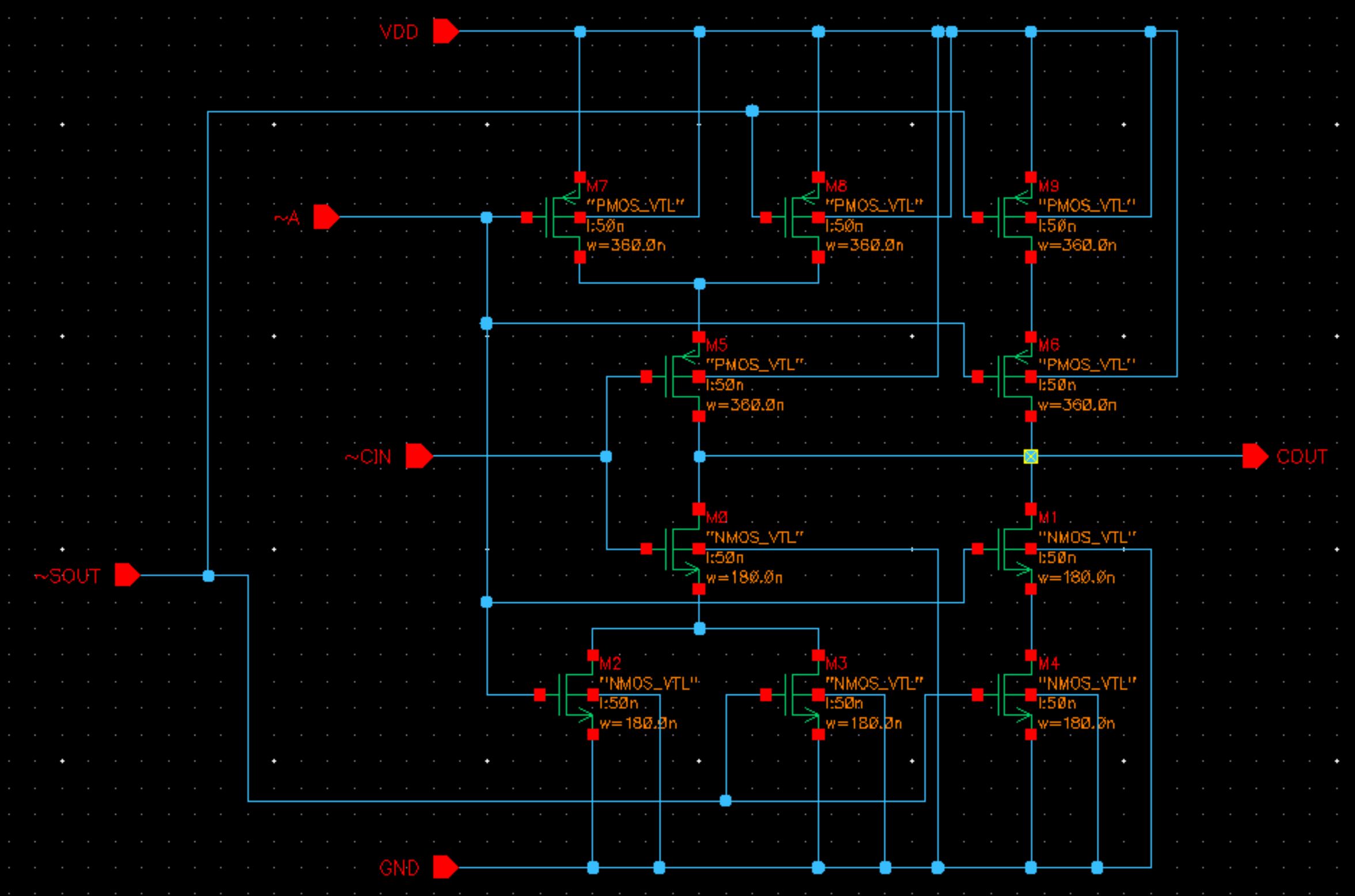


XOR gate schematic (zoomed view) & symbol:

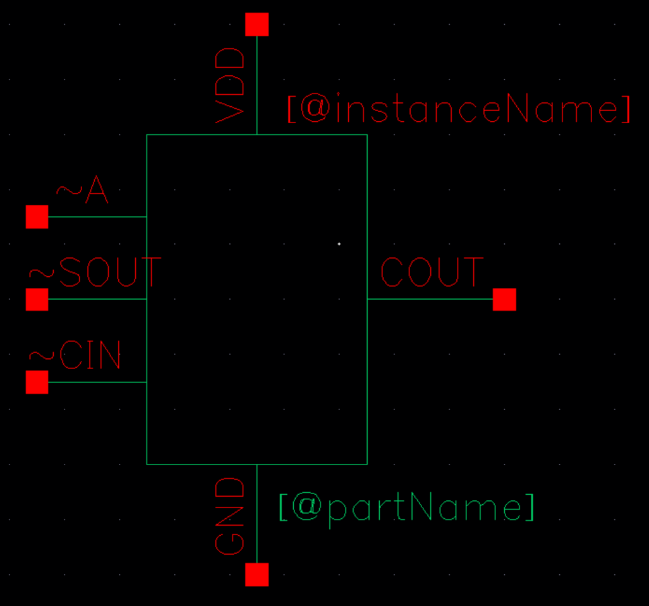
 A picture containing meter

Description automatically generated

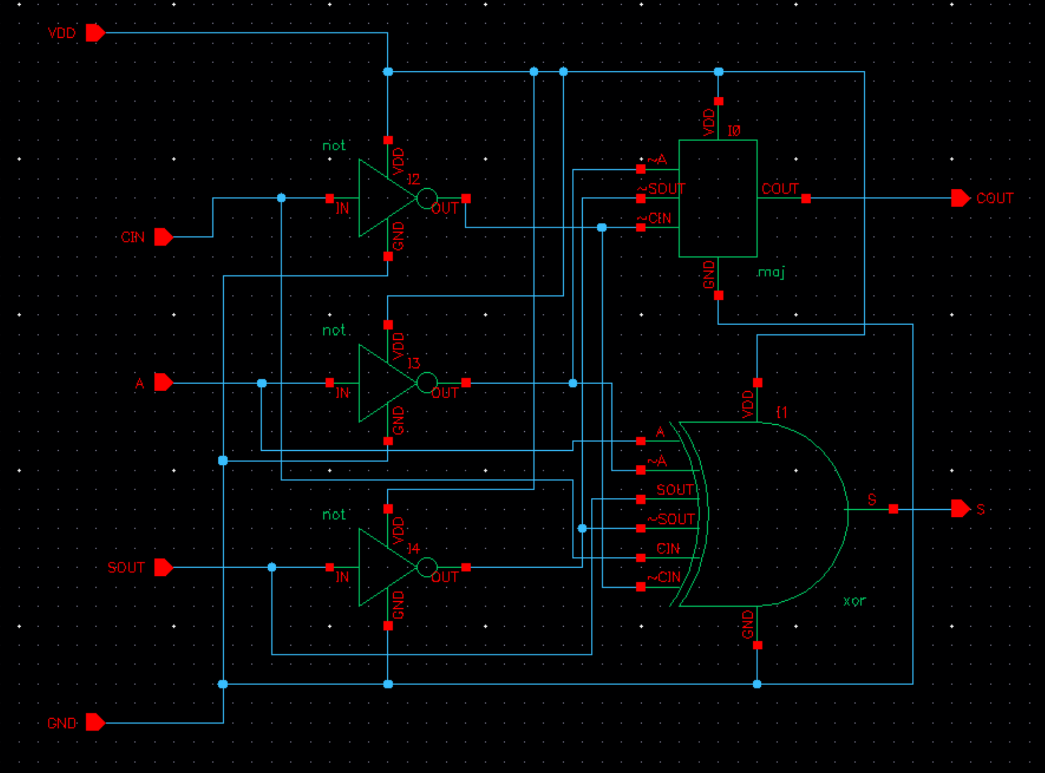
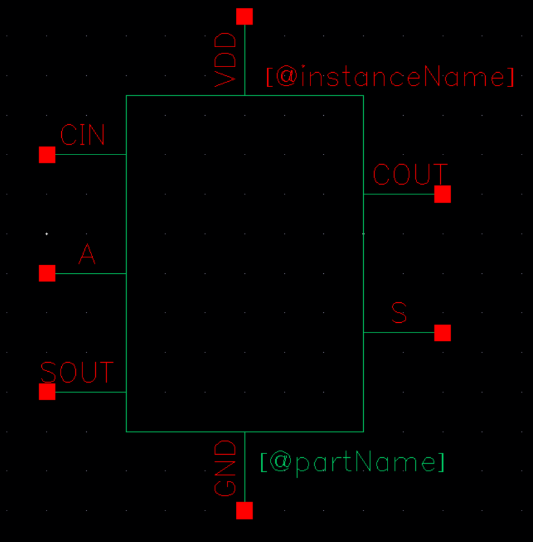
Majority gate schematic:



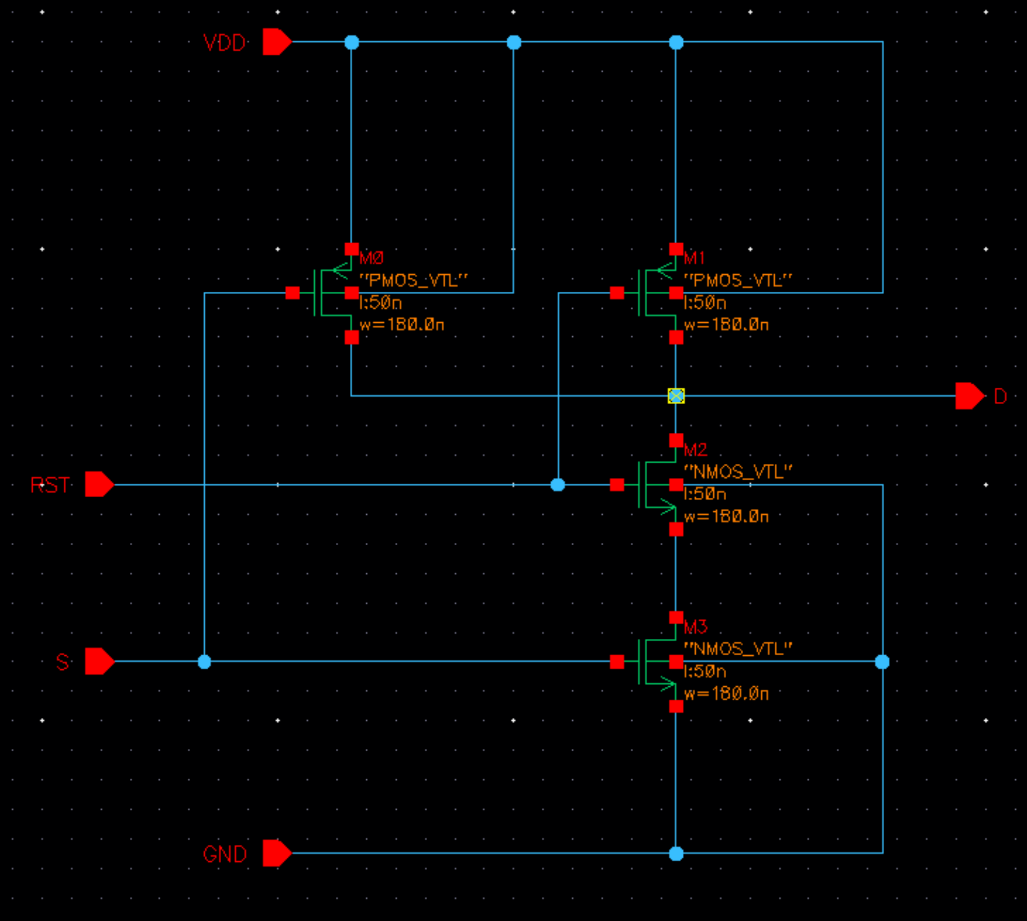
Majority gate symbol:



Full adder schematic & symbol:

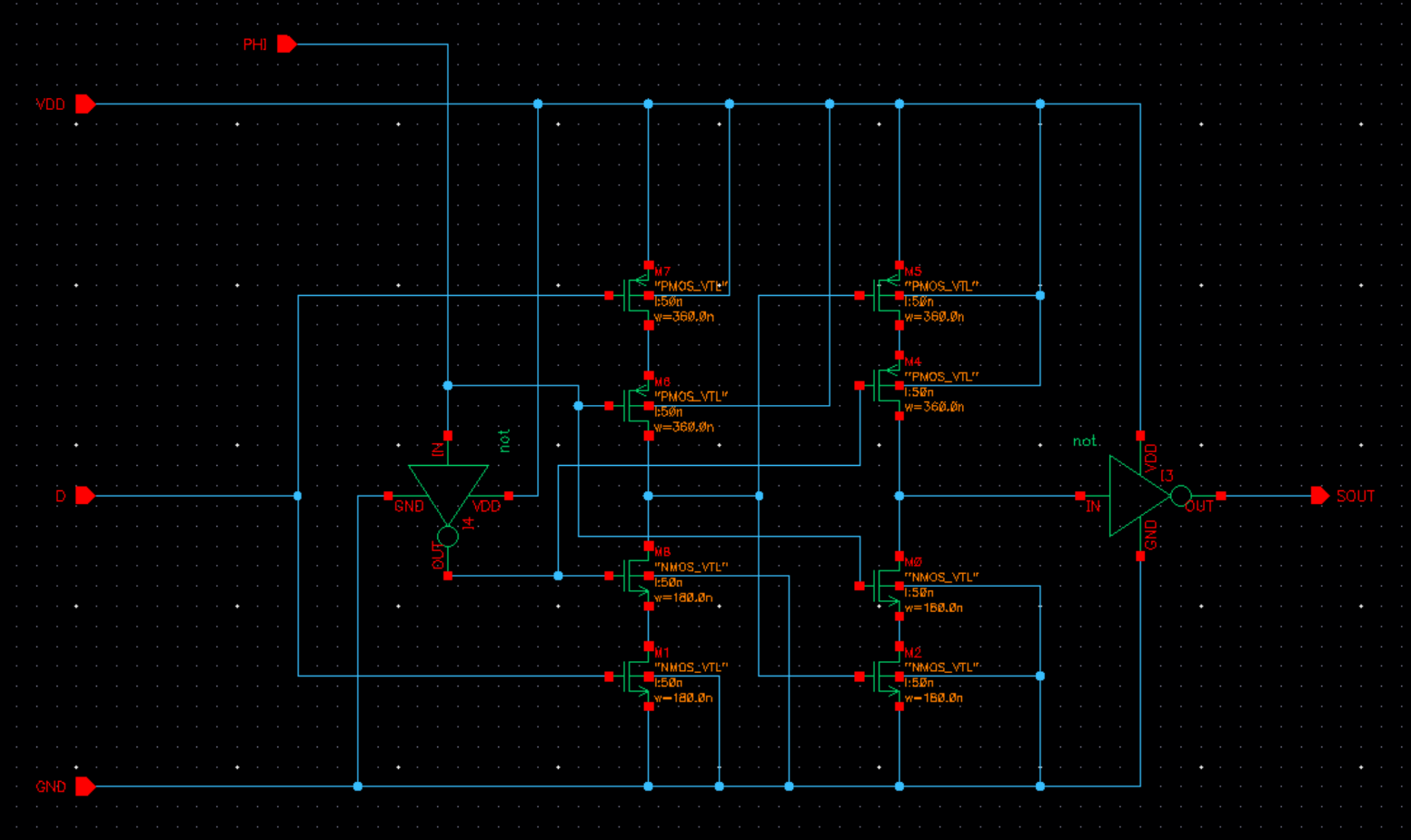
 

Synchronous reset (NAND2) schematic:

 A picture containing diagram

Description automatically generated

Dynamic flip-flop schematic:



Dynamic flip-flop symbol:

A picture containing shape

Description automatically generated

Accumulator schematic:

A picture containing light, outdoor, sitting, traffic

Description automatically generated

**Step 3: Check Functionality of Schematic**

Validation test sequence:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input values before transition** | | | | **Input values after transition** | | | | **Output values before transition** | | | **Output values after transition** | | | **Transistors checked** |
| **A** | **SOUT** | **CIN** | **RST** | **A** | **SOUT** | **CIN** | **RST** | **COUT** | **S** | **D** | **COUT** | **S** | **D** |
| 0 | 0 | 0 | 0 | 0­ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | RST/M1 PMOS  FF/M7, M10, M6, M8, M4 PMOS  I3 NMOS, I4 NMOS  I2 PMOS |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | XOR/M6 PMOS  MAJ/M1, M2 NMOS  I3 PMOS, I4 NMOS  I2 NMOS |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | XOR/M2, M5 PMOS  MAJ/M3, M4 NMOS  I3 NMOS, I4 PMOS  I2 NMOS |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | RST/M1 PMOS  FF/M7, M10, M6, M8, M4 PMOS  FF/M3, M1 NMOS |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | RST/M1 PMOS  FF/M7, M10, M6, M8, M4 PMOS  FF/M7, M5 PMOS |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | XOR/M1 PMOS  MAJ/M NMOS  I3 NMOS, I4 NMOS  I2 PMOS |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | XOR/M10, M13 NMOS  XOR/M9 NMOS  MAJ/M8, M9 NMOS  RST/M2 NMOS |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | XOR/M10, M13, M9, M14 NMOS  MAJ/M8, M9, M5, M6, M7 NMOS  RST/M2, M3 NMOS  FF/M9 NMOS |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | XOR/M6, M2, M5 PMOS  XOR/M14, M15 NMOS  MAJ/M8, M9 NMOS  RST/M2 NMOS  FF/M8 PMOS |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | RST/M1 PMOS  FF/M7, M10, M6, M8, M4 PMOS |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | RST/M1 PMOS  FF/M7, M10, M6, M8, M4 PMOS |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | XOR/M6, M2, M5 PMOS  MAJ/M8, M9 NMOS  RST/M2 NMOS |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | END |

Description of validation test sequence:

The goal of the test sequence is to check that all transistors are turning on correctly. To ensure this, the simulation runs for a total of 13 clock cycles, during which all pull-up and pull-down networks are activated through by specific combinations of input values.

In the FA, the six PMOS and NMOS transistors that make up the three inverters are tested by driving them all with 0 and 1 in the simulation. The XOR gates pull-up network is tested by looking at the value of S (net21) when either one or all three of the inputs are high, for a total of four combinations. At the same time, the MAJ gate’s pull-down network is tested by ensuring the value of COUT is 0 since only one of the three inputs is high. On the other hand, the MAJ gate’s pull-up network is tested by ensuring the value of COUT is 1 when the three combinations of two inputs are high, and when all three inputs are high (four combinations again). At the same time, the XOR gates pull-down network is tested during the three combinations when two of the three inputs are high.

In the reset circuit, the pull-up network is tested by ensuring the value of D (net20) is 1 when RST is 0, and the pull-down network is tested by ensuring the value of D has the opposite polarity of S when RST is 1.

The first sequence is the reset sequence that sets the value of SOUT to 0, testing the reset circuit’s pull-up network.

**0000**

**0001**

Next, only A is high, testing the XOR’s pull-up and the MAJ’s and Reset’s pull-down.

**1010**

Next, only SOUT is high, testing the XOR’s pull-up and the MAJ/Reset pull-down.

**0011**

Here, the reset sequence is used again before the next test.

**0000**

**0001**

Next, only CIN is high, testing the XOR’s pull-up and the MAJ/Reset pull-down.

**0110**

Next, both CIN and SOUT are high, testing the XOR/Reset pull-down and the MAJ pull-up.

**0111**

Next, A, CIN and SOUT are high, testing the XOR/Reset pull-up and the MAJ pull-down.

**1110**

Next, both A and SOUT are high, testing the XOR/Reset pull-down and the MAJ pull-up.

**1011**

Reset sequence

**0000**

**0001**

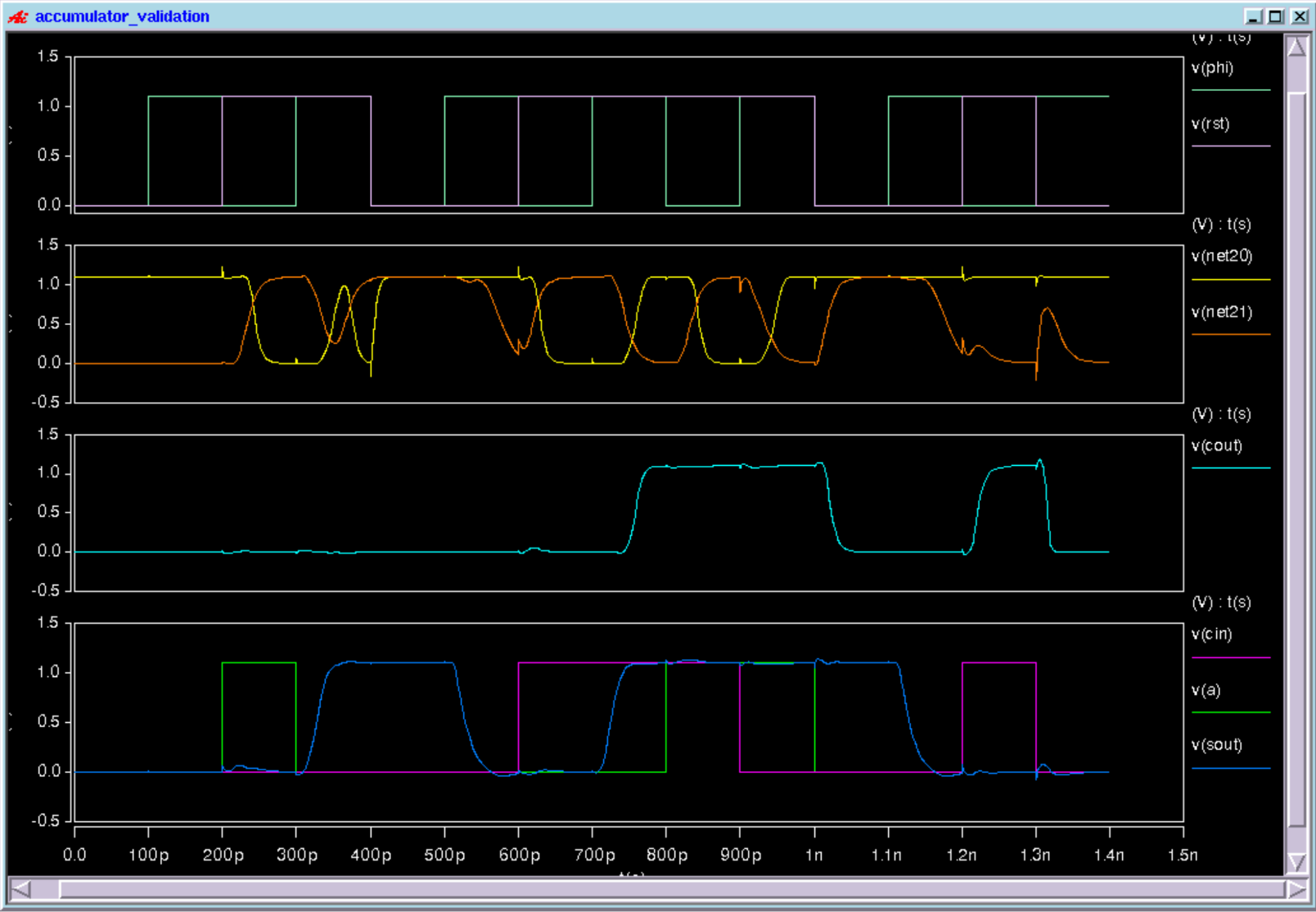
Next, both A and CIN are high, testing the XOR/Reset pull-down and the MAJ pull-up.

**1110**

The final sequence ends the simulation, sets values to 0, and does not test anything.

**0001**

Waveforms:



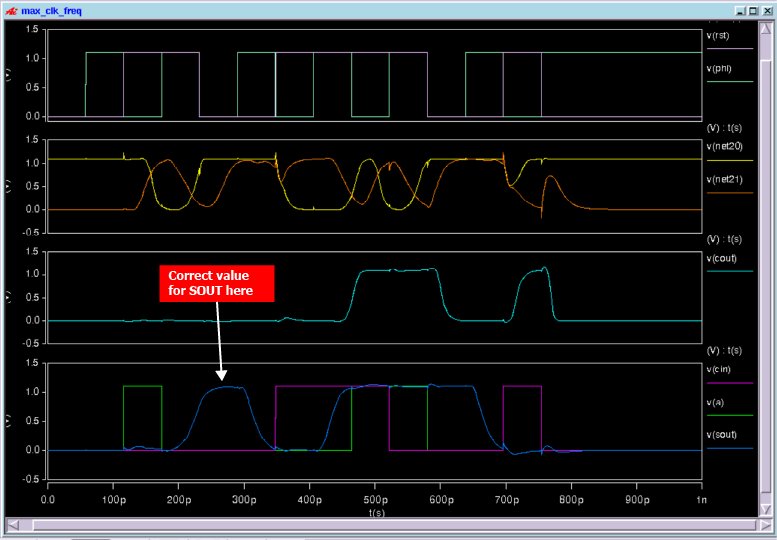
**Step 4: Determine Maximum Clock Frequency**

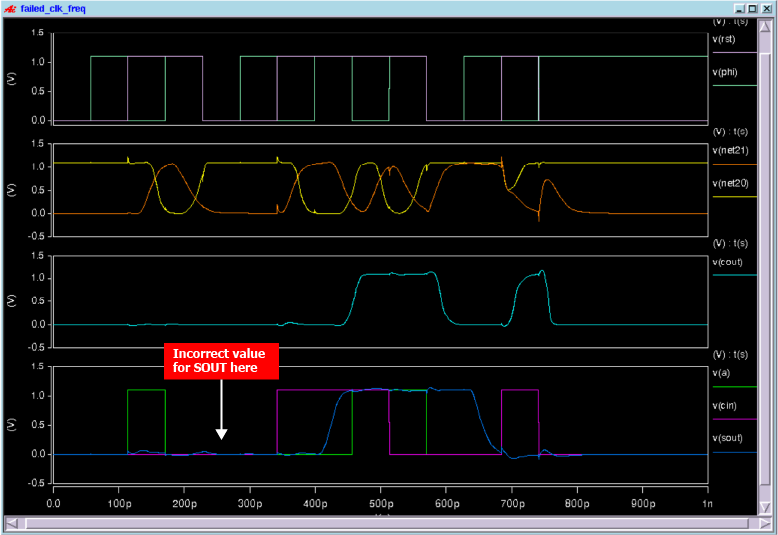
The circuit failed (incorrect value for SOUT) when clock period dropped below 58ps.

Converting to GHz frequency:

**Maximum clock Frequency = 17.241379310345 GHz**

Successful validation sequence at maximum clock frequency:



Failed validation sequence 10% above maximum clock frequency:

**Step 5: Power**

Measurements of dynamic power:

|  |  |  |
| --- | --- | --- |
| **period(ps)** | **freq(GHz)** | **avg power** |
|  |  |  |
| 70 | 14.28571429 | 1.17E-04 |
| 85 | 11.76470588 | 9.97E-05 |
| 100 | 10 | 8.75E-05 |
| 115 | 8.695652174 | 7.76E-05 |
| 130 | 7.692307692 | 6.78E-05 |
| 145 | 6.896551724 | 5.97E-05 |

Plot:

Chart, scatter chart

Description automatically generated

Extrapolation of power at maximum frequency:

At maximum frequency of 17.24137 GHz, average power = 1.31E-04

Chart, line chart, scatter chart

Description automatically generated

Estimate of static power:

Chart, scatter chart

Description automatically generated

Confirmed with HSPICE simulation with inputs of zeroes of 3.87E-07.

**Step 6: Layout**

Accumulator bitslice:

A picture containing lit, computer, table, clock

Description automatically generated

Signals & inverters:

A picture containing lit, building, light, purple

Description automatically generated

XOR gate:

A lit up city at night

Description automatically generated

Majority gate:

A picture containing clock, lit, computer

Description automatically generated

Synchronous reset & dynamic flip-flop:

A picture containing circuit, lit, clock, purple

Description automatically generated

DRC results:

Graphical user interface, application

Description automatically generated

LVS results:

Graphical user interface

Description automatically generated

Maximum clock frequency with parasitics:

The circuit failed (incorrect value for SOUT) when clock period dropped below 121ps.

**Maximum clock Frequency = 8.2644628099174 GHz**

Comparing to max frequency without parasitics of 17.241379310345 GHz, we see that parasitics cause the maximum frequency to decrease by a factor of ~2.

Successful validation sequence at maximum clock frequency:

Graphical user interface, chart

Description automatically generated

Failed validation sequence 10% above maximum clock frequency:

Graphical user interface, chart

Description automatically generated