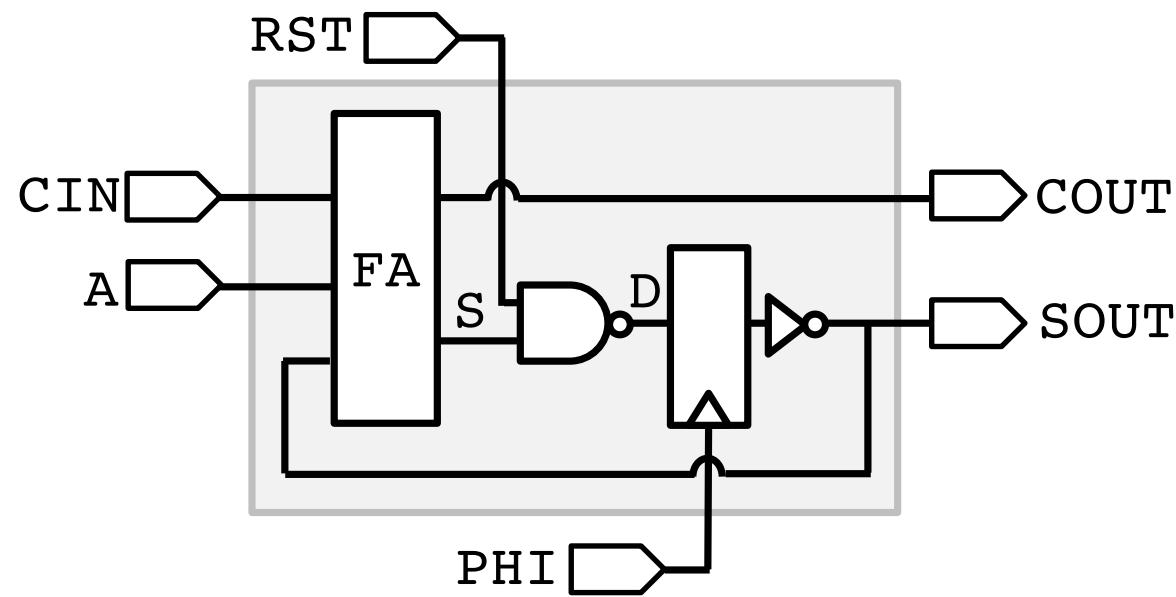
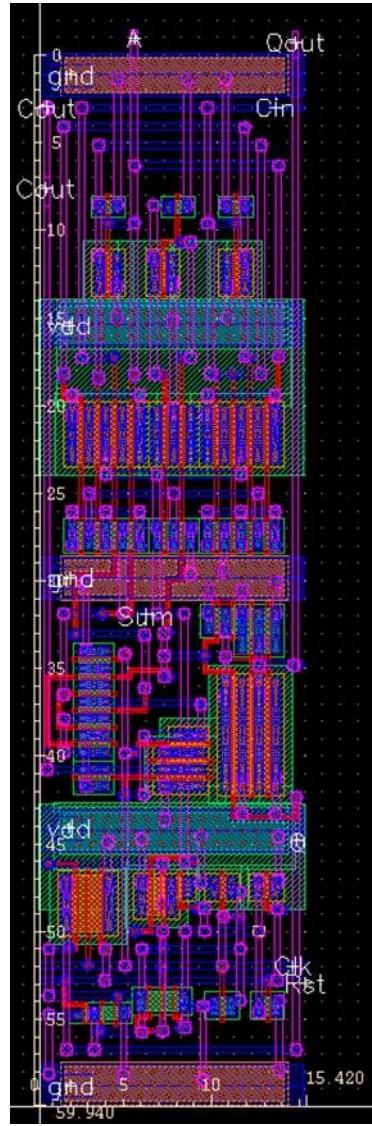


**Intro to Lab 2:
accumulator bitslice
covered in 9/29/2020 lecture**

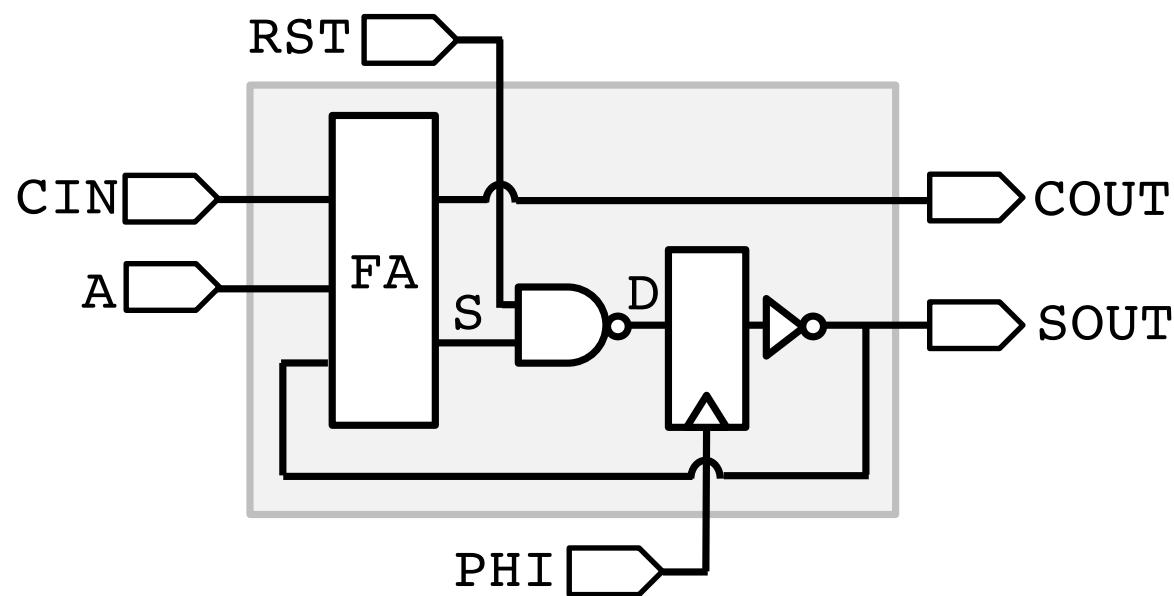
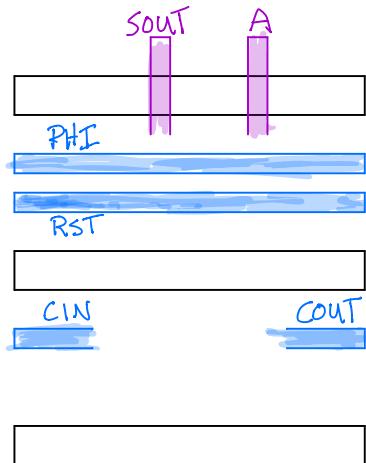
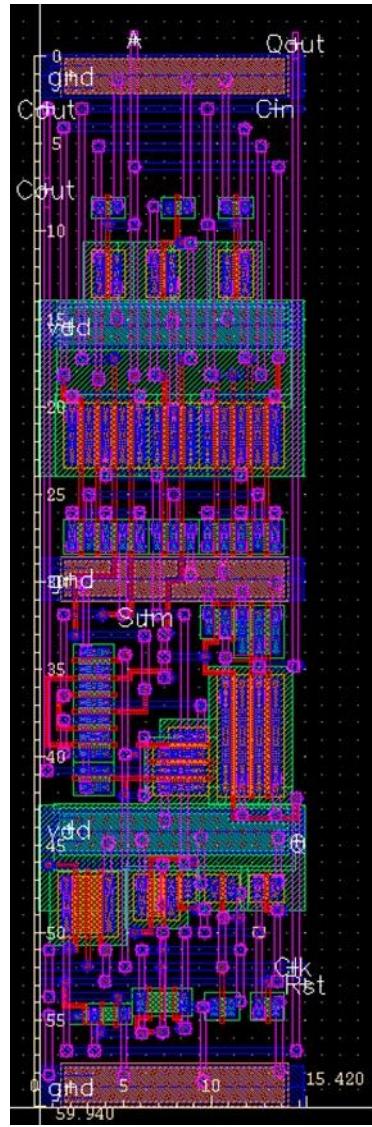
General Lab Feedback

- Plot annotations must be readable
- Submit as pdf with name and ECE558/658 at top
- Read instructions carefully
- Check spelling
- Inputs:
 - Voltage of logic 1 should match supply
 - Rise and fall times are 20% to 80%
 - Transitions should start from 0 or supply
- Get in habit of trying to judge whether numbers are reasonable. Unreasonable numbers may reveal bugs

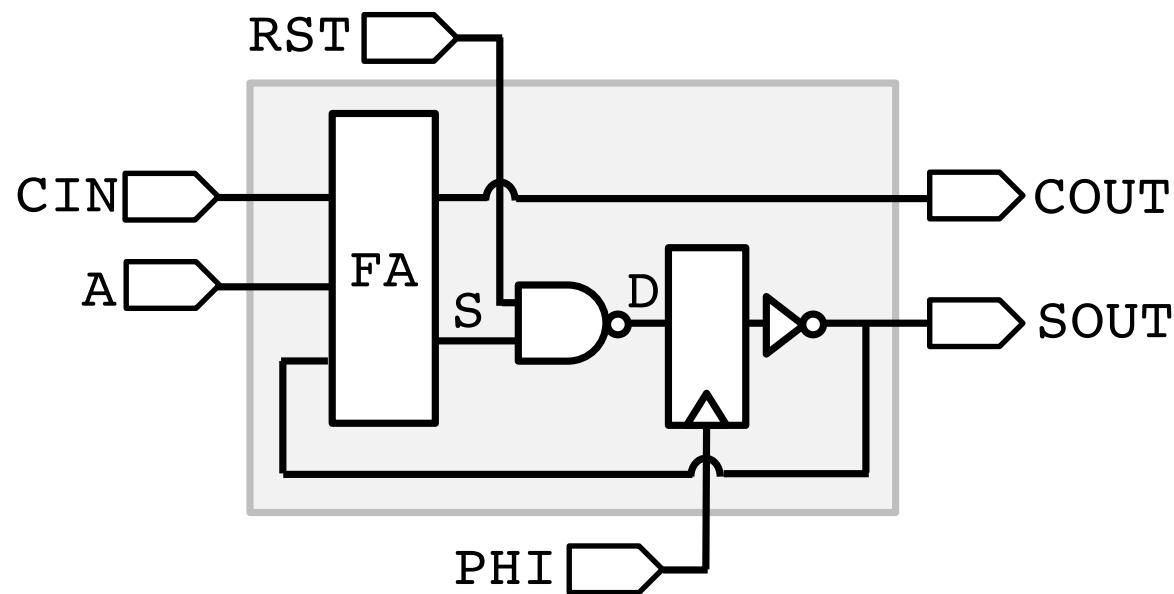
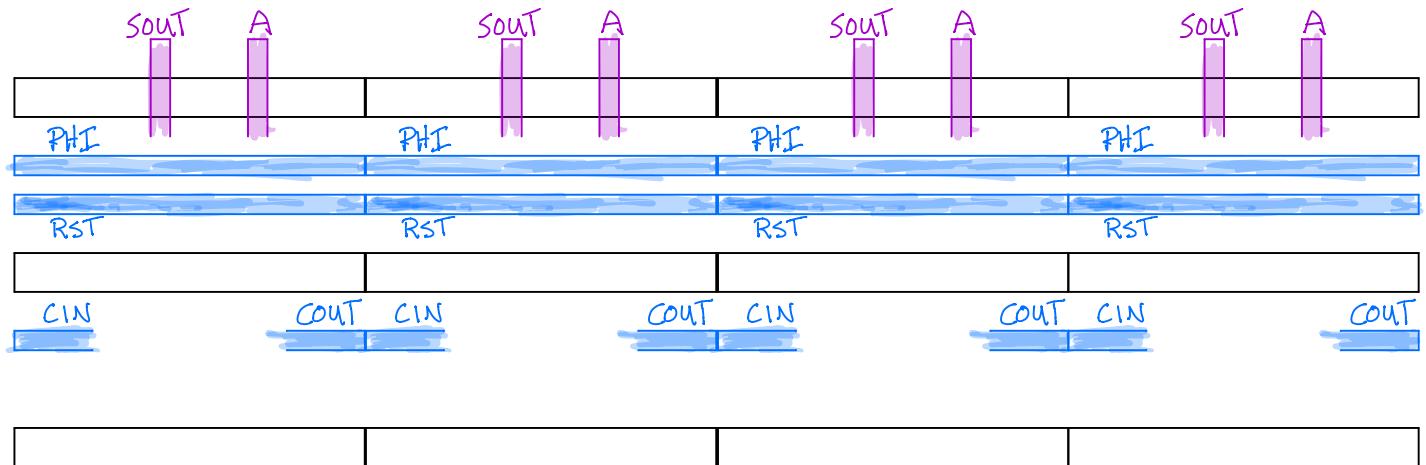
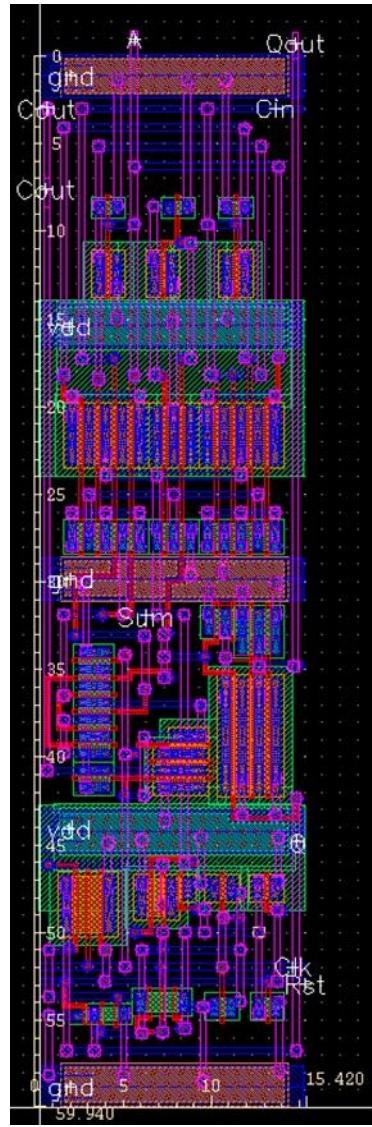
Bitsliced Design and Layout



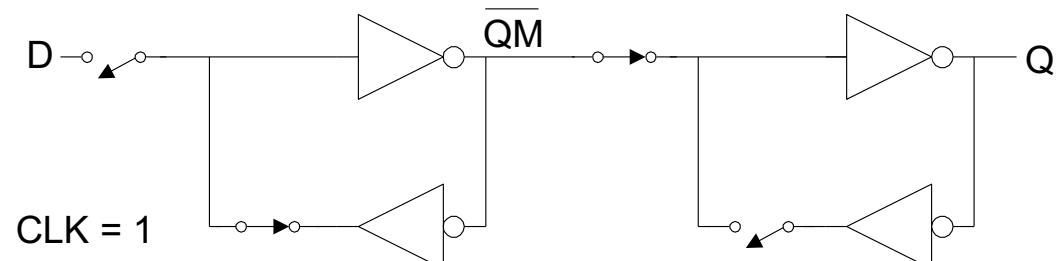
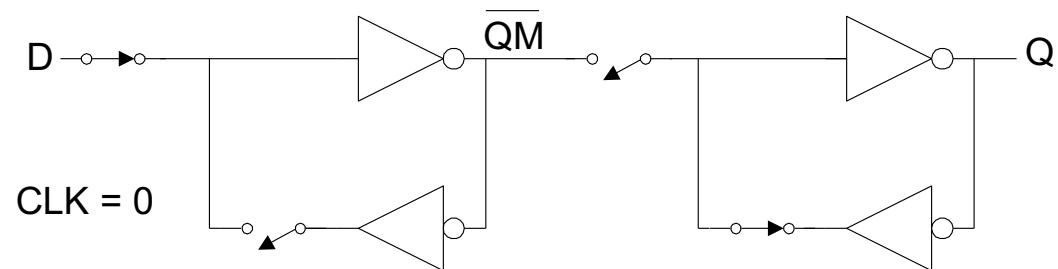
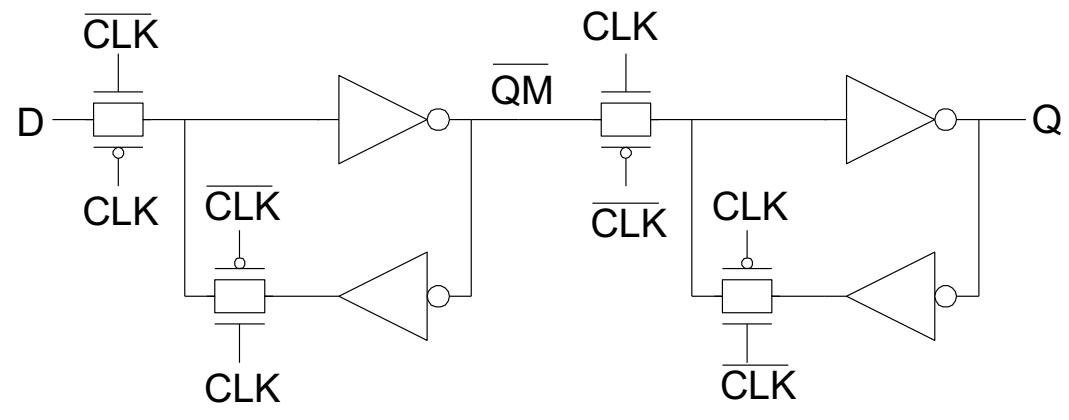
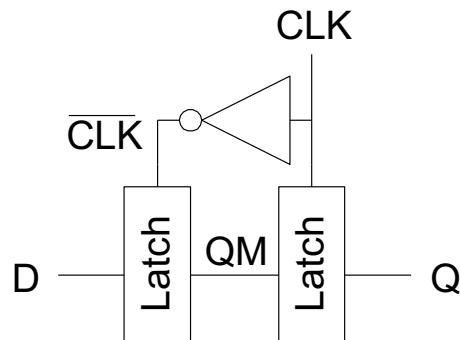
Bitsliced Design and Layout



Bitsliced Design and Layout

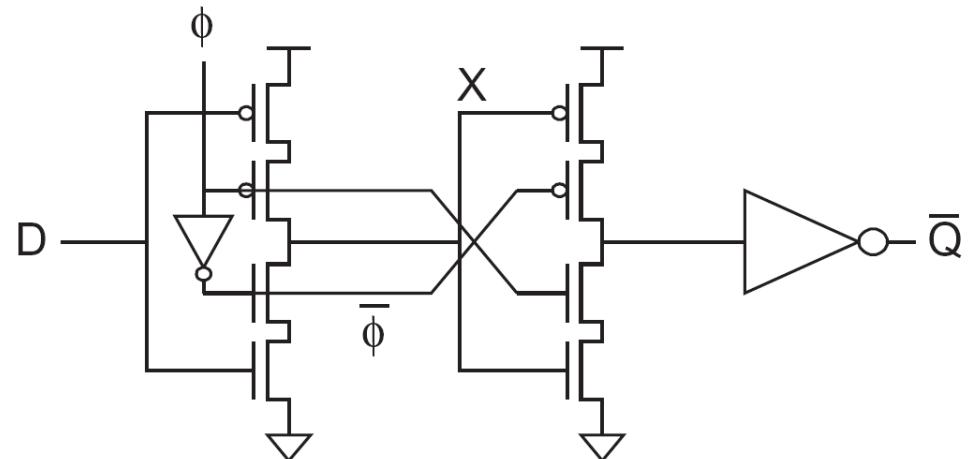


Static Flip-flop (review)



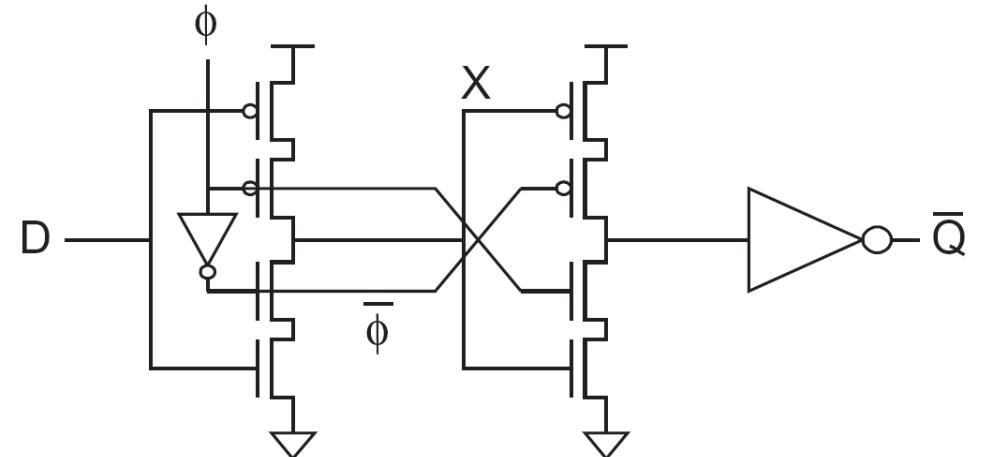
C²MOS Flip-Flop

- Two tristate inverters. Transparent on opposite clk phases



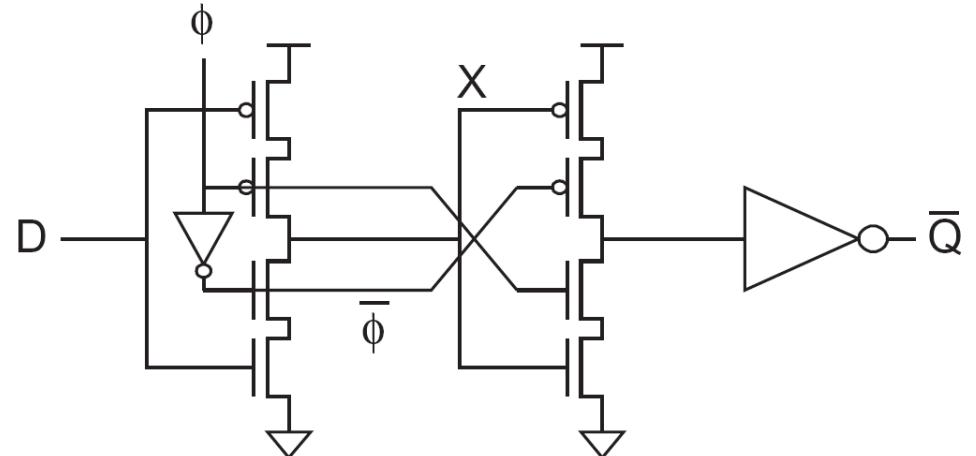
C²MOS Flip-Flop

- ❑ Two tristate inverters. Transparent on opposite clk phases
- ❑ Dynamic — holds state capacitively while nodes are undriven



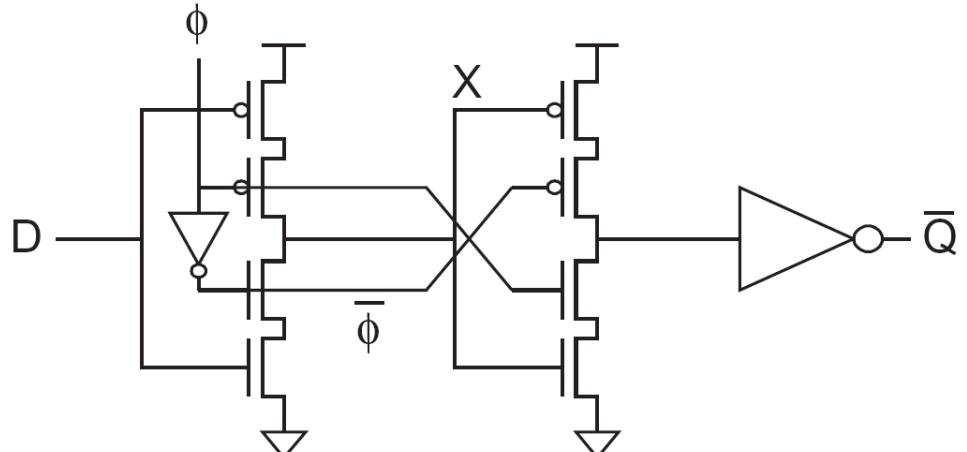
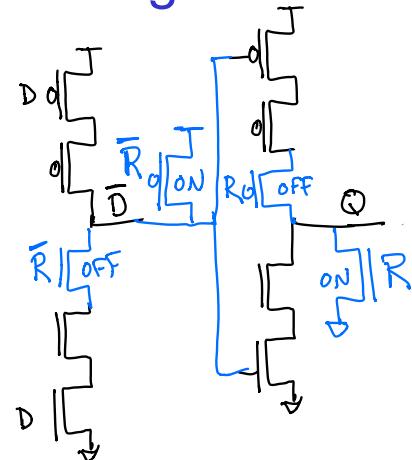
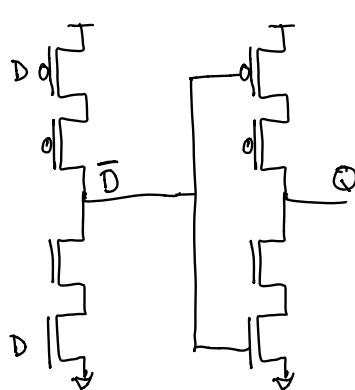
C²MOS Flip-Flop

- ❑ Two tristate inverters. Transparent on opposite clk phases
- ❑ Dynamic — holds state capacitively while nodes are undriven
- ❑ How would you reset it asynchronously without DC current from Vdd to ground?



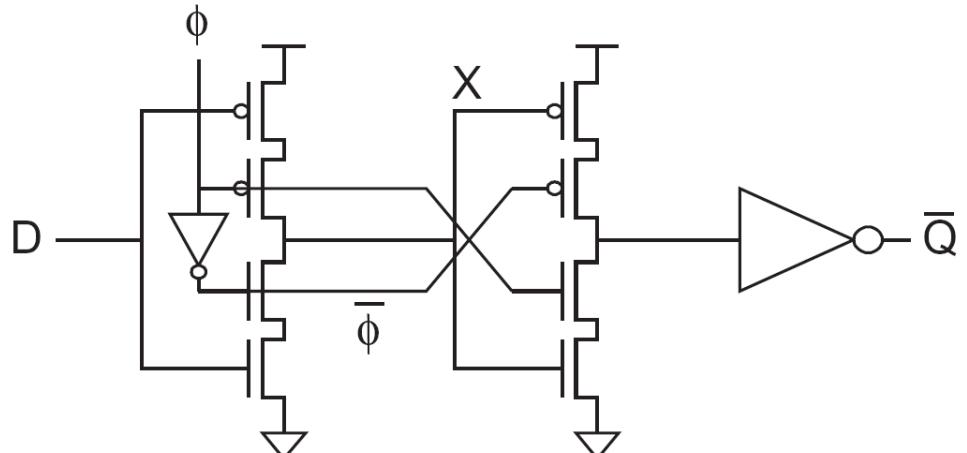
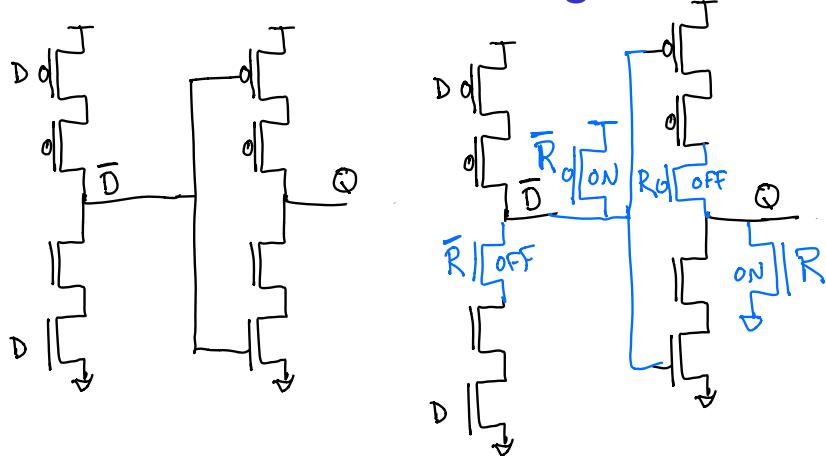
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C²MOS Flip-Flop

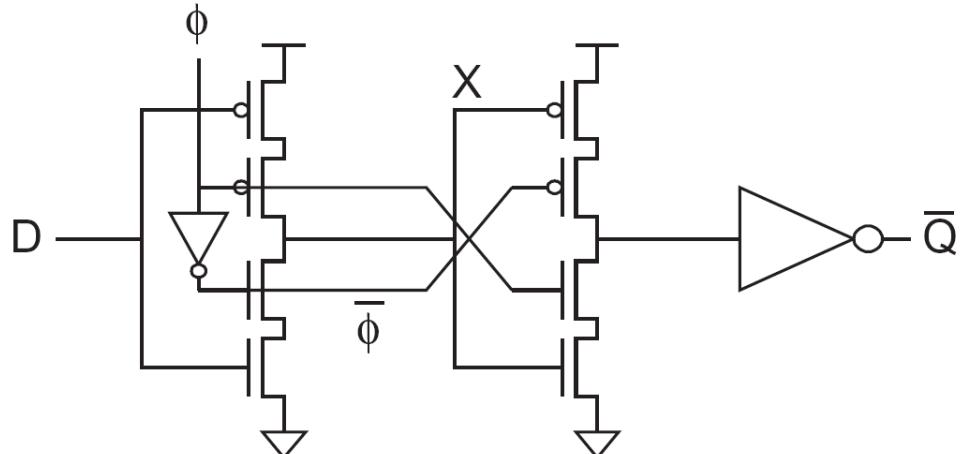
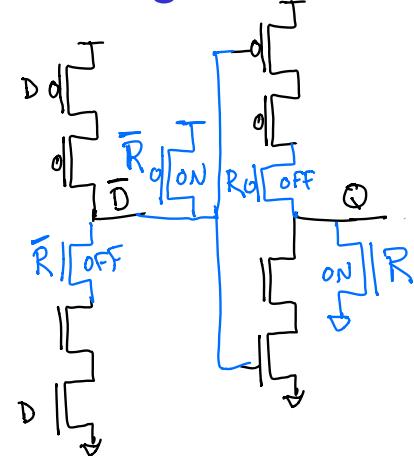
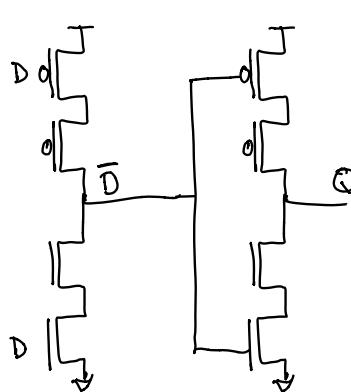
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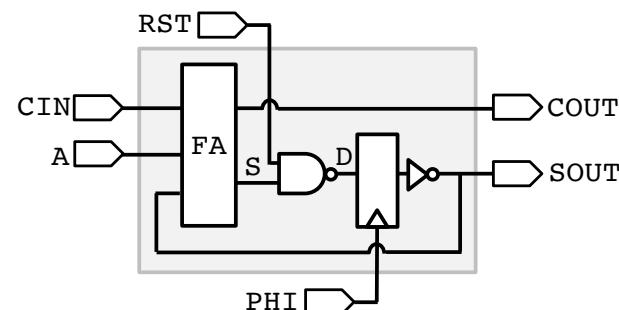
- You will instead use synchronous reset in this lab (see NAND gate)
- NAND/INV cancel each other out. Sout polarity is correct

C²MOS Flip-Flop

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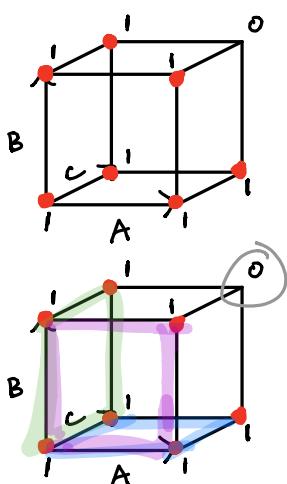
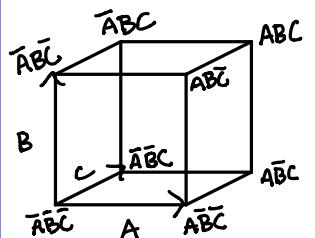
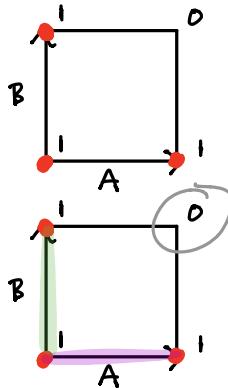
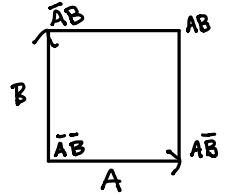


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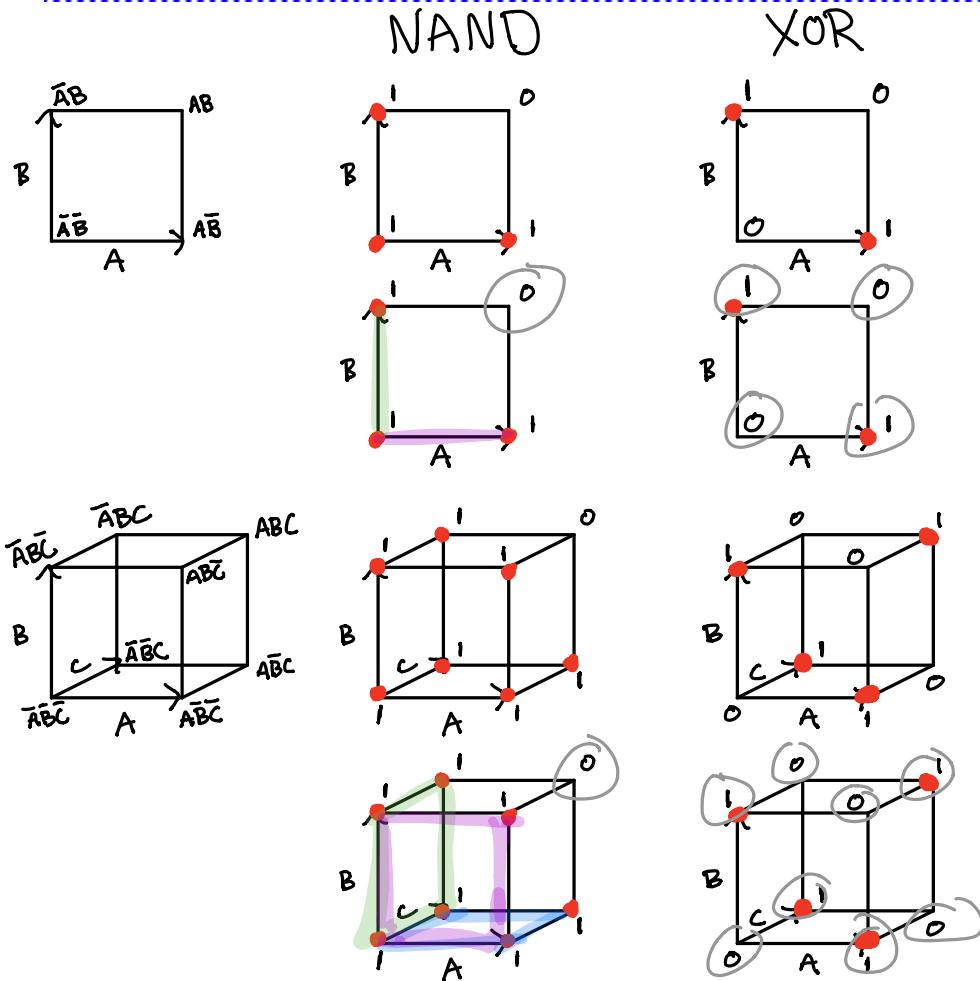


Discuss XOR gate

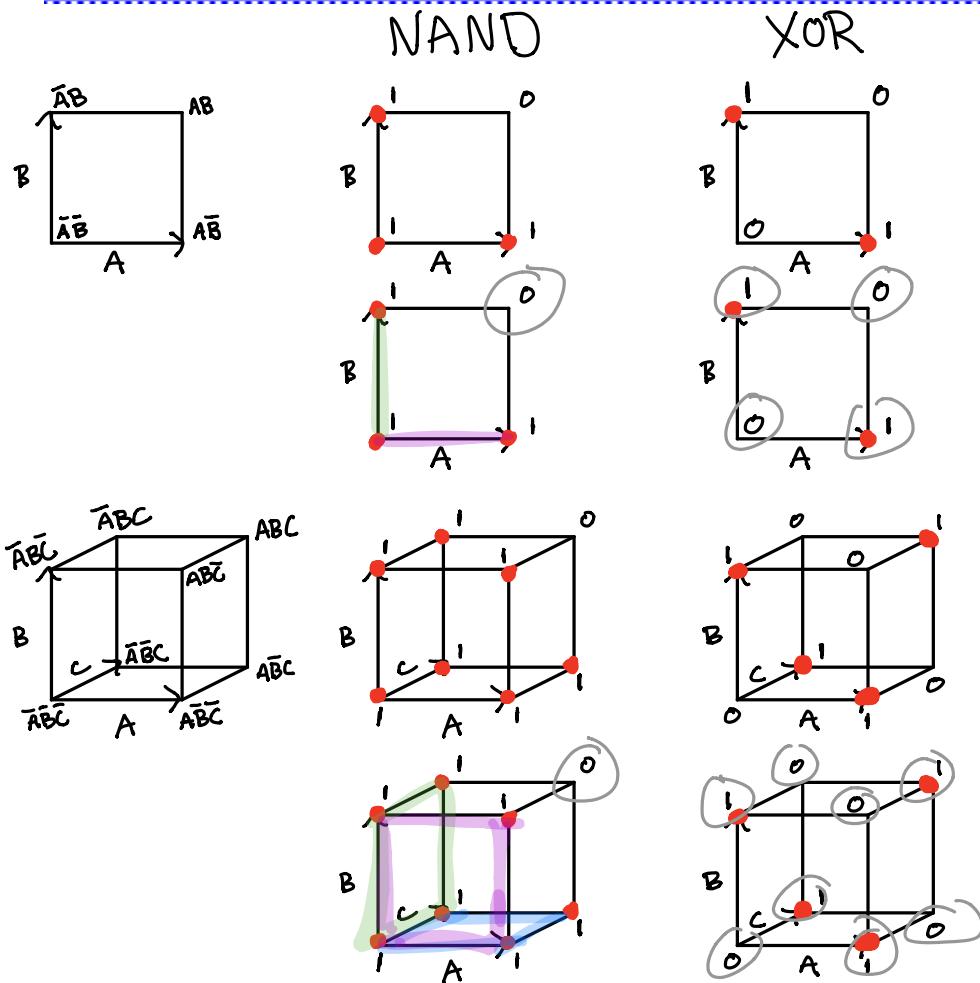
NAND



Discuss XOR gate

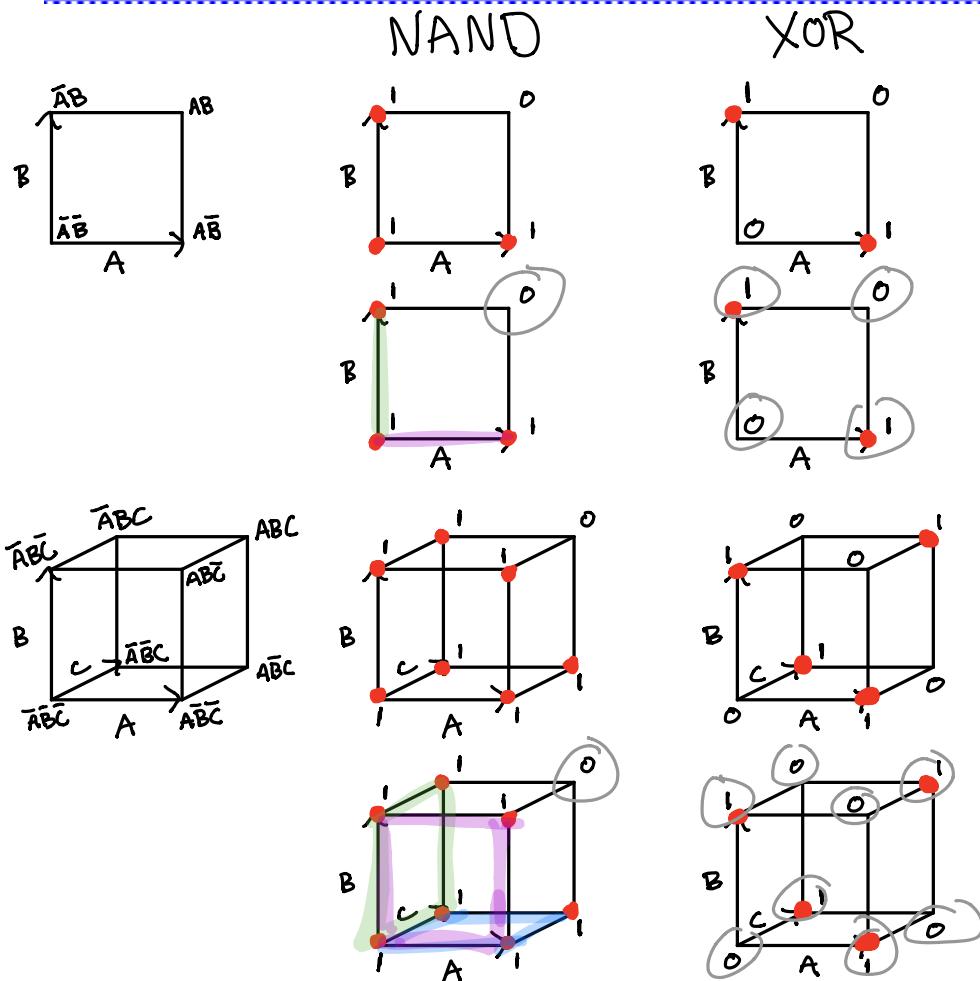


Discuss XOR gate

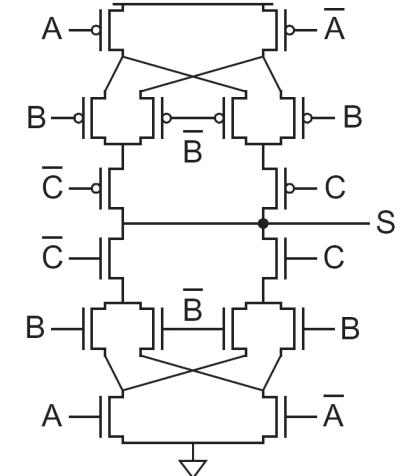


Computing XOR always depends on all inputs.
Therefore static n-input XOR always needs n-transistor stacks for both pull-up and pull-down

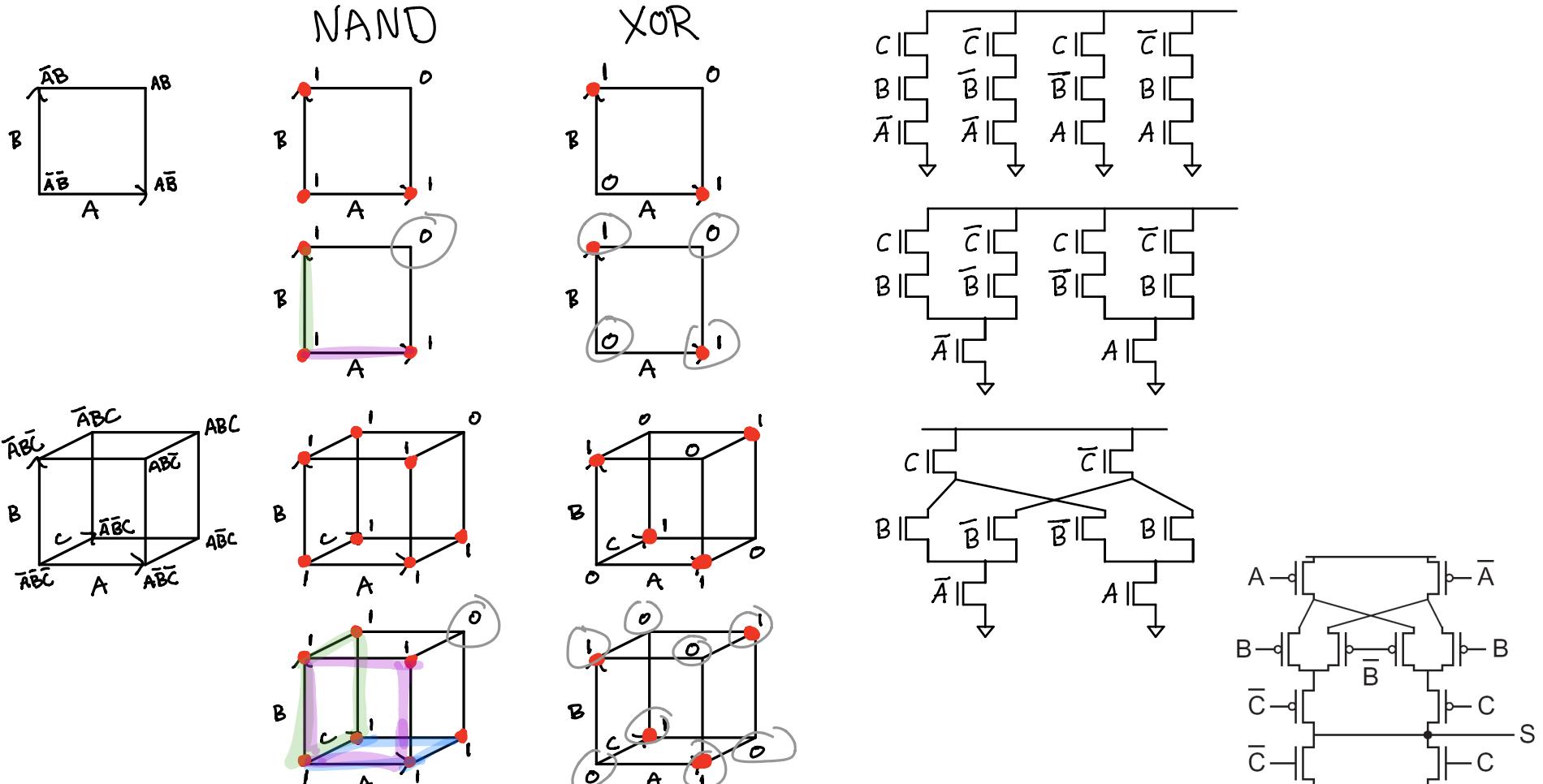
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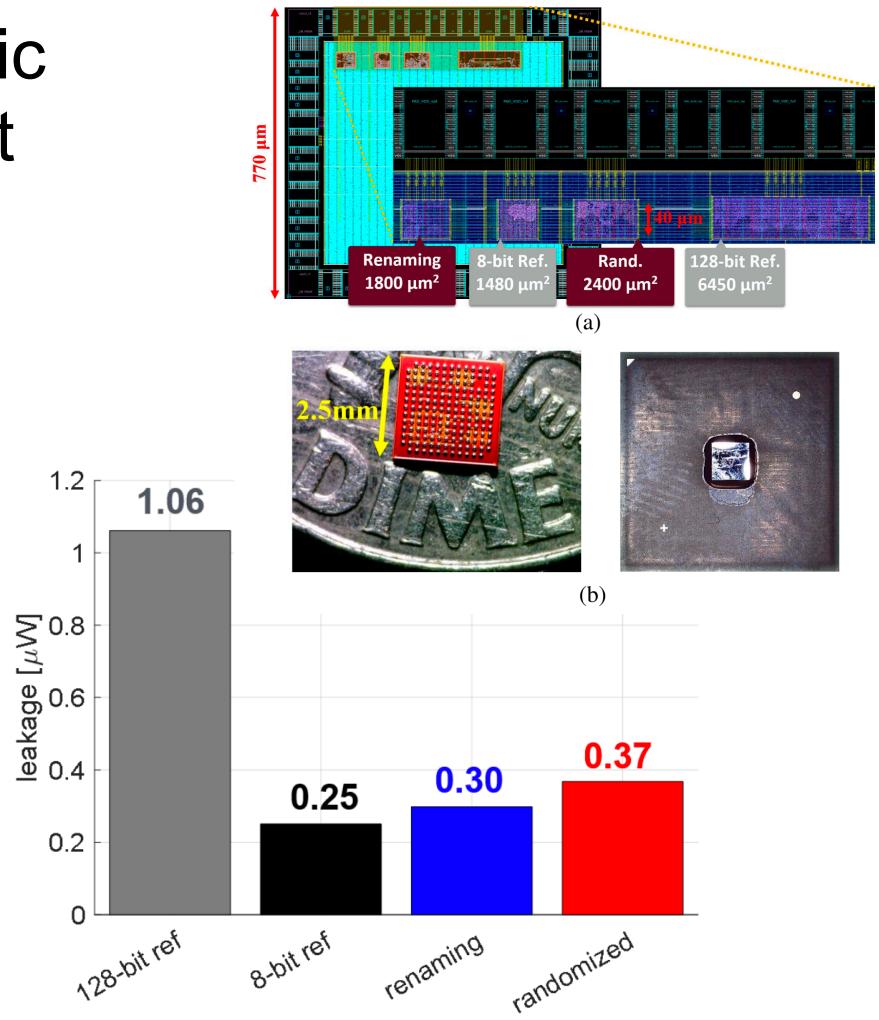
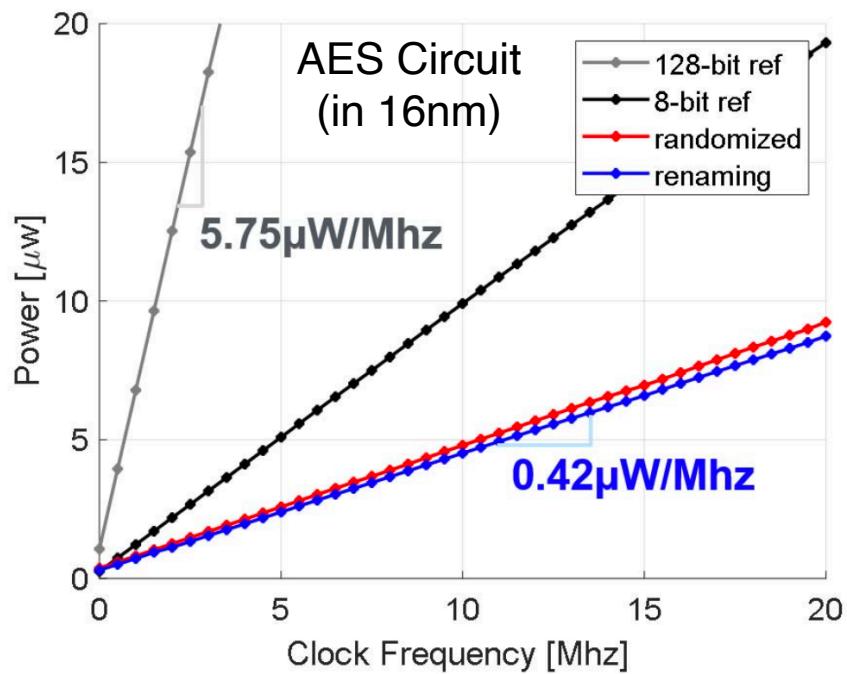
Discuss XOR gate



Computing XOR always depends on all inputs.
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Power Measurement Technique

- Infer both dynamic and static power from overall power at different frequencies



S. N. Dhanuskodi, S. Allen and D. E. Holcomb, "Efficient Register Renaming Architectures for 8-bit AES Datapath at 0.55 pJ/bit in 16-nm FinFET," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 8, pp. 1807-1820, Aug. 2020, doi: 10.1109/TVLSI.2020.2999593.

Power Measurement Example

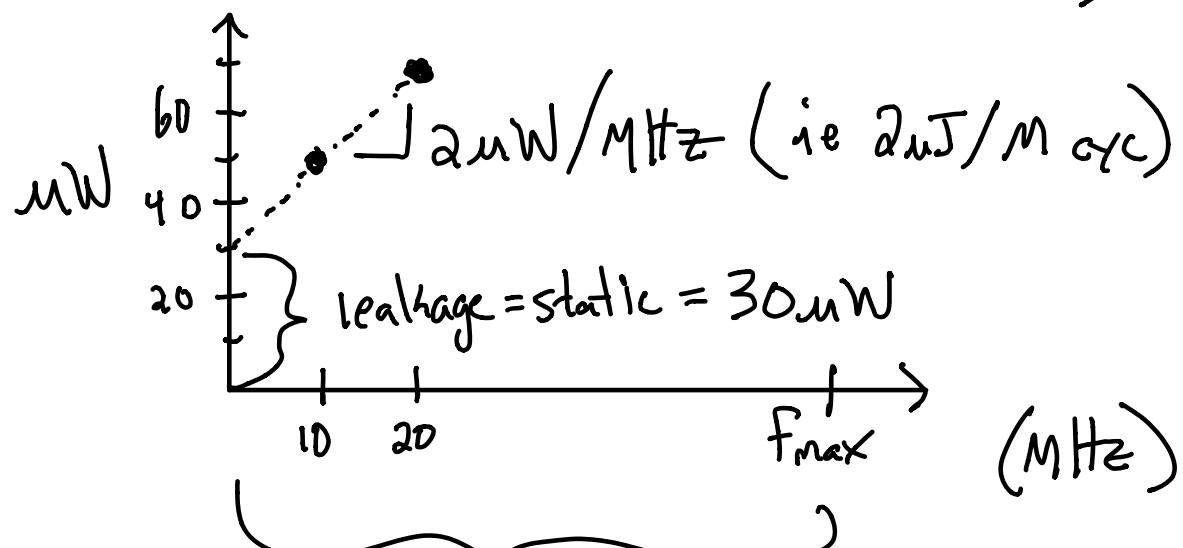


Power Measurement Example

$$W = \frac{J}{s} \quad Hz = \frac{cyc}{s}$$

10 MHz : 50 μW ($= 50 \mu J / 10 M cyc$)

20 MHz : 70 μW ($= 70 \mu J / 20 M cyc$)



if f_{max} = 100 MHz

$$\text{Power} = 30 \mu W + \frac{100 \text{ MHz}}{\text{MHz}} \cdot \frac{2 \mu W}{\text{MHz}} = 230 \mu W$$